

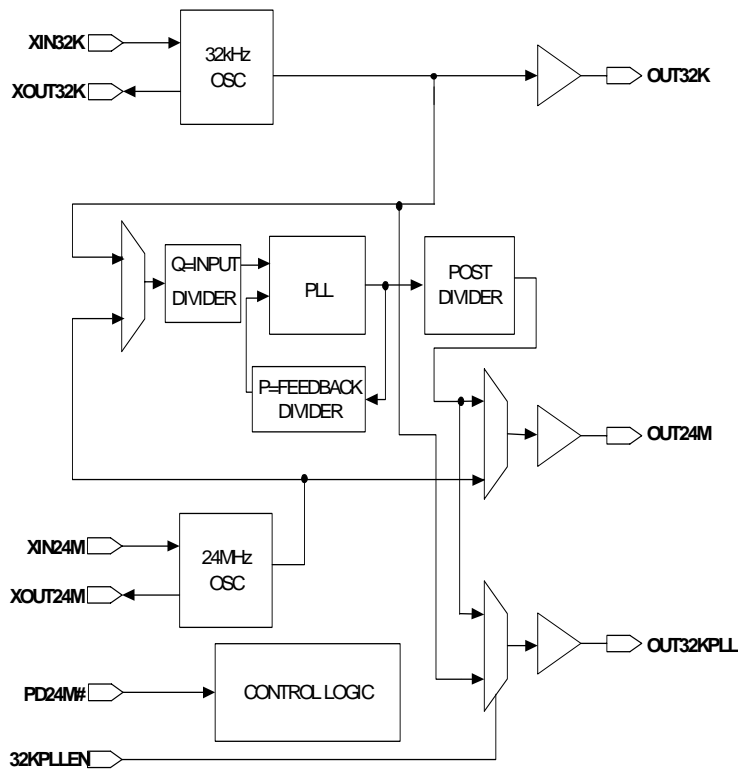


32 kHz and 24 MHz Clock Generator with Precision 32 kHz Input

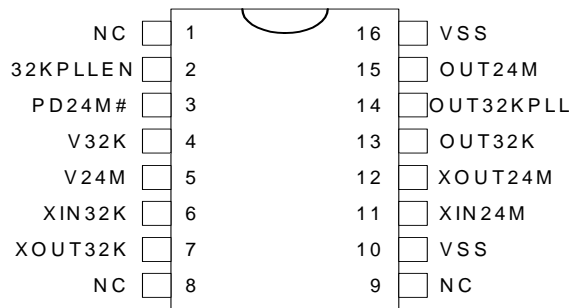
Features

- Precision RTC 32 kHz and 24 MHz output
- Power-down mode (32 kHz on) is < 50 uA
- Suspend mode (V24M = off) is typically 5 uA
- Low RMS period Jitter (< 40 ps)
- 16-pin TSSOP package
- 3.3V ± 5% Voltage Supply
- CY2040-2 multiplier 32.000 kHz × 750 = 24.0 MHz (requires a single 32.000 kHz crystal)
- CY2040-3 enables the 32 kHz and 24.0 MHz oscillators (requires a 32.768 kHz and 24.000 MHz crystal)

Logic Block Diagram



Pin Configuration



Pin Description

Pin #	Symbol	Type	Description
1	NC	NC	No connection (leave it floating).
2	32KPLEN	I, PU	OUT32KPLL (pin 14) output enable (OE). 1 = running, 0 = 3-state. Weak pull-up.
3	PD24M#	I, PU	Power down pin to turn off OUT32M, OUT32KPLL, PLL, post divider and 24-MHz crystal oscillator. Active Low. 1 = running, 0 = power down. Weak pull-up.
4	V32K ^[1]	P	3.3V supply for the 32 kHz oscillator circuit (V _{batt}).
5	V24M ^[1]	P	3.3V supply for the 24 MHz oscillator and PLL circuits (V _{DD}).
6	XIN32K	I	Crystal connection input for OSC1. Recommend using C _{Load} = 6 pF crystal with ESR <= 55 kΩ.
7	XOUT32K	O	Oscillator output pin connected to crystal OSC1.
8	NC	NC	No connection (leave it floating).
9	NC	NC	No connection (leave it floating).
10	VSS	P	Power supply ground.
11	Xin24M	I	Crystal connection input for OSC2. Recommend to use C _{Load} = 10pF crystal with ESR <= 20Ω. Can be left floating if 24M crystal is not used (CY2040-2).
12	OUT24M	O	Oscillator output pin connected to crystal OSC2. Leave this pin unconnected if 24M crystal is not used (CY2040-2).
13	OUT32K	O	3.3V 32 kHz buffered output of the reference crystal.
14	OUT32KPLL	O	32 kHz output. Can be enabled/disabled by 32KPLEN pin.
15	OUT24M	O	3.3V 24 MHz buffered output: either 32 kHz × 750 (-2) or from 24.0 MHz OSC2 (-3).
16	VSS	P	Power supply ground.

Device Configuration

Device	Input Crystals	Output Frequency
CY2040-2	32.000 kHz crystal with C _{Load} = 6pF and ESR <= 55 kΩ.	OUT32K = 32.000 kHz; OUT24M = 24.000 MHz, OUT32KPLL=32.000kHz
CY2040-3	32.768 kHz crystal with C _{Load} = 6pF and ESR <= 55 kΩ. 24.000 MHz crystal with C _{Load} = 10pF and ESR <= 20 Ω.	OUT32K = 32.768 kHz; OUT24M = 24.000 MHz, OUT32KPLL = 32.768 kHz

Note:

1. The two power supply pins, V32K and V24M, should be shorted externally.

Absolute Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage -0.5V to +7.0V

Input Voltage -0.5V to V24M +0.5

Storage Temperature

(Non-Condensing) -55°C to +150°C

Junction Temperature +150°C

Static Discharge Voltage $\geq 2000V$

(per MIL-STD-883, Method 3015)

Operating Conditions

Parameter	Description	Conditions	Min.	Max.	Unit
V32K	V _{batt} , Supply voltage	Relative to V _{SS}	3.135	3.465	V
V24M	V _{DD} , Supply voltage	Relative to V _{SS}	3.135	3.465	V
T _A	Operating Temperature, Ambient	Operating Temperature Range, Ambient	0	70	°C
C _L	Load Capacitance	Max Capacitive Load on OUT32K, OUT32KPLL, and OUT24M		15	pF
t _{PU}	Power-up time for all VDD's to reach minimum specified voltage (power ramps must be monotonic)		0.05	50	ms

DC Characteristics

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
V _{IL}	Input low voltage (PD24M# and 32KPLEN Pins)	V24M = 3.3 \pm 5%			0.2 V _{DD}	V
V _{IH}	Input high voltage (PD24M# and 32KPLEN Pins)	V24M = 3.3 \pm 5%	0.7 V _{DD}			V
I _{IL}	Input low current (PD24M# and 32KPLEN Pins)	V _{IN} = 0V		<1	10	μ A
I _{IH}	Input high current (PD24M# and 32KPLEN Pins)	V _{IN} = V24M		<1	5	μ A
I _{DD}	Dynamic Supply Current with no load at outputs.	V24M = V32K = 3.3 \pm 5%, f _{OUT32K} = 32.768kHz or 32.000kHz, f _{OUT24M} = 24MHz, f _{OUT32KPLL} = 3-state.		10	25	mA
I _{PT}	Power-down Supply Current	V24M = V32K = 3.3 \pm 5% (PD24M# = "0")		20	50	μ A

OUT32K (V32K = 3.3V \pm 5%)

V _{OL}	Output low voltage	V32K = 3.3 \pm 5%, I _{OL} = 8 mA			0.4	V
V _{OH}	Output high voltage	V32K = 3.3 \pm 5%, I _{OH} = -8 mA	V32K - 0.4			

OUT24M (V24M = 3.3V \pm 5%)

V _{OL}	Output low voltage	V24M = 3.3 \pm 5%, I _{OL} = 8 mA			0.4	V
V _{OH}	Output high voltage	V24M = 3.3 \pm 5%, I _{OH} = -8 mA	V24M - 0.4			
I _{OZ}	Output leakage current (OUT24M)	V24M = 3.3 \pm 5%, with output disabled		1	50	μ A

OUT32KPLL (V24M = 3.3V \pm 5%)

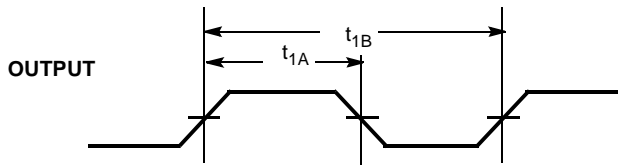
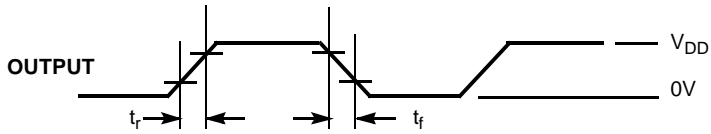
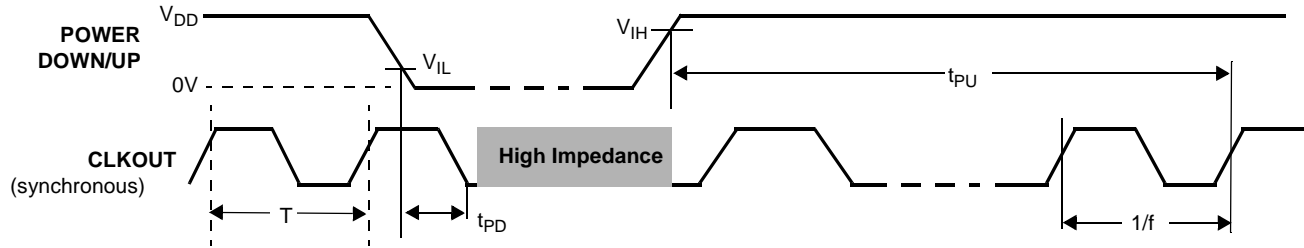
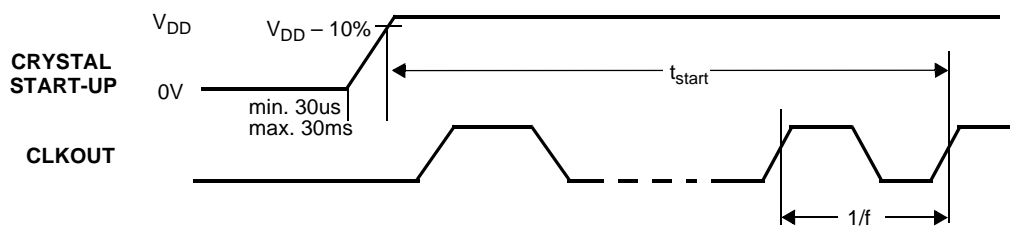
V _{OL}	Output low voltage	V24M = 3.3 \pm 5%, I _{OL} = 8 mA			0.4	V
V _{OH}	Output high voltage	V24M = 3.3 \pm 5%, I _{OH} = -8 mA	V24M - 0.4			

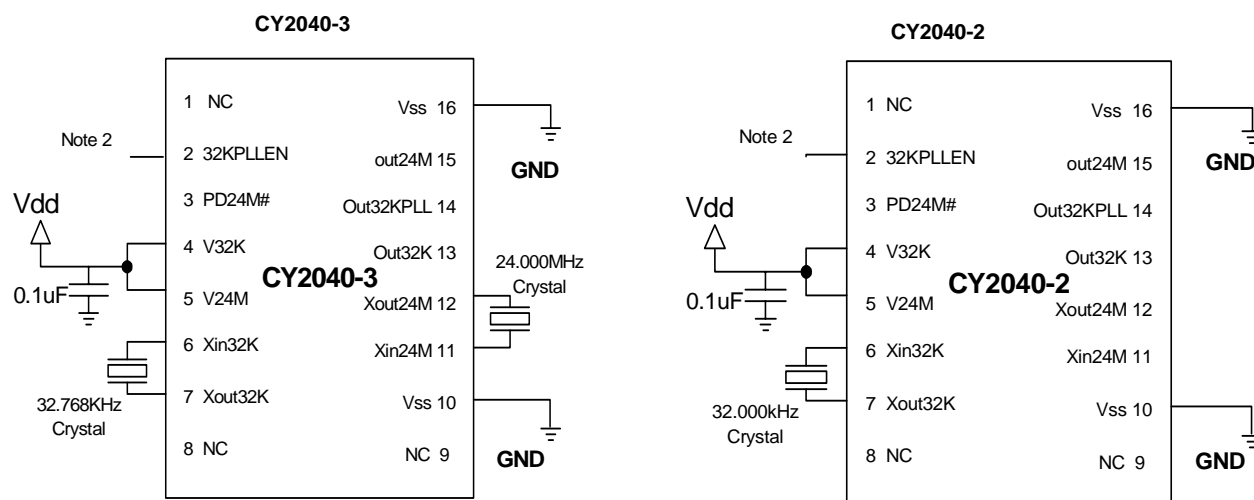
DC Characteristics

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{OZ}	Output leakage current (OUT32KPLL)	V24M = $3.3 \pm 5\%$, with output disabled		1	50	μA

AC Characteristics

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
OUT32K AC Characteristics						
tr1	OUT32K Rise time	20% to 80% V32K			7.0	ns
tf1	OUT32K Fall time	80% to 20% V32K			7.0	ns
dc1	OUT32K Duty Cycle	$C_{LT} = 15$ pF, measured at V32K/2	40		60	%
tj1	Pk-Pk Period jitter	32.000 kHz output directly from oscillator (with crystal), measured at V32K/2		20	40	ns
OUT24M AC Characteristics						
tr2	OUT24M Rise Time	V24M = $3.3 \pm 5\%$; 20% to 80% V24M			4.0	ns
tf2	OUT24M Fall Time	V24M = $3.3 \pm 5\%$; 80% to 20% V24M			4.0	ns
dc2	OUT24M Duty cycle	V24M = $3.3 \pm 5\%$; measured at V24M/2	40		60	%
tj2	RMS Period Jitter (CY2040-2, PLL output)	V24M = V32K = $3.3 \pm 5\%$; 32 kHz as input to PLL; measured at V24M/2			40	ps
	RMS Period Jitter (CY2040-3, osc. output)	V24M = V32K = $3.3 \pm 5\%$; 24 MHz output directly from oscillator; measured at V24M/2			40	ps
tj3	RMS Long-term Jitter (CY2040-2, PLL output)	V24M = V32K = $3.3 \pm 5\%$; 32 kHz as input to PLL; measured at V24M/2 on the 750th output rising edge.			1.5	ns
OUT32KPLL AC Characteristics						
tr3	OUT32KPLL Rise Time	V24M = $3.3 \pm 5\%$; 20% to 80% V24M			7.0	ns
tf3	OUT32KPLL Fall Time	V24M = $3.3 \pm 5\%$; 80% to 20% V24M			7.0	ns
dc3	OUT32KPLL Duty cycle	V24M = $3.3 \pm 5\%$; measured at V24M/2	40		60	%
tj4	Pk-Pk Period Jitter (32 kHz osc. output)	32.000 kHz output directly from oscillator, measured at V24M/2		20	40	ns
Other AC Characteristics						
t_{start}	Osc start up time	From power on (V32K = $3.3 \pm 5\%$). Decided by 32.768 kHz/32.000 kHz crystal startup.			3	sec
t_{PD}	Power down delay time on OUT24M; SYNC	PD24M# pin high to low (T = OUT24M clock period)		T/2	T+25	ns
t_{PU}	Power up time on OUT24M; ASYNC (CY2040-2)	From power down mode; PD24M# pin low to high.		1	5	ms
	Power up time on OUT24M; ASYNC (CY2040-3)	From power down mode; PD24M# pin low to high. Decided by 24 MHz crystal start-up.		6	10	ms

Switching Waveforms
Duty Cycle Timing (dc1, dc2, dc3)

Output Rise/Fall Time

Power Down and Power up Timing (synchronous modes)

Crystal Start-up Timing


Application Circuits

Note:

- To disable the OUT32KPLL output, the 32KPLEN pin should be connected to GND. To enable the OUT32KPLL output, the 32KPLEN pin should be connected to V_{DD}.

Ordering Code	Package Name	Package Type	Operating Range
CY2040ZC-2	Z16	16LD TSSOP	0–70°C
CY2040ZC-3	Z16	16LD TSSOP	0–70°C

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Document Title: CY2040-2/3 32 kHz and 24 MHz Clock Generator with Precision 32 kHz Input Document Number: 38-07122				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	109574	01/17/02	CKN	New Data Sheet
*A	121821	12/14/02	RBI	Power up requirements added to Operating Conditions Information