CY2030

USB, Audio, and I/O Clock Generator for Intel 82440LX Chipset

Features

- **USB, Audio, and I/O clock generator for most motherboards using 5th or 6th generation processors. Can also be used for peripheral systems.**
- **Two copies of 48 MHz USB clocks**
- **One copy of 24 MHz I/O clock**
- **Audio support for 33.8688 MHz, 24.576 MHz, 16.9344 MHz and 12.288 MHz, pin-selectable**
- **Three copies of Ref. clock @ 14.318 MHz**
- **14.318 MHz reference input**
- **Ability to three-state all outputs**
- **Test mode support**
- **Output duty cycle 45% min. to 55% max.**
- **Available in 20-pin SSOP packages**
- **3.3V operation**
- **Internal pull-up resistors on S0, S1, and OE inputs**

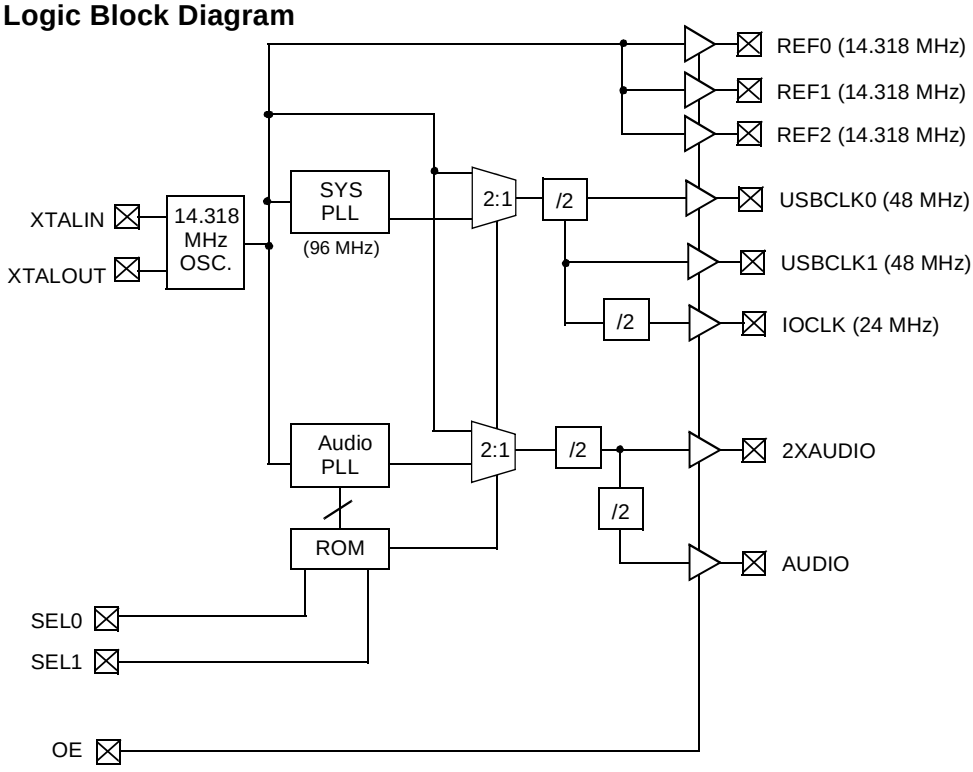
Functional Description

The CY2030 is a peripheral clock generator for most motherboards using fifth and sixth generation processors. The device outputs two copies of a 48 MHz USB clock, as well as one copy of a 24 MHz I/O clock, both of which meet Intel's accuracy, drive, and jitter requirements. Additionally, the part drives two audio clock outputs at 2X and 1X frequencies respectively. These audio clocks support all frequencies that are required by CODECs and FM synthesizers. Finally, the part outputs three reference clocks at 14.318 MHz, which can be used to drive ISA slots, graphics accelerators, and other devices requiring this frequency.

The CY2030 can be used with the CY2275-1 and CY2276-1 (which are CPU, AGP, PCI, and SDRAM clock generators) to provide a complete clock solution for PC motherboards.

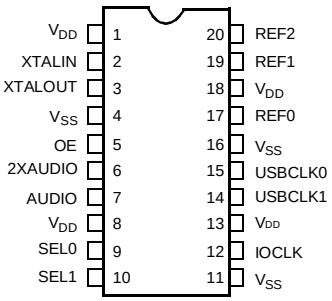
The CY2030 accepts a 14.318 MHz reference signal as its input. The CY2030 has two PLLs, one of which generates the audio clocks, and the other generates the Universal Serial Bus (USB) and I/O clocks. The CY2030 runs off a 3.3V supply.

Logic Block Diagram



Pin Configuration

Top View
SSOP



Pin Summary

Name	Pins	Description
V_{DD}	1	3.3V voltage supply
XTALIN[1, 2]	2	Reference crystal input, typically 14.318 MHz
XTALOUT[1]	3	Reference crystal feedback
V_{SS}	4	Ground
OE	5	Output Enable, active HIGH (internal pull-up resistor to V_{DD}). Three-states all outputs when driven LOW.
2XAUDIO	6	2XAudio clock output, at 33.8688 MHz or 24.576 MHz (See function table below)
AUDIO	7	Audio clock output, at 16.9344 MHz or 12.288 MHz (See function table below)
V_{DD}	8	3.3V voltage supply
SEL0	9	Audio clock select input, bit 0 (internal pull-up resistor to V_{DD})
SEL1	10	Audio clock select input, bit 1 (internal pull-up resistor to V_{DD})
V_{SS}	11	Ground
IOCLK	12	I/O clock output (24.0 MHz)
V_{DD}	13	3.3V Voltage supply
USBCLK1	14	USB clock output (48.0 MHz)
USBCLK0	15	USB clock output (48.0 MHz)
V_{SS}	16	Ground
REF0	17	REF clock output for ISA slots, drives 45 pF loads (14.318 MHz)
V_{DD}	18	3.3V voltage supply
REF1	19	Reference clock output (14.318 MHz)
REF2	20	Reference clock output (14.318 MHz)

Function Table

OE	SEL1	SEL0	XTALIN	2XAudio	Audio	REF [0:2]	USBCLK [0:1]	IOCLK
0	X	X	14.318 MHz	High-Z	High-Z	High-Z	High-Z	High-Z
1	0	0	14.318 MHz	XTALIN/2[3]	XTALIN/4[3]	XTALIN[3]	XTALIN/2[3]	XTALIN/4[3]
1	0	1	14.318 MHz	24.576 MHz	12.288 MHz	14.318 MHz	48 MHz	24 MHz
1	1	0	14.318 MHz	33.8688 MHz	16.9344 MHz	14.318 MHz	48 MHz	24 MHz
1	1	1	14.318 MHz	Low	Low	14.318 MHz	48 MHz	24 MHz

Actual Frequency Values

Clock	Target Frequency (MHz)	Actual Frequency (MHz)	PPM
USBCLK	48.0	48.008	167
IOCLK	24.0	24.004	167
2XAUDIO	33.8688	33.8680	–24
2XAUDIO	24.576	24.5795	144
AUDIO	16.9344	16.9340	–24
AUDIO	12.288	12.2898	144
REF	14.318	14.318	0

Notes:

1. XTALIN and XTALOUT do not have internal compensation capacitors. Therefore, if an external crystal is used with the device, external compensation capacitors are required to match the load capacitance of the crystal.
2. If the reference is an external clock, it should be driven on the XTALIN input, and XTALOUT must be left floating.
3. Intel Test Mode

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage.....–0.5 to +4.6V

Input Voltage.....–0.5V to V_{DD}+0.5

Storage Temperature (Non-Condensing)... –65°C to +150°C

Max. Soldering Temperature (10 sec)..... +260°C

Junction Temperature ..... +150°C

Static Discharge Voltage ..... >2000V (per MIL–STD–883, Method 3015)

Operating Conditions[4]

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage, 3.3V	3.135	3.465	V
T_A	Operating Temperature, Ambient	0	70	°C
C_L	Capacitive Load on All Clock Outputs except REF0 REF0	 10 20	 20 45	pF
$f_{(REF)}$	Reference Clock Input Frequency	14.318	14.318	MHz

Electrical Characteristics V_{DD} = 3.135V to 3.465V, T_A = 0°C to +70°C

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{IH}	High-level Input Voltage	Except Crystal Inputs			2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Inputs				0.8	V
V_{OH}[5]	High-level Output Voltage	V_{DD} = V_{DD} Min.	I_{OH} = –15 mA	All outputs except REF0	2.4		V
V_{OH}[5]	High-level Output Voltage	V_{DD} = V_{DD} Min.	I_{OH} = –38 mA	REF0			
V_{OL}[5]	Low-level Output Voltage	V_{DD} = V_{DD} Min.	I_{OL} = 8 mA	All outputs except REF0		0.4	V
V_{OL}[5]	Low-level Output Voltage	V_{DD} = V_{DD} Min.	I_{OL} = 22 mA	REF0			
I_{IH}	Input High Current	V_{IH} = V_{DD}				5	µA
I_{IL}	Input Low Current	V_{IL} = 0V				100	µA
I_{OZ}	Output Leakage Current	Three-state			–10	+10	µA
I_{DD}	Power Supply Current	V_{DD} = 3.465V, V_{IN} = 0 or V_{DD}				50	mA

Switching Characteristics[5, 6]

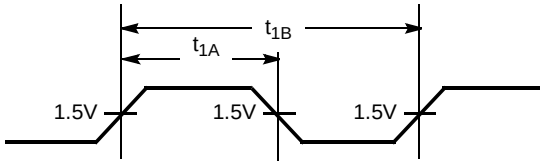
Parameter	Output	Description	Test Conditions	Min.	Max.	Unit
t_1	All	Output Duty Cycle[7]	t_1 = t_{1A} ÷ t_{1B}	45%	55%	
t_2	REF0	REF0 Clock Rise Time	Measured between 0.8V and 2.0V		2.0	ns
t_3	REF0	REF0 Clock Fall Time	Measured between 2.0V and 0.8V		2.0	ns
t_2	All Clock outputs except REF0	Clock Rise Time	Measured between 0.8V and 2.0V		4	ns
t_3	All Clock outputs except REF0	Clock Fall Time	Measured between 2.0V and 0.8V		4	ns
t_4	USBCLK, IOCLK	Cycle-Cycle Clock Jitter	Measured at 1.5V		500	ps

Notes:

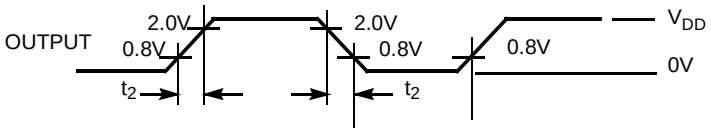
4. Electrical parameters are guaranteed with these operating conditions.
5. Guaranteed by design and characterization, not 100% tested in production.
6. All parameters specified with outputs fully loaded.
7. Duty cycle is measured at 1.5V.

Switching Waveforms

Duty Cycle Timing

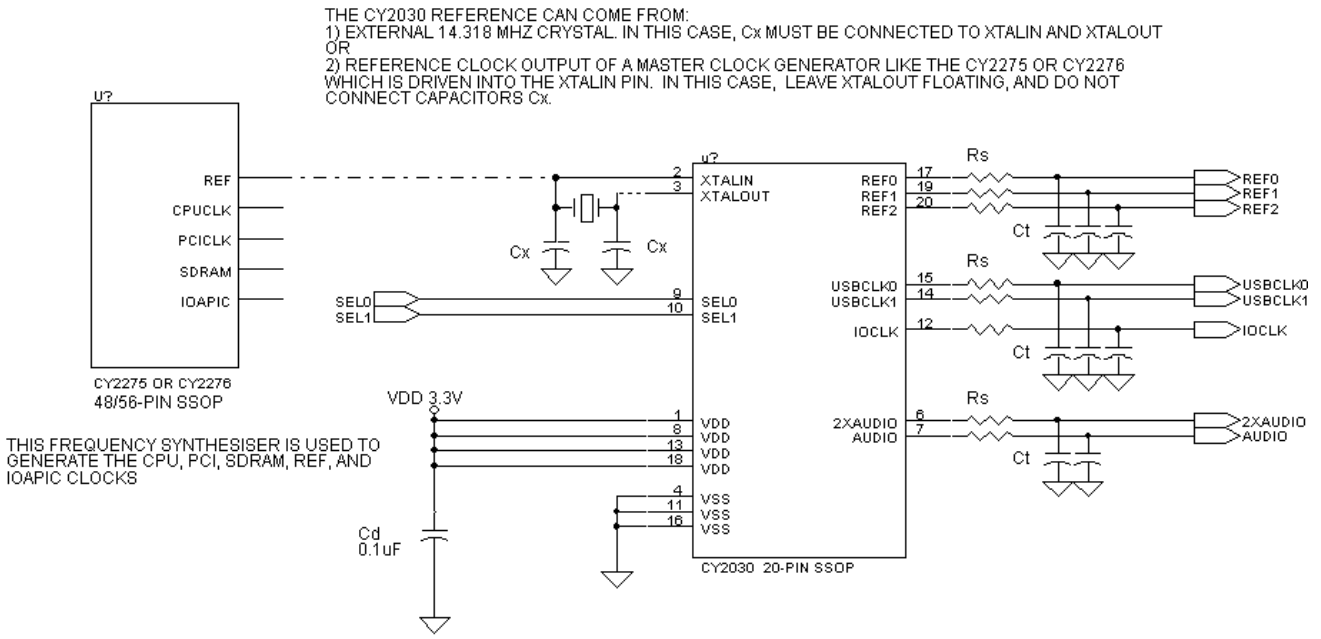


All Outputs Rise/Fall Time



Applications Information

Clock traces must be terminated with either series or parallel termination, as they are normally done. Additionally, the CY2030 does not have crystal load matching capacitors internal to the device, and therefore, external capacitors will be needed when using the device with an external crystal.



Cx = LOAD MATCHING CAPACITORS, REQUIRED WITH EXTERNAL CRYSTALS
= 2 * CRYSTAL LOAD CAPACITANCE

Cd = DECOUPLING CAPACITOR

Ct = OPTIONAL EMI-REDUCING CAPACITORS

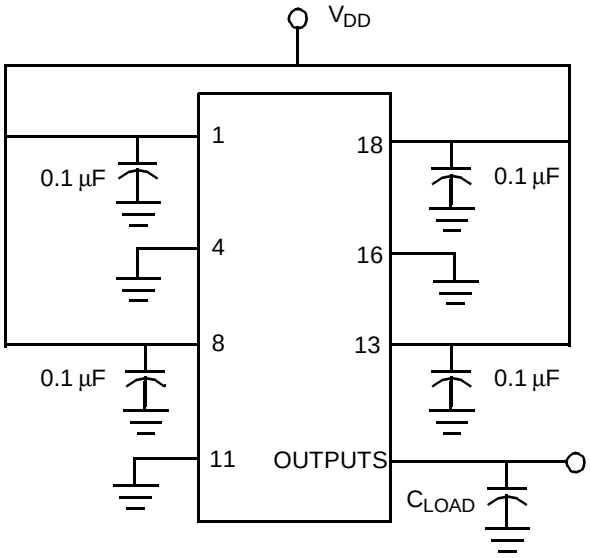
Rs = SERIES TERMINATING RESISTORS

Summary

- A parallel-resonant crystal should be used as the reference to the clock generator. The operating frequency and C_{LOAD} of this crystal should be as specified in the data sheet. Optional trimming capacitors may be needed if a crystal with a different C_{LOAD} is used. Footprints must be laid out for flexibility.
- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1 µF. In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where R_{trace} is the loaded characteristic impedance of the trace, R_{out} is the output impedance of the clock generator (specified in the data sheet), and R_{series} is the series terminating resistor.

  $$R_{series} \geq R_{trace} - R_{out}$$
- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7 pF to 22 pF.
- A Ferrite Bead **may** be used to isolate the Board V_{DD} from the clock generator V_{DD} island. Ensure that the Ferrite Bead offers greater than 50Ω impedance at the clock frequency, under loaded DC conditions. Please refer to the application note “Layout and Termination Techniques for Cypress Clock Generators” for more details.
- If a Ferrite Bead is used, a 10 µF– 22 µF tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

Test Circuit



Note: All capacitors should be placed as close to each pin as possible.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2030PVC-1	O20	20-Pin SSOP	Commercial

Document #: 38-00560-B

Package Diagram

All Dimensions in mm.

20-Pin Shrunk Small Outline Package O20