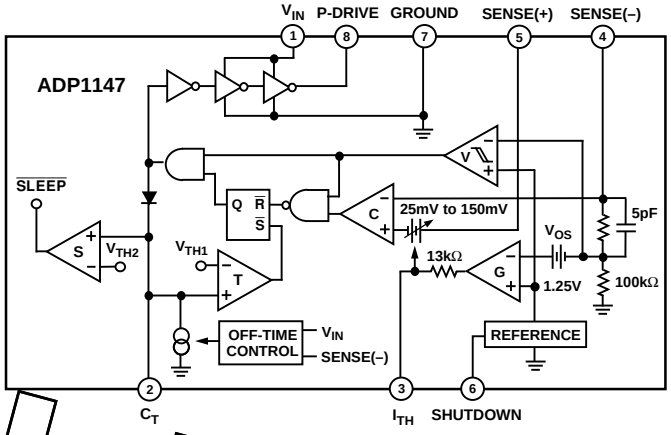
High Efficiency Step-Down Switching Regulator Controller

ADP1147

FEATURES
Over 95% Efficiency
Current-Mode Operation Resulting in Good Line and Load Transient Response
Low Shutdown Current: 22 μA max
Input Voltage Range: 3.5 V to 20 V
Standby Current: 160 μA typ
Short Circuit Protection
8-Pin PDIP and SO Package

APPLICATIONS
Notebook and Palmtop Computers
Cellular Telephones
Modems
Portable Instruments
GPS Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADP1147 is part of a family of step-down switching regulators featuring automatic sleep mode to maintain high efficiency at low output currents. These regulators drive an external P-channel MOSFET at frequencies up to 250 kHz using constant off-time current mode architecture.

Input supply voltages vary from 3.5 V to 20 V maximum. The constant off-time architecture maintains constant ripple current in the inductor easing the design of wide input range regulators.

Low dropout regulation is limited only by the combination of the R_{DS} (on) of the external MOSFET and resistance of the inductor and current sense resistor.

The ADP1147 family incorporates automatic Power Saving Mode to help reduce losses due to switching when load currents drop below the required continuous operation level. In Power Saving Mode, standby power is reduced to only 2 mW at V_{IN} = 10 V. For even greater efficiencies, refer to the ADP1148.

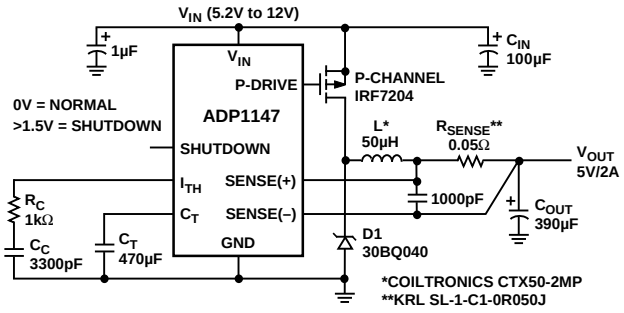


Figure 1. High Efficiency Step-Down Converter (Typical Application)

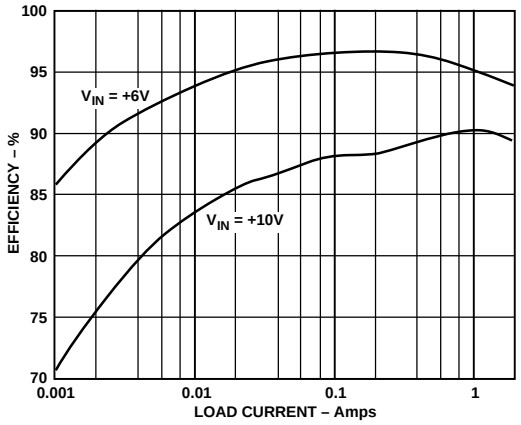


Figure 2. ADP1147-5 Typical Efficiency

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

ADP1147–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ +70°C, (Note 1) V_{IN} = 10 V, $V_{SHUTDOWN}$ = 0 V unless otherwise noted.) (See Figure 17.)

Parameter	Conditions	V_S	ADP1147 Min	Typ	Max	Units
REGULATED OUTPUT VOLTAGE	V_{IN} = 9 V	V_{OUT}				
ADP1147-3-3	I_{LOAD} = 700 mA		3.23	3.33	3.43	V
ADP1147-5	I_{LOAD} = 700 mA		4.90	5.05	5.20	V
OUTPUT VOLTAGE LINE REGULATION	T_A = +25°C V_{IN} = 7 V to 12 V, I_{LOAD} = 50 mA	ΔV_{OUT}	–40	0	+40	mV
OUTPUT VOLTAGE LOAD REGULATION						
ADP1147-3.3	5 mA < I_{LOAD} < 2 A	ΔV_{OUT}		40	65	mV
ADP1147-5	5 mA < I_{LOAD} < 2 A			60	100	mV
Sleep Mode Output Ripple	T_A = +25°C, I_{LOAD} = 0 A			50		mV p-p
INPUT DC SUPPLY CURRENT[2]	T_A = +25°C					
Normal Mode	4 V < V_{IN} < 18 V	I_Q		1.6	2.3	mA
Sleep Mode (ADP1147-3.3)	4 V < V_{IN} < 18 V			160	250	µA
Sleep Mode (ADP1147-5)	5 V < V_{IN} < 18 V			160	250	µA
Shutdown	$V_{SHUTDOWN}$ = 2.1 V, 4 V < V_{IN} < 18 V			10	22	µA
CURRENT SENSE THRESHOLD VOLTAGE						
ADP1147-3.3	$V_{SENSE}(-) = V_{OUT}^+$ 100 mV (Forced) T_A = +25°C			25		mV
	$V_{SENSE}(-) = V_{OUT}^-$ 100 mV (Forced)	$V_5 - V_4$	130	150	170	mV
ADP1147-5	$V_{SENSE}(-) = V_{OUT}^+$ 100 mV (Forced) T_A = +25°C			25		mV
	$V_{SENSE}(-) = V_{OUT}^-$ 100 mV (Forced)		130	150	170	mV
SHUTDOWN PIN THRESHOLD	T_A = +25°C	V_6	0.6	0.8	2	V
SHUTDOWN PIN INPUT CURRENT	0 V < $V_{SHUTDOWN}$ < 8 V, V_{IN} = 18 V T_A = +25°C	I_6		1.2	5	µA
C_T PIN DISCHARGE CURRENT	T_A = +25°C, V_{OUT} in Regulation,		50	70	90	µA
	$V_{SENSE}(-) = V_{OUT}$, V_{OUT} = 0 V	I_2		2	10	µA
OFF-TIME[3]	C_T = 390 pF, I_{LOAD} = 700 mA	t_{OFF}	4	5	6	µs
DRIVER OUTPUT TRANSITION TIMES	T_A = +25°C C_L = 2200 pF (Pin 8) V_{IN} = 6 V	tr, tf		100	200	ns

NOTES
[1]All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.
[2]Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.
[3]In applications where R_{SENSE} is placed at ground potential, the off-time increases approximately 40%.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (Pin 1) . . . . . 20 V to –0.3 V
Continuous Output Current (Pin 8) . . . . . 50 mA
Sense Voltages (Pins 4, 5) . . . . . 10 V to –0.3 V
Operating Ambient Temperature Range . . . . . 0°C to +70°C
Extended Commercial Temperature Range . . –40°C to +85°C
Junction Temperature* . . . . . +150°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

*T_J is calculated from the ambient temperature, T_A, and power dissipation, P_D, according to the following formulas: ADP1147AN-3.3, ADP1147AN-5: $T_J = T_A + (P_D \times 110°C/W)$. ADP1147AR-3.3, ADP1147AR-5: $T_J = T_A + (P_D \times 150°C/W)$.

ORDERING GUIDE

Model	Output Voltage	Package Description	Package Option
ADP1147AN-3.3	3.3 V	Plastic DIP	N-8
ADP1147AR-3.3	3.3 V	SOIC	SO-8
ADP1147AN-5	5 V	Plastic DIP	N-8
ADP1147AR-5	5 V	SOIC	SO-8

ELECTRICAL CHARACTERISTICS (–40°C ≤ T_A ≤ 85°C (Note 1), V_{IN} = 10 V, unless otherwise noted.) (See Figure 17).

Parameter	Conditions	V_S	ADP1147 Min	Typ	Max	Units
REGULATED OUTPUT VOLTAGE	V_{IN} = 9 V					
ADP1147-3.3	I_{LOAD} = 700 mA	V_{OUT}	3.17	3.33	3.4	V
ADP1147-5	I_{LOAD} = 700 mA		4.85	5.05	5.2	V
INPUT DC SUPPLY CURRENT						
Normal Mode	4 V < V_{IN} < 18 V	I_Q		1.6	2.6	mA
Sleep Mode (ADP1147-3.3)	4 V < V_{IN} < 18 V			160	280	µA
Sleep Mode (ADP1147-5)	5 V < V_{IN} < 18 V			160	280	µA
Shutdown	$V_{SHUTDOWN}$ = 2.1 V, 4 V < V_{IN} < 18 V			10	28	µA
CURRENT SENSE THRESHOLD VOLTAGE						
ADP1147-3.3	V_{SENSE}(–)= V_{OUT}^+ 100 mV (Forced)	V_5–V_4				
	T_A = +25°C			25		mV
	V_{SENSE}(–) = V_{OUT}^- 100 mV (Forced)		125	150	175	mV
ADP1147-5	V_{SENSE}(–)= V_{OUT}^+ 100 mV (Forced)					
	T_A = +25°C			25		mV
	V_{SENSE}(–)= V_{OUT}^- 100 mV (Forced)		125	150	175	mV
SHUTDOWN PIN THRESHOLD		V_6	0.55	0.8	2	V
OFF TIME[2]	C_T = 390 pF, I_{LOAD} = 700 mA	t_{OFF}	3.8	5	6	µs

NOTES
[1]All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.
[2]In applications where R_{SENSE} is placed at ground potential, the off time increases approximately 40%.

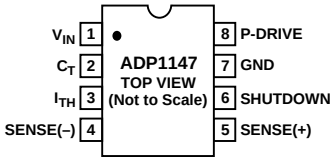
Specifications subject to change without notice.

PIN DESCRIPTION

Mnemonic	Function
V_{IN}	Input Voltage.
C_T	External Capacitor Connection. This capacitor sets the operating frequency of the device. The frequency is also dependent on the input voltage level.
I_{TH}	Error Amplifier Decoupling Pin. Pin 3 voltage level causes the comparator current threshold to increase.
SENSE(–)	This connects to internal resistive divider which senses the output voltage. Pin 4 is also the (–) input for the current comparator.
SENSE(+)	This provides the + input to the current comparator. The offset between Pins 4 and 5 together with R_{SENSE} establish the current trip threshold.
Shutdown	When this pin is pulled high, it keeps the MOSFET turned off. When the pin is pulled to ground, theADP1147 functions normally. This pin cannot be left floating.
GND	Independent ground lines must be connected separately to (a) the negative pin of C_{OUT} and (b) the cathode of the Schottky diode and the negative terminal of C_{IN}.
P-Drive	Provides high current drive for the MOSFET. Voltage swing is from V_{IN} to ground at this pin.

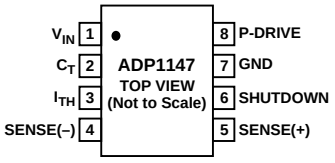
PIN CONFIGURATIONS

N Package
8-Lead Plastic DIP



T_{JMAX} = 125°C, 0_{JA} = 110°C/W

R Package
8-Lead Plastic SOIC



T_{JMAX} = 125°C, 0_{JA} = 150°C/W

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP1147 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

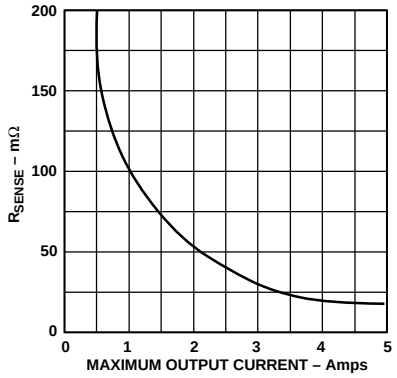


Figure 3. Selecting R_{SENSE} vs. Maximum Output Current

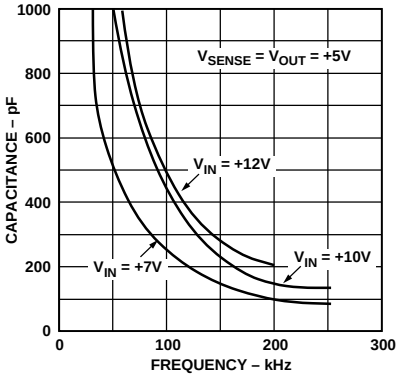


Figure 4. Operating Frequency vs. Timing Capacitor

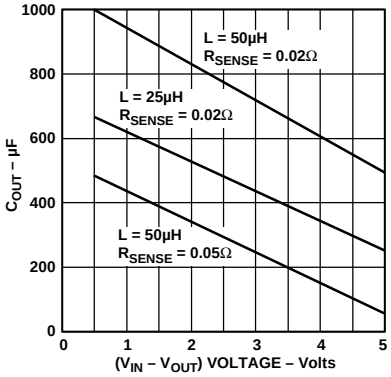


Figure 5. Selecting Minimum Output Capacitor vs. (V_{IN}–V_{OUT}) and Inductor

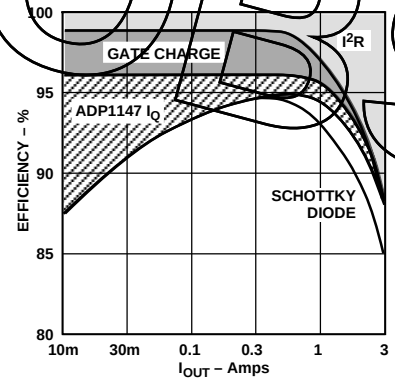
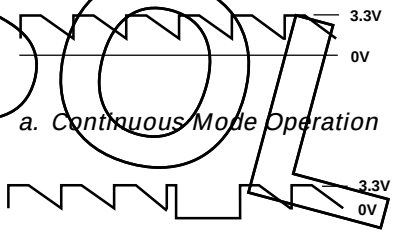


Figure 6. Typical Efficiency Losses



a. Continuous Mode Operation

b. Power Saving Mode

Figure 7. C_T Waveforms

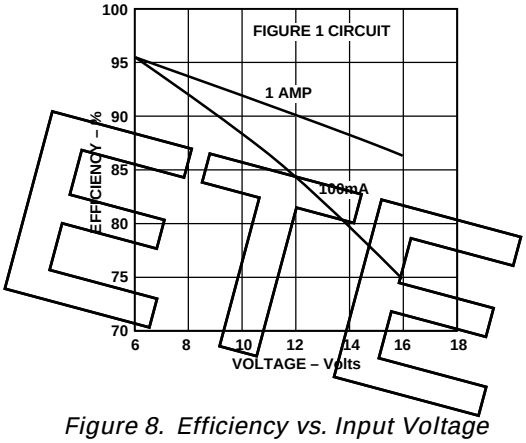


Figure 8. Efficiency vs. Input Voltage

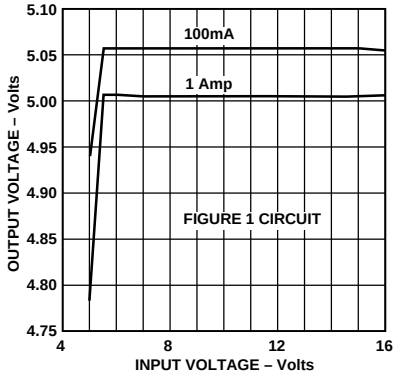


Figure 9. ADP1147-5 Output Voltage vs. Input Voltage

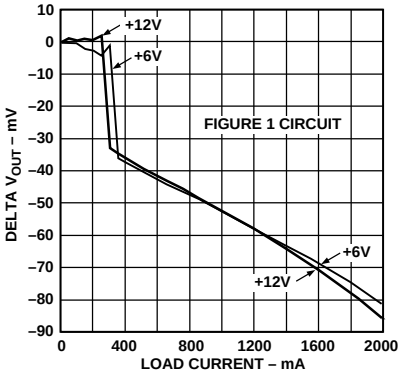


Figure 10. Load Regulation

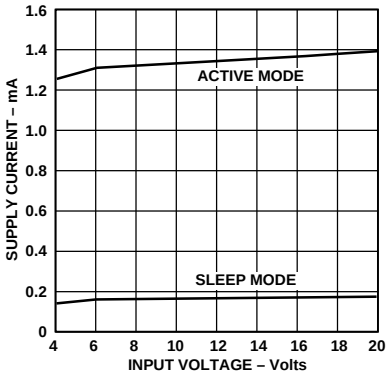


Figure 11. DC Supply Current

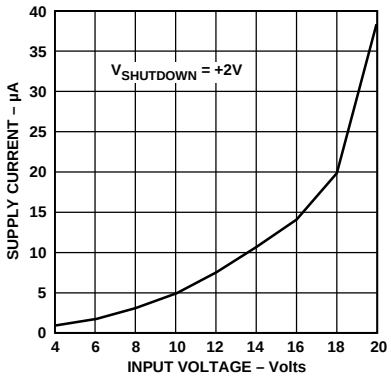


Figure 12. Supply Current in Shutdown

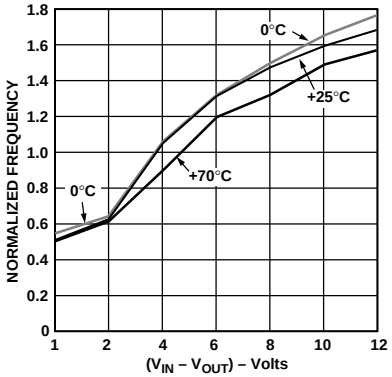


Figure 13. Operating Frequency vs. (V_{IN}–V_{OUT})

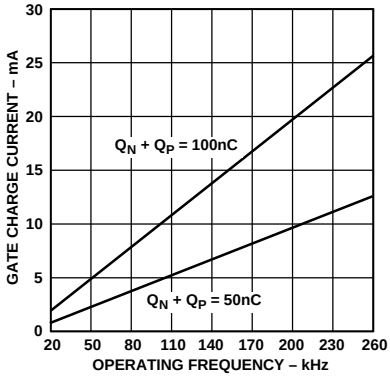


Figure 14. Gate Charge Supply Current

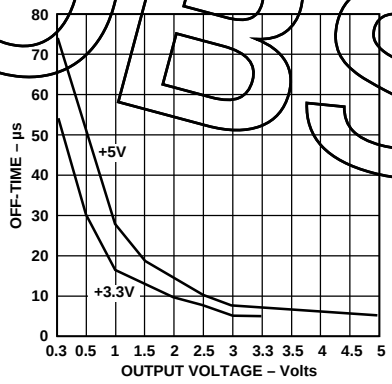


Figure 15. Off-Time vs. V_{OUT}

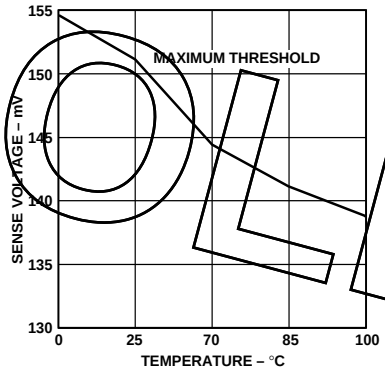


Figure 16. Current Sense Threshold Voltage

TEST CIRCUIT

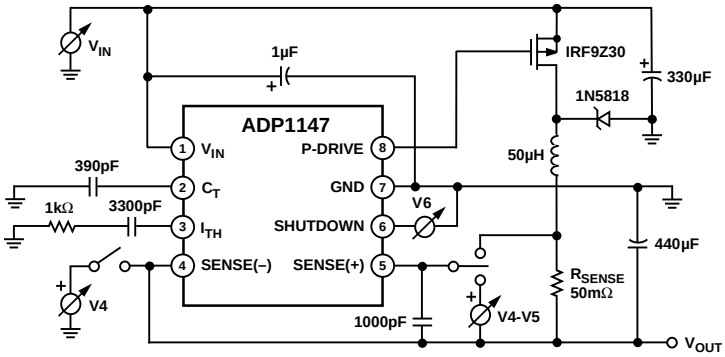


Figure 17.

APPLICATIONS

Description OF ADP1147 Operation*

(See Functional Diagram)

The ADP1147 uses a current mode, constant off time structure to switch an external P-channel MOSFET. The operating frequency of the device is determined by the value of the external capacitor connected to the C_T pin.

The output voltage is sensed by an internal voltage divider which is connected to the Sense(–) pin. A voltage comparator V, and a gain block G compare the values of the divided output voltage with a reference voltage of 1.25 V.

To maximize the efficiency, the ADP1147 automatically switches between two operational modes, power saving and continuous. The comparator is the main control element when the device is in its power saving mode while the gain block is the main control when the output voltage moves to continuous mode. During the continuous mode of the PMOS switch on cycle, the current comparator C monitors the voltage between the Sense(–) and Sense(+) pins. When the voltage level across the resistor reaches the threshold level, the P drive output is switched to V_{IN} which turns off the P-channel MOSFET. The timing capacitor on C_T is now able to discharge at a rate determined by the off time controller. The discharge current is made to be proportional to the value of the output voltage (measured at Sense(–)) to model the inductor current which decays at a rate that is proportional to the output voltage. When the voltage level on the timing capacitor has discharged to the threshold voltage level V_{TH1}, comparator T switches setting the flip flop. This forces the P drive output low and subsequently turns the P-channel MOSFET on. The sequence is then repeated.

As load current increases, the output voltage starts to reduce. This results in the output of the gain circuit increasing the level of the current comparator threshold, thus tracking the load current.

The power saving sequence is very similar to the continuous operation mode with the cycle being interrupted by the voltage comparator. When the output voltage is equal to or above the required regulated value, the P-Channel MOSFET is kept off by comparator V, and the timing capacitor discharges below V_{TH1}. At the point at which the timing capacitor discharges below V_{TH2}, comparator S trips causing the internal sleep bar to go low. The circuit is now in sleep mode and the power MOSFET is turned off. While the circuit remains in this mode, a significant amount of the circuit is turned off dropping the ground current from approximately 1.6 mA to a level of 160 µA. In this state the load current is supplied by the output capacitor. At the point at which the output voltage has been reduced by the level of hysteresis in comparator V, the power MOSFET is turned on once again and the procedure is repeated.

To prevent the current loop operation interfering with the power saving sequence, a built in offset (V_{OS}) is integrated into the gain stage. This prohibits the current comparator threshold from rising until the output voltage level has reduced below the minimum threshold. By utilizing a constant off time structure, the device operating frequency is a function of the input voltage. To reduce the effect of frequency variation as the device approaches dropout, the controller starts to increase the timing capacitor's discharge current as V_{IN} drops below V_{OUT}–1.5 V. While the device is in dropout, the MOSFET is on constantly.

*Component, voltage, current, etc., values are in SI-units (international standard) unless otherwise noted.

The typical application circuit for the ADP1147 is described in Figure 1. The selection of the appropriate external components is controlled by the load current and the selection begins with R_{SENSE}. Once R_{SENSE} value is determined, capacitor C_T and inductor L can be selected. The Power MOSFET and D_1 are then selected and finally capacitors C_{IN} and C_{OUT} are chosen and the feedback loop is compensated.

The circuit as described in Figure 1 can be structured so that input voltages up to 20 V can be accommodated. If the application requires a higher input voltage capability, then the ADP1149 should be considered.

R_{SENSE} Value for Output Current

The choice of R_{SENSE} is based on the required output current. The ADP1147 current comparator has a threshold range that extends from a minimum of 25 mV/R_{SENSE} to a maximum of 150 mV/R_{SENSE}. The current comparator threshold sets the peak of the inductor current, yielding a maximum output current, I_{MAX} equal to the peak value less half the peak-to-peak ripple current. For proper Power Saving Operation Mode, $I_{RIPPLE(P-P)}$ must be less than or equal to the minimum current comparator threshold of 25 mV.

The ADP1147 works well with values of R_{SENSE} from 20 mΩ to 200 mΩ. A graph for selecting R_{SENSE} versus maximum output current is given in Figure 3.

Solving for R_{SENSE} and allowing a margin for variations in the ADP1147 and external component values yields:

$$R_{SENSE} = 100/I_{MAX}\ [m\Omega]$$

The load current below which Power Saving Mode operation commences, $I_{POWER\text{-}SAVING}$ and the peak short circuit current, $I_{SC(PK)}$ both track I_{MAX}. Once R_{SENSE} has been chosen, $I_{POWER\text{-}SAVING}$ and $I_{SC(PK)}$ can be predicted from the following equations:

$$I_{POWER\ SAVING} \sim 15\ mV/R_{SENSE}$$

$$I_{SC(PK)} = 150\ mV/R_{SENSE}$$

The ADP1147 automatically extends t_{OFF} during a short circuit to allow sufficient time for the inductor current to decay between switch cycles. The resulting ripple current causes the average short circuit current $I_{SC(AVG)}$ to be reduced to approximately I_{MAX}.

L and C_T Value Selection for Operating Frequency

The ADP1147 uses a constant off-time architecture with t_{OFF} determined by an external timing capacitor C_T. Each time the P-channel MOSFET switch turns on, the voltage on C_T is reset to approximately 3.3 V. During the off-time, C_T is discharged by a current which is proportional to V_{OUT}. The voltage on C_T is analogous to the current in inductor L, which likewise decays at a rate proportional to V_{OUT}. Therefore the inductor value must track the timing capacitor value.

The value of C_T is calculated from the desired continuous mode operating frequency:

$$C_T = \frac{\left[1 - \frac{V_{OUT} + V_D}{V_{IN} + V_D}\right]}{1.3 \times 10^4 \times f}$$

where V_D is the drop across the Schottky diode.

A graph for selecting C_T versus frequency including the effects of input voltage is given in Figure 4. As the operating frequency is increased, the gate charge losses will reduce efficiency (see

Efficiency section). The full formula for operating frequency is given by:

$$f = \frac{\left[1 - \frac{V_{OUT} + V_D}{V_{IN} + V_D}\right]}{t_{OFF}}$$

where $t_{OFF} = 1.3 \times 10^4 \times C_T \times V_{REG}/V_{OUT}$.

V_{REG} is the desired output voltage (i.e., 5 V or 3.3 V); V_{OUT} is the measured output voltage. Thus $V_{REG}/V_{OUT} = 1$ in regulation.

Note that as V_{IN} decreases, the frequency also decreases. When the input to output voltage differential drops below 1.5 V, the ADP1147 reduces t_{OFF} by increasing the discharge current in C_T. This prevents audible operation before the device goes into dropout.

Once the frequency has been set by C_T, the inductor L must be chosen to provide no more than 25 mV/R_{SENSE} of peak-to-peak inductor ripple current. This is set by the equation:

$$\frac{25\,mV}{R_{SENSE}} = \frac{(V_{OUT} + V_D) \times t_{OFF}}{L_{MIN}} \text{ or}$$

$$L_{MIN} = \frac{(V_{OUT} + V_D) \times t_{OFF} \times R_{SENSE}}{25\,mV}$$

Substituting for t_{OFF} above gives the minimum required inductor value of:

$$L_{MIN} = 5.1 \times 10^5 \times R_{SENSE} \times C_T \times V_{REG}$$

As the inductor value is increased from the minimum value, the ESR requirements for the output capacitor are relaxed at the expense of efficiency. If too small of an inductor is used, the peak inductor current will be discontinuous before ADP1147 commences Power Saving Mode operation. A consequence of this is that the Power Saving Mode threshold will be lower and efficiency will be severely degraded at low currents.

Inductor Core

Once the minimum value for L is known, the selection of the inductor can be made. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy, or "Kool Mμ*"cores. Typical efficiency in Figure 2 reflects molypermalloy core. (Using Kool Mμ core, type CTX 50-4 by Coiltronix, reduces cost by half but the efficiency will be 1–2% less.) Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which causes the inductance to collapse abruptly when the peak design current is exceeded. This results in a sharp increase in inductor ripple current and the output voltage ripple which can cause the Power Saving Mode operation to be falsely triggered in the ADP1147. To prevent this action from occurring, do not allow the core to saturate.

*Kool My is a registered trademark of Magnetics, Inc.

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is "Kool Mμ." Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. Many new designs for surface mount are also available from, e.g., Coiltronics, which do not increase the component height significantly.

Power MOSFET

An external P-channel power MOSFET must be selected for use with the ADP1147. The main selection criteria for the power MOSFET is the threshold voltage $V_{GS(TH)}$ and on resistance $R_{DS(ON)}$.

The minimum input voltage determines whether a standard threshold or logic-level threshold MOSFET must be used. For $V_{IN} > 8$ V, a standard threshold MOSFET ($V_{GS(TH)} < 4$ V) may be used. If V_{IN} is expected to drop below 8 V, a logic level threshold MOSFET ($V_{GS(TH)} < 2.5$ V) is strongly recommended. When a logic level MOSFET is used, the ADP1147 supply voltage must be less than the absolute maximum V_{GS} ratings for the MOSFET (e.g., < ±8 V of IRF7304).

The maximum output current, I_{MAX}, determines the $R_{DS(ON)}$ requirement for power MOSFET. When the ADP1147 is operating in continuous mode, the simplifying assumption can be made that either the MOSFET or Schottky diode is always conducting the average load current. The duty cycles for the MOSFET and diode are given by:

$$\text{P-Channel Duty Cycle} = \frac{V_{OUT} + V_D}{V_{IN} + V_D}$$

$$\text{Schottky Diode Duty Cycle} = \frac{V_{IN} - V_D}{V_{IN} + V_D}$$

From the duty cycle, the required $R_{DS(ON)}$ for the MOSFET can be derived:

$$P\text{-}Ch_{RDS(ON)} = (V_{IN} + V_D) \times P_P / (V_{OUT} + V_D) \times I^2_{MAX} \times (1+\delta_p)$$

where P_p is the allowable power dissipation and δ_p is the temperature dependency of $R_{DS(ON)}$. P_P will be determined by efficiency and/or thermal requirements (see Efficiency section). (1+δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs. temperature curve, but δ = 0.007/°C can be used as an approximation for low voltage MOSFETs.

Output Diode

The Schottky diode D1 shown in Figure 1 will conduct during the off-time. It is important to adequately specify the diode peak current and average power dissipation so as not to exceed the diode ratings.

The most stressful condition for the output diode is under short circuit ($V_{OUT} = 0$). Under this condition, the diode must safely handle $I_{SC(PK)}$ at close to 100% duty cycle. Under normal load conditions, the average current conducted by the diode is:

$$I_{DI} = \frac{V_{IN} - V_{OUT}}{V_{IN} + V_D} \times (I_{LOAD})$$

Remember to keep lead lengths short and observe proper grounding (see Board Layout Suggestions) to avoid ringing and increased dissipation.

The forward voltage drop allowable in the diode is calculated from the maximum short circuit current as:

$$V_F \sim P_D / I_{SC(PK)}$$

where P_D is the allowable power dissipation and will be determined by efficiency and/or thermal requirements (see Efficiency section).

C_{IN} and C_{OUT}

In continuous mode, the source current of the P-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN} . To prevent large voltage transients, a low ESR input capacitor sized for the maximum rms current must be used. The maximum rms capacitor current is given by:

$$C_{IN} \text{ required } I_{RMS} \sim [V_{OUT}(V_{IN} - V_{OUT})]^{0.5} \times I_{MAX} / V_{IN}$$

This formula has a maximum at V_{IN} = 2 V_{OUT}, where I_{RMS} = $I_{OUT}/2$. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question. In addition to C_{IN}, a 0.1 µF to 1 µF decoupling capacitor is required on V_{IN}.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). The ESR of C_{OUT} must be less than twice the value of R_{SENSE} for proper operation of the ADP1147:

$$C_{OUT} \text{ required } ESR < 2\ R_{SENSE}$$

Optimum efficiency is obtained by making the ESR equal to R_{SENSE}. As the ESR is increased up to $2R_{SENSE}$, the efficiency degrades by less than 1%. If the ESR is greater than 2 R_{SENSE}, the voltage ripple on the output capacitor will prematurely trigger Power Saving Mode operation, resulting in disruption of continuous mode and an efficiency hit which can be several percent.

Manufacturers such as Nichicon and Sprague should be considered for high performance capacitors. The OS-CON semiconductor dielectric capacitor from Sprague has the lowest ESR for its size, at a somewhat higher price . Once the ESR requirement for C_{OUT} has been met, the rms current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

In surface-mount applications, multiple capacitors may have to be paralleled to meet the capacitance, ESR, or rms current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface-mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface-mount tantalum, available in case heights ranging from 2 mm to 4 mm. For example, if 200 µF/10 V is called for in an application requiring 3 mm height, two AVX 100 µF/10 V could be used. Consult the manufacturer for other specific recommendations.

At low supply voltages, a minimum capacitance at C_{OUT} is needed to prevent an undesirable low frequency operating mode, (see Figure 5). If C_{OUT} is made too small, the output ripple at low frequencies will be large enough to trip the voltage comparator. This causes the ADP1147 to operate in Power Saving Mode instead of continuous mode. The output remains in regulation at all times, however.

This effect becomes prevalent at lower values of R_{SENSE} and can be improved by higher frequency operation.

Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in dc (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD} \times (ESR)$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} until the regulator loop adapts to the current change and returns V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing which would indicate a stability problem. The external components shown in the Figure 1 circuit will prove adequate compensation for most applications.

A second, more severe transient is caused by hot switching in loads with large (>1 µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the inrush current to these capacitors below the current limit of your design.

Efficiency

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \textit{ Efficiency} = 100\% - (L1 + L2 + L3 + \ldots),$$

where $L1$, $L2$, etc., are the individual losses as a percentage of input power (For high efficiency circuits only small errors are incurred by expressing losses as a percentage of output power.)

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in ADP1147 circuits: (1) ADP1147 DC bias current, (2) MOSFET gate charge current, (3) $I^2 \times R$ losses, and 4. Voltage drop of the Schottky diode:

1. The dc supply current is the current which flows into V_{IN}, Pin 1, less the gate charge current. For V_{IN} = 10 V the ADP1147 dc supply current is 160 µA for no load, and increases proportionally with load up to a constant 1.6 mA after the ADP1147 has entered continuous mode. Because the dc bias current is drawn from V_{IN}, the resulting loss increases with input voltage. For V_{IN} = 10 V the dc bias losses are generally less than 1% for load currents over 30 mA. However, at very low load currents the dc bias current accounts for nearly all of the loss.

2. MOSFET gate charge current results from switching the gate capacitance of the power MOSFET. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} which is typically much larger than the dc supply current. In continuous mode, $I_{GATECHG} = f (Q_P)$. The typical gate charge for a 135 mΩ P-channel power MOSFET is 40 nC. This results in $I_{GATECHG}$ = 4 mA in 100 kHz continuous operation for a 2% to 3% typical midcurrent loss with V_{IN} = 10 V

   Note that the gate charge loss increases directly with both input voltage and operating frequency. This is the principal reason why the highest efficiency circuits operate at moderate frequencies. Furthermore, it argues against using a larger MOSFET than necessary to control $I^2 \times R$ losses.

3. $I^2 \times R$ losses are easily predicted from the dc resistances of the MOSFET, inductor, and current shunt. In continuous mode, the average output current flows through L and R_{SENSE}, but is "chopped" between the P-channel and Schottky diode. The MOSFET $R_{DS(ON)}$ multiplied by the P-channel duty cycle can be summed with the resistances of L and R_{SENSE} to obtain $I^2 \times R$ losses. For example, if the $R_{DS(ON)}$ = 100 mΩ, R_L = 150 mΩ, and R_{SENSE} = 50 mΩ, then the total resistance is 300 mΩ at $V_{IN} = 2\ V_{OUT}$. This results in losses ranging from 3% to 10% as the output current increases from 0.5A to 2A. $I^2 \times R$ losses cause the efficiency to roll-off at high output currents.

4. The Schottky diode is a major source of power loss at high currents and gets worse at high input voltages. The diode loss is calculated by multiplying the forward voltage drop times the Schottky diode duty cycle multiplied by the load current.

Figure 6 shows how the efficiency losses add up in a typical ADP1147 regulator. The gate charge loss is responsible for the majority of the efficiency lost in the midcurrent region. If Power Saving Mode operation was not employed at low currents, the gate charge loss alone would cause the efficiency to drop to unacceptable levels. With Power Saving Mode operation, the dc supply current represents the lone (and unavoidable) loss component which continues to become a higher percentage as output current is reduced. As expected, the $I^2 \times R$ losses and Schottky diode loss dominate at high load currents.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses, MOSFET switching losses, and inductor core losses, generally account for less than 2% total additional loss.

Development Example

As a design example, assume V_{IN} = 5 V (nominal), V_{OUT} = 3.3 V, V_D = 0.4, I_{MAX} = 1A and f = 100 kHz, R_{SENSE}. C_T, and L can immediately be calculated:

$$R_{SENSE} = 100\ mV / 1 = 100\ m\Omega$$

$$t_{OFF} = (1/100\ kHz) \times [1 - (3.7/5.4)] = 3.15\ \mu s$$

$$C_T = 3.15\ \mu s / (1.3 \times 10^4) = 242\ pF$$

$$L = 5.1 \times 10^5 \times 0.1\ \Omega \times 242\ pF \times 3.3\ V = 41\ \mu H$$

Assume that the MOSFET dissipation is to be limited to P_P = 250 mW.

If T_A = 50°C and the thermal resistance of the MOSFET is 50°C/W, then the junction temperatures will be 63°C and $\delta_P = 0.007 \times (63–25) = 0.27$. The required $R_{DS(ON)}$ for the MOSFET can now be calculated:

$$P\text{-}Ch\ R_{DS(ON)} = 5(0.25) / 3.3(1)^2\ (1.27) = 300\ m\Omega$$

The P-channel requirement can be met by a IRF7204 or Si9430DY. Note that the most stringent requirement for the Schottky diode is with V_{OUT} = 0 (i.e., short circuit). During a continuous short circuit, the worst case Schottky diode dissipation rises to:

$$P_D \sim I_{SC(AVG)} \times V_D$$

With the 100 mΩ sense resistor $I_{SC(AVG)}$ = 1A will result, increasing the 0.4 V Schottky diode dissipation to 0.4 W.

C_{IN} will require an rms current rating of at least 0.5A at temperature, and C_{OUT} will require an ESR of 100 mΩ for optimum efficiency.

Now allow V_{IN} to drop to its minimum value. At lower input voltages the operating frequency will decrease and the P-channel will be conducting most of the time causing the power dissipation to increase. At $V_{IN(MIN)}$ = 4.5 V, the frequency will decrease and the P-channel power dissipation increases.

At $V_{IN}(MIN) = 4.5V$: $f_{MIN} = \frac{1}{3.15\,\mu s}\left(1 - \frac{3.7}{4.9}\right) = 78\ kHz$

$$P_P = \frac{3.3(0.125\ \Omega)(1A)^2(1.27)}{4.5} = 116\ mW$$

This last step is necessary to assure that the power dissipation and junction temperature of the P-channel are not exceeded.

Troubleshooting Hints

Since efficiency is critical to ADP1147 applications, it is very important to verify that the circuit is functioning correctly in both continuous and Power Saving Mode operation. The waveform to monitor is the voltage on the timing capacitor, Pin 2, (see Figure 7).

In continuous mode ($I_{LOAD} > I_{POWER\ SAVING}$) the voltage on the C_T pin should be a sawtooth with a 0.9 V p-p swing as shown in Figure 7a. This voltage should never dip below 2 V.

When load currents are low ($I_{LOAD} < I_{POWER\ SAVING}$), Power Saving Mode operation occurs. The voltage on the C_T pin now falls to ground for periods of time as shown in Figure 7b. During this time, the ADP1147 is in sleep mode with the quiescent current reduced to 160 µA.

The inductor current should also be monitored. Look to verify that the peak-to-peak ripple current in continuous mode operation is approximately the same as in Power Saving Mode operation. If the voltage on Pin 2 is falling to ground at high output current, it indicates poor decoupling or grounding.

Board Layout Suggestions

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the ADP1147. These items are also illustrated graphically in the layout diagram of Figure 18. Check the following in your layout:

1. Are the signal and power grounds segregated? The ADP1147 ground (Pin 7) must return separately to (a) the power and (b) signal grounds. The power ground (a) returns to the source anode of the Schottky diode, and (–) plate of C_{IN}, which should have as short lead lengths as possible. The signal ground (b) connects to the (–) plate of C_{OUT}.
2. Does the ADP1147 Sense (–) (Pin 4) connect to a point close to R_{SENSE} and the (+) plate of C_{OUT}?
3. Are the Sense (–) and Sense (+) leads routed together with minimum PC trace spacing? The 1000 pF capacitor between Pins 4 and 5 should be as close as possible to the ADP1147.
4. Does the (+) plate of C_{IN} connect to the source of the P-channel MOSFET as closely as possible? This capacitor provides the ac current to the P-channel MOSFET.
5. Is the input decoupling capacitor (0.1 µF/1 µF) connected closely between V_{IN} (Pin 1) and ground (Pin 7)? This capacitor carries the MOSFET driver peak currents.
6. Is the Shutdown (Pin 6) actively pulled to ground during normal operation? The shutdown pin is high impedance and must not be allowed to float.

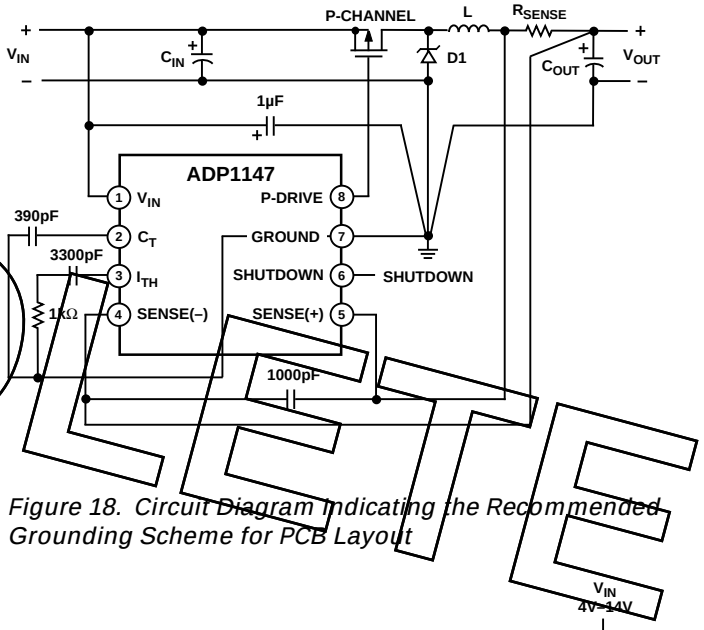


Figure 18. Circuit Diagram Indicating the Recommended Grounding Scheme for PCB Layout

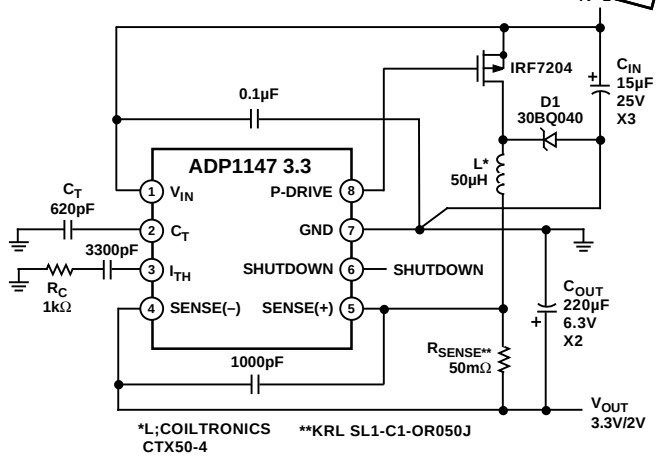
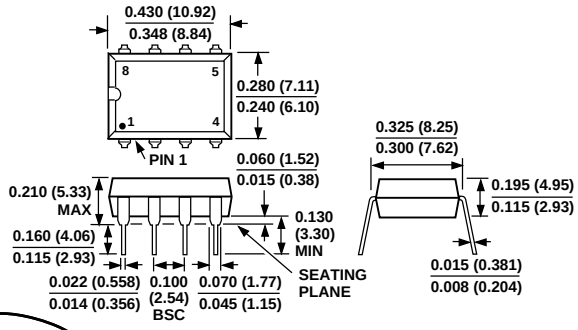


Figure 19. 3.3 V/2A Regulator

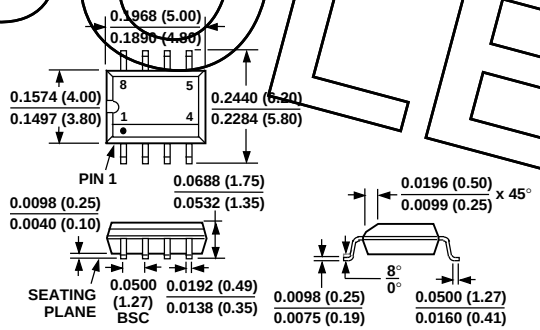
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Plastic DIP
(N-8)



8-Lead Plastic SOIC
(SO-8)



000000000

PRINTED IN U.S.A.