Ordering number: EN2780B

CMOS LSI

No.2780B

# LC7932,7932M

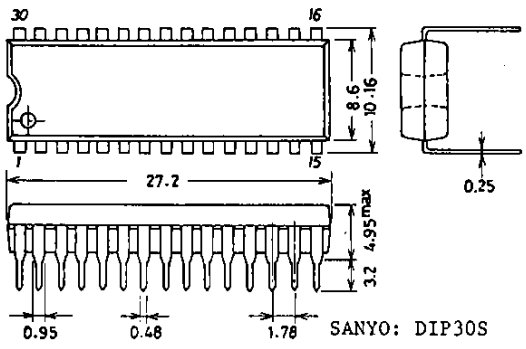
## 16-Bit LED Driver

The LC7932,7932M are LSIs that contain a 16-bit bidirectional shift register and are capable of direct driving a multiple lighting LED (dot matrix or dot array). The LC7932,7932M are especially suited for use in LED display panel,PPC photosensitive drum LED erase head applications.

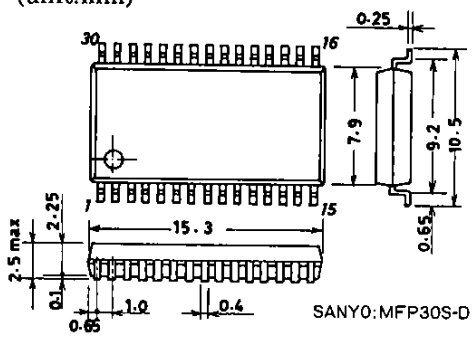
**Features**

- Silicon gate C-MOS device capable of high-speed, high-current drive
- High-speed shiftable 16-bit bidirectional shift register/16-bit latch/output control circuit/16-bit N-channel transistor·open drain output transistor on chip
- Serial shift data is shifted on the positive transition of the clock (CLOCK) pulse.
- The data latch circuit outputs input data when the latch control ($\overline{\text{LATCH}}$) pin is at "L" level and holds output data when the latch control ($\overline{\text{LATCH}}$) pin is at "H" level.
- Maximum ratings of driver output: $V_O = +15V$, $I_{OL} = 30mA$(STATIC) /120mA(DYNAMIC).
- Operating voltage of logic unit: $V_{DD} = 4.5V$ to $5.5V$
- Operating clock frequency: $f_{CLK}$ = DC to 5MHz(max)
- Package : LC7932 : DIP30S
  LC7932M : MFP30S
- The bidirectional shift register is so designed as to cause a shift to occur in the SI to SO direction when L/R = "L" level and in the SO to SI direction when L/R = "H" level.
- When a high level is applied to the LSET pin ("latch set"), the latch data is set to the high level. The latch data does not change when the LSET pin is low or open.

**Package Dimensions** 3061 [LC7932]
(unit:mm)




**Package Dimensions** 3073A [LC7932M]
(unit:mm)





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**Absolute Maximum Ratings** at Ta = 25°C

| | | | | unit |
|---|---|---|---|---|
| Maximum Supply Voltage | $V_{DD}$ max | | −0.3 to +7.0 | V |
| Input Voltage | $V_I$ | | −0.3 to $V_{DD}$+0.3 | V |
| Output Voltage | $V_O$(1) | SOUT(SIN) output | −0.3 to $V_{DD}$+0.3 | V |
| | $V_O$(2) | D1 to D16 output,output Tr OFF | 15 | V |
| Output Current | $I_O$ | D1 to D16 output,per output pin | 30 | mA |
| Operating Temperature | Topr | | −25 to +85 | °C |
| Storage Temperature | Tstg | (Note) | −35 to +125 | °C |
| Allowable Power Dissipation | Pd max | LC7932 Ta = 85°C | 400 | mW |
| | | LC7932M Ta = 85°C | 270 | mW |

(Note) When mounting the MFP package version, do not dip it in solder.

**Allowable Operating Conditions** at Ta = −25°C to +85°C

| | | | | min | typ | max | unit |
|---|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | $V_{DD}$ | | 4.5 | | 5.5 | V |
| Input "H"-Level Voltage | $V_{IH}$ | SIN(SOUT),CLOCK, $\overline{\text{LATCH}}$,BEO, $\overline{\text{STROBE}}$, LSET,L/R | | 0.8$V_{DD}$ | | $V_{DD}$ | V |
| Input "L"-Level Voltage | $V_{IL}$ | SIN(SOUT),CLOCK, $\overline{\text{LATCH}}$,BEO, $\overline{\text{STROBE}}$, LSET,L/R | | $V_{SS}$(L) | | 0.2$V_{DD}$ | V |
| Clock Frequency | fCLK | CLOCK | Duty:50% | | | 5.0 | MHz |
| Clock Pulse Width | $t_{W\phi}$ | CLOCK | | 75 | | | ns |
| Clock Rise/Fall Time | $t_r$,$t_f$ | CLOCK | | | | 200 | ns |
| Data Setup Time | $t_{DS}$ | SIN(SOUT) CLOCK | | 100 | | | ns |
| Data Hold Time | $t_{DH}$ | SIN(SOUT) CLOCK | | 50 | | | ns |
| Latch Pulse Widh | $t_{WL}$ | $\overline{\text{LATCH}}$ | | 100 | | | ns |

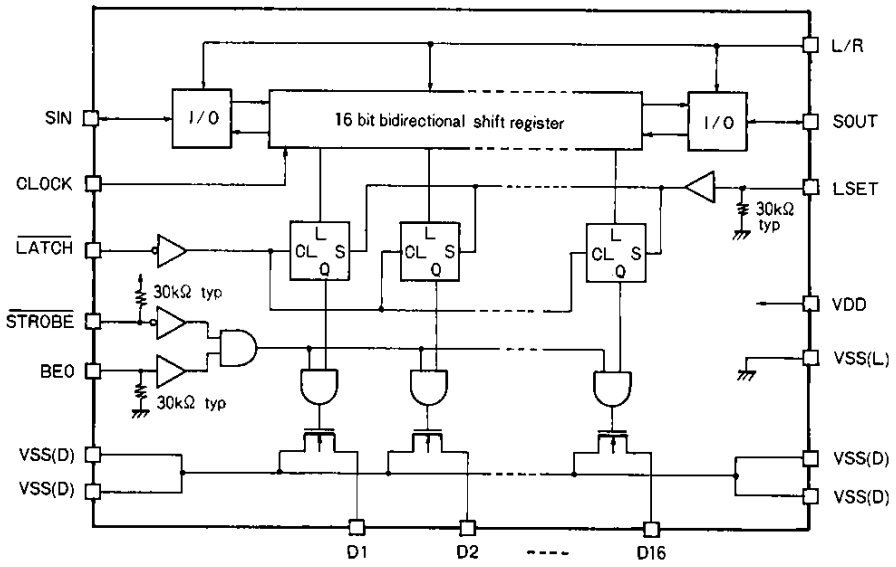
**Electrical Characteristics** at Ta = 25°C

| | | | | | min | typ | max | unit |
|---|---|---|---|---|---|---|---|---|
| Input "H"-Level Current | $I_{IH}$(1) | SIN(SOUT),CLOCK, $\overline{\text{LATCH}}$,L/R | | | | | 10 | μA |
| | $I_{IH}$(2) | BEO,LSET | | | | 170 | | μA |
| Input "L"-Level Current | $I_{IL}$(1) | SIN(SOUT),CLOCK, $\overline{\text{LATCH}}$,L/R | | | −10 | | | μA |
| | $I_{IL}$(2) | $\overline{\text{STROBE}}$ | | | | 170 | | μA |
| Output "H"-Level Voltage | $V_{OH}$ | SOUT(SIN) | $I_{OH}$ = −0.5mA, $V_{DD}$ = 5V | $V_{DD}$−0.5 | | | | V |
| Output "L"-Level Voltage | $V_{OL}$(1) | SOUT(SIN) | $I_{OL}$ = 0.5mA, $V_{DD}$ = 5V | | | | 0.5 | V |
| | $V_{OL}$(2) | D1 to D16 | $I_{OL}$ = 30mA, $V_{DD}$ = 5V | | | | 0.5 | V |
| Output OFF-State Leakage Current | $I_{OFF}$ | D1 to D16 | $V_O$ = 15V | | | | 20 | μA |
| Input Capacitance | $C_{IN}$ | CLOCK | | | | 5.0 | | pF |
| Operating Current | $I_{DD}$ | $V_{DD}$ | fCLK = 5MHz, $V_{DD}$ = 5V, All outputs with no load | | | | 5 | mA |

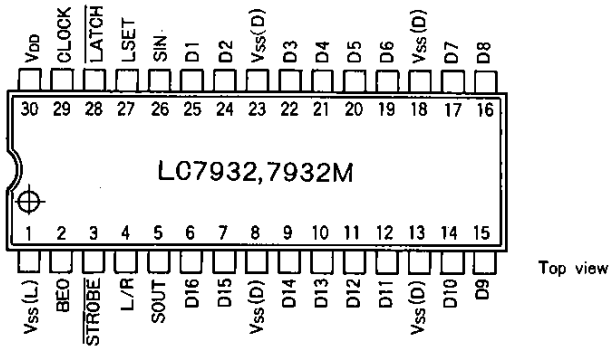
**Switching Characteristics** at Ta = 25°C

| | | | | | min | typ | max | unit |
|---|---|---|---|---|---|---|---|---|
| Clock Latch Delay Width | $t_{CL}$ | CLOCK,$\overline{\text{LATCH}}$ | | $V_{DD}$=5V | 100 | | | ns |
| Latch Clock Delay Width | $t_{LC}$ | CLOCK,$\overline{\text{LATCH}}$ | | $V_{DD}$=5V | 0 | | | ns |
| Output"H"-Level Propagation Delay Time | $t_{PLH}$(1) | $\overline{\text{LATCH}}$ D1 to D16 | Dn; (RL=1.0kΩ, CL=15pF) | $V_{DD}$=5V | | | 400 | ns |
| | $t_{PLH}$(2) | BEO,$\overline{\text{STROBE}}$ D1 to 16 | Dn; (RL=1.0kΩ, CL=15pF) | $V_{DD}$=5V | | | 300 | ns |
| | $t_{PLH}$(3) | CLOCK,SOUT(SIN) | SOUT;CL=15pF | $V_{DD}$=5V | | | 200 | ns |
| Output"L"-Level Propagation Delay Time | $t_{PHL}$(1) | $\overline{\text{LATCH}}$,LSET D1 to D16 | Dn; (RL=1.0kΩ, CL=15pF) | $V_{DD}$=5V | | | 200 | ns |
| | $t_{PHL}$(2) | BEO,$\overline{\text{STROBE}}$ D1 to D16 | Dn; (RL=1.0kΩ, CL=15pF) | $V_{DD}$=5V | | | 100 | ns |
| | $t_{PHL}$(3) | CLOCK,SOUT(SIN) | SOUT;CL=15pF | $V_{DD}$=5V | | | 200 | ns |

## Equivalent Circuit




## Pin Assignment

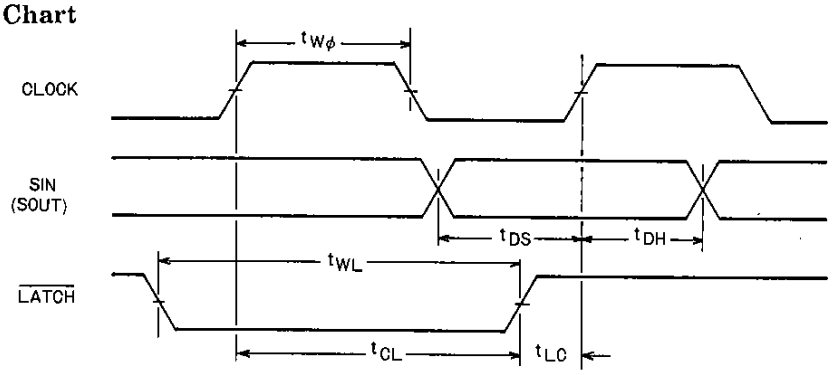



The package comes in two types - DIP30S and MFP30S.

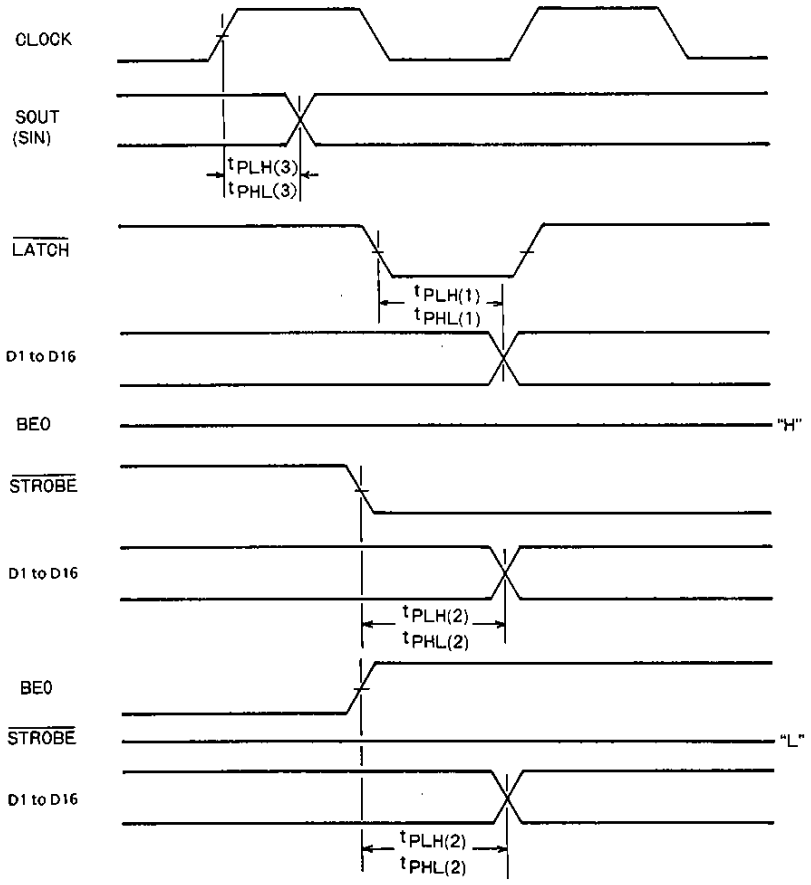
## LED Driver ON/OFF Truth Table

| Latch Data (Q) | BEO | $\overline{\text{STROBE}}$ | LED Driver |
|---|---|---|---|
| 0 | 0 | 0 | OFF |
| 1 | 0 | 0 | OFF |
| 0 | 1 | 0 | OFF |
| 1 | 1 | 0 | ON Driver ON |
| 0 | 0 | 1 | OFF |
| 1 | 0 | 1 | OFF |
| 0 | 1 | 1 | OFF |
| 1 | 1 | 1 | OFF |

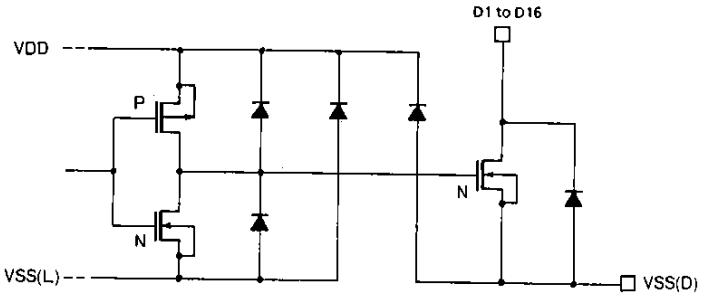
## Input Data Timing Chart




## Output Data Timing Chart



## Equivalent Circuit for Output Driver Section




(Note) L/R="H" level : ( )