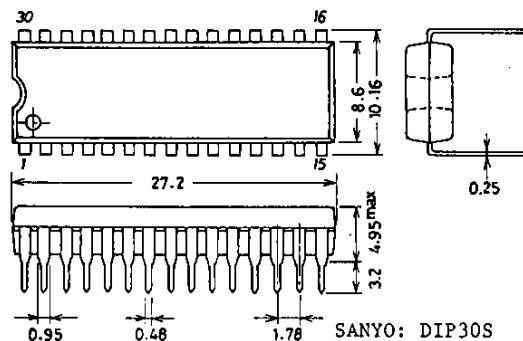


The LC7932,7932M are LSIs that contain a 16-bit bidirectional shift register and are capable of direct driving a multiple lighting LED (dot matrix or dot array). The LC7932,7932M are especially suited for use in LED display panel, PPC photosensitive drum LED erase head applications.

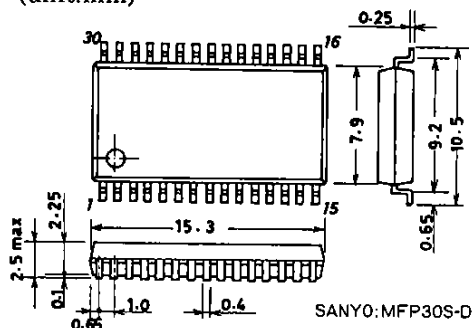
Features

- Silicon gate C-MOS device capable of high-speed, high-current drive
- High-speed shiftable 16-bit bidirectional shift register/16-bit latch/output control circuit/16-bit N-channel transistor-open drain output transistor on chip
- Serial shift data is shifted on the positive transition of the clock (CLOCK) pulse.
- The data latch circuit outputs input data when the latch control (LATCH) pin is at "L" level and holds output data when the latch control (LATCH) pin is at "H" level.
- Maximum ratings of driver output: $V_O = +15V$, $I_{OL} = 30mA$ (STATIC)/120mA(DYNAMIC).
- Operating voltage of logic unit: $V_{DD} = 4.5V$ to $5.5V$
- Operating clock frequency: $f_{CLK} = DC$ to $5MHz$ (max)
- Package: LC7932 : DIP30S
LC7932M : MFP30S
- The bidirectional shift register is so designed as to cause a shift to occur in the SI to SO direction when L/R="L" level and in the SO to SI direction when L/R="H" level.
- When a high level is applied to the LSET pin ("latch set"), the latch data is set to the high level. The latch data does not change when the LSET pin is low or open.

Package Dimensions 3061 [LC7932]
(unit:mm)



Package Dimensions 3073A [LC7932M]
(unit:mm)



LC7932,7932M

Absolute Maximum Ratings at Ta = 25°C

				unit
Maximum Supply Voltage	V _{DD} max		-0.3 to +7.0	V
Input Voltage	V _I		-0.3 to V _{DD} + 0.3	V
Output Voltage	V _O (1)	SOUT(SIN) output	-0.3 to V _{DD} + 0.3	V
	V _O (2)	D1 to D16 output, output Tr OFF	15	V
Output Current	I _O	D1 to D16 output, per output pin	30	mA
Operating Temperature	Topr		-25 to +85	°C
Storage Temperature	Tstg	(Note)	-35 to +125	°C
Allowable Power Dissipation	Pd max	LC7932 Ta = 85°C	400	mW
		LC7932M Ta = 85°C	270	mW

(Note) When mounting the MFP package version, do not dip it in solder.

Allowable Operating Conditions at Ta = -25°C to +85°C

			min	typ	max	unit
Supply Voltage	V _{DD}	V _{DD}	4.5		5.5	V
Input "H"-Level Voltage	V _{IH}	SIN(SOUT), CLOCK, LATCH, BEO, STROBE, LSET, L/R	0.8V _{DD}		V _{DD}	V
Input "L"-Level Voltage	V _{IL}	SIN(SOUT), CLOCK, LATCH, BEO, STROBE, LSET, L/R	V _{SS} (L)	0.2V _{DD}		V
Clock Frequency	fCLK	CLOCK			5.0	MHz
Clock Pulse Width	t _{wφ}	CLOCK	75			ns
Clock Rise/Fall Time	t _r , t _f	CLOCK			200	ns
Data Setup Time	t _{DS}	SIN(SOUT) CLOCK	100			ns
Data Hold Time	t _{DH}	SIN(SOUT) CLOCK	50			ns
Latch Pulse Width	t _{WL}	LATCH	100			ns

Electrical Characteristics at Ta = 25°C

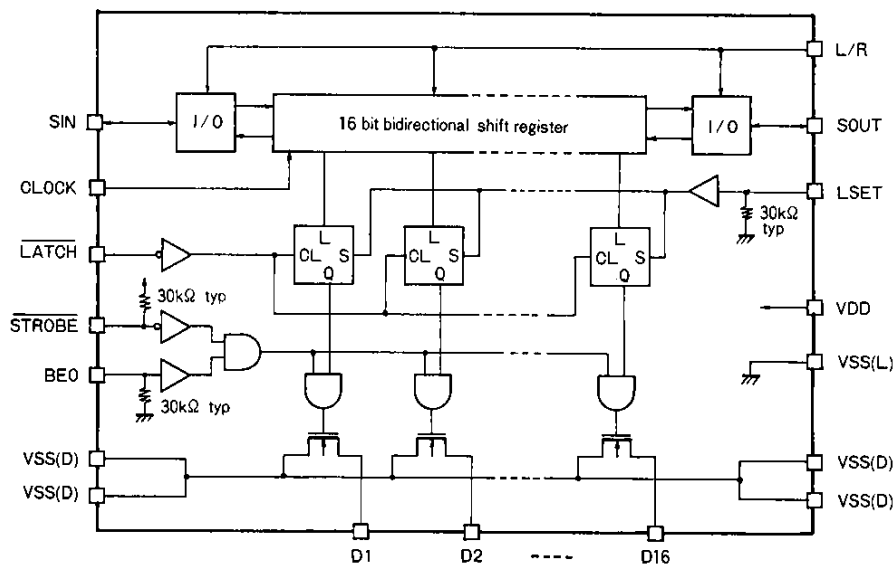
				min	typ	max	unit
Input "H"-Level Current	I _{IH} (1)	SIN(SOUT), CLOCK, LATCH, L/R				10	μA
	I _{IH} (2)	BEO, LSET			170		μA
Input "L"-Level Current	I _{IL} (1)	SIN(SOUT), CLOCK, LATCH, L/R	-10				μA
	I _{IL} (2)	STROBE			170		μA
Output "H"-Level Voltage	V _{OH}	SOUT(SIN)	I _{OH} = -0.5mA, V _{DD} = 5V	V _{DD} - 0.5			V
Output "L"-Level Voltage	V _{OL} (1)	SOUT(SIN)	I _{OL} = 0.5mA, V _{DD} = 5V			0.5	V
	V _{OL} (2)	D1 to D16	I _{OL} = 30mA, V _{DD} = 5V			0.5	V
Output OFF-State Leakage Current	I _{OFF}	D1 to D16	V _O = 15V			20	μA
Input Capacitance	C _{IN}	CLOCK			5.0		pF
Operating Current	I _{DD}	V _{DD}	fCLK = 5MHz V _{DD} = 5V All outputs with no load			5	mA

LC7932,7932M

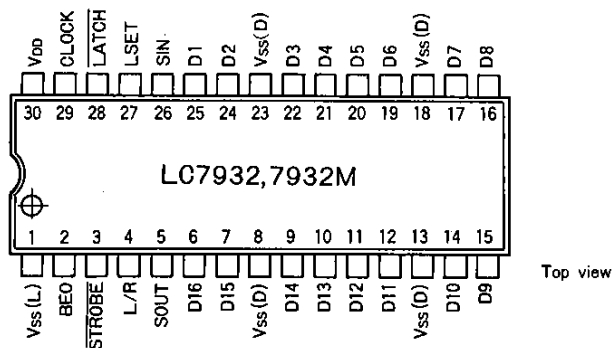
Switching Characteristics at Ta = 25°C

				min	typ	max	unit
Clock Latch Delay Width	t_{CL}	CLOCK, LATCH		$V_{DD}=5V$	100		ns
Latch Clock Delay Width	t_{LC}	CLOCK, LATCH		$V_{DD}=5V$	0		ns
Output "H"-Level Propagation Delay Time	$t_{PLH}(1)$	LATCH D1 to D16	Dn; $\left. \begin{matrix} RL=1.0k\Omega \\ CL=15pF \end{matrix} \right\}$	$V_{DD}=5V$		400	ns
Output "H"-Level Propagation Delay Time	$t_{PLH}(2)$	BEO, STROBE D1 to 16	Dn; $\left. \begin{matrix} RL=1.0k\Omega \\ CL=15pF \end{matrix} \right\}$	$V_{DD}=5V$		300	ns
Output "L"-Level Propagation Delay Time	$t_{PLH}(3)$	CLOCK, SOUT(SIN)	SOUT; $CL=15pF$	$V_{DD}=5V$		200	ns
Output "L"-Level Propagation Delay Time	$t_{PHL}(1)$	LATCH, LSET D1 to D16	Dn; $\left. \begin{matrix} RL=1.0k\Omega \\ CL=15pF \end{matrix} \right\}$	$V_{DD}=5V$		200	ns
Output "L"-Level Propagation Delay Time	$t_{PHL}(2)$	BEO, STROBE D1 to D16	Dn; $\left. \begin{matrix} RL=1.0k\Omega \\ CL=15pF \end{matrix} \right\}$	$V_{DD}=5V$		100	ns
Output "L"-Level Propagation Delay Time	$t_{PHL}(3)$	CLOCK, SOUT(SIN)	SOUT; $CL=15pF$	$V_{DD}=5V$		200	ns

Equivalent Circuit



Pin Assignment

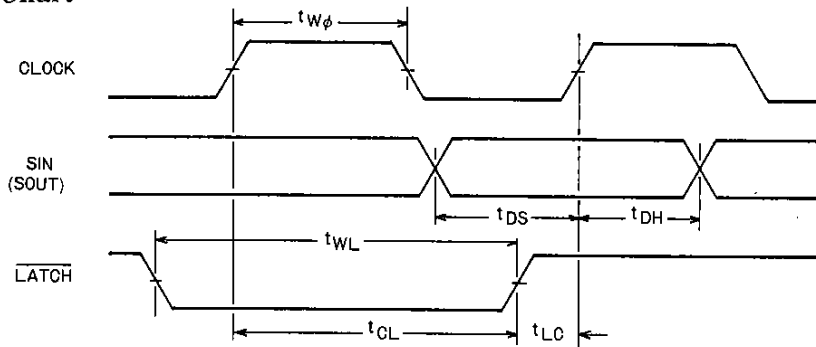


The package comes in two types - DIP30S and MFP30S.

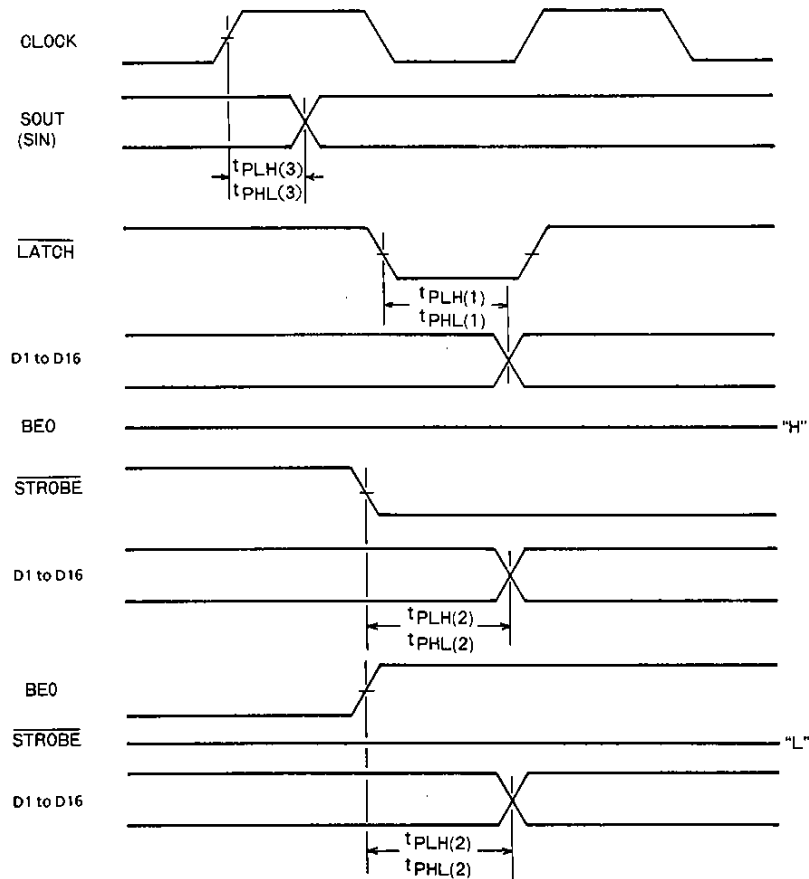
LED Driver ON/OFF Truth Table

Latch Data (Q)	BE0	STROBE	LED Driver
0	0	0	OFF
1	0	0	OFF
0	1	0	OFF
1	1	0	ON Driver ON
0	0	1	OFF
1	0	1	OFF
0	1	1	OFF
1	1	1	OFF

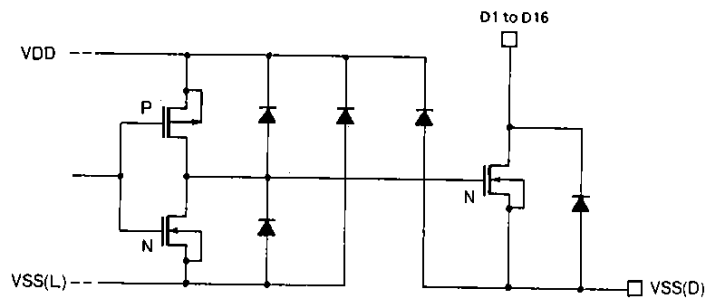
Input Data Timing Chart



Output Data Timing Chart



Equivalent Circuit for Output Driver Section



(Note) L/R="H" level : ()

- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
 - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
 - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.