Ordering number : EN5378

CMOS LSI

LC72322R, 72323R

Single-Chip Microcontroller with PLL and LCD Driver

Overview

The LC72322R and LC72323R are single-chip microcontrollers for use in electronic tuning applications. These ICs include on chip both LCD drivers and a PLL circuit that can operate at up to 150 MHz. The LC72322R and LC72323R feature that these ICs are reversed pin-assignment versions of LC72322 and LC72323 respectively and have the equal functions and specifications to theirs respectively.

Functions

- Stack: Eight levels
- Fast programmable divider
- General-purpose counters: HCTR for frequency measurement and LCTR for frequency or period measurement
- LCD driver for displays with up to 56 segments (1/2 duty, 1/2 bias)
- Program memory (ROM): 4095 (8 KB) 16-bit digits: LC72322R
  3071 (6 KB) 16-bit digits: LC72323R
- Data memory (RAM): 256 4-bit digits
- All instructions are single-word instructions
- Cycle time: 2.67 µs, 13.33 µs, or 40.00 µs (option)
- Unlock FF: 0.55 µs detection, 1.1 µs detection
- Timer FF: 1 ms, 5ms, 25ms, 125ms
- Input ports*: One dedicated key input port and one high-breakdown voltage port
- Output ports*: Two dedicated key output ports, one high-breakdown voltage open-drain port
  Two CMOS output ports (of which one can be switched to be used as LCD driver outputs)
  Seven CMOS output ports (mask option switchable to use as LCD ports)
- I/O ports*: One switchable between input and output in four-bit units and one switchable between input and output in bit units

  Note: * Each port consists of four bits.
- Program runaway can be detected and a special address set (Programmable watchdog timer).
- Voltage detection type reset circuit
- One 6-bit A/D converter
- Two 8-bit D/A converters (PWM): LC72322R only
- One external interrupt
- Hold mode for RAM backup
- Sense FF for hot/cold startup determination
- PLL: 4.5 to 5.5 V
- CPU: 3.5 to 5.5 V
- RAM: 1.3 to 5.5 V
- LC72P321R as OTP used
- Package: QIP80DR

This LSI can easily use CCB that is SANYO's original bus format.

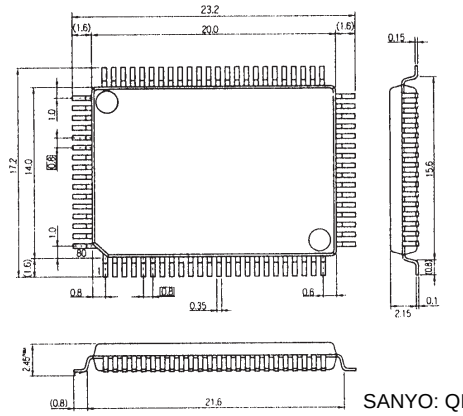
- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

Package Dimensions

unit: mm

3223-QFP80DR

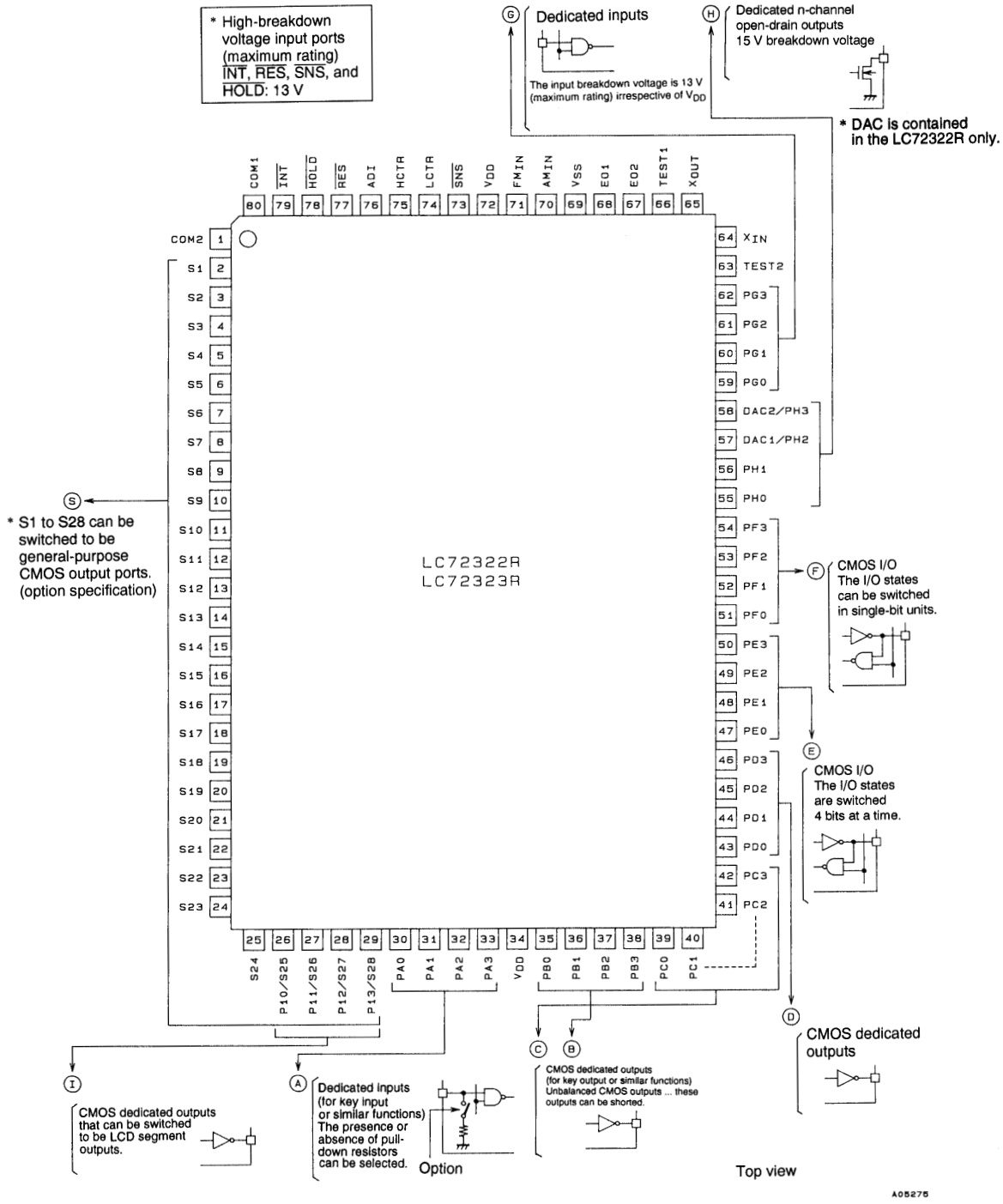
[LC72322R, LC72323R]



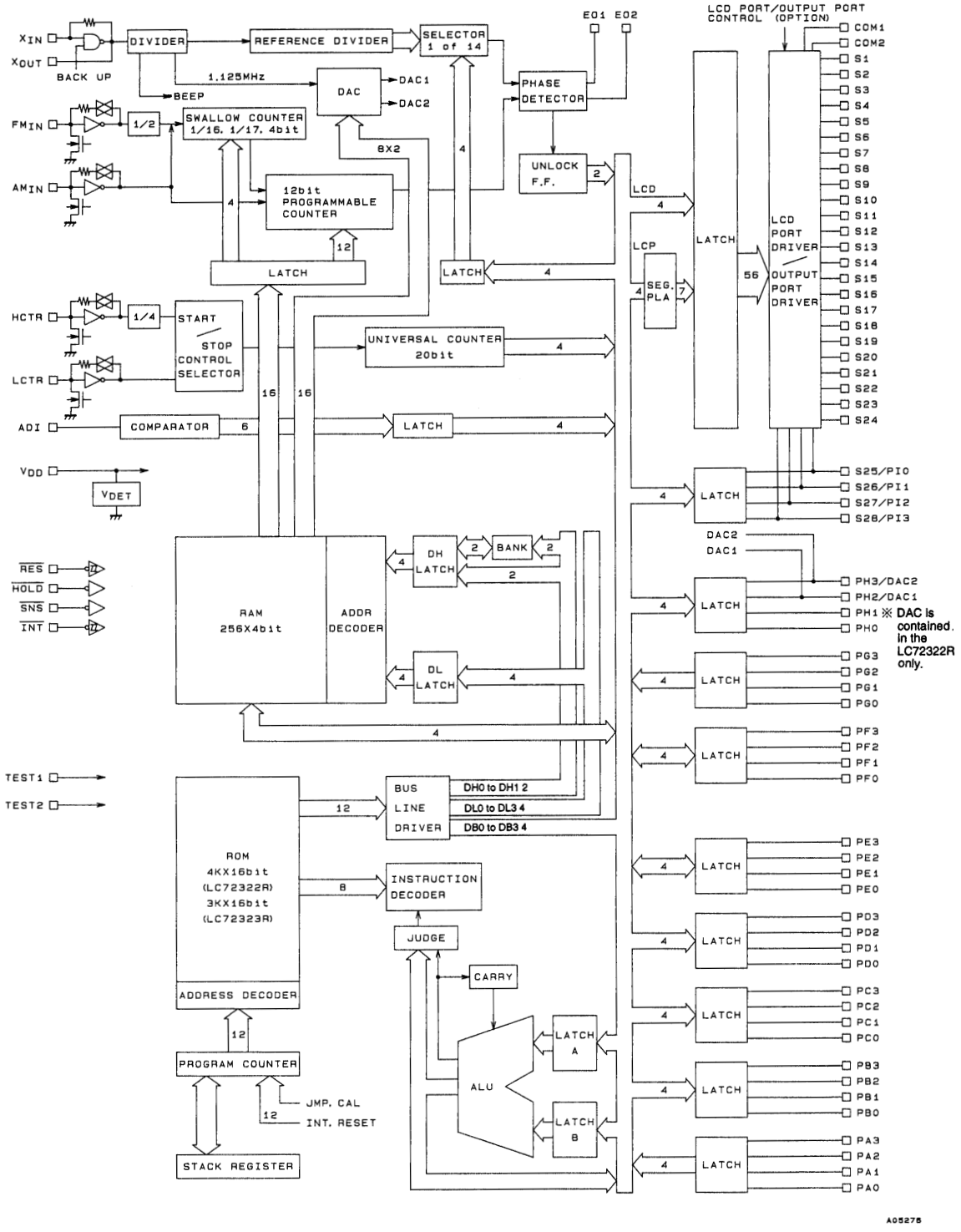
SANYO: QIP80DR

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

Pin Assignment



Block Diagram



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +6.5	V
Input voltage	$V_{IN}1$	$\overline{HOLD}$, $\overline{INT}$, $\overline{RES}$, ADI, $\overline{SNS}$, and the G port	–0.3 to +13	V
	$V_{IN}2$	Inputs other than $V_{IN}1$	–0.3 to V_{DD} + 0.3	V
Output voltage	$V_{OUT}1$	H port	–0.3 to +15	V
	$V_{OUT}2$	Outputs other than $V_{OUT}1$	–0.3 to V_{DD} + 0.3	V
Output current	$I_{OUT}1$	All D and H port pins	0 to 5	mA
	$I_{OUT}2$	All E and F port pins	0 to 3	mA
	$I_{OUT}3$	All B and C port pins	0 to 1	mA
	$I_{OUT}4$	S1 to S28 and all I port pins	0 to 1	mA
Allowable power dissipation	Pd max	Ta = –40 to +85°C	300	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–45 to +125	°C

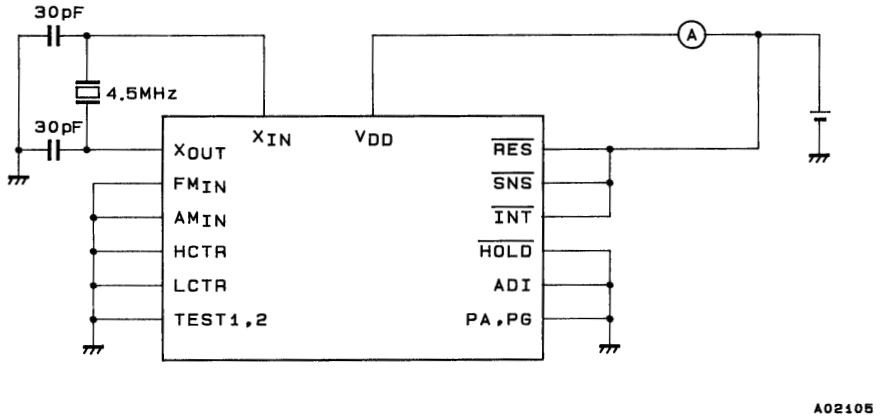
Allowable Operating Ranges at Ta = –40 to +85°C, V_{DD} = 3.5 to 5.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}1$	CPU and PLL operating	4.5		5.5	V
	$V_{DD}2$	CPU operating	3.5		5.5	V
	$V_{DD}3$	Memory retention voltage	1.3		5.5	V
Input high level voltage	$V_{IH}1$	G port	0.7 V_{DD}		8.0	V
	$V_{IH}2$	$\overline{RES}$, $\overline{INT}$, $\overline{HOLD}$	0.8 V_{DD}		8.0	V
	$V_{IH}3$	$\overline{SNS}$	2.5		8.0	V
	$V_{IH}4$	A port	0.6 V_{DD}		V_{DD}	V
	$V_{IH}5$	PE0, PE2 and F ports	0.7 V_{DD}		V_{DD}	V
	$V_{IH}6$	LCTR (period measurement), $V_{DD}1$, PE1 and PE3	0.8 V_{DD}		V_{DD}	V
Input low level voltage	$V_{IL}1$	G port	0		0.3 V_{DD}	V
	$V_{IL}2$	$\overline{RES}$, $\overline{INT}$, PE1, PE3	0		0.2 V_{DD}	V
	$V_{IL}3$	$\overline{SNS}$	0		1.3	V
	$V_{IL}4$	A port	0		0.2 V_{DD}	V
	$V_{IL}5$	PE0, PE2 and F ports	0		0.3 V_{DD}	V
	$V_{IL}6$	LCTR (period measurement), $V_{DD}1$	0		0.2 V_{DD}	V
	$V_{IL}7$	$\overline{HOLD}$	0		0.4 V_{DD}	V
Input frequency	$f_{IN}1$	XIN	4.0	4.5	5.0	MHz
	$f_{IN}2$	FMIN, $V_{IN}2$, $V_{DD}1$	10		130	MHz
	$f_{IN}3$	FMIN, $V_{IN}3$, $V_{DD}1$	10		150	MHz
	$f_{IN}4$	AMIN (L), $V_{IN}4$, $V_{DD}1$	0.5		10	MHz
	$f_{IN}5$	AMIN (H), $V_{IN}5$, $V_{DD}1$	2.0		40	MHz
	$f_{IN}6$	HCTR, $V_{IN}6$, $V_{DD}1$	0.4		12	MHz
	$f_{IN}7$	LCTR (frequency), $V_{IN}7$, $V_{DD}1$	100		500	kHz
	$f_{IN}8$	LCTR (period), $V_{IH}6$, $V_{IL}6$, $V_{DD}1$	1		20×10^3	Hz
Input amplitude	$V_{IN}1$	XIN	0.50		1.5	Vrms
	$V_{IN}2$	FMIN	0.10		1.5	Vrms
	$V_{IN}3$	FMIN	0.15		1.5	Vrms
	$V_{IN}4$, 5	AMIN	0.10		1.5	Vrms
	$V_{IN}6$, 7	LCTR, HCTR	0.10		1.5	Vrms
Input voltage range	$V_{IN}8$	ADI	0		V_{DD}	V

Electrical Characteristics for the Allowable Operating Ranges

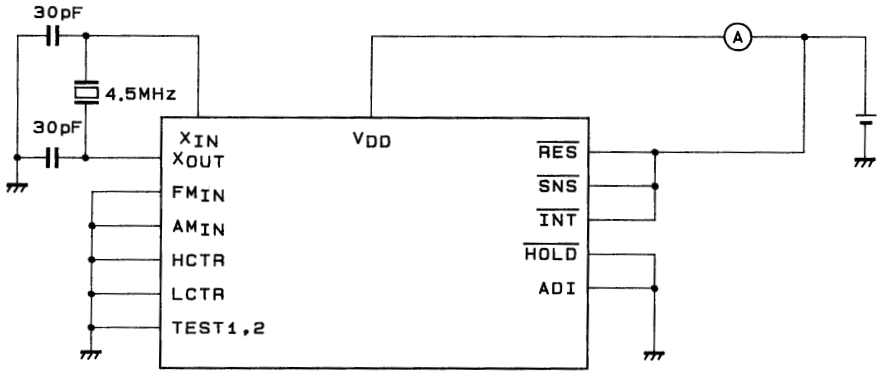
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Hysteresis	V_H	LCTR (period), $\overline{RES}$, $\overline{INT}$, PE1, PE3	0.1 V_{DD}			V
Rejected pulse width	P_{REJ}	$\overline{SNS}$			50	µs
Power-down detection voltage	V_{DET}		2.7	3.0	3.3	V
Input high level current	$I_{IH}1$	$\overline{INT}$, $\overline{HOLD}$, $\overline{RES}$, ADI, $\overline{SNS}$, and G port: V_I = 5.5 V			3.0	µA
	$I_{IH}2$	A, E, and F ports: E and F ports with outputs off, A port with no R_{PD}, $V_I = V_{DD}$			3.0	µA
	$I_{IH}3$	XIN: $V_I = V_{DD}$ = 5.0 V	2.0	5.0	15	µA
	$I_{IH}4$	FMIN, AMIN, HCTR, LCTR: $V_I = V_{DD}$ = 5.0 V	4.0	10	30	µA
	$I_{IH}5$	A port: With an R_{PD}, $V_I = V_{DD}$ = 5.0 V		50		µA
Input low level current	$I_{IL}1$	$\overline{INT}$, $\overline{HOLD}$, $\overline{RES}$, ADI, $\overline{SNS}$, and the G port: $V_I = V_{SS}$			3.0	µA
	$I_{IL}2$	A, E, and F ports: E and F ports with outputs off, A port with no R_{PD}, $V_I = V_{SS}$			3.0	µA
	$I_{IL}3$	XIN: $V_{IN} = V_{SS}$	2.0	5.0	15	µA
	$I_{IL}4$	FMIN, AMIN, HCTR, LCTR: $V_I = V_{SS}$	4.0	10	30	µA
Input floating voltage	V_{IF}	A port: With an R_{PD}			0.05 V_{DD}	V
Pull-down resistance	R_{PD}	A port: With an R_{PD}, V_{DD} = 5.0 V	75	100	200	kΩ
Output high level off leakage current	$I_{OFFH}1$	EO1, EO2: $V_O = V_{DD}$		0.01	10	nA
	$I_{OFFH}2$	B, C, D, E, F, and I ports: $V_O = V_{DD}$			3.0	µA
	$I_{OFFH}3$	H port: $V_O = V_{DD}$			5.0	µA
Output low level off leakage current	$I_{OFFL}1$	EO1, EO2: $V_O = V_{SS}$		0.01	10	nA
	$I_{OFFL}2$	B, C, D, E, F, and I ports: $V_O = V_{SS}$			3.0	µA
Output high level voltage	$V_{OH}1$	B and C ports: I_O = 1 mA	V_{DD} – 2.0	V_{DD} – 1.0	V_{DD} – 0.5	V
	$V_{OH}2$	E and F ports: I_O = 1 mA	V_{DD} – 1.0			V
	$V_{OH}3$	EO1, EO2: I_O = 500 µA	V_{DD} – 1.0			V
	$V_{OH}4$	XOUT: I_O = 200 µA	V_{DD} – 1.0			V
	$V_{OH}5$	S1 to S28 and the I port: I_O = –0.1 mA	V_{DD} – 1.0			V
	$V_{OH}6$	D port: I_O = 5 mA	V_{DD} – 1.0			V
	$V_{OH}7$	COM1, COM2: I_O = 25 µA	V_{DD} – 0.75	V_{DD} – 0.5	V_{DD} – 0.3	V
Output low level voltage	$V_{OL}1$	B and C ports: I_O = 50 µA	0.5	1.0	2.0	V
	$V_{OL}2$	E and F ports: I_O = 1 mA			1.0	V
	$V_{OL}3$	EO1, EO2: I_O = 500 µA			1.0	V
	$V_{OL}4$	XOUT: I_O = 200 µA			1.0	V
	$V_{OL}5$	S1 to S28 and the I port: I_O = 0.1 mA			1.0	V
	$V_{OL}6$	D port: I_O = 5 mA			1.0	V
	$V_{OL}7$	COM1, COM2: I_O = 25 µA	0.3	0.5	0.75	V
	$V_{OL}8$	H port: I_O = 5 mA, $V_{DD}1$	(150 Ω) 0.75		(400 Ω) 2.0	V
Output middle level voltage	V_M1	COM1, COM2: V_{DD} = 5.0 V, I_O = 25 µA	2.0	2.5	3.0	V
A/D conversion error		ADI: $V_{DD}1$	–1/2		+1/2	LSB
Current drain	$I_{DD}1$	$V_{DD}1$, $f_{IN}2$ = 130 MHz		15	20	mA
	$I_{DD}2$	$V_{DD}2$, PLL stopped, CT = 2.67 µs (HOLD mode, Figure 1)		1.5		mA
	$I_{DD}3$	$V_{DD}2$, PLL stopped, CT = 13.33 µs (HOLD mode, Figure 1)		1.0		mA
	$I_{DD}4$	$V_{DD}2$, PLL stopped, CT = 40.00 µs (HOLD mode, Figure 1)		0.7		mA
	$I_{DD}5$	V_{DD} = 5.5 V, oscillator stopped, Ta = 25°C (BACK UP mode, Figure 2)			5	µA
		V_{DD} = 2.5 V, oscillator stopped, Ta = 25°C (BACK UP mode, Figure 2)			1	µA

Test Circuits



Note: PB to PF, PH, and PI are all open. However, PE and PF are specified as output.

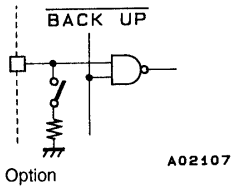
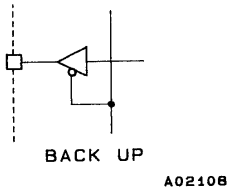
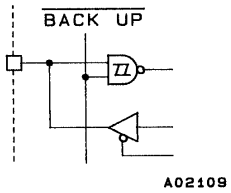
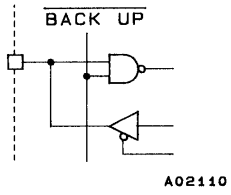
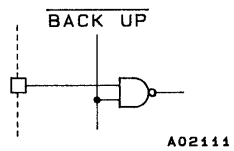
Figure 1 $I_{DD}2$ to $I_{DD}4$ in HOLD Mode



Note: PA to PI, S1 to S4, COM1, and COM2 are all open.

Figure 2 $I_{DD}5$ in BACK UP Mode

Pin Functions

Pin	Pin No.	Functions	I/O	I/O circuit type
PA0 PA1 PA2 PA3	30 31 32 33	Low-threshold type dedicated input ports These pins can be used, for example, for key data acquisition. Built-in pull-down resistors can be specified as an option. This option is in 4-pin units, and cannot be specified for individual pins. Input through these pins is disabled in BACKUP mode.	Input	
PB0 PB1 PB2 PB3 PC0 PC1 PC2 PC3	35 36 37 38 39 40 41 42	Dedicated output ports Since the output transistor impedances are unbalanced CMOS, these pins can be effectively used for functions such as key scan timing. These pins go to the output high-impedance state in BACKUP mode. These pins go to the low level during a reset, i.e., when the $\overline{RES}$ pin is low.	Output	
PD0 PD1 PD2 PD3	43 44 45 46	Dedicated output ports These are normal CMOS outputs. These pins go to the output high-impedance state in BACKUP mode. These pins go to the low level during a reset, i.e., when the $\overline{RES}$ pin is low.		
PE0 PE1 PE2 PE3	47 48 49 50	I/O ports These pins are switched between input and output as follows: Once an input instruction (IN, TPT, or TPF) is executed, these pins latch in the input mode. Once an output instruction (OUT, SPB, or RPB) is executed, they latch in the output mode. These pins go to the input mode during a reset, i.e., when the $\overline{RES}$ pin is low. In BACKUP mode these pins go to the input mode with input disabled.	I/O	PE1, PE3  Others 
PF0 PF1 PF2 PF3	51 52 53 54	I/O ports These pins are switched between input and output by the FPC instruction. The I/O states of this port can be specified for individual pins. These pins go to the input mode during a reset, i.e., when the $\overline{RES}$ pin is low. In BACKUP mode these pins go to the input mode with input disabled.		
PG0 PG1 PG2 PG3	59 60 61 62	Dedicated input ports Input through these pins is disabled in BACKUP mode.	Input	

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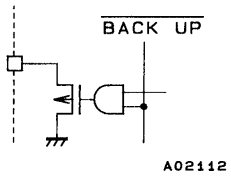
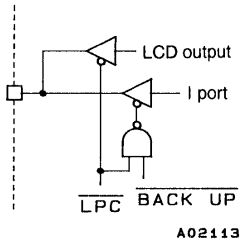
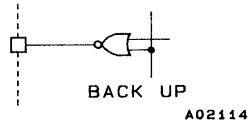
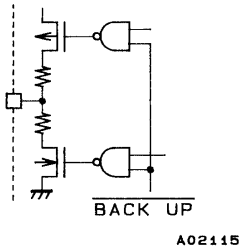
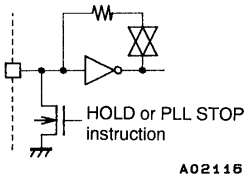
Pin	Pin No.	Functions	I/O	I/O circuit type
PH0 PH1 PH2/DAC*1 PH3/DAC*2	55 56 57 58	Dedicated output ports Since these pins are high-breakdown voltage n-channel transistor open-drain outputs, they can be effectively used for functions such as band power supply switching. And, PH2 and PH3 can also be used for DAC1 and DAC2 output ports respectively. (*: DAC is contained in LC72322R only.) These ports go to the high impedance state during a reset, i.e., when the $\overline{RES}$ pin is low, and in BACKUP mode.	Output	
PI0/S25 PI1/S26 PI2/S27 PI3/S28	26 27 28 29	Dedicated output ports While these pins have a CMOS output circuit structure, they can be switched to function as LCD drivers. Their function is switched by the SS and RS instructions. These pins cannot be switched individually. The LCD driver function is selected and a segment-off signal is output when power is first applied or when $\overline{RES}$ is low. These pins are held at the low level in BACKUP mode. Note that when the general-purpose port use option is specified, these pins output the contents of IPORT when LPC is 1, and the contents of the general-purpose output port LATCH when LPC is 0.	Output	
S1 to S24	2 to 25	LCD driver segment outputs A frame frequency of 100 Hz and a 1/2 duty, 1/2 bias drive type are used. A segment-off signal is output when power is first applied or when $\overline{RES}$ is low. These pins are held at the low level in BACKUP mode. The use of these pins as general-purpose output ports can be specified as an option.	Output	
COM1 COM2	80 1	LCD driver common outputs A 1/2 duty, 1/2 bias drive type is used. The output when power is first applied or when $\overline{RES}$ is low is identical to the normal operating mode output. These pins are held at the low level in BACKUP mode.	Output	
FMIN	71	FM VCO (local oscillator) input The input must be capacitor coupled. The input frequency range is from 10 to 130 MHz. (Max. 150 MHz)	Input	
AMIN	70	AM VCO (local oscillator) input The input must be capacitor coupled The band supported by this pin can be selected using the PLL instruction. High (2 to 40 MHz) → SW Low (0.5 to 10 MHz) → LW and MW		

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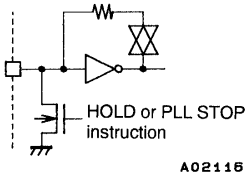
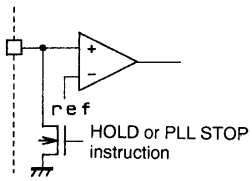
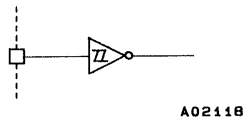
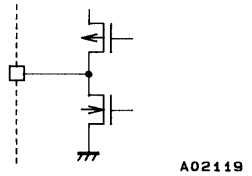
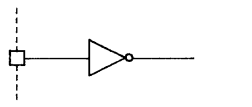
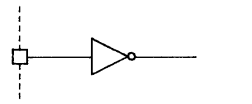
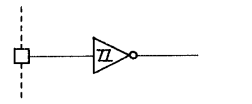
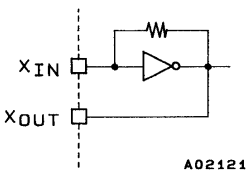
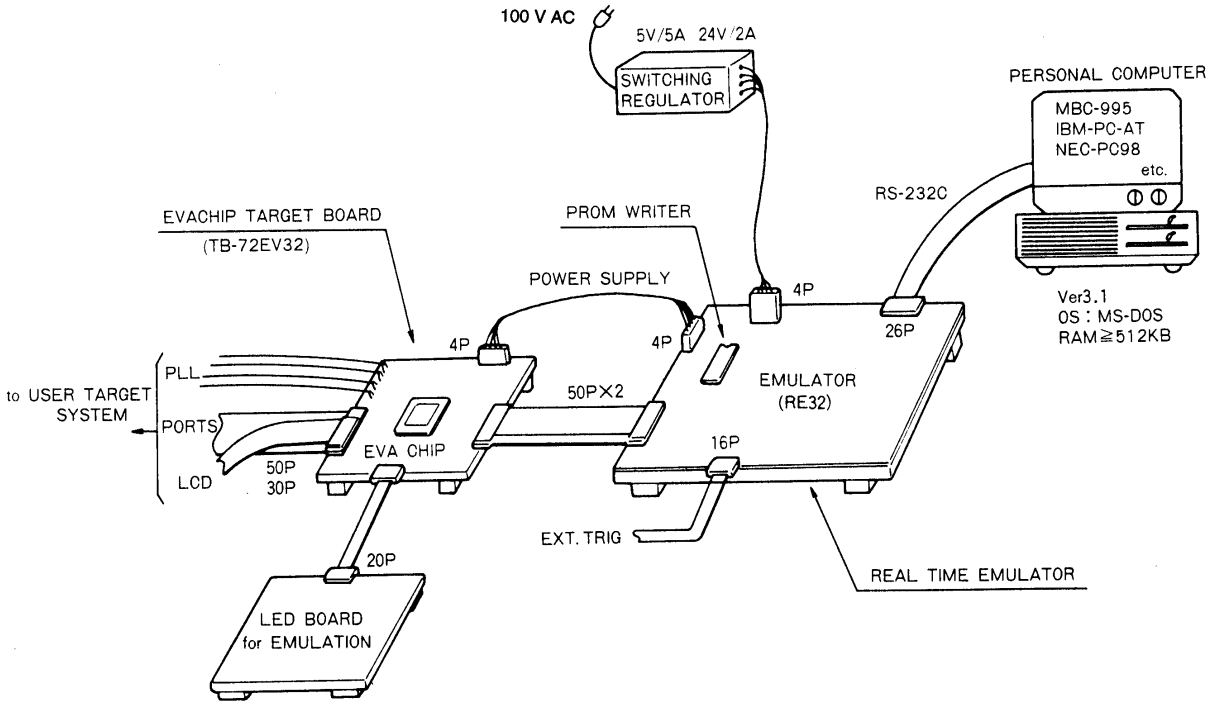
Pin	Pin No.	Functions	I/O	I/O circuit type
HCTR	75	Universal counter input The input must be capacitor coupled. The input frequency range is from 0.4 to 12 MHz. This input can be effectively used for FM IF or AM IF counting.	Input	
LCTR	74	Universal counter input The input must be capacitor coupled for input frequencies in the range 100 to 150 kHz. Capacitor coupling is not required for input frequencies from 1 Hz to 20 kHz. This input can be effectively used for AM IF counting.		
ADI	76	A/D converter input A 1.28 ms period is required for a 6-bit sequential comparison conversion. The full scale input is ((63/96) · V_{DD}) for a data value of 3FH.	Input	
INT	79	External interrupt request input An interrupt is generated when the INTEN flag is set (by an SS instruction) and a falling edge is input.	Input	
EO1 EO2	68 67	Reference frequency and programmable divider phase comparison error outputs Charge pump circuits are built in. EO1 and EO2 are the same.	Output	
$\overline{SNS}$	73	Input pin used to determine if a power outage has occurred in BACKUP mode This pin can also be used as a normal input port.	Input	
$\overline{HOLD}$	78	Input pin used to force the ICs to HOLD mode The IC goes to HOLD mode when the HOLDEN flag is set (by an SS instruction) and the $\overline{HOLD}$ input goes low. A high-breakdown voltage circuit is used so that this input can be used in conjunction with the normal power switch.	Input	
$\overline{RES}$	77	System reset input This signal should be held low for 75 ms after power is first applied to effect a power-up reset. The reset starts when a low level has been input for at least six reference clock cycles.	Input	
XIN XOUT	64 65	Crystal oscillator connections (4.5 MHz) A feedback resistor is built in.	Input Output	
TEST1 TEST2	66 63	LSI test pins. These pins must be connected to V_{SS}.	—	
V_{DD} V_{SS}	34, 72 69	Power supply	—	

Mask Options

No.	Description	Selections
1	WDT (watchdog timer) inclusion selection	WDT included
		No WDT
2	Port A pull-down resistor inclusion selection	Pull-down resistors included
		No pull-down resistors
3	Cycle time selection	2.67 µs
		13.33 µs
		40.00 µs
4	LCD port/general-purpose port selection	LCD ports
		General-purpose output ports

Development Environment

- The LC72P321R is used for OTP.
- The LC72EV321 is used as the evaluation chip.
- A total debugging system is available in which the TB-72EV32 evaluation chip board and the RE32 multifunction emulator are controlled by a personal computer.



LC72322R, 72323R Instruction Table

Abbreviations:
ADDR: Program memory address [12 bits]
b: Borrow
B: Bank number [2 bits]
C: Carry
DH: Data memory address high (row address) [2 bits]
DL: Data memory address low (column address) [4 bits]
I: Immediate data [4 bits]
M: Data memory address
N: Bit position [4 bits]
Pn: Port number [4 bits]
r: General register (one of the locations 00 to 0FH in bank 0)
Rn: Register number [4 bits]
( ): Contents of register or memory
( )N: Contents of bit N of register or memory

Instruction Group	Mnemonic	Operand		Function	Operation	Machine code															
		1st	2nd			D15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	D0
Addition instructions	AD	r	M	Add M to r	r ← (r) + (M)	0	1	0	0	0	0	DH		DL				Rn			
	ADS	r	M	Add M to r, then skip if carry	r ← (r) + (M) skip if carry	0	1	0	0	0	1	DH		DL				Rn			
	AC	r	M	Add M to r with carry	r ← (r) + (M) + C	0	1	0	0	1	0	DH		DL				Rn			
	ACS	r	M	Add M to r with carry, then skip if carry	r ← (r) + (M) + C skip if carry	0	1	0	0	1	1	DH		DL				Rn			
	AI	M	I	Add I to M	M ← (M) + I	0	1	0	1	0	0	DH		DL				I			
	AIS	M	I	Add I to M, then skip if carry	M ← (M) + I skip if carry	0	1	0	1	0	1	DH		DL				I			
	AIC	M	I	Add I to M with carry	M ← (M) + I + C	0	1	0	1	1	0	DH		DL				I			
	AICS	M	I	Add I to M with carry, then skip if carry	M ← (M) + I + C skip if carry	0	1	0	1	1	1	DH		DL				I			
Subtraction instructions	SU	r	M	Subtract M from r	r ← (r) – (M)	0	1	1	0	0	0	DH		DL				Rn			
	SUS	r	M	Subtract M from r, then skip if borrow	r ← (r) – (M) skip if borrow	0	1	1	0	0	1	DH		DL				Rn			
	SB	r	M	Subtract M from r with borrow	r ← (r) – (M) – b	0	1	1	0	1	0	DH		DL				Rn			
	SBS	r	M	Subtract M from r with borrow, then skip if borrow	r ← (r) – (M) – b skip if borrow	0	1	1	0	1	1	DH		DL				Rn			
	SI	M	I	Subtract I from M	M ← (M) – I	0	1	1	1	0	0	DH		DL				I			
	SIS	M	I	Subtract I from M, then skip if borrow	M ← (M) – I skip if borrow	0	1	1	1	0	1	DH		DL				I			
	SIB	M	I	Subtract I from M with borrow	M ← (M) – I – b	0	1	1	1	1	0	DH		DL				I			
	SIBS	M	I	Subtract I from M with borrow, then skip if borrow	M ← (M) – I – b skip if borrow	0	1	1	1	1	1	DH		DL				I			
Comparison instructions	SEQ	r	M	Skip if r equals M	r – M skip if zero	0	0	0	0	0	1	DH		DL				Rn			
	SGE	r	M	Skip if r is greater than or equal to M	r – M skip if not borrow (r) ≥ (M)	0	0	0	0	1	1	DH		DL				Rn			
	SEQI	M	I	Skip if M equal to I	M – I skip if zero	0	0	1	1	0	1	DH		DL				I			
	SGEI	M	I	Skip if M is greater than or equal to I	M – I skip if not borrow (M) ≥ I	0	0	1	1	1	1	DH		DL				I			

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Instruction Group	Mnemonic	Operand 1st	Operand 2nd	Function	Operation	Machine code D15 14 13 12	11 10	9 8	7 6 5 4	3 2 1 D0
Logical operation instructions	AND	M	I	AND I with M	M ← (M) ∧ I	0 0 1 1	0 0	DH	DL	I
	OR	M	I	OR I with M	M ← (M) ∨ I	0 0 1 1	1 0	DH	DL	I
	EXL	r	M	Exclusive OR M with r	r ← (r) ⊕ (M)	0 0 1 0	0 0	DH	DL	Rn
Transfer instructions	LD	r	M	Load M to r	r ← (M)	1 0 0 0	0 0	DH	DL	Rn
	ST	M	r	Store r to M	M ← (r)	1 0 0 0	0 1	DH	DL	Rn
	MVRD	r	M	Move M to destination M referring to r in the same row	[DH, Rn] ← (M)	1 0 0 0	1 0	DH	DL	Rn
	MVRS	M	r	Move source M referring to r to M in the same row	M ← [DH, Rn]	1 0 0 0	1 1	DH	DL	Rn
	MVSR	M1	M2	Move M to M in the same row	[DH, DL1] ← [DH, DL2]	1 0 0 1	0 0	DH	DL1	DL2
	MVI	M	I	Move I to M	M ← I	1 0 0 1	0 1	DH	DL	I
	PLL	M	r	Load M to PLL registers	PLL r ← PLL DATA	1 0 0 1	1 0	DH	DL	Rn
Bit test instructions	TMT	M	N	Test M bits, then skip if all bits specified are true	if M (N) = all 1, then skip	1 0 1 0	0 1	DH	DL	N
	TMF	M	N	Test M bits, then skip if all bits specified are false	if M (N) = all 0, then skip	1 0 1 0	1 1	DH	DL	N
Jump and subroutine call	JMP	ADDR		Jump to the address	PC ← ADDR	1 0 1 1	ADDR (12 bits)			
	CAL	ADDR		Call subroutine	Stack ← (PC) + 1	1 1 0 0	ADDR (12 bits)			
	RT			Return from subroutine	PC ← Stack	1 1 0 1	0 1 0 0	0 0 0 0	0 0 0 0	
	RTI			Return from interrupt	BANK ← Stack PC ← Stack CARRY ← Stack	1 1 0 1	0 1 0 1	0 0 0 0	0 0 0 0	
F/F test instructions	TTM	N		Test timer F/F then skip if it has not been set	if timer F/F = 0, then skip	1 1 0 1	0 1 1 0	0 0 0 0	N	
	TUL	N		Test unlock F/F then skip if it has not been set	if UL F/F = 0, then skip	1 1 0 1	0 1 1 1	0 0 0 0	N	
Status register instructions	SS	N		Set status register	(Status register 1) N ← 1	1 1 0 1	1 1 0 0	0 0 0 0	N	
	RS	N		Reset status register	(Status register 1) N ← 0	1 1 0 1	1 1 0 1	0 0 0 0	N	
	TST	N		Test status register true	if (Status register 2) N = all 1, then skip	1 1 0 1	1 1 1 0	0 0 0 0	N	
	TSF	N		Test status register false	if (Status register 2) N = all 0, then skip	1 1 0 1	1 1 1 1	0 0 0 0	N	
Bank switching instructions	BANK	B		Select bank	BANK ← B	1 1 0 1	0 0	B	0 0 0 0	0 0 0

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Instruction Group	Mnemonic	Operand 1st	Operand 2nd	Function	Operation	Machine code D15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 D0
I/O instructions	LCD	M	I	Output segment pattern to LCD digit direct	LCD (DIGIT) ← M	1 1 1 0	0 0 DH	DL	DIGIT
	LCP	M	I	Output segment pattern to LCD digit through PLA	LCD (DIGIT) ← PLA ← M	1 1 1 0	0 1 DH	DL	DIGIT
	IN	M	P	Input port data to M	M ← (Port (P))	1 1 1 0	1 0 DH	DL	P
	OUT	M	P	Output contents of M to port	(Port (P)) ← M	1 1 1 0	1 1 DH	DL	P
	SPB	P	N	Set port bits	(Port (P)) N ← 1	1 1 1 1	0 0 0 0	P	N
	RPB	P	N	Reset port bits	(Port (P)) N ← 0	1 1 1 1	0 1 0 1	P	N
	TPT	P	N	Test port bits, then skip if all bits specified are true	if (Port (P)) N = all 1, then skip	1 1 1 1	1 0 1 0	P	N
	TPF	P	N	Test port bits, then skip if all bits specified are false	if (Port (P)) N = all 0, then skip	1 1 1 1	1 1 1 1	P	N
Universal counter instructions	UCS	I		Set I to UCCW1	UCCW1 ← I	0 0 0 0	0 0 0 1	0 0 0 0	I
	UCC	I		Set I to UCCW2	UCCW2 ← I	0 0 0 0	0 0 1 1	0 0 0 0	I
Other instructions	FPC	N		F port I/O control	FPC latch ← N	0 0 0 1	0 0 0 0	0 0 0 0	N
	CKSTP			Clock stop	Stop clock if $\overline{HOLD}$ = 0	0 0 0 1	0 0 0 1	0 0 0 0	0 0 0 0
	DAC*	I		Load M to D/A registers	DA reg ← DAC DATA	0 0 0 0	0 0 1 0	0 0 0 0	I
	NOP			No operation		0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Note: * DAC is contained in LC72322R only.