SANYO No.2802A

LC7230

Single-Chip PLL + Controller with LCD Driver

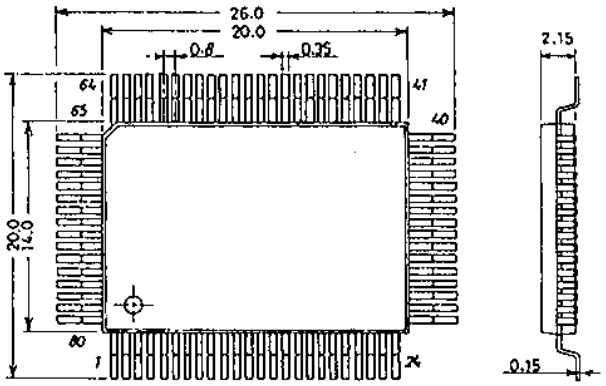
Overview

The LC7230 is a single chip microcontroller with internal LCD driver and phase locked loop (PLL) circuitry. It can be used as an electronic tuner and operates at a frequency of up to 150MHz.
The LC7230 single chip microcontroller contains a large program memory (ROM) and other powerful hardware functions. The instruction set for the CMOS LSI controller enables the user to use it effectively and easily.

Functions

- High-speed and programmable divider
- General purpose counter : HCTR for frequency measurement.
  LCTR for frequency or frequency cycle measurement. Note that the HCTR denotes the Horizontal counter and the LCTR, the Longitudinal counter.
- LCD driver : 56 segments (1/2 duty and 1/2 bias)
- Program memory (ROM) : 16 bits × 4096
- Data memory (RAM) : 4 bits × 256
- All instructions : One-word in length
- Cycle time : 2.67 microseconds
- Stack levels : 4
- Unlock flip-flop (FF) : 0.55-microsecond detection and 1.1-microsecond detection
- Timer flip-flops (FF) : 1 millisecond, 5 milliseconds, 25 milliseconds and 125 milliseconds
- Data input ports : Two ports --- One for exclusive key entry and the other input port with high withstand voltage level. Note that each port consists of four pins.
- Data output ports : 2 for exclusive key output, one open drain type output port with high withstand voltage level, 2 CMOS type output ports (One of them can be used as the LCD driver from a user application program.) Note that each port consists of four pins.
- I/O port : One I/O port controllable in 4-bit units.
  One I/O port controllable in bit units. Note that each I/O port consists of four pins.
- Timeout error detectable and specific address settable
- On-chip voltage-controlled reset circuit
- Six-bit ADC (Analog-Digital Converter)
- Eight-bit DAC × 2 (DAC : Digital-Analog Converter as a Pulse Width Modulator (PWM))
- External interrupt level : One
- HOLD mode : RAM backup at reduced power dissipation
- Sensing flip-flop (FF) circuit for Hot/Cold start decision (V_T = 1.3V to 2.5V)
- PLL (Phase Locked Loop) circuit : 4.5V to 5.5V
- CPU : 3.5V to 5.5V
- RAM : 1.3V to 5.5V

Case Outline 3044B
(unit : mm)



Specifications and information herein are subject to change without notice. SANYO: QIP80A

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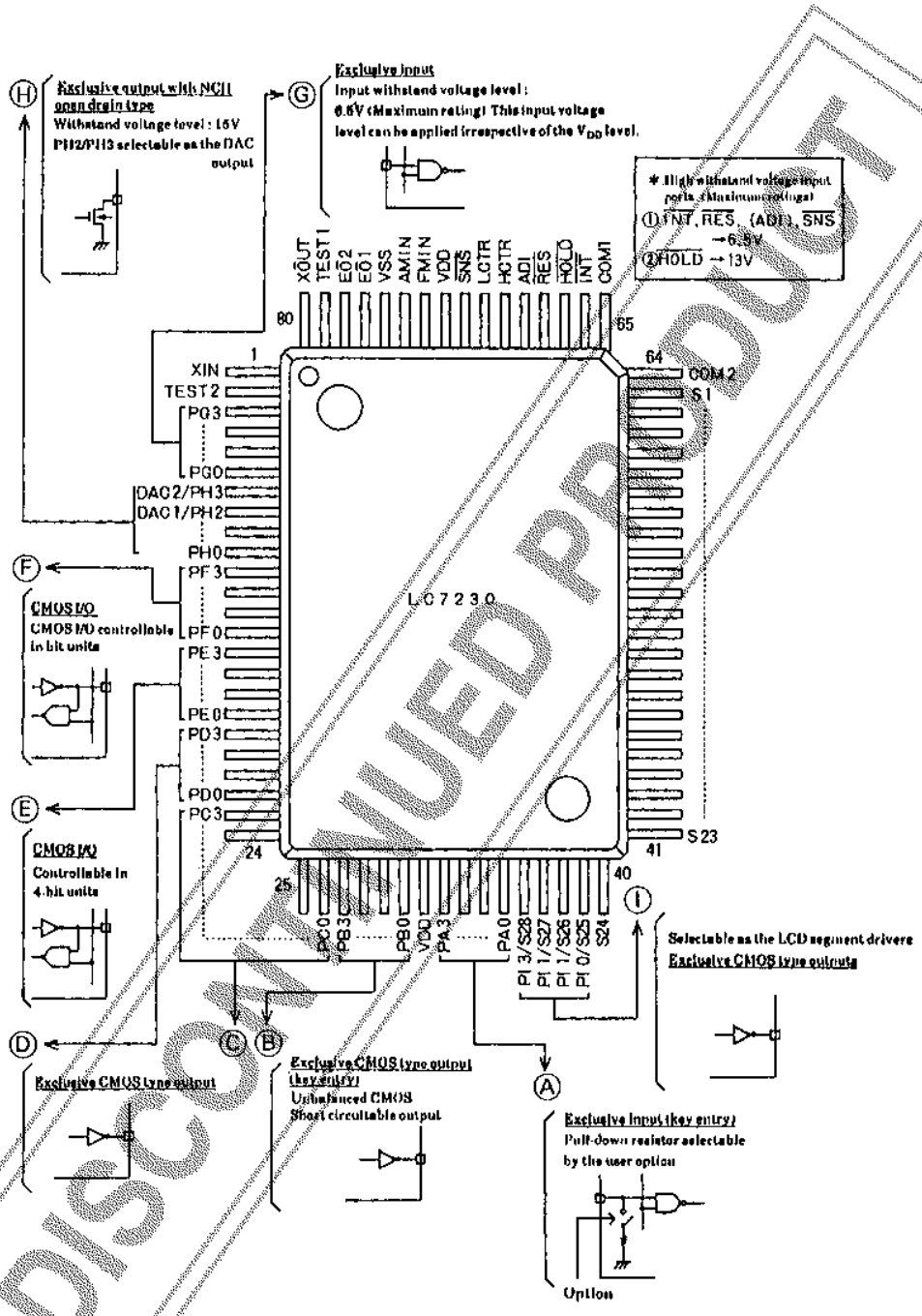
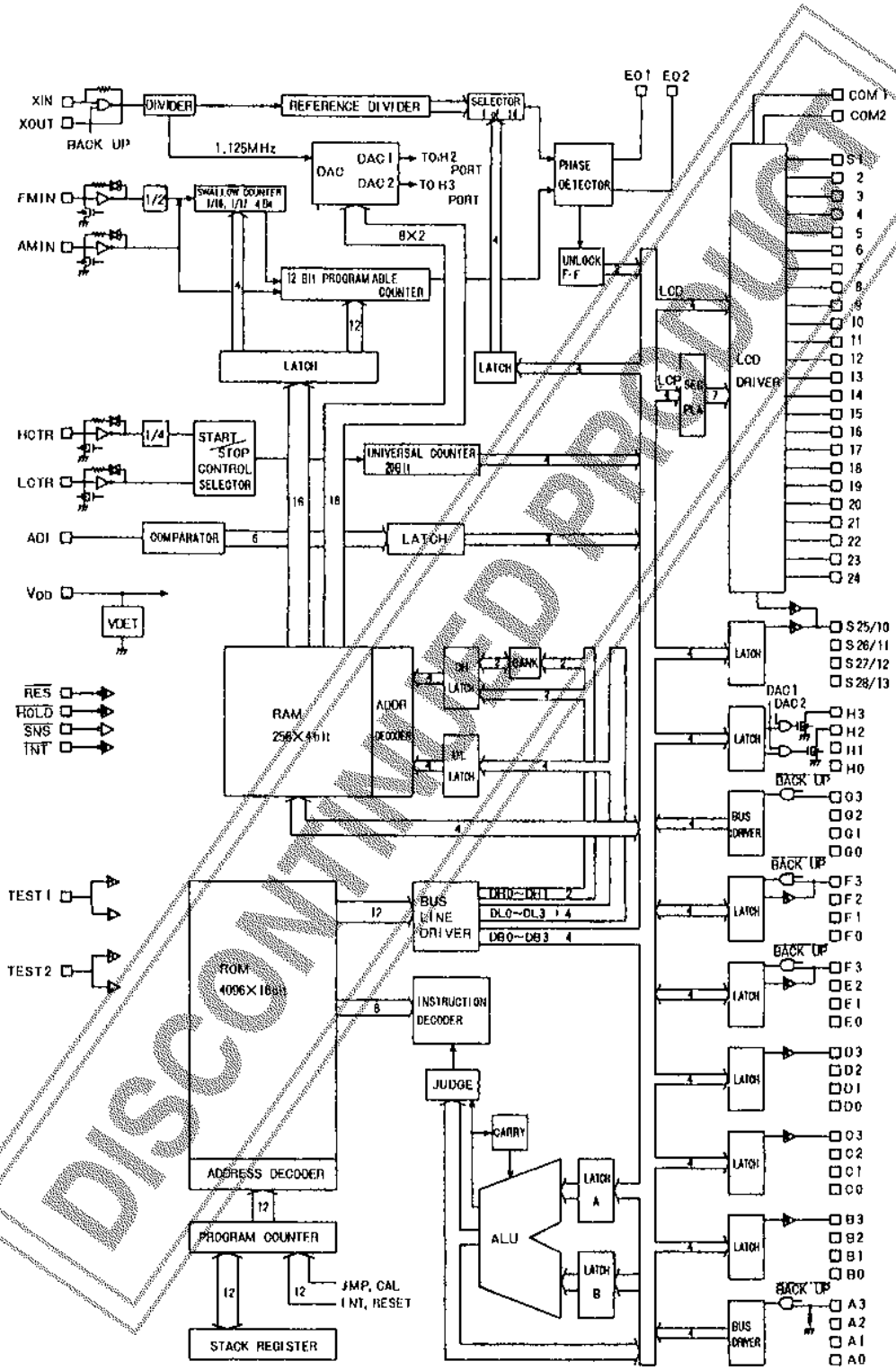
Pin Assignment



Functional Block Diagram



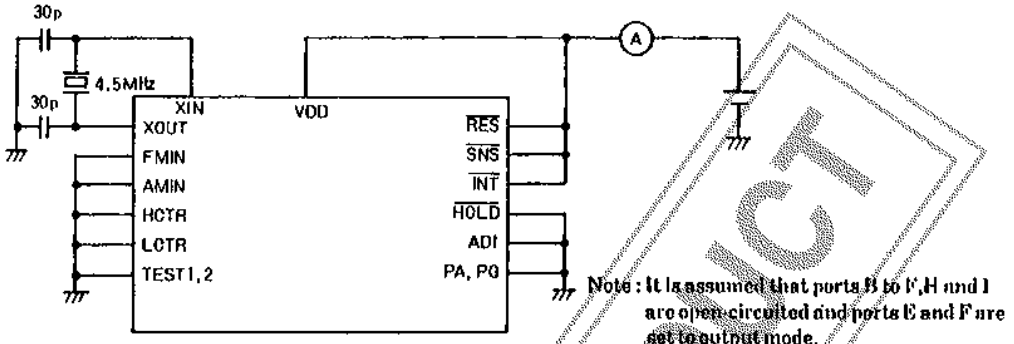
Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0V

				unit
Maximum Supply Voltage	V_{DD} max		−0.3 to 6.5	V
Input Voltage	V_{IN} (1)	$\overline{INT}$,$\overline{RES}$,ADI,$\overline{SNS}$ and port G	−0.3 to 6.5	V
	V_{IN} (2)	$\overline{HOLD}$	−0.3 to 13	V
	V_{IN} (3)	Inputs other than V_{IN} (1), V_{IN} (2)	−0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT} (1)	Port H	−0.3 to 15	V
	V_{OUT} (2)	Output other than V_{OUT} (1)	−0.3 to V_{DD} + 0.3	V
Output Current	I_{OUT} (1)	Each pin of ports D,H	0 to 5	mA
	I_{OUT} (2)	Each pin of ports E,F,I	0 to 3	mA
Allowable Power Dissipation	Pd max	−40 to +85°C	400	mW
Operating Temperature	Topg		−40 to +85	°C
Storage Temperature	Tstg		−45 to +125	°C
Output Current	I_{OUT} (3)	Each pin of ports B,C	0 to 1	mA

Recommended Operating Conditions at Ta = −40 to +85°C, V_{DD} = 3.5 to 5.5V, V_{SS} = 0V

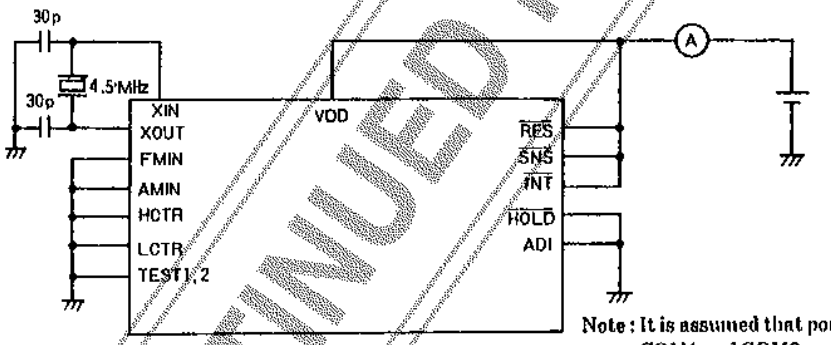
						min	typ	max	unit
Supply Voltage	V_{DD} (1)	CPU and PLL operation				4.5		5.5	V
	V_{DD} (2)	CPU operation				3.5		5.5	V
	V_{DD} (3)	Memory retention				1.3		5.5	V
'H'-Level Input Voltage	V_{IH} (1)	Port G				0.7V_{DD}		5.5	V
	V_{IH} (2)	$\overline{RES}$,$\overline{INT}$				0.8V_{DD}		5.5	V
	V_{IH} (3)	$\overline{SNS}$				2.5		5.5	V
	V_{IH} (4)	Port A				0.6V_{DD}		V_{DD}	V
	V_{IH} (5)	Ports E,F				0.7V_{DD}		V_{DD}	V
	V_{IH} (6)	LCTR (for frequency cycle measurement) V_{DD} (1)				0.8V_{DD}		V_{DD}	V
	V_{IH} (7)	$\overline{HOLD}$				0.8V_{DD}		8.0	V
'L'-Level Input Voltage	V_{IL} (1)	Port G				0		0.3V_{DD}	V
	V_{IL} (2)	$\overline{RES}$,$\overline{INT}$,$\overline{HOLD}$				0		0.2V_{DD}	V
	V_{IL} (3)	$\overline{SNS}$				0		1.3	V
	V_{IL} (4)	Port A				0		0.2V_{DD}	V
	V_{IL} (5)	Ports E,F				0		0.3V_{DD}	V
	V_{IL} (6)	LCTR (for frequency cycle measurement) V_{DD} (1)				0		0.2V_{DD}	V
Input Frequency	f_{IN} (1)	X IN				4.0	4.5	5.0	MHz
	f_{IN} (2)	FM IN	V_{IN} (2)	V_{DD} (1)		10		130	MHz
	f_{IN} (3)	FM IN	V_{IN} (3)	V_{DD} (1)		10		150	MHz
	f_{IN} (4)	AM IN(L)	V_{IN} (4)	V_{DD} (1)		0.5		10	MHz
	f_{IN} (5)	AM IN(H)	V_{IN} (5)	V_{DD} (1)		2.0		40	MHz
	f_{IN} (6)	HCTR	V_{IN} (6)	V_{DD} (1)		0.4		12	MHz
	f_{IN} (7)	LCTR (for frequency measurement) V_{IN} (7) V_{DD} (1)				100		500	kHz
	f_{IN} (8)	LCTR (for frequency cycle measurement) V_{IH} (6), V_{IL} (6) V_{DD} (1)				1		20×10^3	Hz
Input Amplitude	V_{IN} (1)	X IN				0.50		1.5	Vrms
	V_{IN} (2)	FM IN				0.10		1.5	Vrms
	V_{IN} (3)	FM IN				0.15		1.5	Vrms
	V_{IN} (4) (5)	AM IN				0.10		1.5	Vrms
	V_{IN} (6) (7)	LCTR,HCTR				0.10		1.5	Vrms
Input Voltage Range	V_{IN} (8)	ADI				0		V_{DD}	V

Electrical Characteristics (under recommended operating conditions)				min	typ	max	unit
Hysteresis Voltage	V_H	LCTR (frequency cycle measurement), $\overline{RES}$, $\overline{HOLD}$, $\overline{INT}$		0.1V_{DD}			V
Reject Pulse Width	P_{REJ}	$\overline{SNS}$				50	μsec
Power-down Detection Voltage	V_{DET}			2.7	3.0	3.3	V
'H'-Level Input Current	I_{IH} (1)	$\overline{INT}$, $\overline{HOLD}$, $\overline{RES}$, ADI, $\overline{SNS}$, port G, $V_I = 5.5V$				3.0	μA
	I_{IH} (2)	Ports A, E, F, Note that the ports E, F should be set to input mode and that port A is not used with the optional pull-down resistor. $V_I = V_{DD}$				3.0	μA
	I_{IH} (3)	XIN $V_I = V_{DD} = 5.0V$		2.0	5.0	15	μA
	I_{IH} (4)	FMIN, AMIN, HCTR, LCTR, $V_I = V_{DD} = 5.0V$		4.0	10	30	μA
	I_{IH} (5)	Port A with the optional pull-down resistor, $V_I = V_{DD} = 5.0V$			50		μA
'L'-Level Input Current	I_{IL} (1)	$V_I = V_{SS}$				3.0	μA
	I_{IL} (2)	$V_I = V_{SS}$				3.0	μA
	I_{IL} (3)	$V_I = V_{SS}$		2.0	5.0	15	μA
	I_{IL} (3)	$V_I = V_{SS}$		4.0	10	30	μA
Input Floating Voltage	V_{IF}	Port A with the optional pull-down resistor				0.05V_{DD}	V
Pull-Down Resistance	R_{PD}	Port A with the optional pull-down resistor		75	100	200	kΩ
Output OFF Leakage Current	I_{OFFH} (1)	EO1, EO2	$V_O = V_{DD}$		0.01	10	nA
	I_{OFFH} (2)	Ports B, C, D, E, F, I	$V_O = V_{DD}$			3.0	μA
	I_{OFFH} (3)	Port H	$V_O = 13V$			5.0	μA
Output OFF Leakage Current	I_{OFFL} (1)	EO1, EO2	$V_O = V_{SS}$		0.01	10	nA
	I_{OFFL} (2)	Ports B, C, D, E, F, I	$V_O = V_{SS}$			3.0	μA
'H'-Level Output Voltage	V_{OH} (1)	Ports B, C	$I_O = 1mA$	$V_{DD}-2.0$	$V_{DD}-1.0$	$V_{DD}-0.5$	V
	V_{OH} (2)	Ports E, F, I	$I_O = 1mA$	$V_{DD}-1.0$			V
	V_{OH} (3)	EO1, EO2	$I_O = 500μA$	$V_{DD}-1.0$			V
	V_{OH} (4)	XOUT	$I_O = 200μA$	$V_{DD}-1.0$			V
	V_{OH} (5)	S1 to S28	$I_O = -0.1mA$	$V_{DD}-1.0$			V
	V_{OH} (6)	Port D	$I_O = 5mA$	$V_{DD}-1.0$			V
	V_{OH} (7)	COM1, COM2	$I_O = 20μA$	$V_{DD}-0.7$	$V_{DD}-0.5$	$V_{DD}-0.35$	V
'L'-Level Output Voltage	V_{OL} (1)	Ports B, C	$I_O = 50μA$	0.5	1.0	2.0	V
	V_{OL} (2)	Ports E, F, I	$I_O = 1mA$			1.0	V
	V_{OL} (3)	EO1, EO2	$I_O = 500μA$			1.0	V
	V_{OL} (4)	XOUT	$I_O = 200μA$			1.0	V
	V_{OL} (5)	S1 to S28	$I_O = 0.1mA$			1.0	V
	V_{OL} (6)	Port D	$I_O = 5mA$			1.0	V
	V_{OL} (7)	COM1, COM2	$I_O = 20μA$	0.35	0.5	0.7	V
	V_{OL} (8)	Port H	$I_O = 5mA$	0.75 (200Ω)		2.0 (400Ω)	V
'M'-Level Output Voltage	V_M (1)	COM1, COM2, $V_{DD} = 5V$, $I_O = 20μA$		2.0	2.5	3.0	V
AD Conversion Error		ADI	V_{DD} (1)	−1/2		1/2	LSB
Supply Current	I_{DD} (1)	V_{DD} (1), f_{IN} (2) = 130MHz			15	25	mA
	I_{DD} (2)	V_{DD} (2), PLL in stop state (with the HOLD mode ON. See Figure 1.)			2	3	mA
	I_{DD} (3)	$V_{DD} = 5.5V$, OSC in stop state, Ta = 25°C (with the BACKUP mode ON. See Figure 2.)				5	μA
		$V_{DD} = 2.5V$, OSC in stop state, Ta = 25°C (with the BACKUP mode ON. See Figure 2.)				1	μA



Note : It is assumed that ports B to F, H and I are open-circuited and ports E and F are set to output mode.

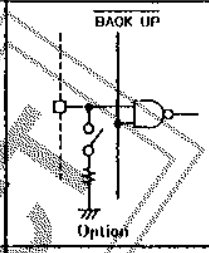
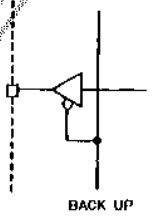
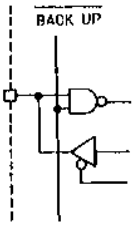
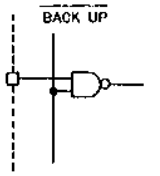
Figure 1. I_{DD} (2) at HOLD mode



Note : It is assumed that ports A to I, S1 to S24, COM1 and COM2 are open-circuited.

Figure 2. I_{DD} (3) at BACKUP mode

Pin Description

Pin Name	Pin No.	Functional Description	I/O	I/O Circuit Type
PA_0 PA_1 PA_2 PA_3	35 34 33 32	Used exclusively for data input. Low threshold type. These port pins can be used for key data entry. Pull-down resistance can be selected by the user option. In this selection, all the four port pins are controlled at a time. That is, the pull-down resistor cannot be selected for each port pin individually. Input to the port pins is inhibited during the BACKUP mode ON.	Input	
PB_0 PB_1 PB_2 PB_3 PC_0 PC_1 PC_2 PC_3	30 29 28 27 26 25 24 23	Used exclusively for data output. Can be used for key scan timing signal output because these ports are composed of CMOS transistors with unbalanced impedance. Enter into output high impedance state at the BACKUP mode. Placed in "L" level state at the reset ($\overline{RES}$="L").	Output	
PD_0 PD_1 PD_2 PD_3	22 21 20 19	Used exclusively for data output. Normal CMOS output type. Enter into output high impedance state at the BACKUP mode. Placed in the "L" level state at the reset ($\overline{RES}$="L").		
PE_0 PE_1 PE_2 PE_3	18 17 16 15	Used for data input and output. The port is set to the input mode once the input instruction (IN, TPT, or TPF) is executed in your application program while set to the output mode if the output instruction (OUT, SPB, RPB) is used. The operation mode once selected by such an instruction can be effective until an instruction of different type is used in your application program. Set to the input mode at the reset ($\overline{RES}$="L"). Set to the input mode at the BACKUP mode. In this case, note that data input to this port is inhibited.	Input/ output	
PF_0 PF_1 PF_2 PF_3	14 13 12 11	Used for data input and output. This port is controlled by the FPC instruction. Each port pin can be set to the input mode or the output mode by that instruction. Set to the input mode at the reset ($\overline{RES}$="L"). This port is set to the input mode at the BACKUP mode. In this case, note that data input to this port is inhibited.		
PG_0 PG_1 PG_2 PG_3	6 5 4 3	Used exclusively for data input. Data input to the port is inhibited at the BACKUP mode.	Input	

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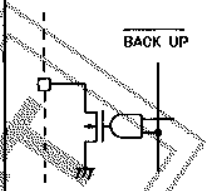
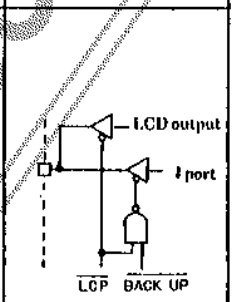
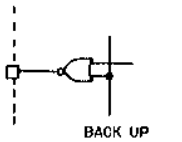
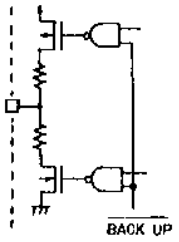
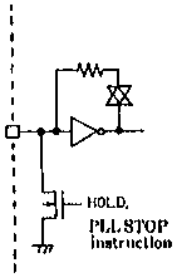
Pin Name	Pin No.	Functional Description	I/O	I/O Circuit Type
PH_0 PH_1 PH_2 PH_3	10 9 8 7	Used exclusively for data output. This port can be used for frequency band power source selection because this port has Nch open drain output circuit at high withstand voltage level. Port pins H2 and H3 can be also used as the DAC1 and DAC2 outputs, respectively. Enter into high impedance state at the reset ($\overline{RES}$="L") and the BACKUP mode.	Output	
PI_0/S25 PI_1/S26 PI_2/S27 PI_3/S28	39 38 37 36	Used exclusively for data output. This port has the CMOS type output circuit and can be selected as the LCD driver output ports. The port operation mode can be selected by the SS or RS instruction. The output mode cannot be selected by such an instruction in bit units. This port is set to the LCD driver output mode at the reset ($\overline{RES}$="L") and at power supply. In this case, segment display is forced into the OFF state. This port is fixed to the "L" level at the BACKUP mode.	Output	
S1 to S24	63 to 40	Used for driving segments. That is, these ports are used as the LCD output drivers. The frame frequency for segment output is 100Hz. The lighting format is 1/2 duty and 1/2 bias. The segment display is forced into the OFF state at the reset ($\overline{RES}$="L") and power supply. This port is set to the "L" level at the BACKUP mode.	Output	
COM1 COM2	65 64	Used for LCD drive common signal output. The lighting format is 1/2 duty and 1/2 bias. Normal output at the reset ($\overline{RES}$="L") and power supply. These ports are set to the "L" level at the BACKUP mode.	Output	
FM IN		Used for FM VCO input (local oscillation). Note that the VCO means Voltage-Controlled Oscillation. Input through capacitor coupling is required. The input frequency range is between 10MHz and 130MHz.	Input	
AM IN		Used for AM VCO input (local oscillation). Note that the VCO means Voltage-Controlled Oscillation. Input through capacitor coupling is required. Frequency bands can be selected by CW1 of the PLL instruction. Hi (2 to 40MHz) → SW Lo (0.5 to 10MHz) → LW, MW		

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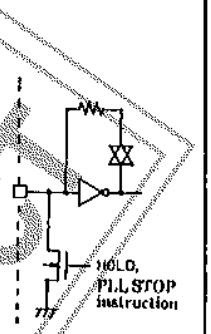
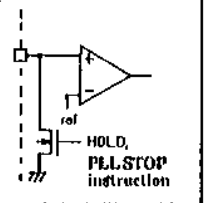
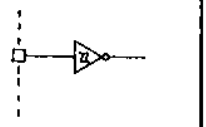
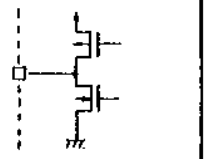
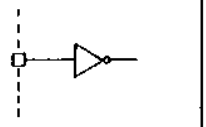
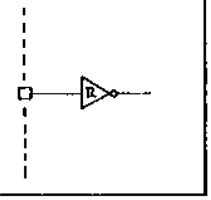
Pin Name	Pin No.	Functional Description	I/O	I/O Circuit Type
HCTR	70	Used for universal counter input. Input through capacitor coupling is required. The input frequency range is between 0.4MHz and 12MHz. This port can be used for counting FM IF and AM IF.	Input	
LCTR	71	Used for universal counter input. Input through capacitor coupling is required when the input frequency range is between 100kHz and 500kHz. Input through capacitor coupling is not required when the input frequency range is between 1Hz and 20kHz. This port can be used for counting AM IF.		
ADI	69	Used for AD converter input. The AD converter is composed of a 6-bit sequential comparator requiring a conversion time of 1.28 milliseconds. Full-scale data (3FH) : $V_{DD} \times 63/96$	Input	
$\overline{INT}$	66	Used for interrupt request signal input. Interrupt request becomes active if falling signal edge is detected at the port with the INTEN flag already set. Note that this flag is set by the SS instruction.	Input	
EO1 EO2	77 78	Used for phase comparison error output. Note that reference signal frequency and programmable divider output signal frequency are compared in their phase. On-chip charge pump available. The EO1 and the EO2 has the same circuit type.	Output	
SNS	72	Used at the BACKUP mode for power failure signal input. This port can be used as a normal input port.	Input	
$\overline{HOLD}$	67	Used for HOLD mode request signal input. The HOLD mode becomes active if the $\overline{HOLD}$ pin logic changes to "L" with the HOLDEN flag already ON. Note that this flag is set by the SS instruction. The withstand voltage level of this port is high in order that the port can be used together with a power switch.	Input	

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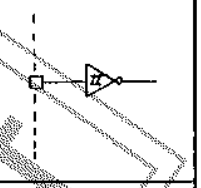
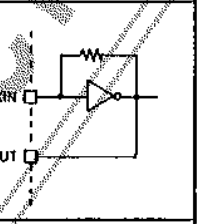
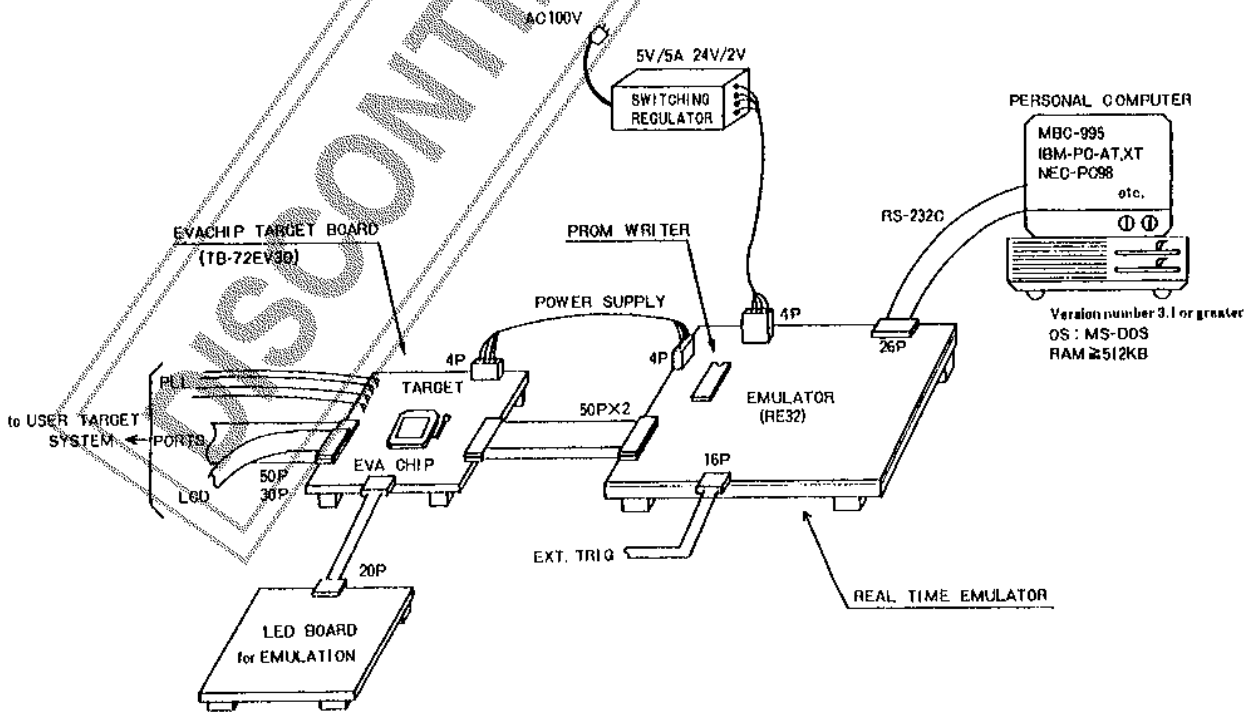
Pin Name	Pin No.	Functional Description	I/O	I/O Circuit Type
$\overline{RES}$	68	Used for the system reset request input. The power up "L" level reset request signal must be applied to this port for more than 75 milliseconds. The reset "L" level start request signal must be applied to this port for more than five fundamental clock cycles.	Input	
XIN XOUT	1 80	These two pins are used for X'tal oscillation frequency (4.5MHz) input and output. On-chip feedback resistor available.	Input/ output	
TEST1 TEST2	2 79	These two pins are used for LST test signal input. They should be open-circuited or connected with the V_{SS} pin.	–	–
V_{DD} V_{SS}	31, 73 76	Power source	–	–

Options

1. Pull-down resistor selectable for port pins PA_0 to PA_3 by the user option
2. Watchdog timer (WDT) circuit internally selectable

Development support tool system

- EVA chip : LC72EV30
- Host personal computer-controlled total debug system : Target board (TB-72EV30) and High functional emulator (RE32).



Instruction set for the LC7230 single chip controller

Abbreviations : ADDR : Program memory address(12 bits)
b : Borrow
B : Bank number (2 bits)
C : Carry
DH : Data memory address high(Row address)(2 bits)
DL : Data memory address Low(Column address)(4 bits)
I : Immediate data(4 bits)
M : Data memory address
N : Bit position(4 bits)
Pn : Port number(4 bits)
r : General register(One of the address between 00H and 0FH in each bank area)
Rn : Register number(4 bits)
( ) : Contents of register or memory
( )n : Contents of bit N of register or memory

Instruction type	Mnemonic	Operand 1st	Operand 2nd	Functional Description	Operations Description	Machine Code D15 14 13 12	11 10	9 8	7 6 5 4	3 2 1 0
Addition instruction	AD	r	M	Add M to r	r←(r)+(M)	0 1 0 0	0 0	DH	DL	Rn
	ADS	r	M	Add M to r,then skip if carry	r←(r)+(M) skip if carry	0 1 0 0	0 1	DH	DL	Rn
	AC	r	M	Add M to r with carry	r←(r)+(M)+C	0 1 0 0	1 0	DH	DL	Rn
	ACS	r	M	Add M to r with carry,then skip if carry	r←(r)+(M)+C skip if carry	0 1 0 0	1 1	DH	DL	Rn
	AI	M	I	Add I to M	M←(M)+I	0 1 0 1	0 0	DH	DL	I
	AIS	M	I	Add I to M,then skip if carry	M←(M)+I skip if carry	0 1 0 1	0 1	DH	DL	I
	AIC	M	I	Add I to M with carry	M←(M)+I+C	0 1 0 1	1 0	DH	DL	I
	AICS	M	I	Add I to M with carry,then skip if carry	M←(M)+I+C skip if carry	0 1 0 1	1 1	DH	DL	I
Subtraction instruction	SU	r	M	Subtract M from r	r←(r)−(M)	0 1 1 0	0 0	DH	DL	Rn
	SUS	r	M	Subtract M from r,then skip if borrow	r←(r)−(M) skip if borrow	0 1 1 0	0 1	DH	DL	Rn
	SB	r	M	Subtract M from r with borrow	r←(r)−(M)−b	0 1 1 0	1 0	DH	DL	Rn
	SBS	r	M	Subtract M from r with borrow, then skip if borrow	r←(r)−(M)−b skip if borrow	0 1 1 0	1 1	DH	DL	Rn
	SI	M	I	Subtract I from M	M←(M)−I	0 1 1 1	0 0	DH	DL	I
	SIS	M	I	Subtract I from M,then skip if borrow	M←(M)−I skip if borrow	0 1 1 1	0 1	DH	DL	I
	SIB	M	I	Subtract I from M with borrow	M←(M)−I−b	0 1 1 1	1 0	DH	DL	I
	SIBS	M	I	Subtract I from M with borrow, then skip if borrow	M←(M)−I−b skip if borrow	0 1 1 1	1 1	DH	DL	I
Compare instruction	SEQ	r	M	Skip if r equals M	r−M skip if zero	0 0 0 0	0 1	DH	DL	Rn
	SGE	r	M	Skip if r is greater than or equal to M	r−M Skip if not borrow(r)≥(M)	0 0 0 0	1 1	DH	DL	Rn
	SEQI	M	I	Skip if M equal to I	M−I skip if zero	0 0 1 1	0 1	DH	DL	I
	SGEI	M	I	Skip if M is greater than or equal to I	M−I skip if not borrow(M)≥I	0 0 1 1	1 1	DH	DL	I
Logic operations instruction	AND	M	I	AND I with M	M←(M)∧I	0 0 1 1	0 0	DH	DL	I
	OR	M	I	OR I with M	M←(M)∨I	0 0 1 1	1 0	DH	DL	I
	EXL	r	M	Exclusive OR M with r	r←(r)⊕(M)	0 0 1 0	0 0	DH	DL	Rn
Transfer instruction	LD	r	M	Load M to r	r←(M)	1 0 0 0	0 0	DH	DL	Rn
	ST	M	r	Store r to M	M←(r)	1 0 0 0	0 1	DH	DL	Rn
	MVRD	r	M	Move M to destination M referring to r in the same row	[DH.Rn]←(M)	1 0 0 0	1 0	DH	DL	Rn
	MVRS	M	r	Move source M referring to r to M in the same row	M←[DH.Rn]	1 0 0 0	1 1	DH	DL	Rn

Instruction type	Mnemonic	Operand 1st	Operand 2nd	Functional Description	Operations Description	Machine Code DI5 14 13 12	11 10 9 8	7 6 5 4	3 2 1 DI0
Transfer instruction	MVSR	M1	M2	Move M to M in the same row	[DH,DL1]←[DH,DL2]	1 0 0 1	0 0 DH	DL1	DL2
	MVI	M	I	Move I to M	M←I	1 0 0 1	0 1 DH	DL	I
	PLL	M	r	Load M to PLL registers	PLLr←PLL DATA	1 0 0 1	1 0 DH	DL	Rn
Bit test instruction	TMT	M	N	Test M bits,then skip if all bits specified are true	if M(N)=all "1", then skip	1 0 1 0	0 1 DH	DL	N
	TMF	M	N	Test M bits,then skip if all bits specified are false	if M(N)=all "0", then skip	1 0 1 0	1 1 DH	DL	N
Jump-subroutine instruction	JMP	ADDR		Jump to the address	PC←ADDR	1 0 1 1	ADDR (12 bits)		
	CAL	ADDR		Call subroutine	Stack←(PC)+1	1 1 0 0	ADDR (12 bits)		
	RT			Return from subroutine	PC←Stack	1 1 0 1	0 0 0 0	0 0 0 0	0 0 0 0
	RTI			Return from interrupt	PC←Stack	1 1 0 1	0 1 0 1	0 0 0 0	0 0 0 0
F/F test instruction	TTM	N		Test timer F/F then skip if it has not been set	if Timer F/F="0", then skip	1 1 0 1	0 1 1 0	0 0 0 0	N
	TUL	N		Test unlock F/F then skip if it has not been set	if UL F/F="0", then skip	1 1 0 1	0 1 1 1	0 0 0 0	N
Status register instruction	SS	N		Set status register	(Status register I)N←1	1 1 0 1	1 1 0 0	0 0 0 0	N
	RS	N		Reset status register	(Status register I)N←0	1 1 0 1	1 1 0 1	0 0 0 0	N
	TST	N		Test status register true	if (Status register 2)N =all "1", then skip	1 1 0 1	1 1 1 0	0 0 0 0	N
	TSF	N		Test status register false	if(Status register 2)N =all "0" ;then skip	1 1 0 1	1 1 1 1	0 0 0 0	N
Bank switching instruction	BANK	B		Select Bank	BANK←B	1 1 0 1	0 0 B	0 0 0 0	0 0 0 0
Input/output (I/O) instruction	LCD	M	I	Output segment pattern to LCD digit direct	LCD(DIGIT)←M	1 1 1 0	0 0 DH	DL	DIGIT
	LCI	M	I	Output segment pattern to LCD digit through PLA	LCD(DIGIT)←PLA←M	1 1 1 0	0 1 DH	DL	DIGIT
	IN	M	P	Input port data to M	M←(Port(P))	1 1 1 0	1 0 DH	DL	P
	OUT	M	P	Output contents of M to port	(Port(P))←M	1 1 1 0	1 1 DH	DL	P
	SPB	P	N	Set port bits	(Port(P))N←1	1 1 1 1	0 0 0 0	P	N
	RPB	P	N	Reset port bits	(Port(P))N←0	1 1 1 1	0 1 0 1	P	N
	TPT	P	N	Test port bits,then skip if all bits specified are true	if(Port(P))N=all "1", then skip	1 1 1 1	1 0 1 0	P	N
	TPF	P	N	Test port bits,then skip if all bits specified are false	if(Port(P))N=all "0", then skip	1 1 1 1	1 1 1 1	P	N
Universal counter instruction	UCS	I		Set I to UCCW1	UCCW←I	0 0 0 0	0 0 0 1	0 0 0 0	I
	UCC	I		Set I to UCCW2	UCCW2←I	0 0 0 0	0 0 1 1	0 0 0 0	I
Other instructions	FPC	N		Fport I/O control	FPC Latch←N	0 0 0 1	0 0 0 0	0 0 0 0	N
	CKSTP			Clock stop	Stop clock if $\overline{HOLD}$=0	0 0 0 1	0 0 0 1	0 0 0 0	0 0 0 0
	DAC	I		Load M to D/A registers	DAreg←DAC DATA	0 0 0 0	0 0 1 0	0 0 0 0	I
	NOP			No operation		0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0