



# LC7219, 7219M

## PLL Frequency Synthesizers

### Overview

The LC7219 and LC7219M are high-performance, phase-locked loop (PLL) frequency synthesizer ICs that operate over the AM and FM radio wavebands. They feature excellent frequency tracking, making them ideal as reference frequency sources for use in AM/FM tuners, television and audio-video equipment, and high-quality car-stereo applications.

The LC7219 and LC7219M operate from a 5 V supply and are available in 24-pin DIPs and 24-pin MFPs, respectively.

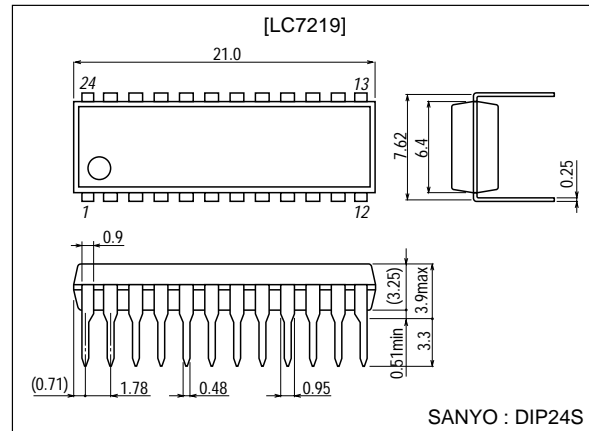
### Features

- Programmable divider.
- General-purpose universal counter.  
(The IF signal count must be used together with the SD (station detect) signal from IF-IC).
- Unlock detector.
- 8 Hz real-time clock output.
- Ten selectable reference frequencies.
- 400 kHz microcontroller system-clock output.
- Swallow counter.
- Shift register.
- 5 V supply.
- 24-pin DIP and 24-pin MFP.

### Package Dimensions

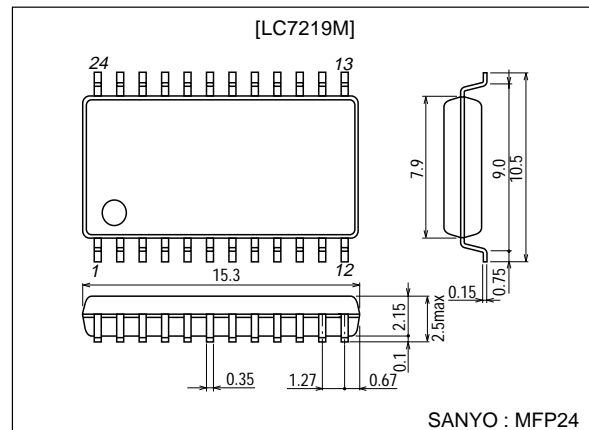
unit:mm

3067A-DIP24S



unit:mm

3045B-MFP24



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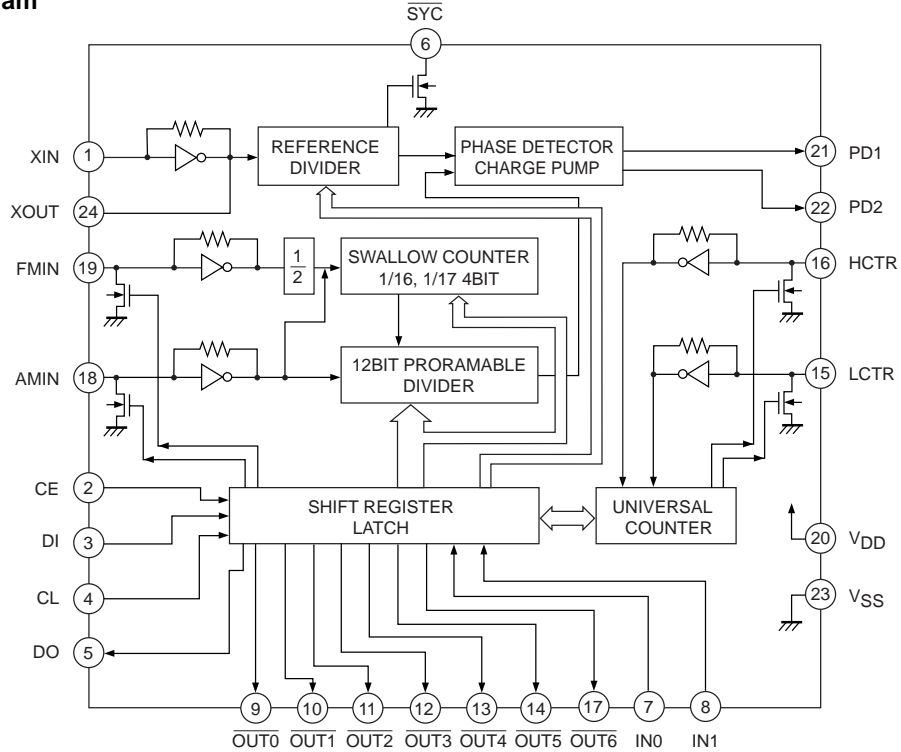
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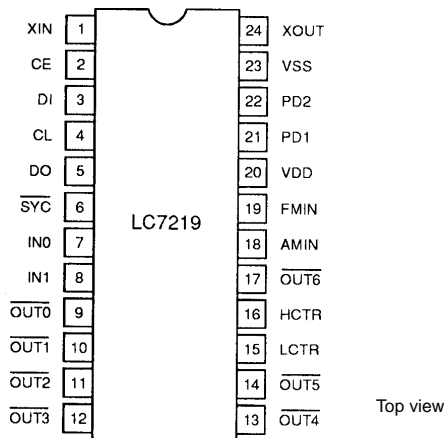
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## Block Diagram



## Pin Assignment



## Pin Description

Number	Name	Description
1	XIN	7.2MHz crystal oscillator input
2	CE	Chip-enable input
3	DI	Data input from microcontroller
4	CL	Clock input
5	DO	Data output to microcontroller
6	$\overline{\text{SYC}}$	400kHz, 66% duty cycle, system-clock output
7, 8	IN0, IN1	Shift register data inputs
9 to 14, 17	$\overline{\text{OUT0}}$ to $\overline{\text{OUT6}}$	Shift register data outputs
15	LCTR	Period or frequency measurement general-purpose counter input
16	HCTR	Frequency measurement general-purpose counter input
18	AMIN	AM band VCO signal input
19	FMIN	FM band VCO signal input
20	VDD	Supply voltage
21, 22	PD1, PD2	Phase-detector charge pump outputs
23	VSS	Ground
24	XOUT	7.2MHz crystal oscillator output

# LC7219, 7219M

## Specifications

**Absolute Maximum Ratings** at  $T_a = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\ max}$		-0.3 to +7.0	V
CE, CL, DI, IN0 and IN1 input voltage	$V_{IN1}$		-0.3 to +7.0	V
Input voltage for all other pins	$V_{IN2}$		-0.3 to $V_{DD}+0.3$	V
DO and SYNC output voltage	$V_{OUT1}$		-0.3 to +7.0	V
OUT1 and OUT2 output voltage	$V_{OUT2}$		-0.3 to $V_{DD}+0.3$	V
OUT0 and OUT3 to OUT6 output voltage	$V_{OUT3}$		-0.3 to +15.0	V
Output voltage for all other pins	$V_{OUT4}$		-0.3 to $V_{DD}+0.3$	V
Allowable power dissipation	Pd max		350 (LC7219)	mW
			350 (LC7219M)	
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +125	°C

**Recommended Operating Conditions** at  $T_a = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage range	$V_{DD1}$	$V_{DD}$	4.5		6.5	V
Supply voltage range for crystal oscillator operation	$V_{DD2}$	$V_{DD}$	3.5		6.5	V
CE, CL, DI, IN0 and IN1 high-level input voltage	$V_{IH1}$		2.2		6.5	V
LCTR high-level output voltage	$V_{IH2}$	Period measurement, $V_{DD}=4.5$ to $6.5\text{V}$	$0.7V_{DD}$		$V_{DD}$	V
CL, CE, DI, IN0 and IN1 low-level input voltage	$V_{IL1}$		0		0.7	V
LCTR low-level output voltage	$V_{IL2}$	Period measurement, $V_{DD}=4.5$ to $6.5\text{V}$	0		$0.3V_{DD}$	V
DO and SYNC output voltage	$V_{OUT1}$				6.5	V
OUT0 and OUT3 to OUT6 output voltage	$V_{OUT2}$				13	V
XIN input frequency	$f_{IN1}$	Sine wave, capacitive coupling, $V_{DD}=3.5$ to $6.5\text{V}$	1.0	7.2	8.0	MHz
FMIN input frequency*1	$f_{IN2}$	Sine wave, capacitive coupling, $V_{DD}=4.5$ to $6.5\text{V}$ See table 5	10		130	MHz
AMIN input frequency	$f_{IN3}$	Sine wave, capacitive coupling, $V_{DD}=4.5$ to $6.5\text{V}$ See table 5	0.5		40.0	MHz
HCTR input frequency*2	$f_{IN4}$	Period measurement, sine wave, capacitive coupling, $V_{DD}=4.5$ to $6.5\text{V}$	10		60	MHz
LCTR input frequency	$f_{IN5}$	Frequency measurement, sine wave, capacitive coupling, $V_{DD}=4.5$ to $6.5\text{V}$	15		500	KHz
		Period measurement, pulse wave DC coupling, $V_{DD}=4.5$ to $6.5\text{V}$	0.001		20.0	
Crystal oscillator frequency	$f_{XTAL}$	$X_{IN}-X_{OUT}$ : Crystal impedance $\leq 50\Omega$	3.0	7.2	8.0	MHz
XIN rms input amplitude	$V_{IN1}$	Sine wave, capacitive coupling, $V_{DD}=4.5$ to $6.5\text{V}$	0.5		1.5	Vrms
FMIN rms input amplitude*1	$V_{IN2}$	Sine wave, capacitive coupling, $V_{DD}=4.5$ to $6.5\text{V}$	0.07		1.5	Vrms
AMIN rms input amplitude	$V_{IN3}$	Sine wave, capacitive coupling, $V_{DD}=4.5$ to $6.5\text{V}$	0.07		1.5	Vrms
HCTR rms input amplitude*2	$V_{IN4}$	Frequency measurement, $V_{DD}=4.5$ to $6.5\text{V}$	0.07		1.5	Vrms
LCTR rms input amplitude	$V_{IN5}$	Frequency measurement, sine wave, capacitive coupling, $V_{DD}=4.5$ to $6.5\text{V}$	0.07		1.5	Vrms

### Notes

- $f_{IN2}=10$  to  $160\text{MHz}$  for  $V_{IN2}=0.1\text{V}(\text{min})$
- $f_{IN4}=10$  to  $70\text{MHz}$  for  $V_{IN4}=0.1\text{V}(\text{min})$

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**Electrical Characteristics** at  $T_a = -40$  to  $+85^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
XIN internal resistance	$R_{f1}$			1		$\text{M}\Omega$
FMIN internal resistance	$R_{f2}$			500		$\text{k}\Omega$
AMIN internal resistance	$R_{f3}$			500		$\text{k}\Omega$
HCTR internal resistance	$R_{f4}$			500		$\text{k}\Omega$
LCTR internal resistance	$R_{f5}$			500		$\text{k}\Omega$
LCTR hysteresis width	$V_H$		$0.1V_{DD}$		$0.6V_{DD}$	V
CE, CL and DI high-level input current	$I_{IH1}$	$V_{IN}=6.5\text{V}$			5	$\mu\text{A}$
INO and IN1 high-level input current	$I_{IH2}$	$V_{IN}=V_{DD}$			5	$\mu\text{A}$
XIN high-level input current	$I_{IH3}$	$V_{IN}=V_{DD}$			20	$\mu\text{A}$
AMIN and FMIN high-level input current	$I_{IH4}$	$V_{IN}=V_{DD}$			40	$\mu\text{A}$
HCTR and LCTR high-level input current	$I_{IH5}$	$V_{IN}=V_{DD}$			40	$\mu\text{A}$
CE, CL and DI low-level input current	$I_{IL1}$	$V_{IN}=V_{SS}$			5	$\mu\text{A}$
INO and IN1 low-level input current	$I_{IL2}$	$V_{IN}=V_{SS}$			5	$\mu\text{A}$
XIN low-level input current	$I_{IL3}$	$V_{IN}=V_{SS}$			20	$\mu\text{A}$
FMIN and AMIN low-level input current	$I_{IL4}$	$V_{IN}=V_{SS}$			40	$\mu\text{A}$
HCTR and LCTR low-level input current	$I_{IL5}$	$V_{IN}=V_{SS}$			40	$\mu\text{A}$
OUT1 to OUT2 high-level output voltage	$V_{OH1}$	$I_O=1\text{mA}$	$V_{DD}-1$			V
PD1 to PD2 high-level output voltage	$V_{OH2}$	$I_O=0.5\text{mA}$	$V_{DD}-1$			V
OUT1 to OUT2 low-level output voltage	$V_{OL1}$	$I_O=1\text{mA}$			1.0	V
PD1 to PD2 low-level output voltage	$V_{OL2}$	$I_O=0.5\text{mA}$			1.0	V
OUT3 to OUT6 low-level output voltage	$V_{OL3}$	$I_O=5\text{mA}$			1.0	V
OUT0 low-level output voltage	$V_{OL4}$	$I_O=1\text{mA}$			1.0	V
DO low-level output voltage	$V_{OL5}$	$I_O=5\text{mA}$			1.0	V
SYC low-level output voltage	$V_{OL6}$	$I_O=0.5\text{mA}$ , $V_{DD}=3.5$ to $6.5\text{V}$			1.0	V
OUT0 and OUT3 to OUT6 output off leakage current	$I_{OFF1}$	$V_O=13\text{V}$			5	$\mu\text{A}$
DO output off leakage current	$I_{OFF2}$	$V_O=6.5\text{V}$			5	$\mu\text{A}$
SYC output off leakage current	$I_{OFF3}$	$V_O=6.5\text{V}$			5	$\mu\text{A}$
PD1 and PD2 low-level off leakage current	$I_{OFFL}$	$V_O=V_{SS}$		0.01	10.0	nA
PD1 and PD2 high-level off leakage current	$I_{OFFH}$	$V_O=V_{DD}$		0.01	10.0	nA
FMIN and HCTR input capacitance	$C_{IN}$		1	2	3	pF
Supply current	$I_{DD}$	$f_{IN2}=130\text{MHz}$ , $V_{IN2}=70\text{mV}$ , $7.2\text{MHz}$ , crystal oscillator running, inputs grounded outputs open PLL inhibited, oscillator running, inputs grounded, outputs open		20	30	mA
				1.0		mA

## Functional Description

### Serial Data Input

The LC7219 and LC7219M are initialized by 36-bit data on the serial data input, DI, after power-on as shown in figure 1 and table 1.

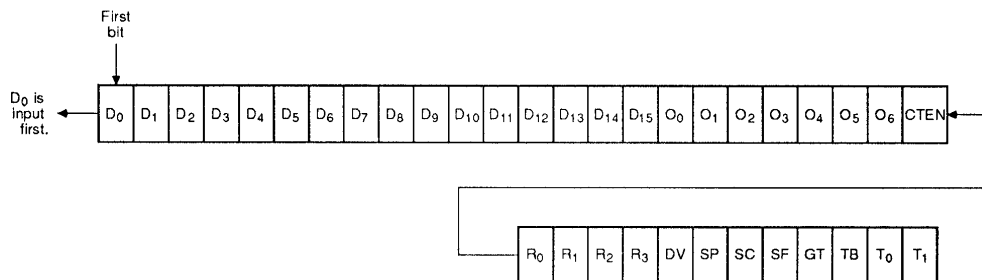


Figure 1. Input data format

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Table 1. Input data bits

Bits	Name	Description	Related bits
1 to 16	D <sub>0</sub> to D <sub>15</sub>	Programmable divider ratio D <sub>15</sub> is the msb. The lsb is determined by the setting of the DV and SP flags as shown in table 6. D <sub>0</sub> to D <sub>3</sub> are ignored if D <sub>4</sub> is the lsb.	DV, SP
17 to 23	O <sub>0</sub> to O <sub>6</sub>	Output port data Data bits O <sub>0</sub> to O <sub>6</sub> are latched into the $\overline{\text{OUT}}_0$ to $\overline{\text{OUT}}_6$ ports, respectively. When a data bit is 1, the corresponding output pin is LOW, and when 0, HIGH. These outputs can be used for frequency band selection. If TB is 1, the O <sub>0</sub> bit is ignored and the 8 Hz timebase signal is output on $\overline{\text{OUT}}_0$ .	TB
24	CTEN	General-purpose counter enable When CTEN is 0, the 20-bit general-purpose counter is reset and the HCTR and LCTR inputs are pulled to ground. When the CTEN flag is 1, the counter is enabled and the signal on HCTR or LCTR, selected by SC, is measured. Note that the general-purpose counter output should be transferred to the external controller before CTEN is set to 0.	SC, SF, GT
25 to 28	R <sub>0</sub> to R <sub>3</sub>	Reference frequency select Bits R <sub>0</sub> to R <sub>3</sub> disable the PLL or select the reference frequency as shown in table 2. When the PLL is disabled, the programmable divider is stopped, AMIN and FMIN are pulled to ground, and the charge-pump outputs become high impedance.	
29, 30	DV, SP	Divider select and sensitivity select DV select the local-oscillator input FMIN or AMIN. SP selects the input frequency range when AMIN is selected as shown in table 6.	
31, 32	SC, SF	General-purpose counter input select and frequency/period measurement select SC selects the general-purpose counter input. SF selects frequency or period measurement when LCTR is selected as shown in table 7. When HCTR is selected, the counter is in frequency measurement mode.	CTEN, GT
33	GT	General-purpose counter time interval select Bit GT selects the measurement time interval or the number of periods to be measured. When GT=1, then 30 ms or 2 periods are selected, and when GT=0, 60 ms or 1 period is selected.	CTEN, SC, SF
34	TB	Timebase output enable When TB is 1, the 8 Hz, 40% duty cycle timebase signal is output on $\overline{\text{OUT}}_0$ . The O <sub>0</sub> bits is ignored.	O <sub>0</sub>
35, 36	T <sub>0</sub> , T <sub>1</sub>	Test control bits Bits T <sub>0</sub> to T <sub>1</sub> are used for device testing and are set to 0 for normal operation.	

The reference frequency is selected by bits R<sub>0</sub> to R<sub>3</sub> as shown in table 2.

Table 2. Reference frequency selection

R <sub>0</sub>	R <sub>1</sub>	R <sub>2</sub>	R <sub>3</sub>	Reference frequency (kHz)
0	0	0	0	100
0	0	0	1	50
0	0	1	0	25
0	0	1	1	25
0	1	0	0	12.5
0	1	0	1	6.25
0	1	1	0	3.125
0	1	1	1	3.125

Table 2. Reference frequency selection—continued

R <sub>0</sub>	R <sub>1</sub>	R <sub>2</sub>	R <sub>3</sub>	Reference frequency (kHz)
1	0	0	0	10
1	0	0	1	9
1	0	1	0	5
1	0	1	1	1
1	1	0	0	PLL inhibit
1	1	0	1	
1	1	1	0	
1	1	1	1	

## Serial Data Input Timing

The timing for the serial data input is shown in figure 2. The first four bits, A<sub>0</sub> to A<sub>3</sub>, are the mode select bits. In 36-bit transfer mode, the final data bits are T<sub>0</sub> and T<sub>1</sub>, and in 24-bit transfer mode, O<sub>6</sub> and CTEN.

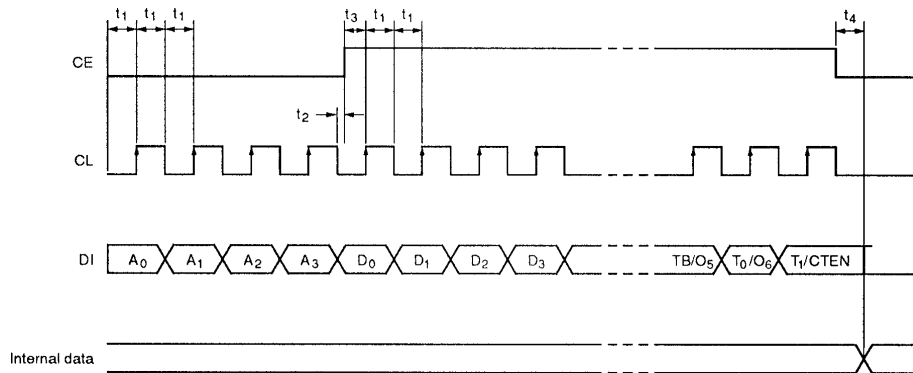


Figure 2. Input timing

### Note

$t_1 \geq 1.5\mu\text{s}$ ,  $t_2 \geq 0\mu\text{s}$ ,  $t_3 \geq 1.5\mu\text{s}$ ,  $t_4 < 1.5\mu\text{s}$

**Serial Data Output**

The LC7219 and LC7219M both have an internal 28-bit shift register that comprise two bits representing the state of IN0 and IN1 (I<sub>0</sub> and I<sub>1</sub>, respectively), a 20-bit general-purpose counter address (C<sub>0</sub> to C<sub>19</sub>) and unlock flags (UL0 to UL3) as shown in table 3.

The shift register contents are clocked out on DO when the serial data output mode is selected as shown in figure 3. The internal circuit of outputs DO and OUT0 to OUT6 are shown in figure 4.

Table 3. Shift register data

Bits	Name	Description
1, 2	I <sub>0</sub> , I <sub>1</sub>	Input port data I <sub>0</sub> is the state of IN0, and I <sub>1</sub> , the state of IN1.
3, 4		Invalid
5 to 24	C <sub>0</sub> to C <sub>19</sub>	General-purpose counter value Bits C <sub>0</sub> to C <sub>19</sub> are the latched value of the 20-bit counter. C <sub>19</sub> is the msb.
25 to 28	UL3 to UL0	PLL unlock status bits Bits UL0 to UL3 are the latched data from the unlock detector circuit. When the phase error exceeds the value for a given bit as shown below for a 7.2MHz crystal, the bit is set. UL0 is set when $\Phi_{ERROR} \geq 1.1\mu s$ UL1 is set when $\Phi_{ERROR} \geq 2.2\mu s$ UL2 is set when $\Phi_{ERROR} \geq 3.3\mu s$ UL3 is set when $\Phi_{ERROR} \geq 0.55\mu s$

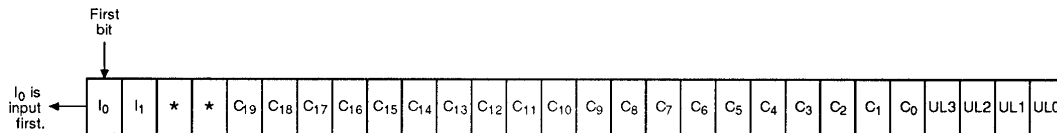


Figure 3. Shift register data format

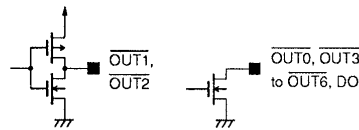


Figure 4. Output driver internal circuits

**Serial Data Output Timing**

The timing for the serial data output is shown in figure 5. Bits A<sub>0</sub> to A<sub>3</sub> are the mode select bits. When CE goes HIGH, I<sub>0</sub> is output on DO, and each subsequent data bit is output on the falling edge of CL. CE should be held HIGH for 27 clock cycles to allow all data to be output.

In serial data output mode, DO is forced HIGH when CE goes LOW as shown in figure 5. DO goes LOW when the status of IN0 changes. In frequency or period measurement modes, DO goes LOW when frequency or period measurement is completed.

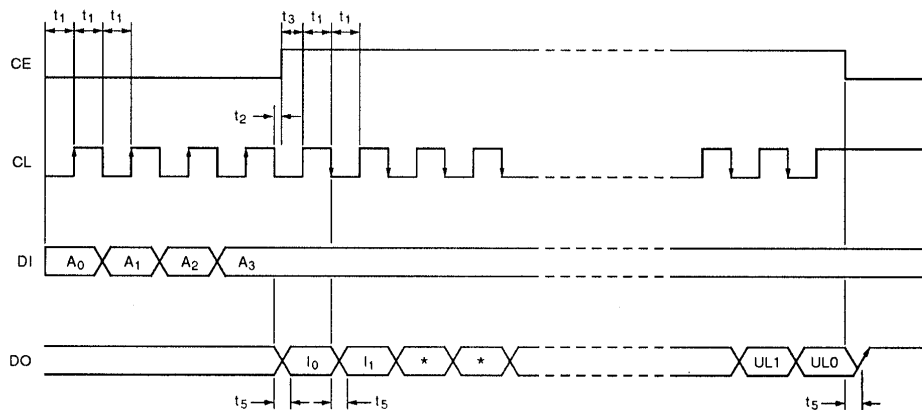


Figure 5. Output timing

**Note**

t<sub>1</sub> ≥ 1.5μs, t<sub>2</sub> ≥ 0μs, t<sub>3</sub> ≥ 1.5μs, t<sub>5</sub> < 1.5μs

**Serial Bus Data Transfer**

The LC7219 and LC7219M can both transfer data in three different modes-36-bit input data transfer, 24-bit input data transfer and 28-bit output data transfer. The transfer mode is selected by the four data bits on DI immediately prior to CE going HIGH as shown in figure 6 and table 4. These bits are synchronized to the clock and are latched into the mode register on the rising edge of CE.

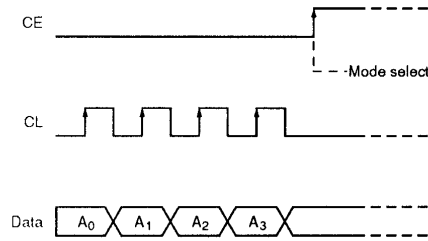


Figure 6. Transfer mode select

Table 4. Mode selection

Mode	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	Description
36-bit serial data input	0	0	0	1	All bits of the control data are clocked in on DI. This mode could be used after power-up to initialize the device. It can also be used to modify the values of bits R <sub>0</sub> to R <sub>1</sub> .
24-bit serial data input	0	0	1	0	24 bits of the control data are clocked in on DI. This mode is used to input the programmable divider ratio bits, the output port bits and the general-purpose counter enable bit.
serial data output	0	0	1	1	Data is output on DO. The data comprises the input data, the general-purpose counter value and the PLL unlock flags.
Illegal	0	0	0	0	Data cannot be transferred.
	0	1	×	×	
	1	0	×	×	
	1	1	×	×	

**Note**

× = don't care

**Programmable Divider**

The configuration of the programmable divider is shown in figure 7. Input mode selection is shown in table 5.

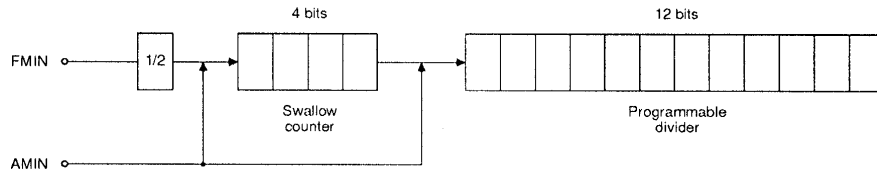


Figure 7. Programmable divider

Table 5. Programmable divider selection

DV	SP	Input frequency range (MHz)	1/2 divider	1/16 and 1/17 pulse swallower	12-bit programmable divider	Input port
1	×	10 to 160	✓	✓	✓	FMIN
0	1	2 to 40	–	✓	✓	AMIN
0	0	0.5 to 10.0	–	–	✓	AMIN

**Note**

× = don't care

When an FM signal is input on FMIN, the actual divider ratio is double the set ratio. For channel steps of 1, 5 and 9 kHz, a 3.6MHz crystal should be used. The programmable divider ratio is determined by the setting of the DV and SP bits as shown in table 6.

Table 6. Divider ratio settings

DV	SP	lsb	Set ratio	Actual ratio
1	×	D0	256 to 65535	Twice set ratio
0	1	D0	256 to 65535	Set ratio
0	0	D4	4 to 4096	Set ratio

**Note**

× = don't care

**General-purpose Counter**

The 20-bit general-purpose counter is used for both frequency and period measurement as shown in figure 8. The measurement mode is selected by bits SC and SF as shown in table 7. The counter value is output on DO with the msb first.

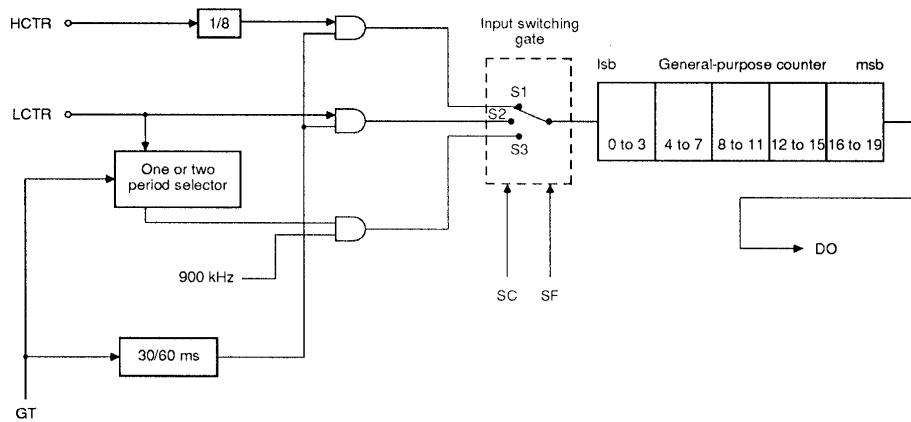


Figure 8. General-purpose counter

Table 7. General-purpose counter mode selection

SC	SF	Input port	Parameter
1	×	HCTR	Frequency measurement (sine wave)
0	1	LCTR	Frequency measurement (sine wave)
0	0	LCTR	Period measurement (pulse wave)

**Note**

× = don't care

In frequency measurement mode, the input cycles during a 30 or 60 ms interval are counted. Either LCTR or HCTR can be selected as the counter input.

In period measurement mode, LCTR is the single input, and the 900kHz cycles in one or two periods of the LCTR signal are counted.

The counter starts when the CTEN flag is set. The serial input data is latched in on the falling edge of CE. The input data on HCTR or LCTR should be input within 10 ms of this transition.

The period or frequency measurement count should be read while CTEN is still set to 1, as the counter is reset by setting CTEN to 0. CTEN should be set to 0 before each measurement.

The LCTR signal is passed directly to the counter input. The HCTR signal is passed through a divide-by-eight prescaler. The actual HCTR frequency is, therefore, eight times the measured frequency.

When the universal counter is used as the IF counter, the state of the IF-IC SD (station detect) signal must be checked by the microcontroller, and the IF counter buffer output turned on only after the SD signals are activated. Auto-search techniques using only the IF counter are not advisable since it is possible that the search can stop incorrectly at a location that does not have a station due to the IF counter buffer output leakage.

DO goes HIGH when the CTEN flag is set to 1, and LOW when frequency or period measurement is completed. DO can be monitored to check for measurement completion. The timing for the general-purpose counter is shown in figure 9.



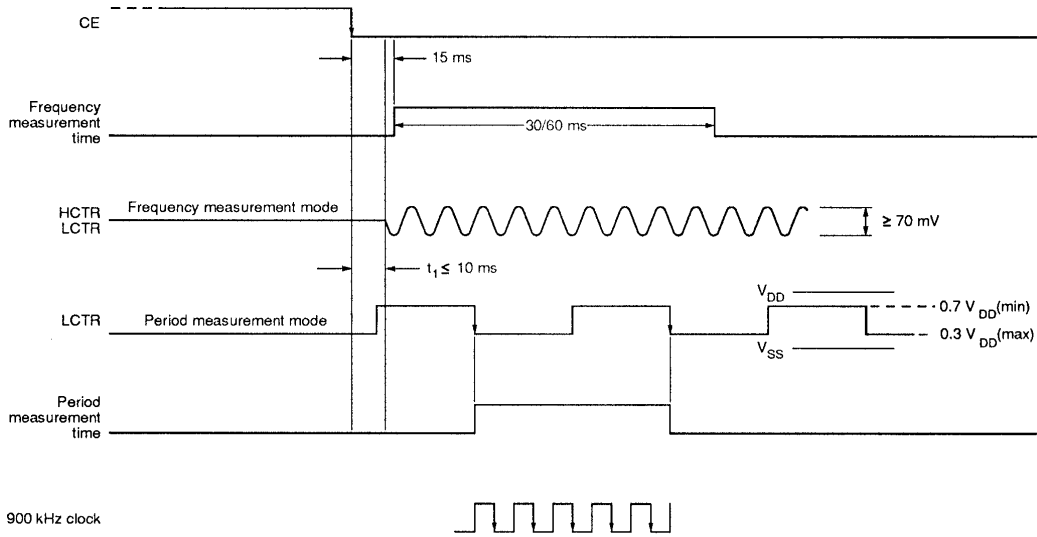


Figure 9. General-purpose counter timing

### Using DO monitor IN0

If the general-purpose counter is not being used and CTEN is 0, DO can be used to monitor changes in the external input signal IN0 as shown in figure 10.

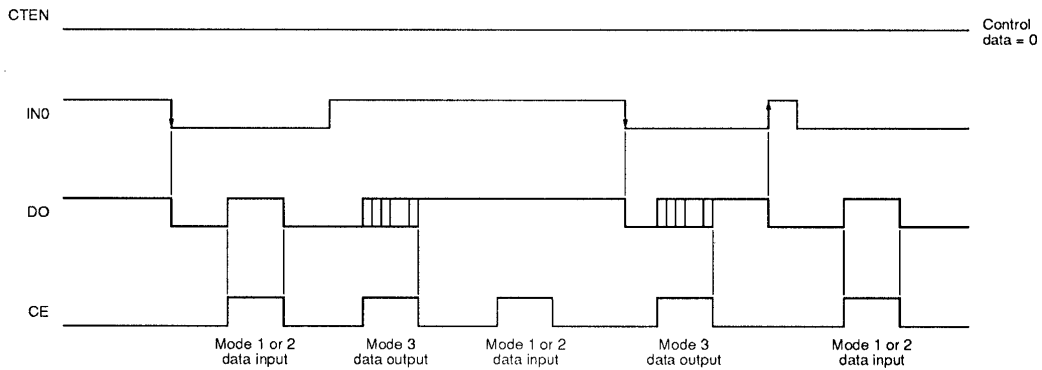


Figure 10. IN0 output monitoring timing

### Notes

1. Specify serial data output. DO goes HIGH after data is output on DO and CE goes LOW.
2. DO goes LOW when IN0 changes.

### Using DO to monitor for measurement completion

DO can be used to monitor for frequency or period measurement completion as shown in figure 11.

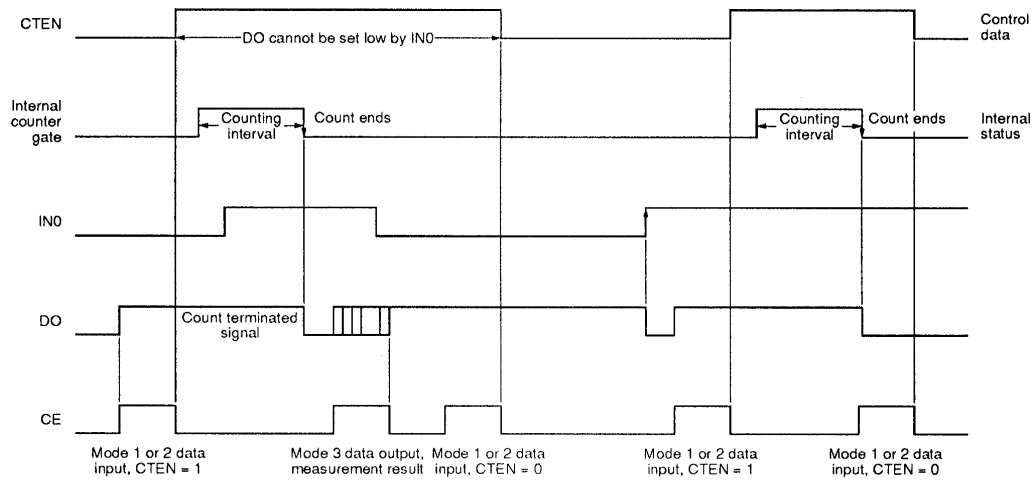


Figure 11. Measurement completion timing

#### Notes

1. Setting CTEN to 1 sets DO HIGH and prevents IN0 from affecting DO.
2. DO goes LOW when the measurement is complete.

## Phase-locked Loop

### Reading the PLL unlock flags

The PLL unlock flags are set on the rising edge of the internal  $\Phi_{ERROR}$  signal and cleared on the rising edge of the CE signal. In serial data output mode, the flags set since the last rising edge of CE can be read. This is the interval  $t_0$  to  $t_1$  shown in figure 12.

Each PLL unlock flag is set if the corresponding time interval is exceeded as follows.

UL0 is set when  $\Phi_{ERROR} \geq 1.11\mu s$

UL1 is set when  $\Phi_{ERROR} \geq 2.22\mu s$

UL2 is set when  $\Phi_{ERROR} \geq 3.33\mu s$

UL3 is set when  $\Phi_{ERROR} \geq 0.55\mu s$

The flag values for different error ranges, where  $\Phi_{ERROR}$  is the phase error for the 7.2MHz crystal, are as follows.

If  $\Phi_{ERROR} < 0.55\mu s$ , UL=0000

If  $0.55\mu s \leq \Phi_{ERROR} < 1.11\mu s$ , UL=1000

If  $1.11\mu s \leq \Phi_{ERROR} < 2.22\mu s$ , UL=1001

If  $2.22\mu s \leq \Phi_{ERROR} < 3.33\mu s$ , UL=1011

If  $3.33\mu s \leq \Phi_{ERROR}$ , UL=1111

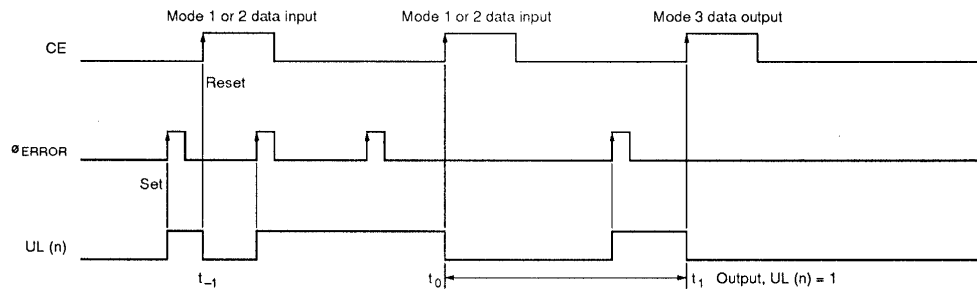


Figure 12. PLL unlock flag timing

# LC7219, 7219M

## Application Notes

The recommended crystal oscillator for the LC7219 and LC7219M is the Nihon Dempa Kogyo Co., Ltd. (NDK) LN-X-0702 (NR-18 type) or the LN-P-0001 (AT-51 type). The oscillator is connected as shown in figure 13.

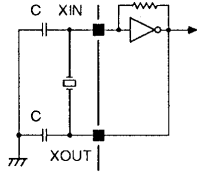


Figure 13. Crystal oscillator connection

The device parameters for crystal oscillator frequencies 3.6MHz and 7.2MHz are shown in table 8.

Table 8. Device parameters vs. crystal frequency

Parameter	Crystal frequency	
	7.2MHz	3.6MHz
Timebase clock	8Hz	4Hz
System clock	400kHz	200kHz
Frequency measurement interval	30/60ms	60/120ms
Period measurement check signal	900kHz	450kHz
Reference frequencies	1kHz, 5kHz, 9kHz, 10kHz, 25kHz, 50kHz, 100kHz,	0.5kHz, 2.5kHz, 4.5kHz, 5kHz, 12.5kHz, 25kHz, 50kHz,
Data input/output timing	$t_1$ 1.5 $\mu$ s, $t_3$ 1.5 $\mu$ s	$t_1$ 3 $\mu$ s, $t_2$ 3 $\mu$ s

## Typical Application

Figure 14 shows a TV/AM/FM system using the IF counting system for electronic tuning.

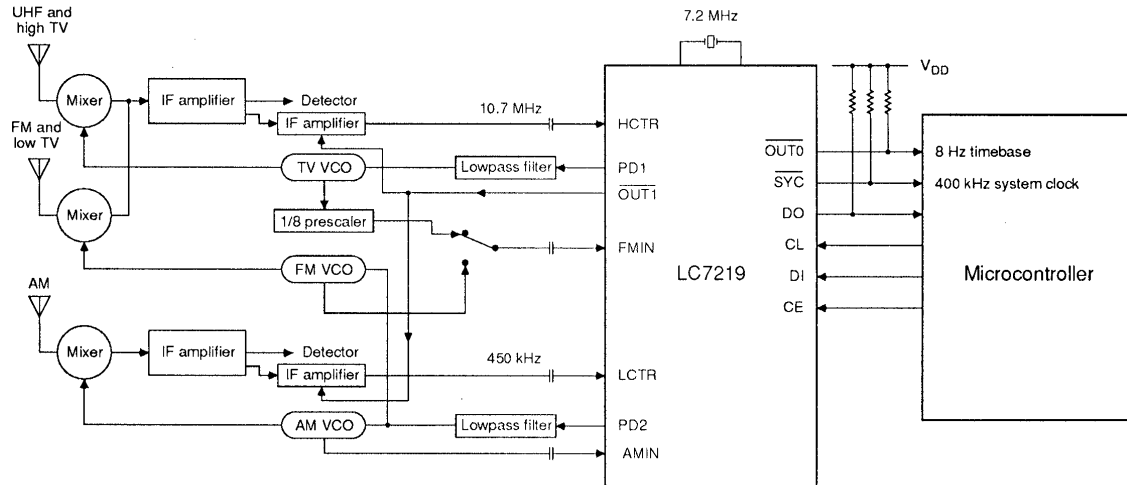


Figure 14. TV/AM/FM system

The FMIN, AMIN, HCTR, and LCTR inputs should be capacitively coupled using a capacitor in the range 50 to 100pF. These coupling capacitors should be as close as possible to their respective inputs to minimize the effects of stray capacitance.

The IF signals measurement should be done after the IF-IC SD (station detect) signal are activated.

The circuit characteristics for each mode, TV, FM and AM, are shown in table 9.

Table 9. Circuit characteristics

Mode	DV	SP	Tuning frequency steps	RF frequency	IF frequency	VCO frequency	PLL reference frequency	Programmable divider ratio
TV	1	×	50kHz	637.75MHz (UHF)	10.7MHz	648.45MHz	3.125kHz	12,969
FM	1	×	100kHz	90MHz	10.7MHz	100.7MHz	50kHz	1,007
AM	0	0	10kHz	1,000kHz	450kHz	1,450kHz	10kHz	145

## Note

× = don't care

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