CY7C135
CY7C1342

4K x 8 Dual-Port Static RAM and 4K x 8 Dual-Port SRAM with Semaphores

Features

- **True Dual-Ported memory cells which allow simultaneous reads of the same memory location**
- **4K x 8 organization**
- **0.65-micron CMOS for optimum speed/power**
- **High-speed access: 15 ns**
- **Low operating power: I_{CC} = 160 mA (max.)**
- **Fully asynchronous operation**
- **Automatic power-down**
- **Semaphores included on the 7C1342 to permit software handshaking between ports**
- **Available in 52-pin PLCC**
- **Pb-Free packages available**

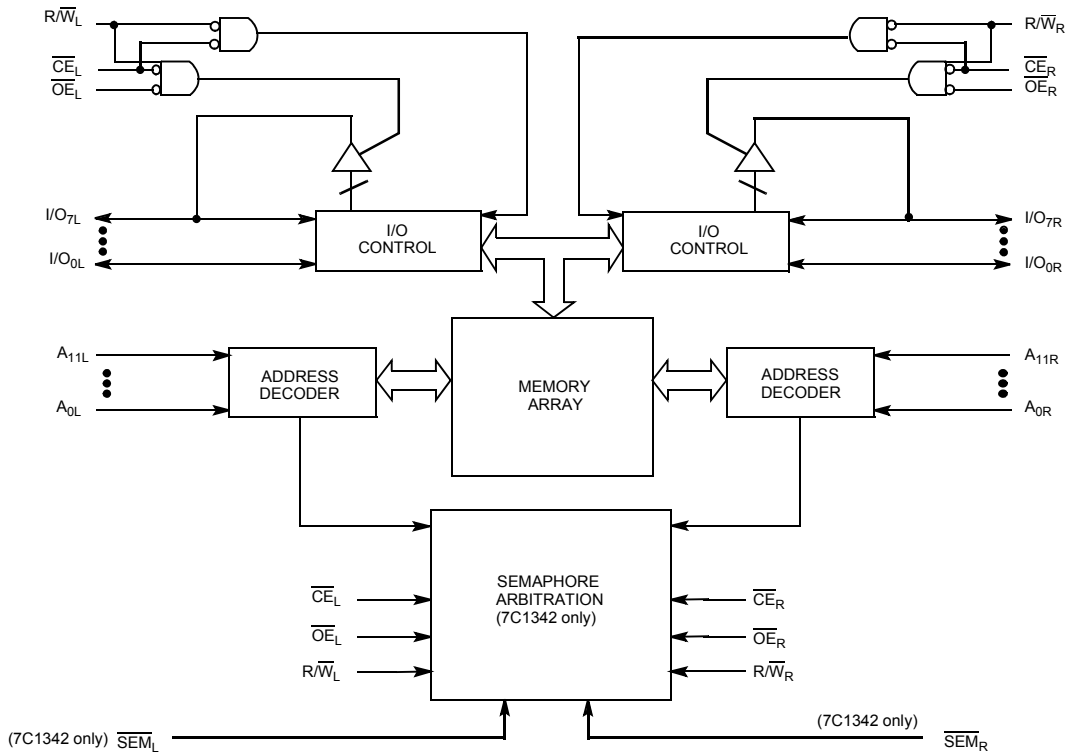
Functional Description

The CY7C135 and CY7C1342 are high-speed CMOS 4K x 8 dual-port static RAMs. The CY7C1342 includes semaphores that provide a means to allocate portions of the dual-port RAM or any shared resource. Two ports are provided permitting independent, asynchronous access for reads and writes to any location in memory. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: chip enable ($\overline{CE}$), read or write enable (R/$\overline{W}$), and output enable ($\overline{OE}$). The CY7C135 is suited for those systems that do not require on-chip arbitration or are intolerant of wait states. Therefore, the user must be aware that simultaneous access to a location is possible. Semaphores are offered on the CY7C1342 to assist in arbitrating between ports. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a chip enable ($\overline{CE}$) pin or $\overline{SEM}$ pin (CY7C1342 only).

The CY7C135 and CY7C1342 are available in 52-pin PLCC.

Logic Block Diagram

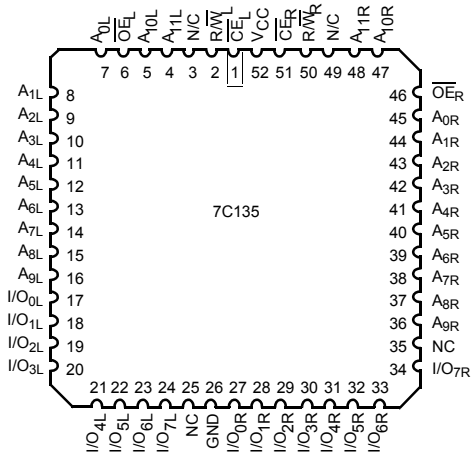


Selection Guide

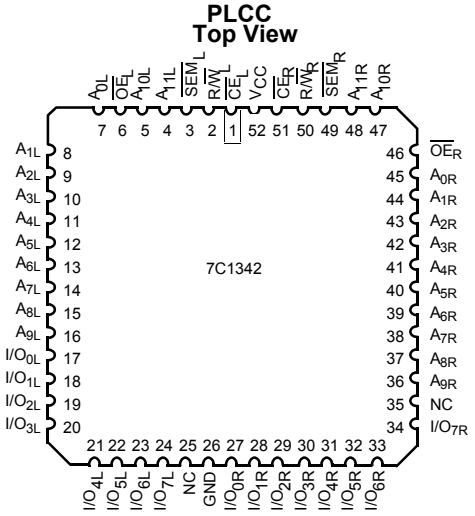
		7C135-15 7C1342-15	7C135-20 7C1342-20	7C135-25 7C1342-25	7C135-35 7C1342-35	7C135-55 7C1342-55	Unit
Maximum Access Time		15	20	25	35	55	ns
Maximum Operating Current	Commercial	220	190	180	160	160	mA
Maximum Standby Current for I_{SB1}	Commercial	60	50	40	30	30	mA

Pin Configurations

PLCC Top View



PLCC Top View



Pin Definitions

Left Port	Right Port	Description
$A_{0L–11L}$	$A_{0R–11R}$	Address Lines
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{SEM}_L$ (CY7C1342 only)	$\overline{SEM}_R$ (CY7C1342 only)	Semaphore Enable. When asserted LOW, allows access to eight semaphores. The three least significant bits of the address lines will determine which semaphore to write or read. The I/O_0 pin is used when writing to a semaphore. Semaphores are requested by writing a 0 into the respective location.

Maximum Ratings[1]

Storage Temperature .....–65°C to+150°C

Ambient Temperature with Power Applied.....–55°C to+125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24) .....–0.5V to+7.0V

DC Voltage Applied to Outputs in High Z State .....–0.5V to+7.0V

DC Input Voltage[2].....–3.0V to +7.0V

Static Discharge Voltage.....> 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current.....> 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7C135-15 7C1342-15 Min.	7C135-15 7C1342-15 Max.	7C135-20 7C1342-20 Min.	7C135-20 7C1342-20 Max.	7C135-25 7C1342-25 Min.	7C135-25 7C1342-25 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2		2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–10	+10	–10	+10	–10	+10	µA
I_{OZ}	Output Leakage Current	Outputs Disabled, GND ≤ V_O ≤ V_{CC}		–10	+10	–10	+10	–10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		220		190		180	mA
			Ind.						190	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[3]	Com'l		60		50		40	mA
			Ind.						50	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[3]	Com'l		130		120		110	mA
			Ind.						120	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0[3]	Com'l		15		15		15	mA
			Ind.						30	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥V_{CC} – 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[3]	Com'l		125		115		100	mA
			Ind.						115	

Notes:
1. The Voltage on any input or I/O pin cannot exceed the power pin during power-up.
2. Pulse width < 20 ns.
3. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.

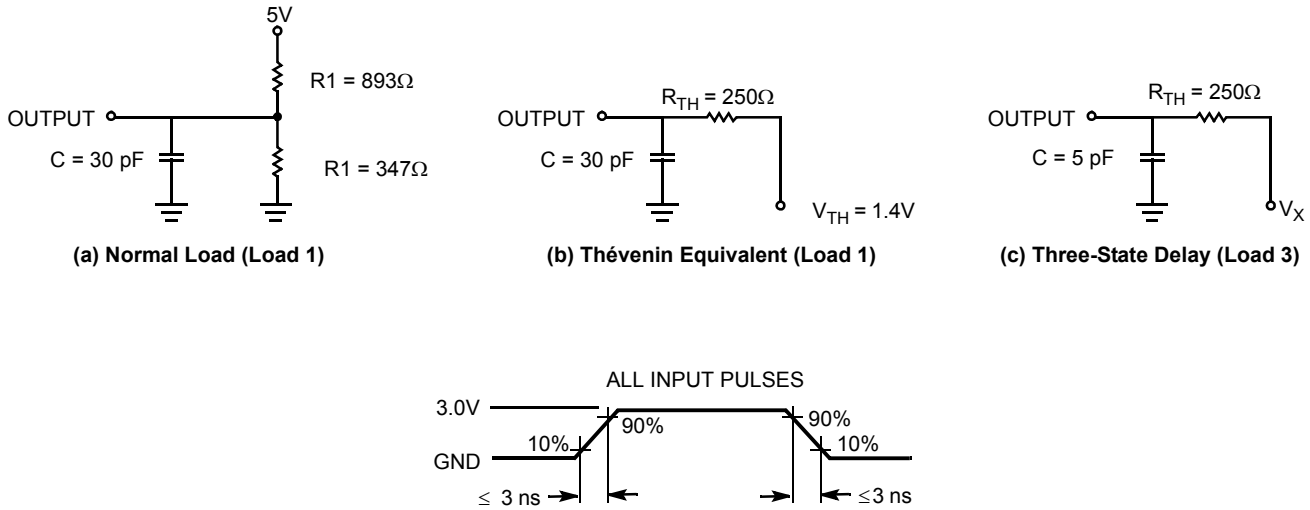
Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Test Conditions		7C135-35 7C1342-35 Min.	7C135-35 7C1342-35 Max.	7C135-55 7C1342-55 Min.	7C135-55 7C1342-55 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4		0.4	V
V_{IH}				2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–10	+10	–10	+10	μA
I_{OZ}	Output Leakage Current	Outputs Disabled, GND ≤ V_O ≤ V_{CC}		–10	+10	–10	+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		160		160	mA
		V_{CC} = Max., I_{OUT} = 0 mA	Ind.		180		180	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[3]	Com'l		30		30	mA
			Ind.		40		40	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[3]	Com'l		100		100	mA
			Ind.		110		110	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0[3]	Com'l		15		15	mA
			Ind.		30		30	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[3]	Com'l		90		90	mA
			Ind.		100		100	

Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms



(a) Normal Load (Load 1) **(b) Thévenin Equivalent (Load 1)** **(c) Three-State Delay (Load 3)**

Note:
4. Tested initially and after any design or process changes that may affect these parameters.

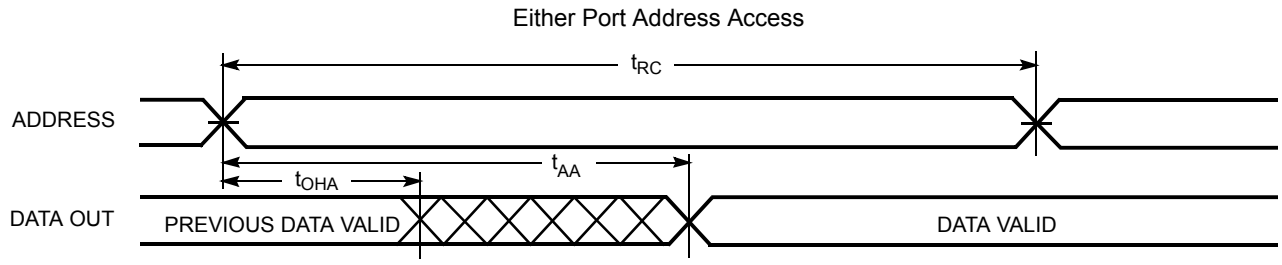
Switching Characteristics Over the Operating Range[5]

Parameter	Description	7C135-15 7C1342-15		7C135-20 7C1342-20		7C135-25 7C1342-25		7C135-35 7C1342-35		7C135-55 7C1342-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	15		20		25		35		55		ns
t_{AA}	Address to Data Valid		15		20		25		35		55	ns
t_{OHA}	Output Hold From Address Change	3		3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		20		25		35		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		13		15		20		25	ns
t_{LZOE}[6,7,8]	$\overline{OE}$ Low to Low Z	3		3		3		3		3		ns
t_{HZOE}[6,7,8]	$\overline{OE}$ HIGH to High Z		10		13		15		20		25	ns
t_{LZCE}[6,7,8]	$\overline{CE}$ LOW to Low Z	3		3		3		3		3		ns
t_{HZCE}[6,7,8]	$\overline{CE}$ HIGH to High Z		10		13		15		20		25	ns
t_{PU}[8]	$\overline{CE}$ LOW to Power Up	0		0		0		0		0		ns
t_{PD}[8]	$\overline{CE}$ HIGH to Power Down		15		20		25		35		55	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	15		20		25		35		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		15		20		30		50		ns
t_{AW}	Address Set-Up to Write End	12		15		20		30		50		ns
t_{HA}	Address Hold from Write End	2		2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	Write Pulse Width	12		15		20		25		50		ns
t_{SD}	Data Set-Up to Write End	10		13		15		15		25		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{HZWE}[7,8]	R/$\overline{W}$ LOW to High Z		10		13		15		20		25	ns
t_{LZWE}[7,8]	R/$\overline{W}$ HIGH to Low Z	3		3		3		3		3		ns
t_{WDD}[9]	Write Pulse to Data Delay		30		40		50		60		70	ns
t_{DDD}[9]	Write Data Valid to Read Data Valid		25		30		30		35		40	ns
SEMAPHORE TIMING[10]												
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10		10		10		15		15		ns
t_{SWRD}	SEM Flag Write to Read Time	5		5		5		5		5		ns
t_{SPS}	SEM Flag Contention Window	5		5		5		5		5		ns

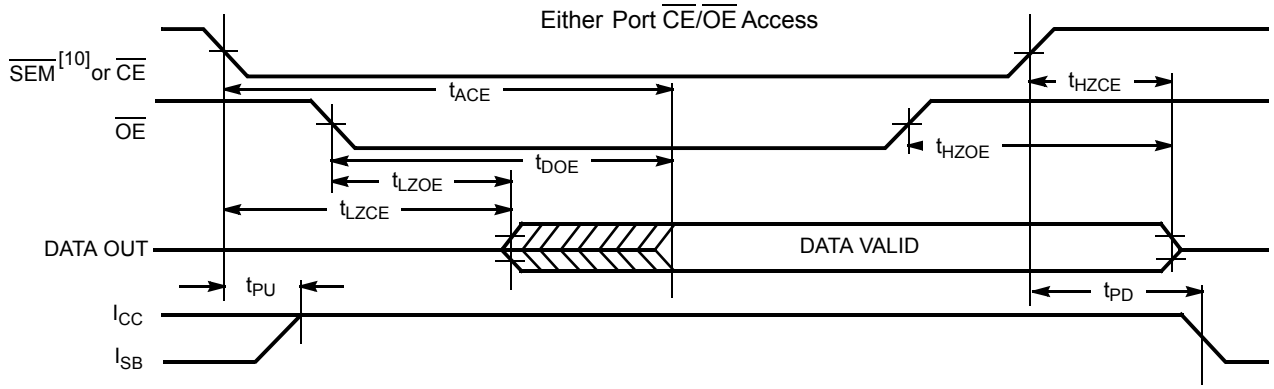
Notes:
5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
7. Test conditions used are Load 3.
8. This parameter is guaranteed but not tested.
9. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Port-to-Port Delay waveform.
10. Semaphore timing applies only to CY7C1342.

Switching Waveforms

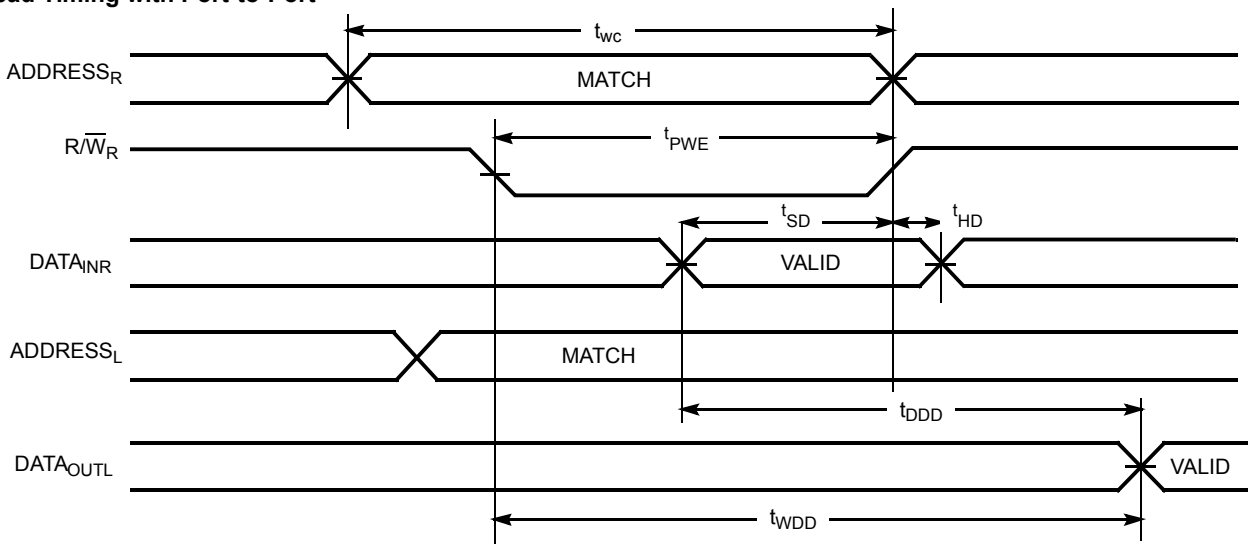
Read Cycle No. 1[11,12]



Read Cycle No. 2[11,13]



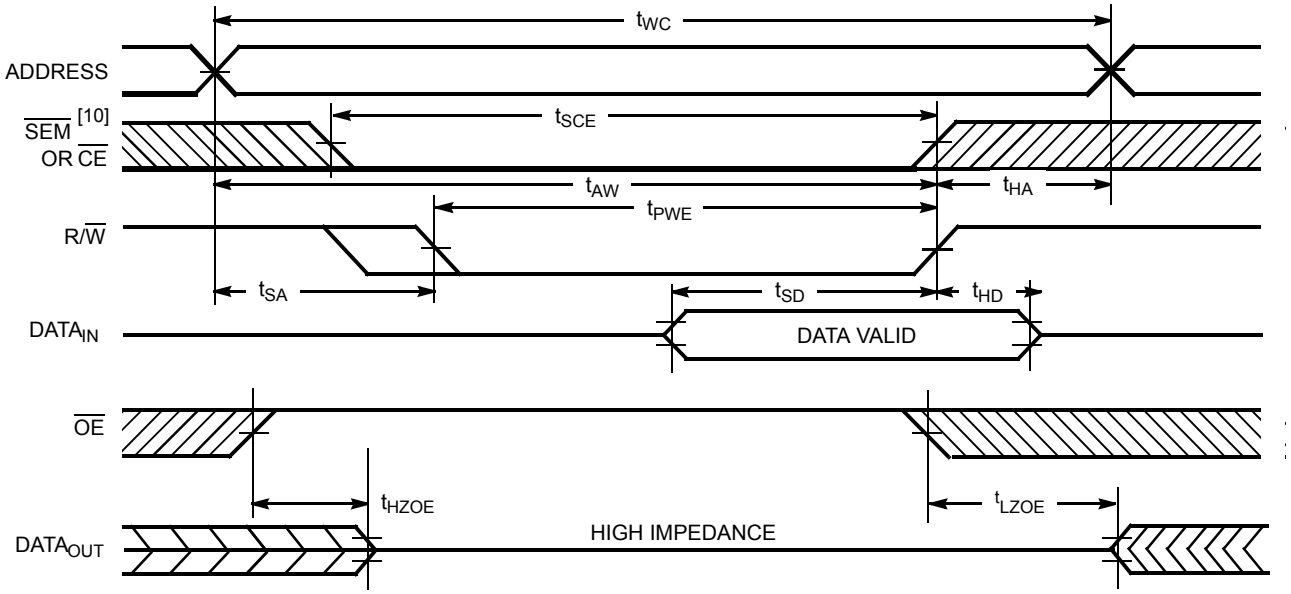
Read Timing with Port-to-Port[14]



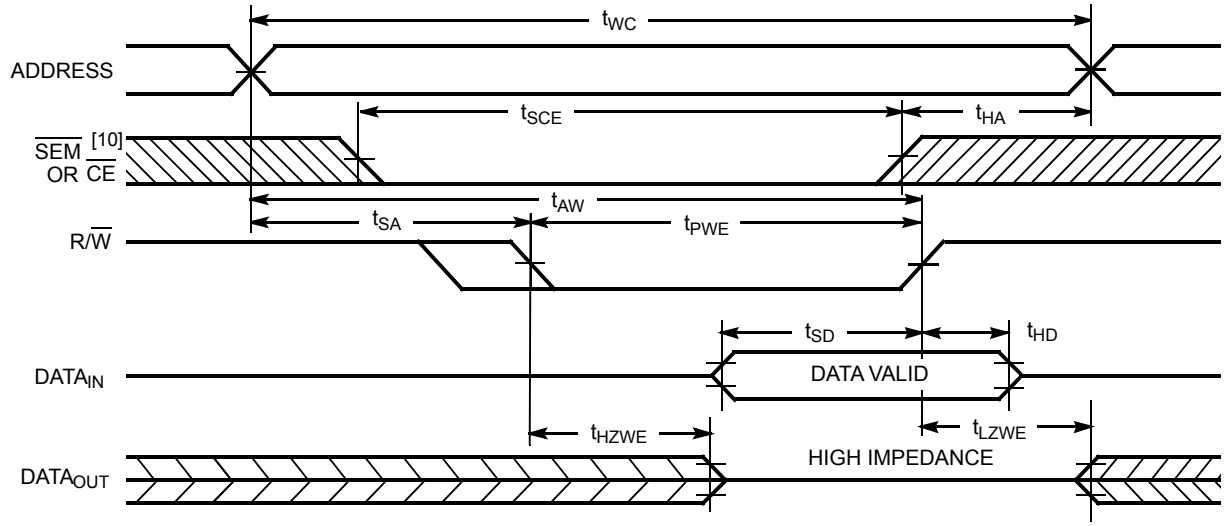
Notes:
11. R/$\overline{W}$ is HIGH for read cycle.
12. Device is continuously selected, $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IL}.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
14. $\overline{CE}_L$ = $\overline{CE}_R$ =LOW; R/$\overline{W}_L$ = HIGH

Switching Waveforms (continued)

Write Cycle No. 1: OE Three-States Data I/Os (Either Port)[15, 16, 17]



Write Cycle No. 2:R/W Three-States Data I/Os (Either Port)[16, 18]

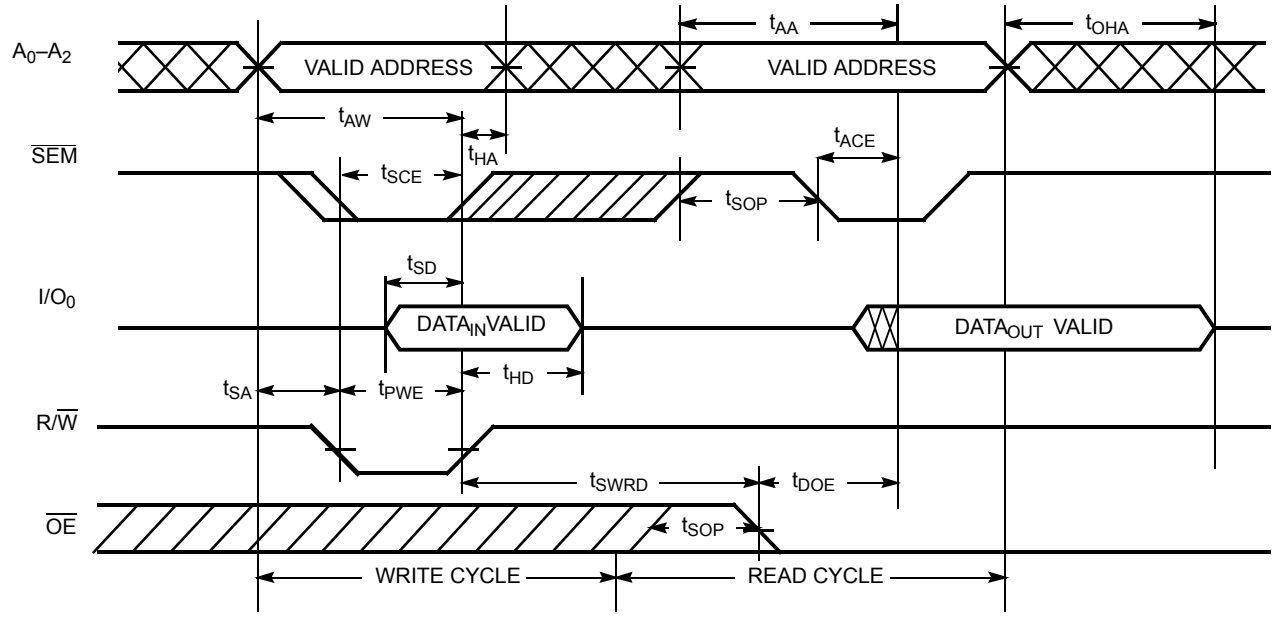


Notes:

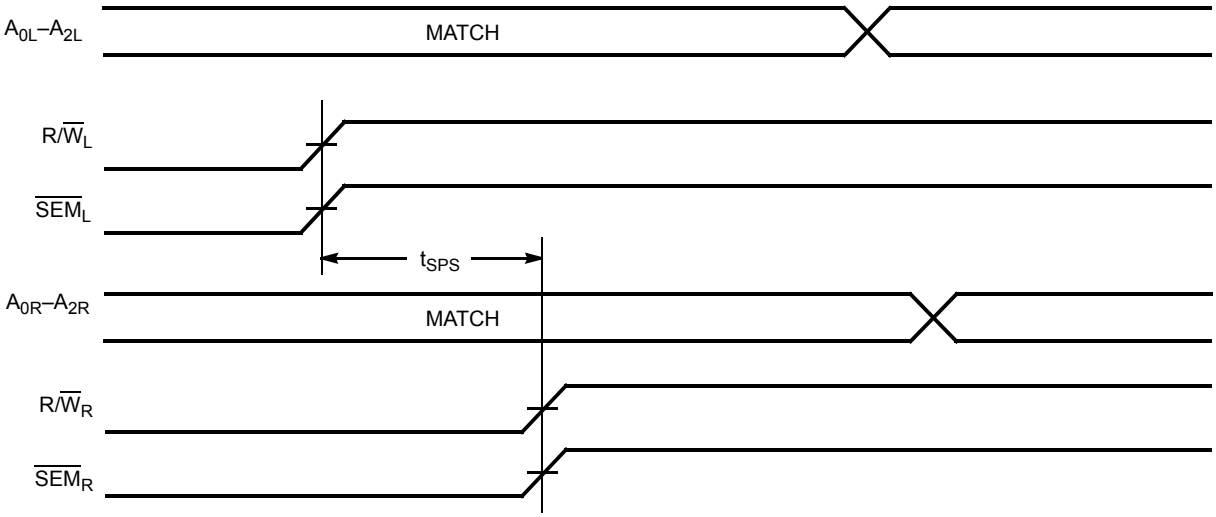
15. The internal write time of the memory is defined by the overlap of CE or SEM LOW and R/W LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
16. R/W must be HIGH during all address transactions.
17. If OE is LOW during a R/W controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If OE is HIGH during a R/W controlled write cycle (as in this example), this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
18. Data I/O pins enter high-impedance when OE is held LOW during write.

Switching Waveforms (continued)

Semaphore Read After Write Timing, Either Side (CY7C1342 only)[19]



Timing Diagram of Semaphore Contention (CY7C1342 only)[20, 21, 22]



Notes:
19. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).
20. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH.
21. Semaphores are reset (available to both ports) at cycle start.
22. If t_{SPS} is violated, it is guaranteed that only one side will gain access to the semaphore.

Architecture

The CY7C135 consists of an array of 4K words of 8 bits each of dual-port RAM cells, I/O and address lines, and control signals ($\overline{CE}$, $\overline{OE}$, R/$\overline{W}$). Two semaphore control pins exist for the CY7C1342 ($SEM_{L/R}$).

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/$\overline{W}$ in order to guarantee a valid write. Since there is no on-chip arbitration, the user must be sure that a specific location will not be accessed simultaneously by both ports or erroneous data could result. A write operation is controlled by either the $\overline{OE}$ pin (see Write Cycle No. 1 timing diagram) or the R/$\overline{W}$ pin (see Write Cycle No. 2 timing diagram). Data can be written t_{HZOE} after the $\overline{OE}$ is deasserted or t_{HZWE} after the falling edge of R/$\overline{W}$. Required inputs for write operations are summarized in *Table 1*.

If a location is being written to by one port and the opposite port attempts to read the same location, a port-to-port flowthrough delay is met before the data is valid on the output. Data will be valid on the port wishing to read the location t_{DDD} after the data is presented on the writing port.

Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data will be available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ are asserted. If the user of the CY7C1342 wishes to access a semaphore, the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$ pin. Required inputs for read operations are summarized in *Table 1*.

Semaphore Operation

The CY7C1342 provides eight semaphore latches which are separate from the dual port memory locations. Semaphores are used to reserve resources which are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{SEM}$ or $\overline{OE}$ must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control over the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip enable for the semaphore latches. $\overline{CE}$ must remain HIGH during $\overline{SEM}$ LOW. A_{0-2} represents the semaphore address. $\overline{OE}$ and R/$\overline{W}$ are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a 0 is written to the left port of an unused semaphore, a one will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing a zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore will be set to one for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port would immediately own the semaphore. *Table 2* shows sample semaphore operations.

When reading a semaphore, all eight data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports request a semaphore control by writing a 0 to a semaphore within t_{SPS} of each other, it is guaranteed that only one side will gain access to the semaphore.

Initialization of the semaphore is not automatic and must be reset during initialization program at power-up. All semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

Table 1. Non-Contending Read/Write

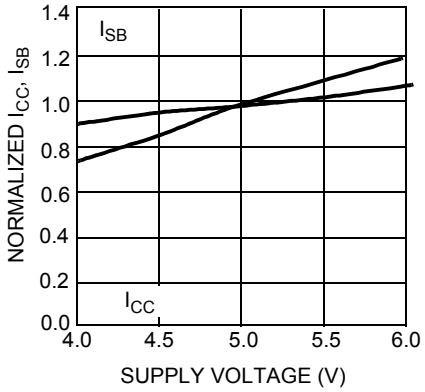
Inputs				Outputs	Operation
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	$I/O_0 – I/O_7$	
H	X	X	H	High Z	Power-Down
H	H	L	L	Data Out	Read Semaphore
X	X	H	X	High Z	I/O Lines Disabled
H	L	X	L	Data In	Write to Semaphore
L	H	L	H	Data Out	Read
L	L	X	H	Data In	Write
L	X	X	L		Illegal Condition

Table 2. Semaphore Operation Example

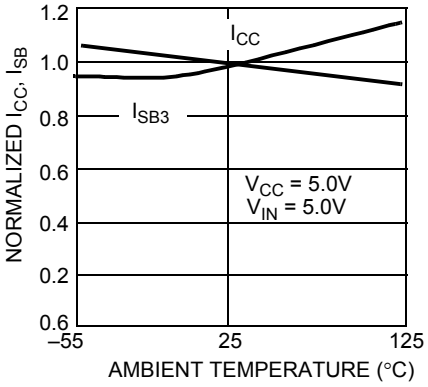
Function	I/O_{0-7} Left	I/O_{0-7} Right	Status
No Action	1	1	Semaphore free
Left port writes semaphore	0	1	Left port obtains semaphore
Right port writes 0 to semaphore	0	1	Right side is denied access
Left port writes 1 to semaphore	1	0	Right port is granted access to Semaphore
Left port writes 0 to semaphore	1	0	No change. Left port is denied access
Right port writes 1 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore address
Right port writes 0 to semaphore	1	0	Right port obtains semaphore
Right port writes 1 to semaphore	1	1	No port accessing semaphore
Left port writes 0 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore

Typical DC and AC Characteristics

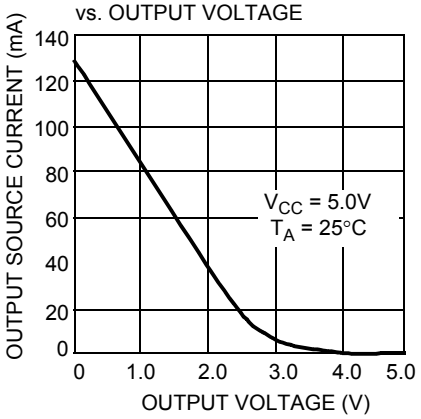
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



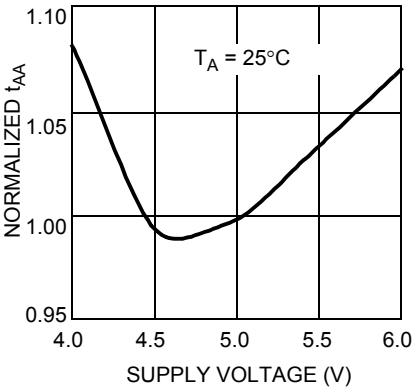
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



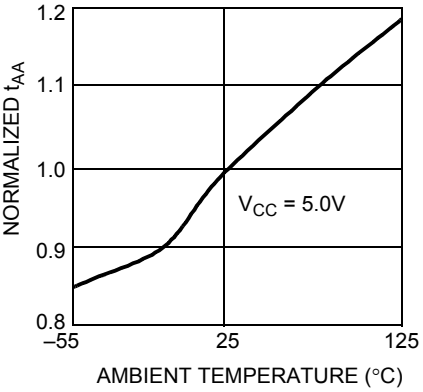
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



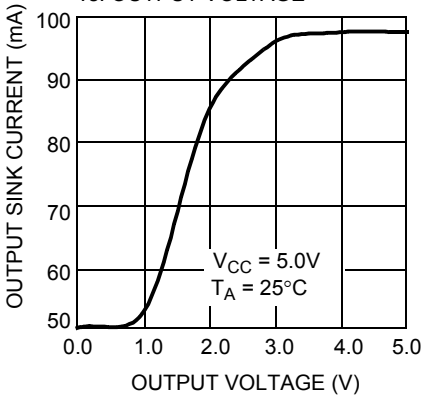
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



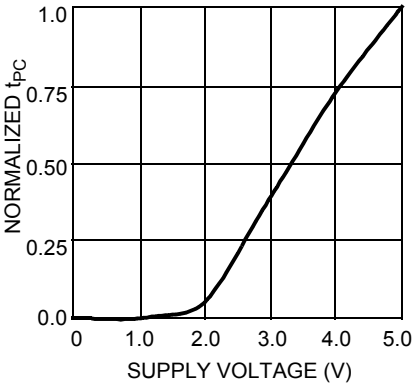
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



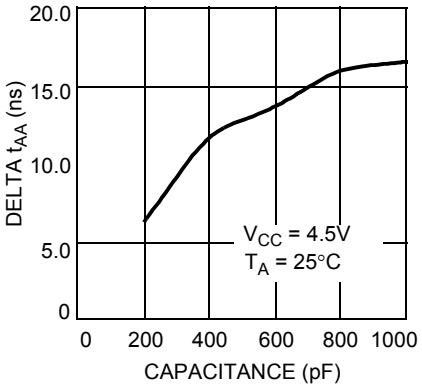
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



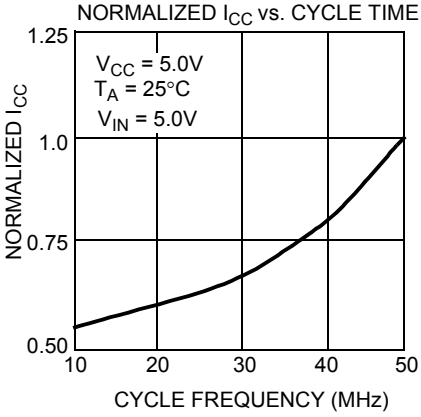
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED ICC vs. CYCLE TIME



Ordering Information

4K x8 Dual-Port SRAM

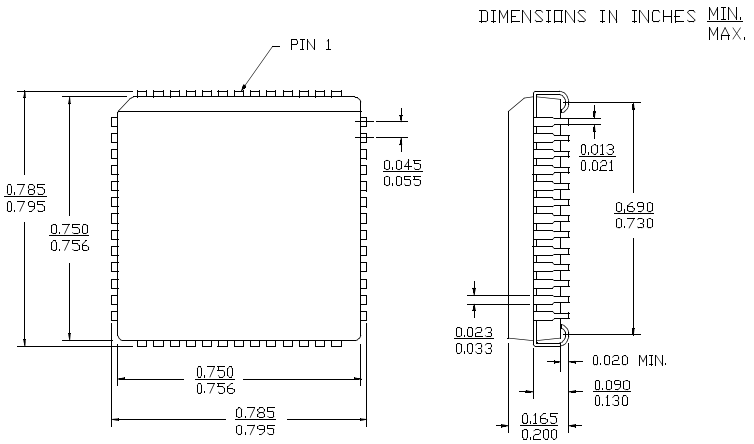
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C135–15JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C135-15JXC	J69	52-Lead Pb-Free Plastic Leaded Chip Carrier	
20	CY7C135–20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
25	CY7C135–25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C135-25JXC	J69	52-Lead Pb-Free Plastic Leaded Chip Carrier	
	CY7C135–25JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C135–35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C135–35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
55	CY7C135–55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C135–55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial

4K x8 Dual-Port SRAM with Semaphores

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
15	CY7C1342–15JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
20	CY7C1342–20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
25	CY7C1342–25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1342–25JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C1342–35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1342–35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
55	CY7C1342–55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1342–55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial

Package Diagrams

52-Lead Plastic Leaded Chip Carrier J69
52-Lead Pb-Free Plastic Leaded Chip Carrier J69



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Document History Page

Document Title: CY7C135/CY7C1342 4K x 8 Dual Port Static RAM and 4K x 8 Dual Port Static RAM w/Semaphores Document Number: 38-06038				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110181	10/21/01	SZV	Change from Spec number: 38-00541 to 38-06038
*A	122288	12/27/02	RBI	Power up requirements added to Maximum Ratings Information
*B	236763	SEE ECN	YDT	Removed cross information from features section
*C	393413	See ECN	YIM	Added Pb-Free Logo Added Pb-Free parts to ordering information: CY7C135-15JXC, CY7C135-25JXC