8Mbit SGRAM

128K x 32bit x 2 Banks
Synchronous Graphic RAM
LVTTL

Revision 2.4

May 1998

Samsung Electronics reserves the right to change products or specification without notice.

Downloaded from Elcodis.com electronic components distributor

Revision History

Revision 2.4 (May 1998)

- Added KM4132G271B-7 product(143MHz @ CL =3).

Revision 2.3 (March 1998)

- Added Reverse Type Package in *ODERING INFORMATION and PIN CONFIGURATION.*
- Removed KM4132G271B-H/12 product(-H : 100MHz @ CL =2, -12 : 83MHz @ CL=3).
- Changed the Current values of ICC1, ICC3N, ICC4, ICC5, ICC6, ICC7 in *DC CHARACTERISTICS.*
- Changed tSAC from 6 to 6.5 @ 125MHz, tSS from 2 to 2.5 @ 125MHz in *AC PARAMETER* .
- Delete a page including *FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE.*

Revision 2.1 (November 1997)

- Changed the Height of TQFP Package from 1.4mmMAX to 1.2mmMax in *PACKAGE DIMENSIONS.*

Revision 2.0 (October 1997)

- Added -H binning(100MHz @ CL =2).
- Changed some values in *DC CHARACTERISTICS.*
- Changed some values in *AC PARAMETER* (tSAC / tOH / tSHZ / tRP / tRC / tBPL / tBWC etc.).
- Removed a AC Parameter, tBAL(Block write data-in to Active command period) in *AC PARAMETER* .
- Changed some values in *FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE.*
- Added the Package Type description(PQFP, TQFP) in *PACKAGE DIMENSIONS.*

Downloaded from Elcodis.com electronic components distributor

128K x 32Bit x 2 Banks Synchronous Graphic RAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Dual bank / Pulse $\overline{RAS}$
- MRS cycle with address key programs
  - -. CAS Latency (2, 3)
  - -. Burst Length (1, 2, 4, 8 & full page)
  - -. Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Burst Read Single-bit Write operation
- DQM 0-3 for byte masking
- Auto & self refresh
- 16ms refresh period (1K cycle)
- 100 Pin PQFP, TQFP (14 x 20 mm)
- Reverse Type Package offers the best signal routing

Graphics Features

- SMRS cycle.
  - -. Load mask register
  - -. Load color register
- Write Per Bit(Old Mask)
- Block Write(8 Columns)

GENERAL DESCRIPTION

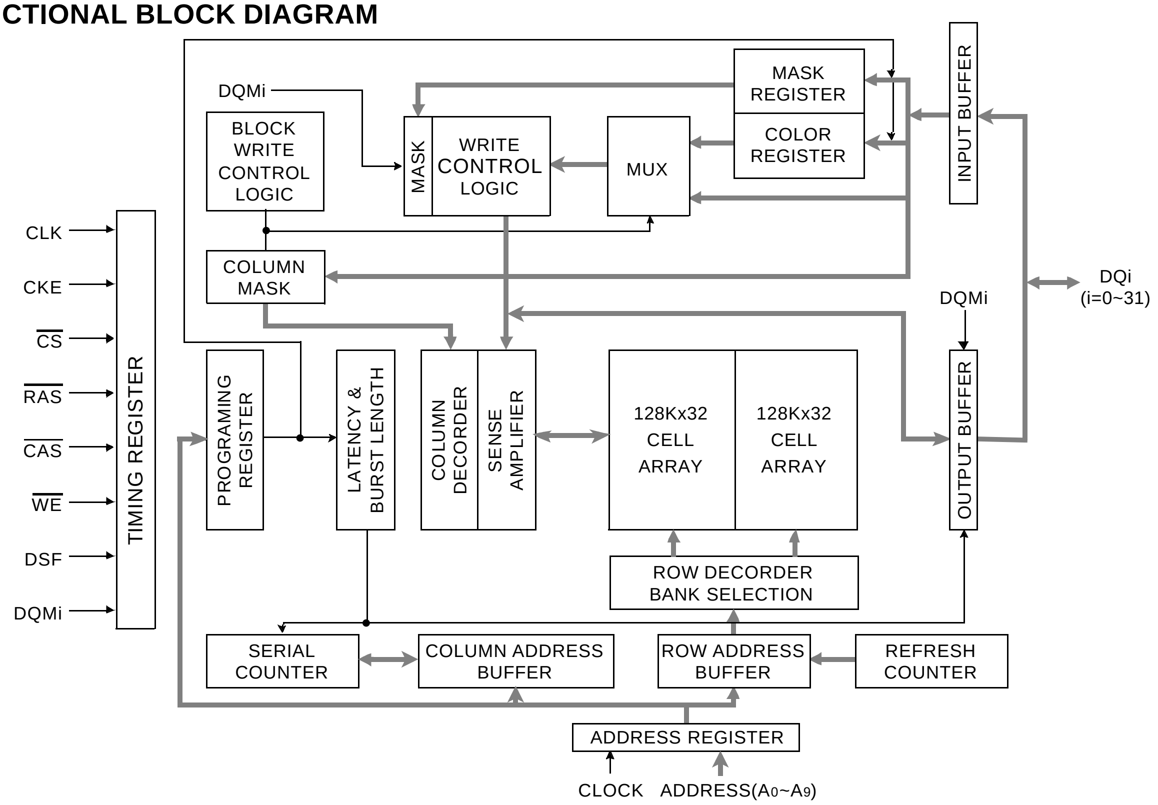
The KM4132G271B is 8,388,608 bits synchronous high data rate Dynamic RAM organized as 2 x 131,072 words by 32 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length, and programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.
Write per bit and 8 columns block write improves performance in graphics systems.

ORDERING INFORMATION

Part NO.	Max Freq.	Interface	Package
KM4132G271BQ(R)-7	143MHz	LVTTL	100 PQFP
KM4132G271BQ(R)-8	125MHz		
KM4132G271BQ(R)-10	100MHz		
KM4132G271BTQ(R)-7	143MHz	LVTTL	100 TQFP
KM4132G271BTQ(R)-8	125MHz		
KM4132G271BTQ(R)-10	100MHz		

* ~G271BQR# / ~G271BTQR# : Reverse Type Package

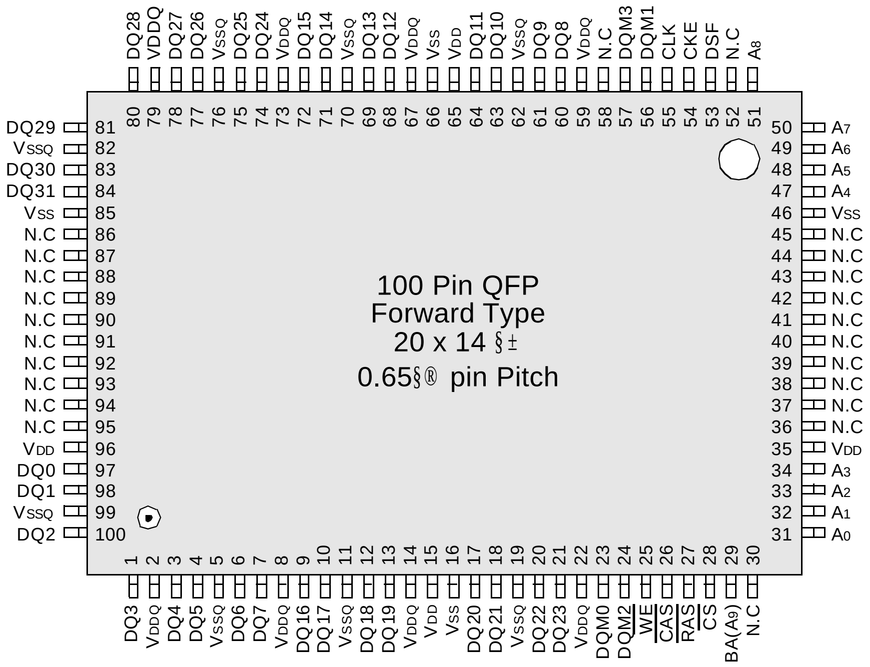
FUNCTIONAL BLOCK DIAGRAM



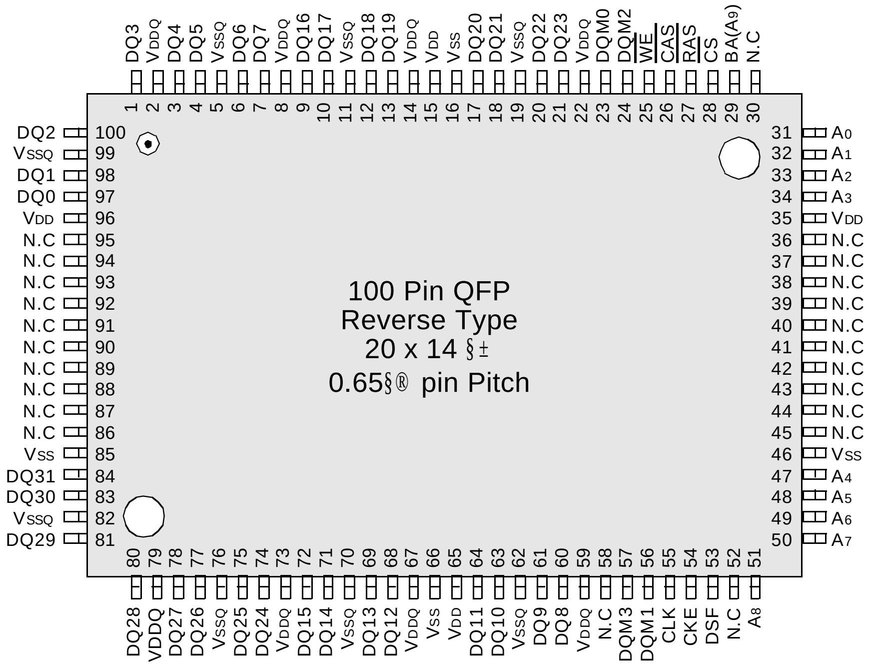
Downloaded from Elcodis.com electronic components distributor

PIN CONFIGURATION (TOP VIEW)

Forward Type



Reverse Type



Downloaded from Elcodis.com electronic components distributor

PIN CONFIGURATION DESCRIPTION

PIN	NAME	INPUT FUNCTION
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQMi
CKE	Clock *Enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one clock $+t_{SS}$ prior to new command. Disable input buffers for power down in standby.
A_0 ~ A_8	*Address*	Row / Column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_8, Column address : CA_0 ~ CA_7
A_9(BA)	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and Row precharge.
DQMi	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active.(Byte Masking)
DQi	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
DSF	*Define Special Function*	Enables write per bit, block write and special mode register set.
V_{DD}/V_{SS}	*Power Supply /Ground*	Power Supply : +3.3V±0.3V/Ground
V_{DDQ}/V_{SSQ}	*Data Output Power /Ground*	Provide isolated Power/Ground to DQs for improved noise immunity.
N.C	*No Connection*	

Downloaded from Elcodis.com electronic components distributor

ABSOLUTE MAXIMUM RATINGS (Voltage referenced to V_{SS})

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	
Input low voltage	V_{IL}	-0.3	0	0.8	V	Note 1
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-5	-	5	uA	Note 2
Output leakage current	I_{OL}	-5	-	5	uA	Note 3
Output Loading Condition	see figure 1					

Note : 1. V_{IL} (min) = -1.5V AC(pulse width ≤ 5ns).
2. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V.
3. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DD}.

CAPACITANCE (${V_{DD}}/{V_{DDQ}}$ = 3.3V, T_A = 25°C, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_9)	C_{IN1}	-	4	pF
Input capacitance (CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DSF & DQM)	C_{IN2}	-	4	pF
Data input/output capacitance (DQ_0 ~ DQ_{31})	C_{OUT}	-	5	pF

DECOUPLING CAPACITANCE GUIDE LINE

Recommended decoupling capacitance added to power line at board.

Parameter	Symbol	Value	Unit
Decoupling Capacitance between V_{DD} and V_{SS}	C_{DC1}	0.1 + 0.01	uF
Decoupling Capacitance between V_{DDQ} and V_{SSQ}	C_{DC2}	0.1 + 0.01	uF

Note : 1. V_{DD} and V_{DDQ} pins are separated each other.
All V_{DD} pins are connected in chip. All V_{DDQ} pins are connected in chip.
2. V_{SS} and V_{SSQ} pins are separated each other
All V_{SS} pins are connected in chip. All V_{SSQ} pins are connected in chip.

Downloaded from Elcodis.com electronic components distributor

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C $V_{IH(min)}$ /$V_{IL(max)}$ =2.0V/0.8V)

Parameter	Symbol	Test Condition	CAS Latency	Speed			Unit	Note
				-7	-8	-10		
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min), $t_{CC} \geq t_{CC}$(min), I_{OL} = 0 mA		180	160	150	mA	1
Precharge Standby Current in power-down mode	I_{CC2}P	CKE $\leq V_{IL}$(max), t_{CC} = 15ns		2			mA	
	I_{CC2}PS	CKE $\leq V_{IL}$(max), CLK $\leq V_{IL}$(max), $t_{CC} = \infty$		2				
Precharge Standby Current in non power-down mode	I_{CC2}N	CKE $\geq V_{IH}$(min), $\overline{CS} \geq V_{IH}$(min), t_{CC} = 15ns Input signals are changed one time during 30ns		35			mA	
	I_{CC2}NS	CKE $\geq V_{IH}$(min), CLK $\leq V_{IL}$(max), $t_{CC} = \infty$ Input signals are stable		15				
Active Standby Current in power-down mode	I_{CC3}P	CKE $\leq V_{IL}$(max), t_{CC} = 15ns		3			mA	
	I_{CC3}PS	CKE $\leq V_{IL}$(max), CLK $\leq V_{IL}$(max), $t_{CC} = \infty$		3				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3}N	CKE $\geq V_{IH}$(min), $\overline{CS} \geq V_{IH}$(min), t_{CC} = 15ns Input signals are changed one time during 30ns		50			mA	
	I_{CC3}NS	CKE $\geq V_{IH}$(min), CLK $\leq V_{IL}$(max), $t_{CC} = \infty$ Input signals are stable		25				
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA, Page Burst All bank Activated, t_{CCD} = t_{CCD}(min)	3	300	280	210	mA	1
			2	180	180	160		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		90	90	90	mA	2
Self Refresh Current	I_{CC6}	CKE $\leq$ 0.2V		2			mA	
Operating Current (One Bank Block Write)	I_{CC7}	$t_{CC} \geq t_{CC}$(min), I_{OL}=0mA, t_{BWC}(min)		210	190	150	mA	

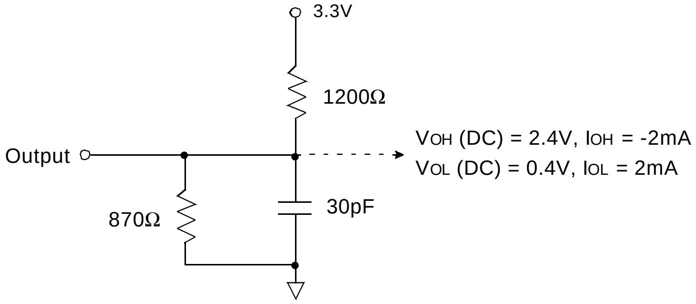
Note : 1. Measured with outputs open. Addresses are changed only one time during tcc(min).

2. Refresh period is 32ms. Addresses are changed only one time during tcc(min).

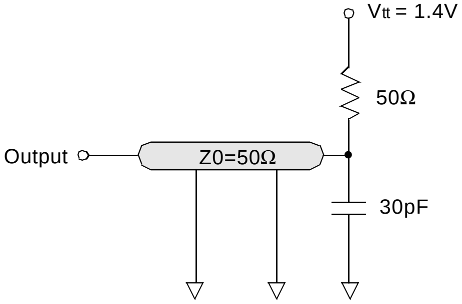
Downloaded from Elcodis.com electronic components distributor

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70°C)

Parameter	Value
AC input levels	V_{ih}/V_{il} = 2.4V / 0.4V
Input timing measurement reference level	1.4V
Input rise and fall time(See note 3)	t_R/t_F=1ns/ 1ns
Output timing measurement reference level	1.4V
Output load condition	See Fig. 2



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-7		-8		-10		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS Latency=3	t_{CC}	7	1000	8	1000	10	1000	ns	1
	CAS Latency=2		12		12		13			
CLK to valid output delay	CAS Latency=3	t_{SAC}	-	6	-	6.5	-	7	ns	1, 2
	CAS Latency=2		-	8	-	8	-	9		
Output data hold time		t_{OH}	2.5		2.5		2.5		ns	2
CLK high pulse width		t_{CH}	2.5		3		3.5		ns	3
CLK low pulse width		t_{CL}	2.5		3		3.5		ns	3
Input setup time		t_{SS}	2		2.5		2.5		ns	3
Input hold time		t_{SH}	1		1		1		ns	3
CLK to output in Low-Z		t_{SLZ}	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}	-	6	-	6.5	-	7	ns	
	CAS latency=2		-	8	-	8	-	9		

* All AC parameters are measured from half to half.

Note : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)=1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

Downloaded from Elcodis.com electronic components distributor

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version			Unit	Note
		-7	-8	-10		
Row active to row active delay	$t_{RRD(min)}$	14	16	20	ns	1
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay	$t_{RCD(min)}$	16	16	20	ns	1
Row precharge time	$t_{RP(min)}$	21	20	20	ns	1
Row active time	$t_{RAS(min)}$	49	48	50	ns	1
	$t_{RAS(max)}$	100			us	
Row cycle time	$t_{RC(min)}$	70	70	70	ns	1
Last data in to new col. address delay	$t_{CDL(min)}$	1			CLK	2
Last data in to row precharge	$t_{RDL(min)}$	1			CLK	2
Last data in to burst stop	$t_{BDL(min)}$	1			CLK	2
Col. address to col. address delay	$t_{CCD(min)}$	1			CLK	3
Block write data-in to PRE command delay	$t_{BPL(min)}$	1			CLK	
Block write cycle time	$t_{BWC(min)}$	1			CLK	1, 3
Number of valid output data	CAS latency=3	2			CLK	4
	CAS latency=2	1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. This parameter means minimum $\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ delay at block write cycle only.
4. In case of row precharge interrupt, auto precharge and read burst stop.

Downloaded from Elcodis.com electronic components distributor

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	DQM	A_9	A_8	A_7~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	L	X	OP CODE			1, 2
	Special Mode Register Set								H					1,2,7
Refresh	Auto Refresh		H	H	L	L	L	H	L	X	X			3
	Self Refresh	Entry		L										3
		Exit	L	H	L	H	H	H	X	X	X			3
					H	X	X	X						3
Bank Active & Row Addr.	Write Per Bit Disable		H	X	L	L	H	H	L	X	V	Row Address		4, 5
	Write Per Bit Enable								H					4,5,9
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	L	X	V	L	Column Address	4
	Auto Precharge Enable											H		4, 6
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	L	X	V	L	Column Address	4, 5
	Auto Precharge Enable											H		4,5,6,9
Block Write & Column Addr.	Auto Precharge Disable		H	X	L	H	L	L	H	X	V	L	Column Address	4, 5
	Auto Precharge Enable											H		4,5,6,9
Burst Stop			H	X	L	H	H	L	L	X	X			7
Precharge	Bank Selection		H	X	L	L	H	L	L	X	V	L	X	
	Both Banks										X	H		
Clock Suspend or Active Power Down		Entry	H	L	L	H	H	H	X	X	X			
					H	X	X	X						
		Exit	L	H	X	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	L	H	H	H	X	X	X			
					H	X	X	X						
		Exit	L	H	L	V	V	V	V	X				
					H	X	X	X	X					
DQM			H	X						V	X			8
No Operation Command			H	X	L	H	H	H	X	X	X			
					H	X	X	X						

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_9 : Program keys. (@MRS)
A_5, A_6 : LMR or LCR select. (@SMRS)
Color register exists only one per DQi which both banks share.
So dose Mask Register.
Color or mask is loaded into chip through DQ pin.
2. MRS can be issued only at both banks precharge state.
SMRS can be issued only if DQ's are idle.
A new command can be issued at the next clock of MRS/SMRS.

Downloaded from Elcodis.com electronic components distributor

SIMPLIFIED TRUTH TABLE

3. Auto refresh functions as same as CBR refresh of DRAM.
   The automatical precharge without Row precharge command is meant by "Auto".
   Auto/Self refresh can be issued only at both precharge state.
4. A_9 : Bank select address.
   If "Low" at read, (block) write, Row active and precharge, bank A is selected.
   If "High" at read, (block) write, Row active and precharge, bank B is selected.
   If A_8 is "High" at Row precharge, A_9 is ignored and both banks are selected.
5. It is determined at Row active cycle.
   whether Normal/Block write operates in write per bit mode or not.
   For A bank write, at A bank Row active, for B bank write, at B bank Row active.
   Terminology : Write per bit =I/O mask
   (Block) Write with write per bit mode=Masked(Block) Write
6. During burst read or write with auto precharge, new read/(block) write command cannot be issued.
   Another bank read/(block) write command can be issued at t_{RP} after the end of burst.
7. Burst stop command is valid only at full page burst length.
8. DQM sampled at positive going edge of a CLK.
   masks the data-in at the very CLK(Write DQM latency is 0)
   but makes Hi-Z state the data-out of 2 CLK cycles after.(Read DQM latency is 2)
9. Graphic features added to SDRAM's original features.
   If DSF is tied to low, graphic functions are disabled and chip operates as a 8M SDRAM with 32 DQ's.

SGRAM vs SDRAM

Function	**MRS**		**Bank Active**		**Write**	
DSF	L	H	L	H	L	H
SGRAM Function	MRS	SMRS	Bank Active with Write per bit Disable	Bank Active with Write per bit Enable	Normal Write	Block Write

If DSF is low, SGRAM functionality is identical to SDRAM functionality .

SGRAM can be used as an unified memory by the appropriate DSF control
--> SGRAM=Graphic Memory + Main Memory

Downloaded from Elcodis.com electronic components distributor

MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with MRS

Address	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
Function	W.B.L	TM		CAS Latency			BT	Burst Length		

(Note 1)

Test Mode		
A_8	A_7	**Type**
0	0	Mode Register Set
0	1	Vendor Use Only
1	0	
1	1	

Write Burst Length	
A_9	Length
0	Burst
1	Single Bit

CAS Latency			
A_6	A_5	A_4	**Latency**
0	0	0	Reserved
0	0	1	-
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Type	
A_3	**Type**
0	Sequential
1	Interleave

Burst Length				
A_2	A_1	A_0	**BT=0**	**BT=1**
0	0	0	1	Reserved
0	0	1	2	Reserved
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	256(Full)	Reserved

(Note 2)

Special Mode Register Programmed with SMRS

Address	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
Function	X			LC	LM	X				

Load Color		**Load Mask**	
A_6	Function	A_5	Function
0	Disable	0	Disable
1	Enable	1	Enable

(Note 3)

POWER UP SEQUENCE

1. Apply power and start clock, Attempt to maintain CKE= "H", DQM= "H" and the other pins are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

cf.) Sequence of 4 & 5 may be changed.

The device is now ready for normal operation.

Note : 1. If A_9 is high during MRS cycle, "Burst Read Single Bit Write" function will be enabled.
2. The full column burst(256bit) is available only at Sequential mode of burst type.
3. If LC and LM both high(1), data of mask and color register will be unknown.

Downloaded from Elcodis.com electronic components distributor

BURST SEQUENCE (BURST LENGTH = 4)

Initial address		Sequential				Interleave			
A_1	A_0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

BURST SEQUENCE (BURST LENGTH = 8)

Initial address			Sequential								Interleave							
A_2	A_1	A_0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

PIXEL to DQ MAPPING(at BLOCK WRITE)

Column address			3 Byte	2 Byte	1 Byte	0 Byte
A_2	A_1	A_0	I/O$_{31}$ - I/O$_{24}$	I/O$_{23}$ - I/O$_{16}$	I/O$_{15}$ - I/O$_{8}$	I/O$_{7}$ - I/O$_{0}$
0	0	0	DQ$_{24}$	DQ$_{16}$	DQ$_{8}$	DQ$_{0}$
0	0	1	DQ$_{25}$	DQ$_{17}$	DQ$_{9}$	DQ$_{1}$
0	1	0	DQ$_{26}$	DQ$_{18}$	DQ$_{10}$	DQ$_{2}$
0	1	1	DQ$_{27}$	DQ$_{19}$	DQ$_{11}$	DQ$_{3}$
1	0	0	DQ$_{28}$	DQ$_{20}$	DQ$_{12}$	DQ$_{4}$
1	0	1	DQ$_{29}$	DQ$_{21}$	DQ$_{13}$	DQ$_{5}$
1	1	0	DQ$_{30}$	DQ$_{22}$	DQ$_{14}$	DQ$_{6}$
1	1	1	DQ$_{31}$	DQ$_{23}$	DQ$_{15}$	DQ$_{7}$

Downloaded from Elcodis.com electronic components distributor

DEVICE OPERATIONS

CLOCK (CLK)

The clock input is used as the reference for all SGRAM operations. All operations are synchronized to the positive going edge of the clock. The clock transitions must be monotonic between V_{IL} and V_{IH}. During operation with CKE high all inputs are assumed to be in a valid state (low or high) for the duration of set-up and hold time around positive edge of the clock for proper functionality and I_{CC} specifications.

CLOCK ENABLE (CKE)

The clock enable(CKE) gates the clock onto SGRAM. If CKE goes low synchronously with clock (set-up and hold time are the same as other inputs), the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. All other inputs are ignored from the next clock cycle after CKE goes low. When both banks are in the idle state and CKE goes low synchronously with clock, the SGRAM enters the power down mode from the next clock cycle. The SGRAM remains in the power down mode ignoring the other inputs as long as CKE remains low. The power down exit is synchronous as the internal clock is suspended. When CKE goes high at least "t_{SS} + 1_{CLOCK}" before the high going edge of the clock, then the SGRAM becomes active from the same clock edge accepting all the input commands.

BANK SELECT (A_9)

This SGRAM is organized as two independent banks of 131,072 words x 32 bits memory arrays. The A_9 inputs is latched at the time of assertion of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ to select the bank to be used for the operation. When A_9 is asserted low, bank A is selected. When A_9 is asserted high, bank B is selected. The bank select A_9 is latched at bank activate, read, write mode register set and precharge operations.

ADDRESS INPUT (A_0 ~ A_8)

The 17 address bits required to decode the 131,072 word locations are multiplexed into 9 address input pins(A_0~A_8). The 9 bit row address is latched along with $\overline{\text{RAS}}$ and A_9 during bank activate command. The 8 bit column address is latched along with $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and A_9 during read or write command.

NOP and DEVICE DESELECT

When $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ are high, the SGRAM performs no operation (NOP). NOP does not initiate any new operation, but is needed to complete operations which require more than single clock cycle like bank activate, burst read, auto refresh, etc. The device deselect is also a NOP and is entered by asserting $\overline{\text{CS}}$ high. $\overline{\text{CS}}$ high disables the command decoder so that $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, DSF and all the address inputs are ignored.

POWER-UP

The following sequence is recommended for POWER UP

1. Power must be applied to either CKE and DQM inputs to pull them high and other pins are NOP condition at the inputs before or along with V_{DD}(and V_{DDQ}) supply.
   The clock signal must also be asserted at the same time.
2. After V_{DD} reaches the desired voltage, a minimum pause of 200 microseconds is required with inputs in NOP condition.
3. Both banks must be precharged now.
4. Perform a minimum of 2 Auto refresh cycles to stabilize the internal circuitry.
5. Perform a MODE REGISTER SET cycle to program the CAS latency, burst length and burst type as the default value of mode register is undefined.
   At the end of one clock cycle from the mode register set cycle, the device is ready for operation.
   When the above sequence is used for Power-up, all the outputs will be in high impedance state. The high impedance of outputs is not guaranteed in any other power-up sequence.
   cf.) Sequence of 4 & 5 may be changed.

MODE REGISTER SET (MRS)

The mode register stores the data for controlling the various operating modes of SGRAM. It programs the CAS latency, addressing mode, burst length, test mode and various vendor specific options to make SGRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the SGRAM. The mode register is written by asserting low on $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and DSF (The SGRAM should be in active mode with CKE already high prior to writing the mode register). The state of address pins A_0 ~ A_8 and A_9 in the same cycle as $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and DSF going low is the data written in the mode register. One clock cycle is required to complete the write in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as both banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length field uses A_0 ~ A_2, burst type uses A_3, addressing mode uses A_4 ~ A_6, A_7 ~ A_8 are used for vendor specific options or test mode. And the write burst length is programmed using A_9. A_7 ~ A_8 must be set to low for normal SGRAM operation. Refer to table for specific codes for various burst length, addressing modes and CAS latencies.

Downloaded from Elcodis.com electronic components distributor

DEVICE OPERATIONS

BANK ACTIVATE

The bank activate command is used to select a random row in an idle bank. By asserting low on $\overline{RAS}$ and $\overline{CS}$ with desired row and bank addresses, a row access is initiated. The read or write operation can occur after a time delay of t_{RCD}(min) from the time of bank activation. t_{RCD}(min) is an internal timing parameter of SGRAM, therefore it is dependent on operating clock frequency. The minimum number of clock cycles required between bank activate and read or write command should be calculated by dividing t_{RCD}(min) with cycle time of the clock and then rounding off the result to the next higher integer. The SGRAM has two internal banks on the same chip and shares part of the internal circuitry to reduce chip area, therefore it restricts the activation of both banks immediately. Also the noise generated during sensing of each bank of SGRAM is high requiring some time for power supplies to recover before the other bank can be sensed reliably. t_{RRD}(min) specifies the minimum time required between activating different banks. The number of clock cycles required between different bank activation must be calculated similar to t_{RCD} specification. The minimum time required for the bank to be active to initiate sensing and restoring the complete row of dynamic cells is determined by t_{RAS}(min) specification before a precharge command to that active bank can be asserted. The maximum time any bank can be in the active state is determined by t_{RAS}(max). The number of cycles for both t_{RAS}(min) and t_{RAS}(max) can be calculated similar to t_{RCD} specification.

BURST READ

The burst read command is used to access burst of data on consecutive clock cycles from an active row in an active bank. The burst read command is issued by asserting low on $\overline{CS}$ and $\overline{CAS}$ with $\overline{WE}$ being high on the positive edge of the clock. The bank must be active for at least t_{RCD}(min) before the burst read command is issued. The first output appears CAS latency number of clock cycles after the issue of burst read command. The burst length, burst sequence and latency from the burst read command is determined by the mode register which is already programmed. The burst read can be initiated on any column address of the active row. The address wraps around if the initial address does not start from a boundary such that number of outputs from each I/O are equal to the burst length programmed in the mode register. The output goes into high-impedance at the end of the burst, unless a new burst read was initiated to keep the data output gapless. The burst read can be terminated by issuing another burst read or burst write in the same bank or the other active bank or a precharge command to the same bank. The burst stop command is valid only at full page burst length where the output does not go into high impedance at the end of burst and the burst is wrapped around..

BURST WRITE

The burst write command is similar to burst read command, and is used to write data into the SGRAM on consecutive clock cycles in adjacent addresses depending on burst length and burst sequence. By asserting low on $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ with valid column address, a write burst is initiated. The data inputs are provided for the initial address in the same clock cycle as the burst write command. The input buffer is deselected at the end of the burst length, even though the internal writing may not have been completed yet. The writing can not complete to burst length. The burst write can be terminated by issuing a burst read and DQM for blocking data inputs or burst write in the same or the other active bank. The burst stop command is valid only at full page burst length where the writing continues at the end of burst and the burst is wrapped around. The write burst can also be terminated by using DQM for blocking data and precharging the bank " t_{RDL} " after the last data input to be written into the active row. See DQM OPERATION also.

DQM OPERATION

The DQM is used to mask input and output operations. It works similar to $\overline{OE}$ during read operation and inhibits writing during write operation. The read latency is two cycles from DQM and zero cycle for write, which means DQM masking occurs two cycles later in the read cycle and occurs in the same cycle during write cycle. DQM operation is synchronous with the clock, therefore the masking occurs for a complete cycle. The DQM signal is important during burst interrupts of write with read or precharge in the SGRAM. Due to asynchronous nature of the internal write, the DQM operation is critical to avoid unwanted or incomplete writes when the complete burst write is not required. DQM is also used for device selection, byte selection and bus control in a memory system. DQM0 controls DQ0 to DQ7, DQM1 controls DQ8 to DQ15, DQM2 controls DQ16 to DQ23, DQM3 controls DQ24 to DQ31. DQM masks the DQ's by a byte regardless that the corresponding DQ's are in a state of WPB masking or Pixel masking. Please refer to DQM timing diagram also.

PRECHARGE

The precharge operation is performed on an active bank by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ and A_8 with valid A_9 of the bank to be precharged. The precharge command can be asserted anytime after t_{RAS}(min) is satisfied from the bank activate command in the desired bank. "t_{RP}" is defined as the minimum time required to precharge a bank. The minimum number of clock cycles required to complete row precharge is calculated by dividing "t_{RP}" with clock cycle time and rounding up to the next higher integer. Care should be taken to make sure that burst write is completed or DQM is used to inhibit writing before precharge command is asserted. The maximum time any bank can be active is specified by t_{RAS}(max). Therefore, each bank has to be precharged within t_{RAS}(max) from the bank activate command. At the end of precharge, the bank enters the idle state and is ready to be activated again.

Downloaded from Elcodis.com electronic components distributor

DEVICE OPERATIONS (Continued)

Entry to Power Down, Auto refresh, Self refresh and Mode register Set etc. is possible only when both banks are in idle state.

AUTO PRECHARGE

The precharge operation can also be performed by using auto precharge. The SGRAM internally generates the timing to satisfy t_{RAS}(min) and "t_{RP}" for the programmed burst length and CAS latency. The auto precharge command is issued at the same time as burst read or burst write by asserting high on A_8. If burst read or burst write command is issued with low on A_8, the bank is left active until a new command is asserted. Once auto precharge command is given, no new commands are possible to that particular bank until the bank achieves idle state.

BOTH BANKS PRECHARGE

Both banks can be precharged at the same time by using Precharge all command. Asserting low on $\overline{CS}$, $\overline{RAS}$, and $\overline{WE}$ with high on A_8 after both banks have satisfied t_{RAS}(min) requirement, performs precharge on both banks. At the end of t_{RP} after performing precharge all, both banks are in idle state.

AUTO REFRESH

The storage cells of SGRAM need to be refreshed every 16ms to maintain data. An auto refresh cycle accomplishes refresh of a single row of storage cells. The internal counter increments automatically on every auto refresh cycle to refresh all the rows. An auto refresh command is issued by asserting low on $\overline{CS}$,$\overline{RAS}$ and $\overline{CAS}$ with high on CKE and $\overline{WE}$. The auto refresh command can only be asserted with both banks being in idle state and the device is not in power down mode (CKE is high in the previous cycle). The time required to complete the auto refresh operation is specified by "t_{RC}(min)". The minimum number of clock cycles required can be calculated by driving "t_{RC}" with clock cycle time and them rounding up to the next higher integer. The auto refresh command must be followed by NOP's until the auto refresh operation is completed. Both banks will be in the idle state at the end of auto refresh operation. The auto refresh is the preferred refresh mode when the SGRAM is being used for normal data transactions. The auto refresh cycle can be performed once in 15.6us or a burst of 1024 auto refresh cycles once in 16ms.

SELF REFRESH

The self refresh is another refresh mode available in the SGRAM. The self refresh is the preferred refresh mode for data retention and low power operation of SGRAM. In self refresh mode, the SGRAM disables the internal clock and all the input buffers except CKE. The refresh addressing and timing are internally generated to reduce power consumption.

The self refresh mode is entered from all banks idle state by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE with high on $\overline{WE}$. Once the self refresh mode is entered, only CKE state being low matters, all the other inputs including the clock are ignored in order to remain in the self refresh mode.

The self refresh is exited by restarting the external clock and then asserting high on CKE. This must be followed by NOP's for a minimum time of "t_{RC}" before the SGRAM reaches idle state to begin normal operation. If the system uses burst auto refresh during normal operation, it is recommended to use burst 1024 auto refresh cycles immediately after exiting self refresh.

DEFINE SPECIAL FUNCTION(DSF)

The DSF controls the graphic applications of SGRAM. If DSF is tied to low, SGRAM functions as 128K x 32 x2 Bank SDRAM. SGRAM can be used as an unified memory by the appropriate DSF command. All the graphic function modes can be entered only by setting DSF high when issuing commands which otherwise would be normal SDRAM commands. SDRAM functions such as $\overline{RAS}$ Active, Write, and WCBR change to SGRAM functions such as $\overline{RAS}$ Active with WPB, Block Write and SWCBR respectively. See the section below for the graphic functions that DSF controls.

SPECIAL MODE REGISTER SET(SMRS)

There are two kinds of special mode registers in SGRAM.One is color register and the other is mask register. Those usage will be explained in the "WRITE PER BIT" and "BLOCK WRITE" sections. When A_5 and DSF goes high in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low, Load Mask Register(LMR) process is executed and the mask registers are filled with the masks for associated DQ's through DQ pins. And when A_6 and DSF goes high in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low, Load Color Register(LCR) process is executed and the color register is filled with color data for associated DQ's through the DQ pins. If both A_5 and A_6 are high at SMRS, data of mask and color cycle are required to complete the write in the mask register and the color register at LMR and LCR respectively. A new command can be issued in the next clock of LMR or LCR. SMRS, compared with MRS, can be issued at the active state under the condition that DQ's are idle. As in write operation, SMRS accepts the data needed through DQ pins. Therefore bus contention must be avoided. The more detailed materials can be obtained by referring corresponding timing diagram.

Downloaded from Elcodis.com electronic components distributor

DEVICE OPERATIONS (Continued)

WRITE PER BIT

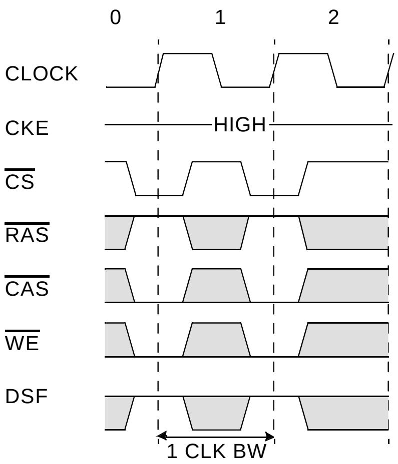
Write per bit(i.e. I/O mask mode) for SGRAM is a function that selectively masks bits of data being written to the devices. The mask is stored in an internal register and applied to each bit of data written when the mask is enabled. Bank active command with DSF=High enables write per bit for associated bank. Bank active command with DSF=Low disables write per bit for the associated bank. The mask used for write per bit operations is stored in the mask register accessed by SWCBR(Special Mode Register Set Command). When a mask bit=1, the associated data bit is written when a write command is executed and write per bit has been enabled for the bank being written. When a mask bit=0, the associated data bit is unaltered when a write command is executed and the write per bit has been enabled for the bank being written. No additional timing conditions are required for write per bit operations. Write per bit writes can be either single write, burst writes or block writes. DQM masking is the same for write per bit and non-WPB write.

BLOCK WRITE

Block write is a feature allowing the simultaneous writing of consecutive 8 columns of data within a RAM device during a single access cycle. During block write the data to be written comes from an internal "color" register and DQ I/O pins are used for independent column selection. The block of column to be written is aligned on 8 column boundaries and is defined by the column address with the 3 LSB′s ignored. Write command with DSF=1 enables block write for the associated bank. A write command with DSF=0 enables normal write for the associated bank. The block width is 8 column where column="n" bits for by "n" part. The color register is the same width as the data port of the chip.It is written via a SWCBR where data present on the DQ pin is to be coupled into the internal color register. The color register provides the data masked by the DQ column select, WPB mask(If enabled), and DQM byte mask. Column data masking(Pixel masking) is provided on an individual column basis for each byte of data. The column mask is driven on the DQ pins during a block write command. The DQ column mask function is segmented on a per bit basis(i.e. DQ[0:7] provides the column mask for data bits[0:7], DQ[8:15] provides the column mask for data bits[8:15], DQ0 masks column[0] for data bits[0:7], DQ9 masks column [1] for data bits [8:15], etc). Block writes are always non-burst, independent of the burst length that has been programmed into the mode register. Back to back block writes are allowed provided that the specified block write cycle time(t_{BWC}) is satisfied. If write per bit was enabled by the bank active command with DSF=1, then write per bit masking of the color register data is enabled.

If write per bit was disabled by a bank active command with DSF=0, the write per bit masking of the color register data is disabled. DQM masking provides independent data byte masking during block write exactly the same as it does during normal write operations, except that the control is extended to the consecutive 8 columns of the block write.

Timing Diagram to Illustrate t_{BWC}



Downloaded from Elcodis.com electronic components distributor

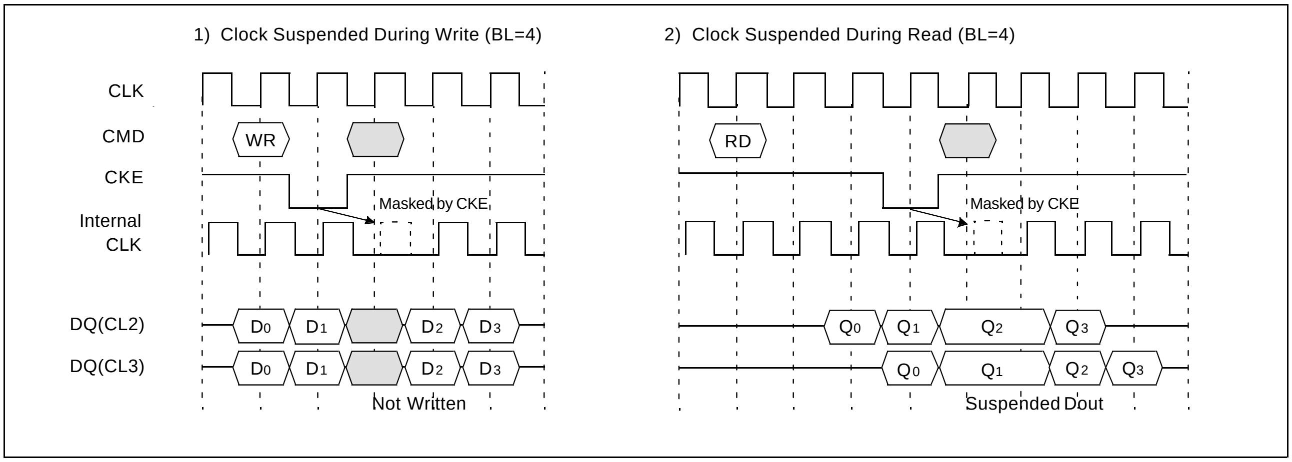
SUMMARY OF 1M Byte SGRAM BASIC FEATURES AND BENEFITS

Features	128K x 32 x 2 SGRAM	Benefits
Interface	Synchronous	Better interaction between memory and system without wait-state of asynchronous DRAM. High speed vertical and horizontal drawing. High operating frequency allows performance gain for SCROLL, FILL, and BitBLT.
Bank	2 ea	Pseudo-infinite row length by on-chip interleaving operation. Hidden row activation and precharge.
Page Depth / 1 Row	256 bit	High speed vertical and horizontal drawing.
Total Page Depth	1024 bytes	High speed vertical and horizontal drawing.
Burst Length(Read)	1, 2, 4, 8 Full Page	Programmable burst of 1, 2, ,4, 8 and full page transfer per column addresses.
Burst Length(Write)	1, 2, 4, 8 Full Page	Programmable burst of 1, 2, ,4, 8 and full page transfer per column addresses.
	BRSW	Switch to burst length of 1 at write without MRS.
Burst Type	Sequential & Interleave	Compatible with Intel and Motorola CPU based system.
CAS Latency	2, 3	Programmable CAS latency.
Block Write	8 Columns	High speed FILL, CLEAR, Text with color registers. Maximum 32 byte data transfers(e.g. for 8bpp : 32 pixels) with plane and byte masking functions.
Color Register	1 ea.	A and B bank share.
Mask Register	1 ea.	Write-per-bit capability(bit plane masking). A and B banks share.
Mask function	DQM$_{0-3}$	Byte masking(pixel masking for 8bpp system) for data-out/in
	Write per bit	Each bit of the mask register directly controls a corresponding bit plane.
	Pixel Mask at Block Write	Byte masking(pixel masking for 8bpp system) for color by DQi

Downloaded from Elcodis.com electronic components distributor

BASIC FEATURE AND FUNCTION DESCRIPTIONS

1. CLOCK Suspend

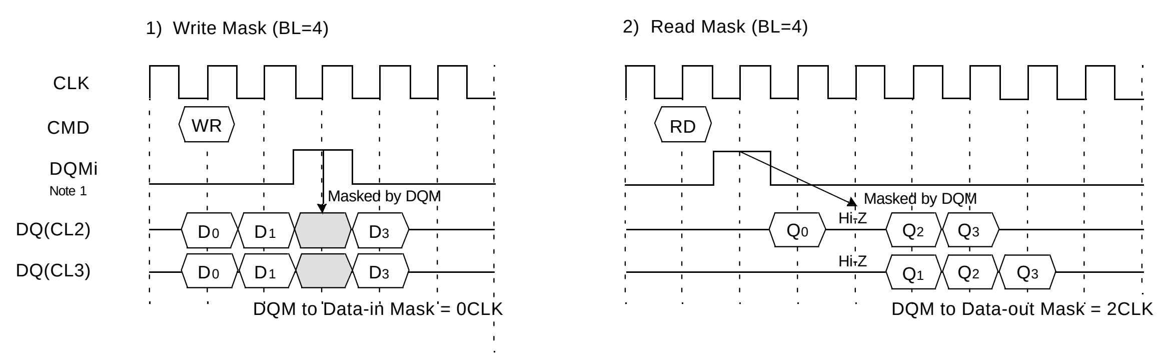


1) Clock Suspended During Write (BL=4)

2) Clock Suspended During Read (BL=4)

Note : CKE to CLK disable/enable=1 clock

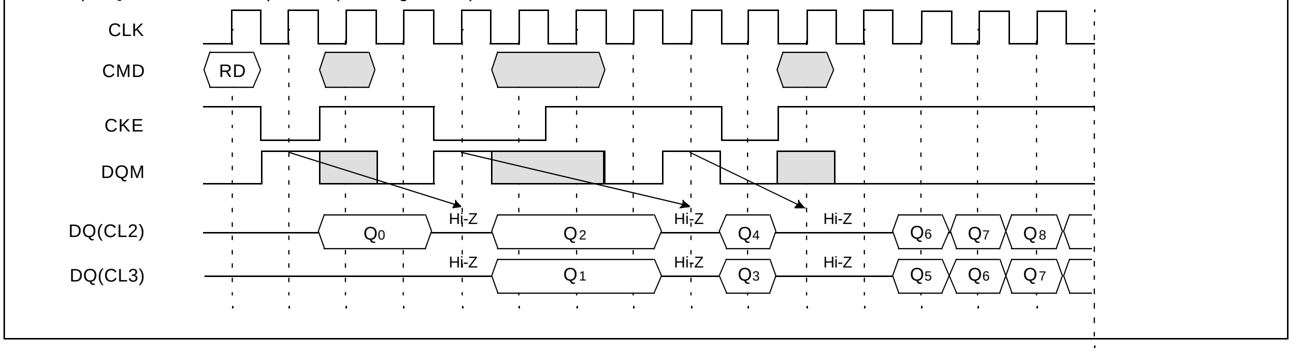
2. DQM Operation



1) Write Mask (BL=4)

2) Read Mask (BL=4)

3) DQM with Clock Suspended (Full Page Read) Note 2

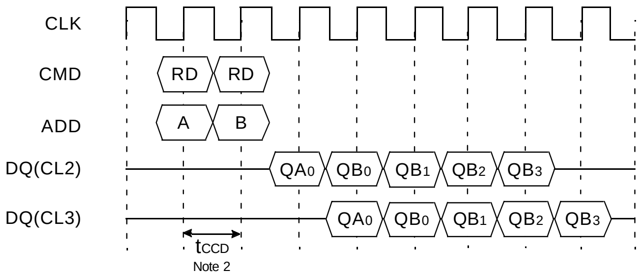


***Note :** 1. There are 4 DQMi(i=0~3).
Each DQMi masks 8 DQi´s.(1 Byte, 1 Pixel for 8 bpp)
2. DQM makes data out Hi-Z after 2 clocks which should masked by CKE " L".

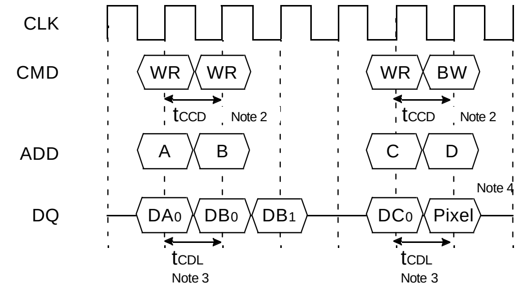
Downloaded from Elcodis.com electronic components distributor

3. $\overline{\text{CAS}}$ Interrupt (I)

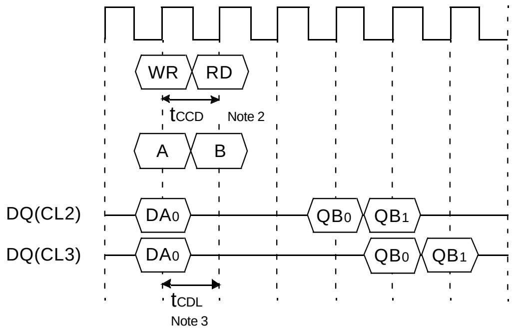
1) Read interrupted by Read (BL=4) Note 1



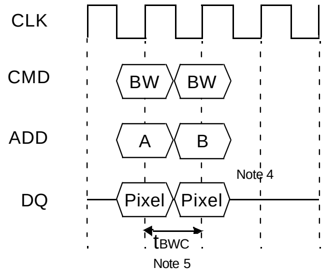
2) Write interrupted by(Block) Write (BL=2)



3) Write interrupted by Read (BL=2)



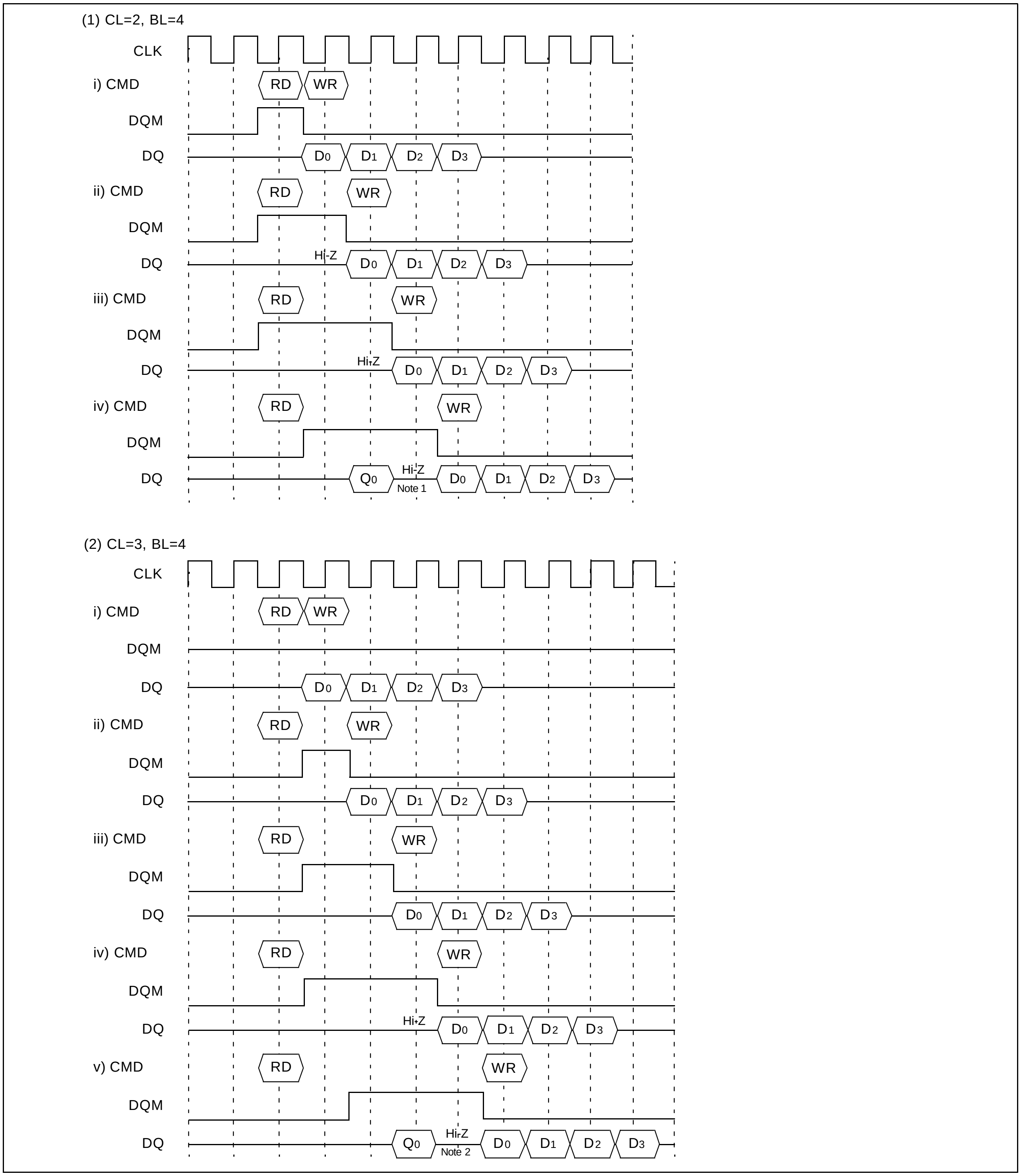
4) Block Write to Block Write



***Note :** 1. By " Interrupt ", It is possible to stop burst read/write by external command before the end of burst.
By "$\overline{\text{CAS}}$ Interrupt" , to stop burst read/write by $\overline{\text{CAS}}$ access ; read, write and block write.
2. t_{CCD} : $\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ delay. (=1CLK)
3. t_{CDL} : Last data in to new column address delay. (=1CLK)
4. Pixel :Pixel mask.
5. t_{BWC} : Block write minimum cycle time.

Downloaded from Elcodis.com electronic components distributor

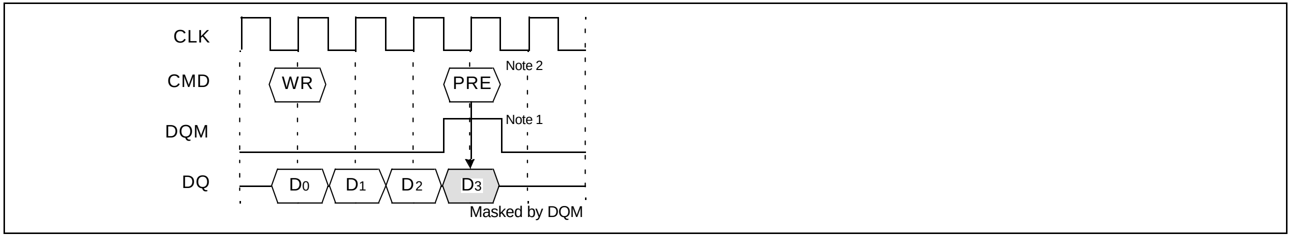
4. $\overline{\text{CAS}}$ Interrupt (II) : Read Interrupted by Write & DQM



***Note :** 1. To prevent bus contention, there should be at least one gap between data in and data out.
2. To prevent bus contention, DQM should be issued which makes at least one gap between data in and data out.

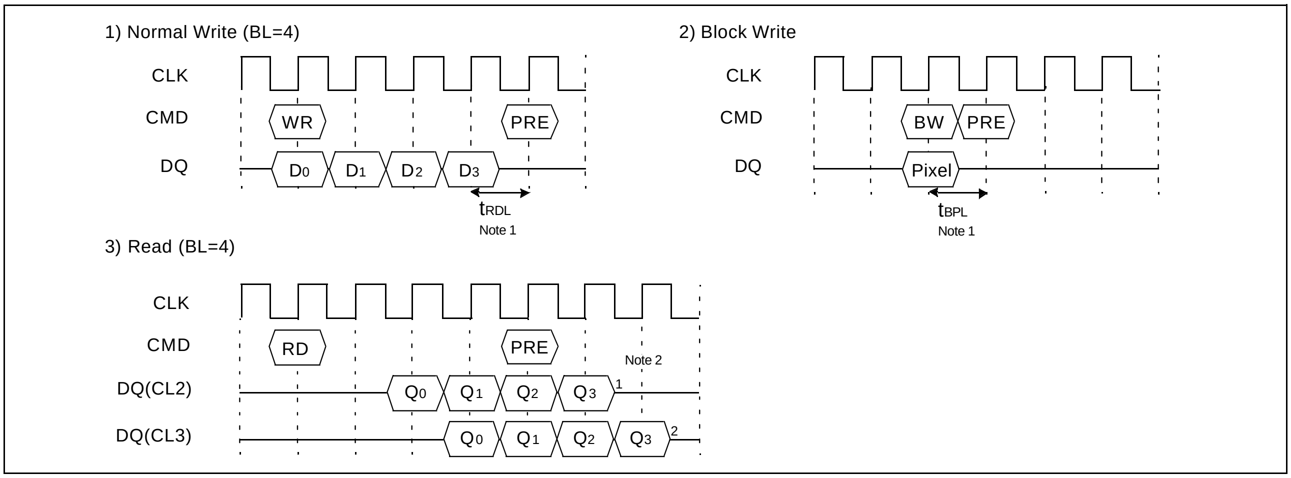
Downloaded from Elcodis.com electronic components distributor

5. Write Interrupted by Precharge & DQM



***Note :** 1. To inhibit invalid write, DQM should be issued.
2. This precharge command and burst write command should be of the same bank, otherwise it is not precharge interrupt but only another bank precharge of dual banks operation.

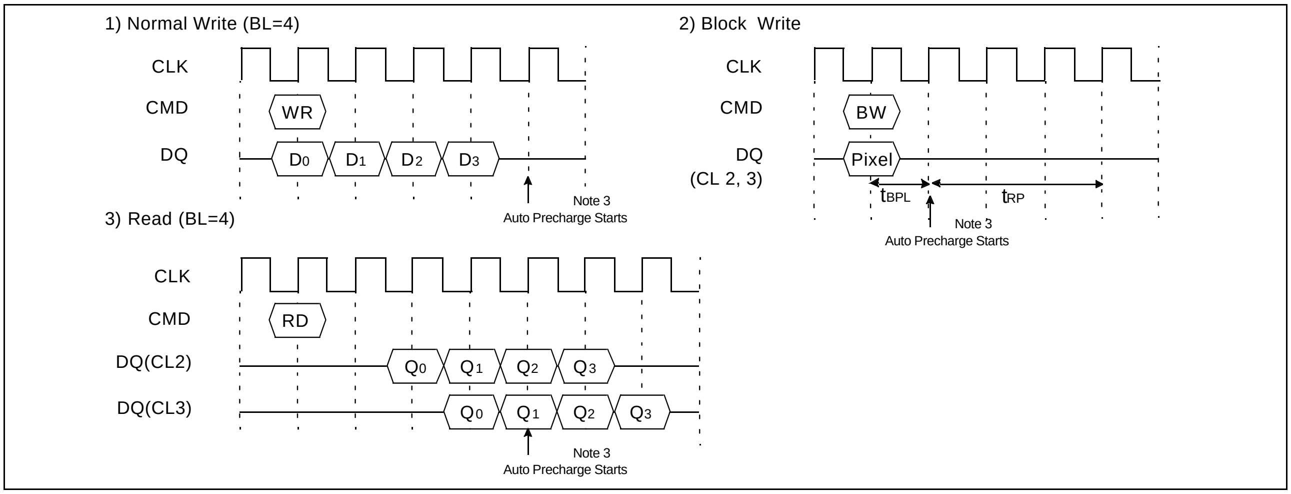
6. Precharge


1) Normal Write (BL=4)

2) Block Write

3) Read (BL=4)

7. Auto Precharge


1) Normal Write (BL=4)

2) Block Write

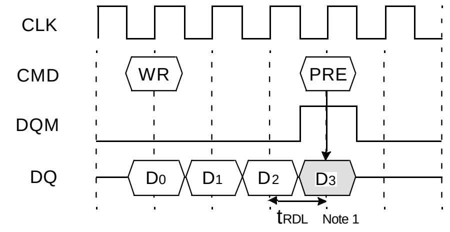
3) Read (BL=4)

***Note :** 1. tBPL : Block write data-in to PRE command delay
2. Number of valid output data after Row Precharge : 1, 2 for CAS Latency =2, 3 respectively.
3. The row active command of the precharge bank can be issued after tRP from this point.
The new read/write command of other activated bank can be issued from this point.
At burst read/write with auto precharge, $\overline{\text{CAS}}$ interrupt of the same/another bank is illegal.

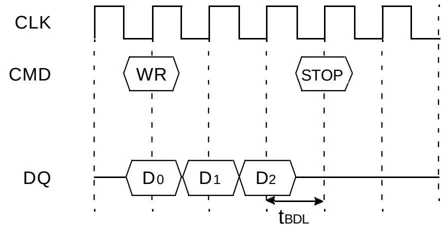
Downloaded from Elcodis.com electronic components distributor

8. Burst Stop & Precharge Interrupt

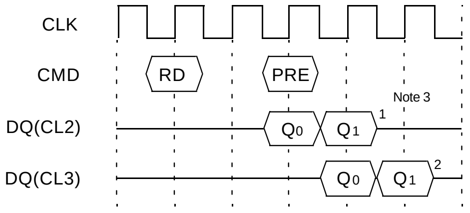
1) Write Interrupted by Precharge (BL=4)



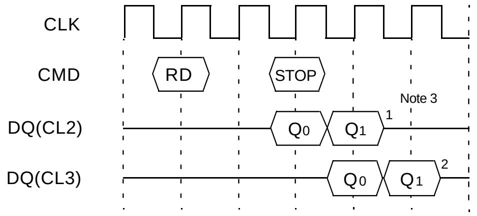
2) Write Burst Stop (Full Page Only)



3) Read Interrupted by Precharge (BL=4)

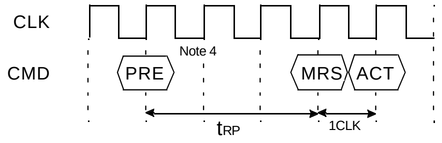


4) Read Burst Stop (Full Page Only)

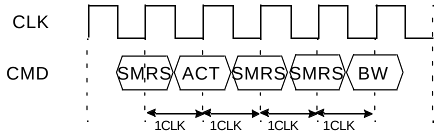


9. MRS & SMRS

1) Mode Register Set



2) Special Mode Register Set



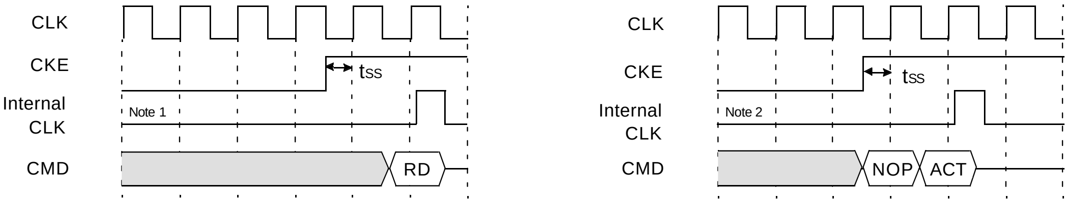
***Note :** 1. t_{RDL} : 1 CLK, Last Data in to Row Precharge.
2. t_{BDL} : 1 CLK, Last Data in to Burst Stop Delay.
3. Number of valid output data after Row precharge or burst stop : 1, 2 for CAS latency= 2, 3 respectiviely.
4. PRE : Both banks precharge if necessary.
MRS can be issued only at all bank precharge state.

Downloaded from Elcodis.com electronic components distributor

10. Clock Suspend Exit & Power Down Exit

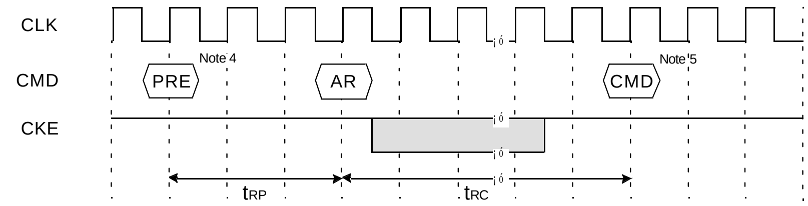
1) Clock Suspend (=Active Power Down) Exit

2) Power Down (=Precharge Power Down) Exit

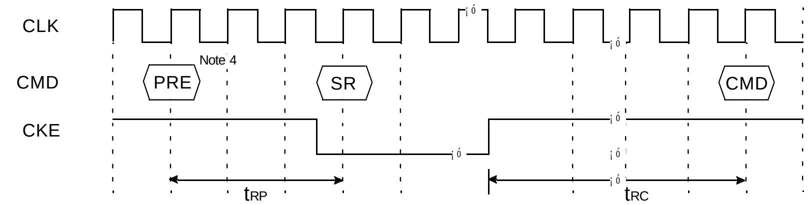


11. Auto Refresh & Self Refresh

1) Auto Refresh[Note 3]



2) Self Refresh[Note 6]



***Note :** 1. Active power down : one or more bank active state.
2. Precharge power down : both bank precharge state.
3. The auto refresh is the same as CBR refresh of conventional DRAM.
No precharge commands are required after Auto Refresh command.
During tRC from auto refresh command, any other command can not be accepted.
4. Before executing auto/self refresh command, both banks must be idle state.
5. (S)MRS, Bank Active, Auto/Self Refresh, Power Down Mode Entry.
6. During self refresh mode, refresh interval and refresh operation are perfomed internally.
After self refresh entry, self refresh mode is kept while CKE is LOW.
During self refresh mode, all inputs expect CKE will be don′t cared, and outputs will be in Hi-Z state.
During tRC from self refresh exit command, any other command can not be accepted.
Before/After self refresh mode, burst auto refresh cycle (1K cycles) is recommended.

Downloaded from Elcodis.com electronic components distributor

12. About Burst Type Control

Basic MODE	Sequential Counting	At MRS A_3 = "0". See the BURST SEQUENCE TABLE. (BL=4,8) BL=1, 2, 4, 8 and full page wrap around.
	Interleave Counting	At MRS A_3 = "1". See the BURST SEQUENCE TABLE. (BL=4,8) BL=4, 8. At BL=1, 2 Interleave Counting = Sequential Counting
Pseudo- MODE	*Pseudo- Decrement Sequential Counting*	At MRS A_3 = "1".(See to Interleave Counting Mode) Starting Address LSB 3 bits $A_{0\text{-}2}$ should be "000" or "111".@BL=8. -- if LSB="000" : Increment Counting. -- if LSB="111" : Decrement Counting. For Example,(Assume Addresses except LSB 3 bits are all 0, BL=8) -- @ write, LSB="000", Accessed Column in order 0-1-2-3-4-5-6-7 -- @ read, LSB="111", Accessed Column in order 7-6-5-4-3-2-1-0 At BL=4, same applications are possible. As above example, at Interleave Counting mode, by confining starting address to some values, *Pseudo*-Decrement Counting Mode can be realized. See the BURST SEQUENCE TABLE carefully.
	Pseudo- Binary Counting	At MRS A_3 = "0".(See to Sequential Counting Mode) $A_{0\text{-}2}$ = "111".(See to Full Page Mode) Using Full Page Mode and Burst Stop Command, Binary Counting Mode can be realized. -- @ Sequential Counting, Accessed Column in order 3-4-5-6-7-1-2-3(BL=8) -- @ *Pseudo*-Binary Counting, Accessed Column in order 3-4-5-6-7-8-9-10(Burst Stop command) Note. The next column address of 256 is 0.
Random MODE	Random column Access t_{CCD} = 1 CLK	Every cycle Read/Write Command with random column address can realize Random Column Access. That is similar to Extended Data Out (EDO) Operation of conventional DRAM.

13. About Burst Length Control

Basic MODE	1	At MRS $A_{2,1,0}$ = "000". At auto precharge, t_{RAS} should not be violated.
	2	At MRS $A_{2,1,0}$ = "001". At auto precharge, t_{RAS} should not be violated.
	4	At MRS $A_{2,1,0}$ = "010".
	8	At MRS $A_{2,1,0}$ = "011".
	Full Page	At MRS $A_{2,1,0}$ = "111". Wrap around mode(Infinite burst length)should be stopped by burst stop, $\overline{\text{RAS}}$ interrupt or $\overline{\text{CAS}}$ interrupt.
Special MODE	BRSW	At MRS A_9 = "1". Read burst =1, 2, 4, 8, full page/write Burst =1 At auto precharge of write, t_{RAS} should not be violated.
	Block Write	8 Column Block Write. LSB A0-2 are ignored. Burst length=1. t_{BWC} should not be violated. At auto precharge, t_{RAS} should not be violated.
Random MODE	Burst Stop	t_{BDL} = 1, Valid DQ after burst stop is 1, 2 for CL=2, 3 respectively Using burst stop command, it is possible only at full page burst length.
Interrupt MODE	$\overline{\text{RAS}}$ Interrupt (Interrupted by Precharge)	Before the end of burst, Row precharge command of the same bank stops read/write burst with Row precharge. t_{RDL} = 1 with DQM, valid DQ after burst stop is 1, 2 for CL= 2, 3 respectively During read/write burst with auto precharge, $\overline{\text{RAS}}$ interrupt cannot be issued.
	$\overline{\text{CAS}}$ Interrupt	Before the end of burst, new read/write stops read/write burst and starts new read/write burst or block write. During read/write burst with auto precharge, $\overline{\text{CAS}}$ interrupt can not be issued.

Downloaded from Elcodis.com electronic components distributor

14. Mask Functions

1) Normal Write

I/O masking : By Mask at Write Per Bit Mode, the selected bit planes keep the original data.

If bit plane 0, 3, 7, 9, 15, 22, 24, and 31 keep the original value.

i) STEP

¨ç SMRS(LMR) :Load mask[31-0]="0111, 1110, 1011, 1111, 0111, 1101, 0111, 0110"

¨è Row Active with DSF "H" :Write Per Bit Mode Enable

¨é Perform Normal Write.

i) ILLUSTRATION

I/O(=DQ)	31 24	23 16	15 8	7 0
External Data-in	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
DQMi	DQM$_3$=0	DQM$_2$=0	DQM$_1$=0	DQM$_0$=1
Mask Register	0 1 1 1 1 1 1 0	1 0 1 1 1 1 1 1	0 1 1 1 1 1 0 1	0 1 1 1 0 1 1 0
Before Write	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1
After Write	0 1 1 1 1 1 1 0	1 0 1 1 1 1 1 1	1 0 0 0 0 0 1 0	1 1 1 1 1 1 1 1

Note 1

2) Block Write

Pixel masking : By Pixel Data issued through DQ pin, the selected pixels keep the original data.

See PIXEL TO DQ MAPPING TABLE.

If Pixel 0, 4, 9, 13, 18, 22, 27 and 31 keep the original white color.

Assume 8bpp,

White = "0000,0000", Red="1010,0011", Green = "1110,0001", Yellow = "0000,1111", Blue = "1100,0011"

i) STEP

¨ç SMRS(LCR) :Load color(for 8bpp, through x32 DQ color0-3 are loaded into color registers)

Load(color3, color2, color1, color0) = (Blue, Green, Yellow, Red)

= "1100,0011, 1110, 0001, 0000, 1111, 1010, 0011"

¨è Row Active with DSF "L" : I/O Mask by Write Per Bit Mode Disable

¨é Block write with DQ[31-0] = "0111, 0111, 1011, 1011, 1101, 1101, 1110, 1110"

i) ILLUSTRATION

I/O(=DQ)		31 24	23 16	15 8	7 0
DQMi		DQM$_3$=0	DQM$_2$=0	DQM$_1$=0	DQM$_0$=1
Color Register		Color3=Blue	Color2=Green	Color1=Yellow	Color0=Red
Before Block Write & DQ (Pixel data)	000	White DQ$_{24}$=H	White DQ$_{16}$=H	White DQ$_8$=H	White DQ$_0$=L
	001	White DQ$_{25}$=H	White DQ$_{17}$=H	White DQ$_9$=L	White DQ$_1$=H
	010	White DQ$_{26}$=H	White DQ$_{18}$=L	White DQ$_{10}$=H	White DQ$_2$=H
	011	White DQ$_{27}$=L	White DQ$_{19}$=H	White DQ$_{11}$=H	White DQ$_3$=H
	100	White DQ$_{28}$=H	White DQ$_{20}$=H	White DQ$_{12}$=H	White DQ$_4$=L
	101	White DQ$_{29}$=H	White DQ$_{21}$=H	White DQ$_{13}$=L	White DQ$_5$=H
	110	White DQ$_{30}$=H	White DQ$_{22}$=L	White DQ$_{14}$=H	White DQ$_6$=H
	111	White DQ$_{31}$=L	White DQ$_{23}$=H	White DQ$_{15}$=H	White DQ$_7$=H
After Block Write	000	Blue	Green	Yellow	White
	001	Blue	Green	White	White
	010	Blue	White	Yellow	White
	011	White	Green	Yellow	White
	100	Blue	Green	Yellow	White
	101	Blue	Green	White	White
	110	Blue	White	Yellow	White
	111	White	Green	Yellow	White

Note 2

***Note :** 1. DQM byte masking.

2. At normal write, ONE column is selected among columns decorded by A$_{2-0}$(000-111).
At block write, instead of ignored address A$_{2-0}$, DQ$_{0-31}$ control each pixel.

Downloaded from Elcodis.com electronic components distributor

(Continued)

Pixel and I/O masking : By Mask at Write Per Bit Mode, the selected bit planes keep the original data.
By Pixel Data issued through DQ pin, the selected pixels keep the original data.
See PIXEL TO DQ MAPPING TABLE.

Assume 8bpp,
White = "0000,0000", Red="1010,0011", Green ="1110,0001", Yellow ="0000,1111", Blue ="1100,0011"

i) STEP

¨ç SMRS(LCR) : Load color(for 8bpp, through x 32 DQ color0-3 are loaded into color registers)
Load(color3, color2, color1, color0) = (Blue, Green, Yellow, Red)
= "1100,0011,1110,0001,0000,1111,1010,0011"

¨è SMRS(LMR): Load mask. Mask[31-0] ="1111,1111,1101,1101, 0100,0010,0111,0110"
--> Byte 3 : No I/O Masking ; Byte 2 : I/O Masking ; Byte 1 : I/O and Pixel Masking ; Byte 0 : DQM Byte Masking

¨é Row Active with DSF "H" : I/O Mask by Write Per Bit Mode Enable

¨ê Block Write with DQ[31-0] = "0111,0111,1111,1111,0101,0101,1110,1110" (Pixel Mask)

i) ILLUSTRATION

I/O(=DQ)	31 24	23 16	15 8	7 0
Color Register	Blue 1 1 0 0 0 0 1 1	Green 1 1 1 0 0 0 0 1	Yellow 0 0 0 0 1 1 1 1	Red 1 0 1 0 0 0 1 1
DQMi	DQM3=0	DQM2=0	DQM1=0	DQM0=1
Mask Register	1 1 1 1 1 1 1 1	1 1 0 1 1 1 0 1	0 1 0 0 0 0 1 0	0 1 1 1 0 1 1 0
Before Write	Yellow 0 0 0 0 1 1 1 1	Yellow 0 0 0 0 1 1 1 1	Green 1 1 1 0 0 0 0 1	White 0 0 0 0 0 0 0 0
After Write	Blue 1 1 0 0 0 0 1 1	Blue 1 1 0 0 0 0 1 1	Red 1 0 1 0 0 0 1 1	White 0 0 0 0 0 0 0 0

Note 1

I/O(=DQ)		31 24	23 16	15 8	7 0
DQMi		DQM3=0	DQM2=0	DQM1=0	DQM0=1
Color Register		Color3=Blue	Color2=Green	Color1=Yellow	Color0=Red
Before Block Write & DQ (Pixel data)	000	Yellow DQ_{24}=H	Yellow DQ_{16}=H	Green DQ_{8}=H	White DQ_{0}=L
	001	Yellow DQ_{25}=H	Yellow DQ_{17}=H	Green DQ_{9}=L	White DQ_{1}=H
	010	Yellow DQ_{26}=H	Yellow DQ_{18}=H	Green DQ_{10}=H	White DQ_{2}=H
	011	Yellow DQ_{27}=L	Yellow DQ_{19}=H	Green DQ_{11}=L	White DQ_{3}=H
	100	Yellow DQ_{28}=H	Yellow DQ_{20}=H	Green DQ_{12}=H	White DQ_{4}=L
	101	Yellow DQ_{29}=H	Yellow DQ_{21}=H	Green DQ_{13}=L	White DQ_{5}=H
	110	Yellow DQ_{30}=H	Yellow DQ_{22}=H	Green DQ_{14}=H	White DQ_{6}=H
	111	Yellow DQ_{31}=L	Yellow DQ_{23}=H	Green DQ_{15}=L	White DQ_{7}=H
After Block Write	000	Blue	**Blue**	**Red**	White
	001	Blue	**Blue**	Green	White
	010	Blue	**Blue**	**Red**	White
	011	Yellow	**Blue**	Green	White
	100	Blue	**Blue**	**Red**	White
	101	Blue	**Blue**	Green	White
	110	Blue	**Blue**	**Red**	White
	111	Yellow	**Blue**	Green	White

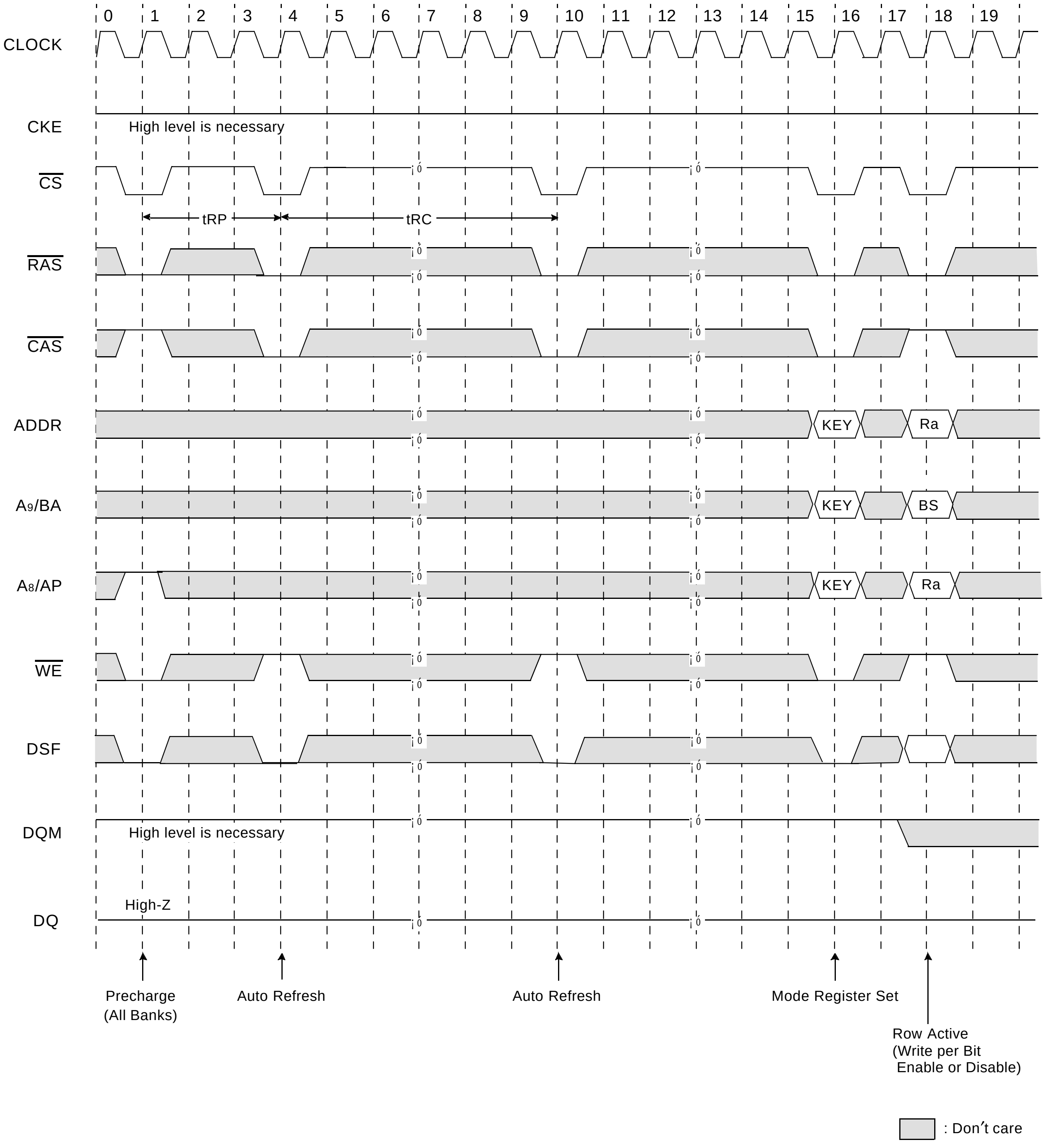
Note 2 Note 1

PIXEL MASK **I/O MASK** **PIXEL & I/O MASK** **BYTE MASK**

***Note :** 1. DQM byte masking.
2. At normal write, ONE column is selected among columns decorded by A_{2-0}(000-111).
At block write, instead of ignored address A_{2-0}, DQ_{0-31} control each pixel.

Downloaded from Elcodis.com electronic components distributor

Power On Sequence & Auto Refresh



Precharge
(All Banks)

Auto Refresh

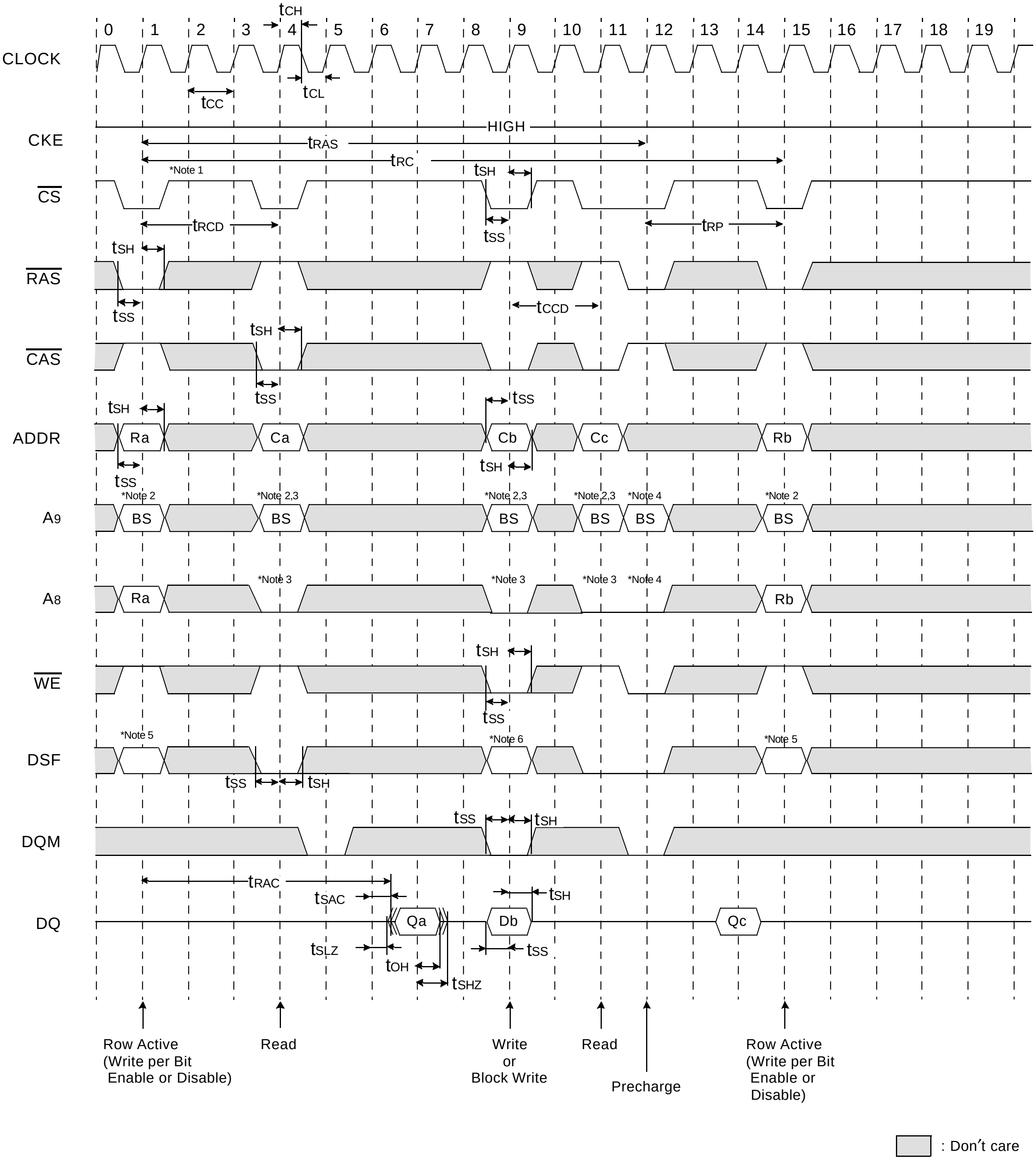
Auto Refresh

Mode Register Set

Row Active
(Write per Bit
Enable or Disable)

Downloaded from Elcodis.com electronic components distributor

Single Bit Read-Write-Read Cycle(Same Page) @CAS Latency=3, Burst Length=1



Downloaded from Elcodis.com electronic components distributor

***Note :** 1. All input can be don't care when $\overline{CS}$ is high at the CLK high going edge.
2. Bank active & read/write are controlled by A_9.

A_9	Active & Read/Write
0	Bank A
1	Bank B

3. Enable and disable auto precharge function are controlled by A_8 in read/write command.

A_8	A9	Operation
0	0	Disable auto precharge, leave bank A active at end of burst.
	1	Disable auto precharge, leave bank B active at end of burst.
1	0	Enable auto precharge, precharge bank A at end of burst.
	1	Enable auto precharge, precharge bank B at end of burst.

4. A_8 and A_9 control bank precharge when precharge command is asserted.

A_8	A_9	Precharge
0	0	Bank A
0	1	Bank B
1	X	Both Bank

5. Enable and disable Write-per Bit function are controlled by DSF in Row Active command.

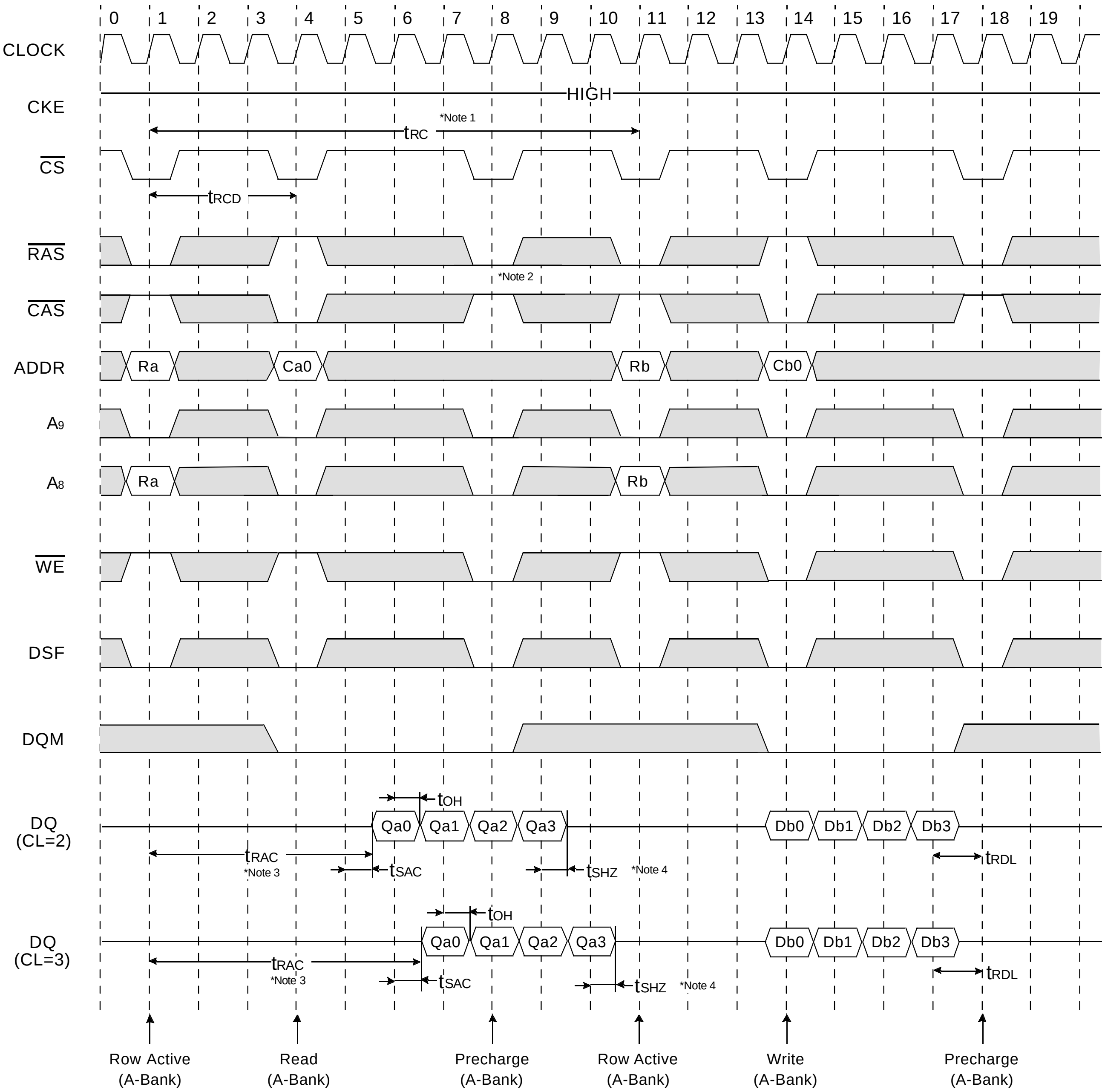
A_9	DSF	Operation
0	L	Bank A row active, disable write per bit function for bank A
	H	Bank A row active, enable write per bit function for bank A
1	L	Bank B row active, disable write per bit function for bank B
	H	Bank B row active, enable write per bit function for bank B

6. Block write/normal write is controlled by DSF.

DSF	Operation	Minimum cycle time
L	Normal write	t_{CCD}
H	Block write	t_{BWC}

Downloaded from Elcodis.com electronic components distributor

Read & Write Cycle at Same Bank @Burst Length=4



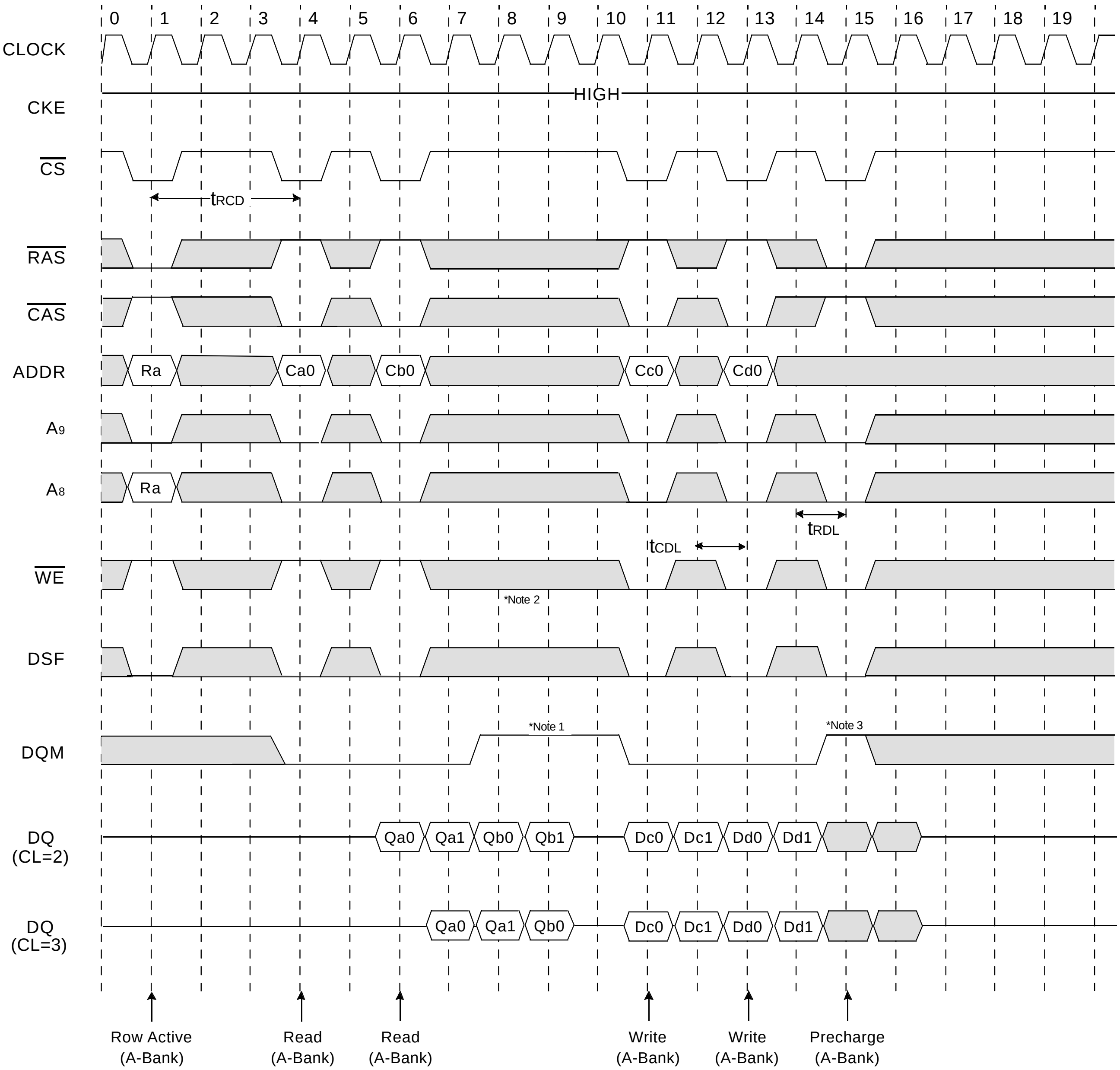
▨ : Don′t care

***Note :**

1. Minimum row cycle times is required to complete internal DRAM operation.
2. Row precharge can interrupt burst on any cycle. [CAS Latency - 1] valid output data available after Row enters precharge. Last valid output will be Hi-Z after tSHZ from the clcok.
3. Access time from Row address. tCC *(tRCD + CAS latency - 1) + tSAC
4. Ouput will be Hi-Z after the end of burst. (1, 2, 4, & 8)
   At Full page bit burst, burst is wrap-around.

Downloaded from Elcodis.com electronic components distributor

Page Read & Write Cycle at Same Bank @Burst Length=4

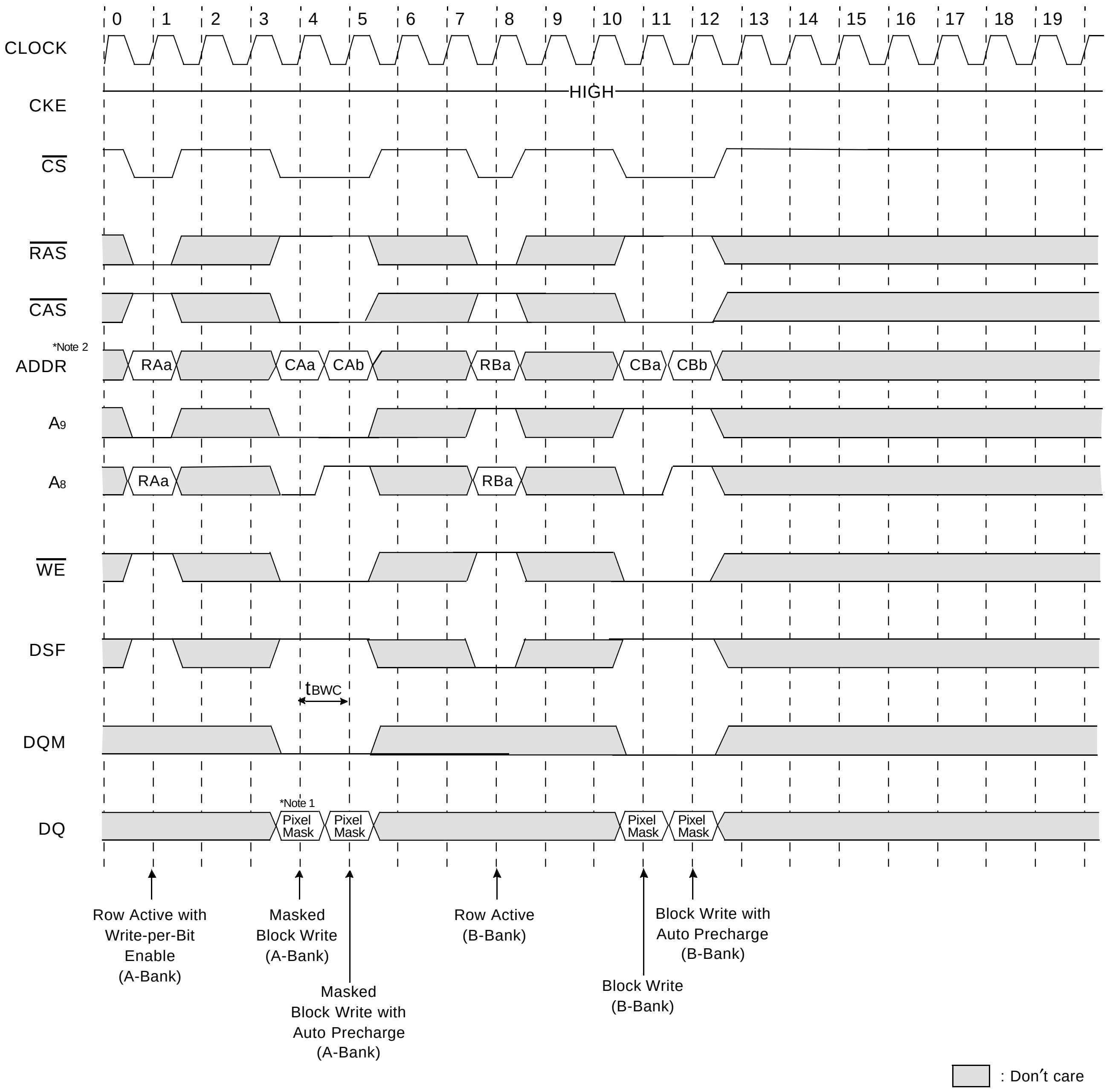


▭ : Don't care

***Note :**
1. To write data before burst read ends, DQM should be asserted three cycle prior to write command to avoid bus contention.
2. Row precharge will interrupt writing. Last data input, tRDL before Row precharge, will be written.
3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.

Downloaded from Elcodis.com electronic components distributor

Block Write cycle(with Auto Precharge)

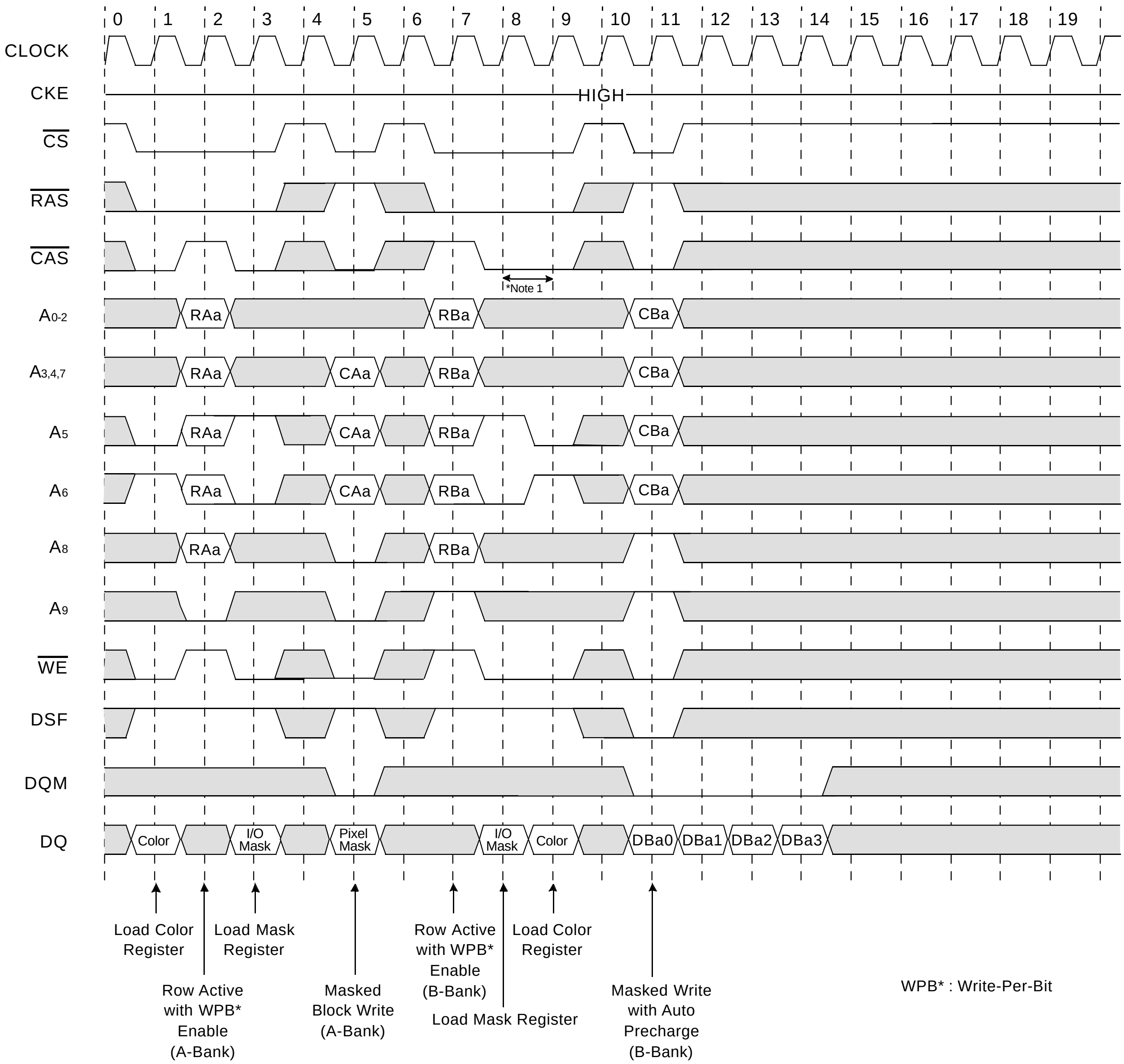


***Note :** 1. Column Mask(DQi=L : Mask, DQi=H :Non Mask)

2. At Block Write, $CA_{0\sim2}$ are ignored.

Downloaded from Elcodis.com electronic components distributor

SMRS and Block/Normal Write @ Burst Length=4

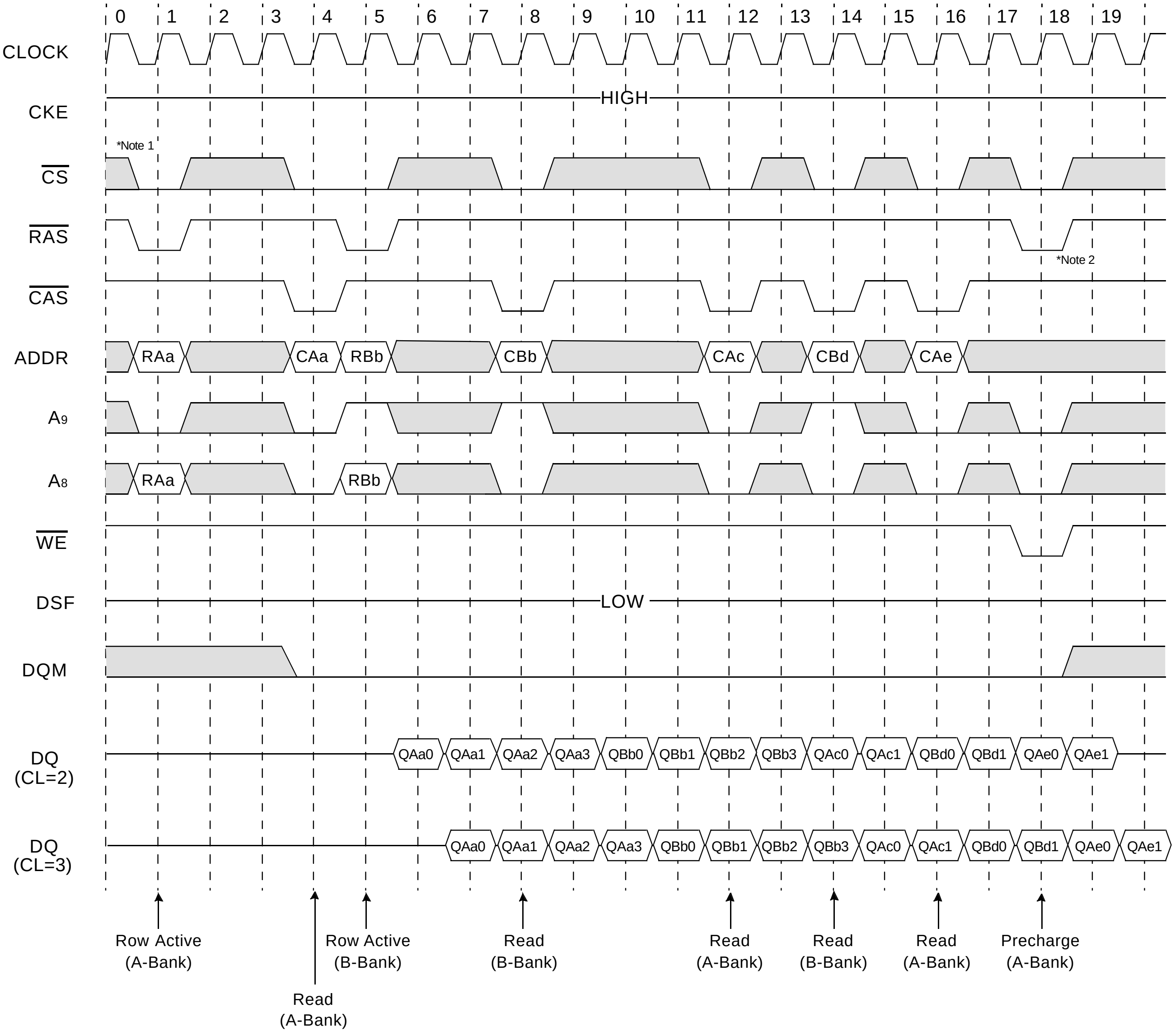


▭ : Don't care

***Note :** 1. At the next clock of special mode set command, new command is possible.

Downloaded from Elcodis.com electronic components distributor

Page Read Cycle at Different Bank @Burst Length=4



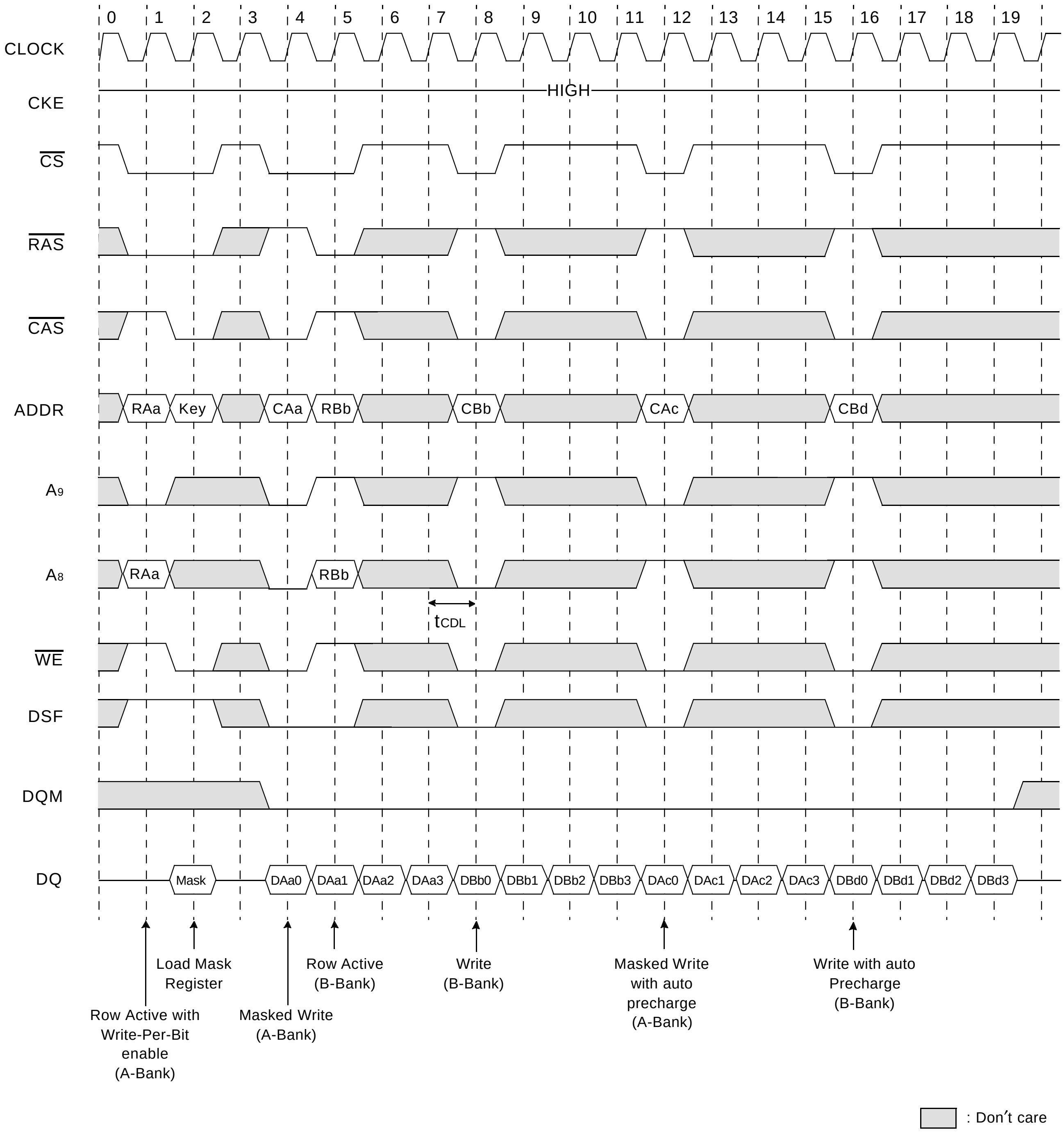
▨ : Don't care

***Note :** 1. CS can be don't care when RAS, CAS and WE are high at the clock high going edge.

2. To interrupt a burst read by row precharge, both the read and the precharge banks must be the same.

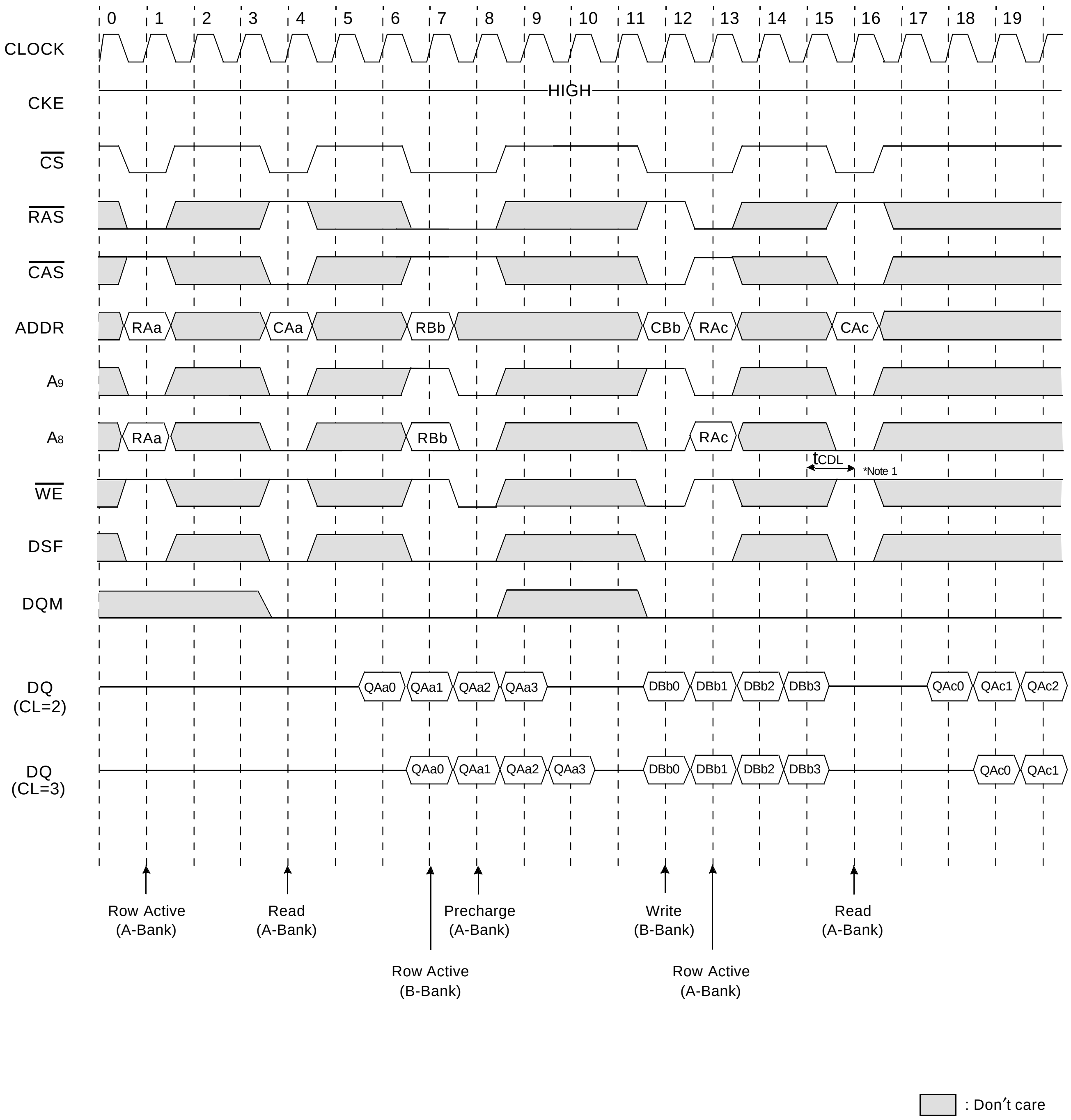
Downloaded from Elcodis.com electronic components distributor

Page Write Cycle at Different Bank @Burst Length=4



Downloaded from Elcodis.com electronic components distributor

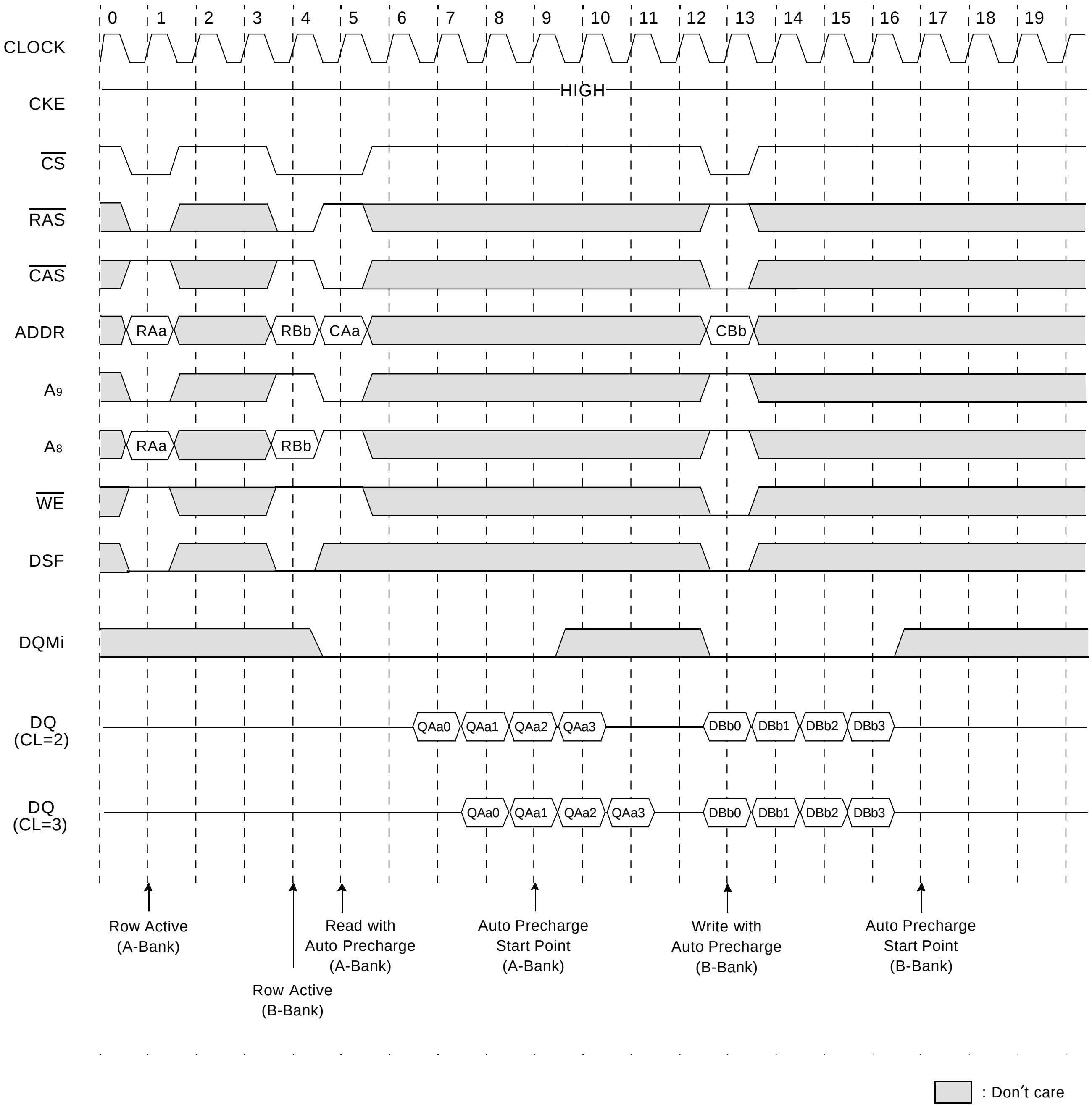
Read & Write Cycle at Different Bank @Burst Length=4



***Note :** 1. tCDL should be met to complete write.

Downloaded from Elcodis.com electronic components distributor

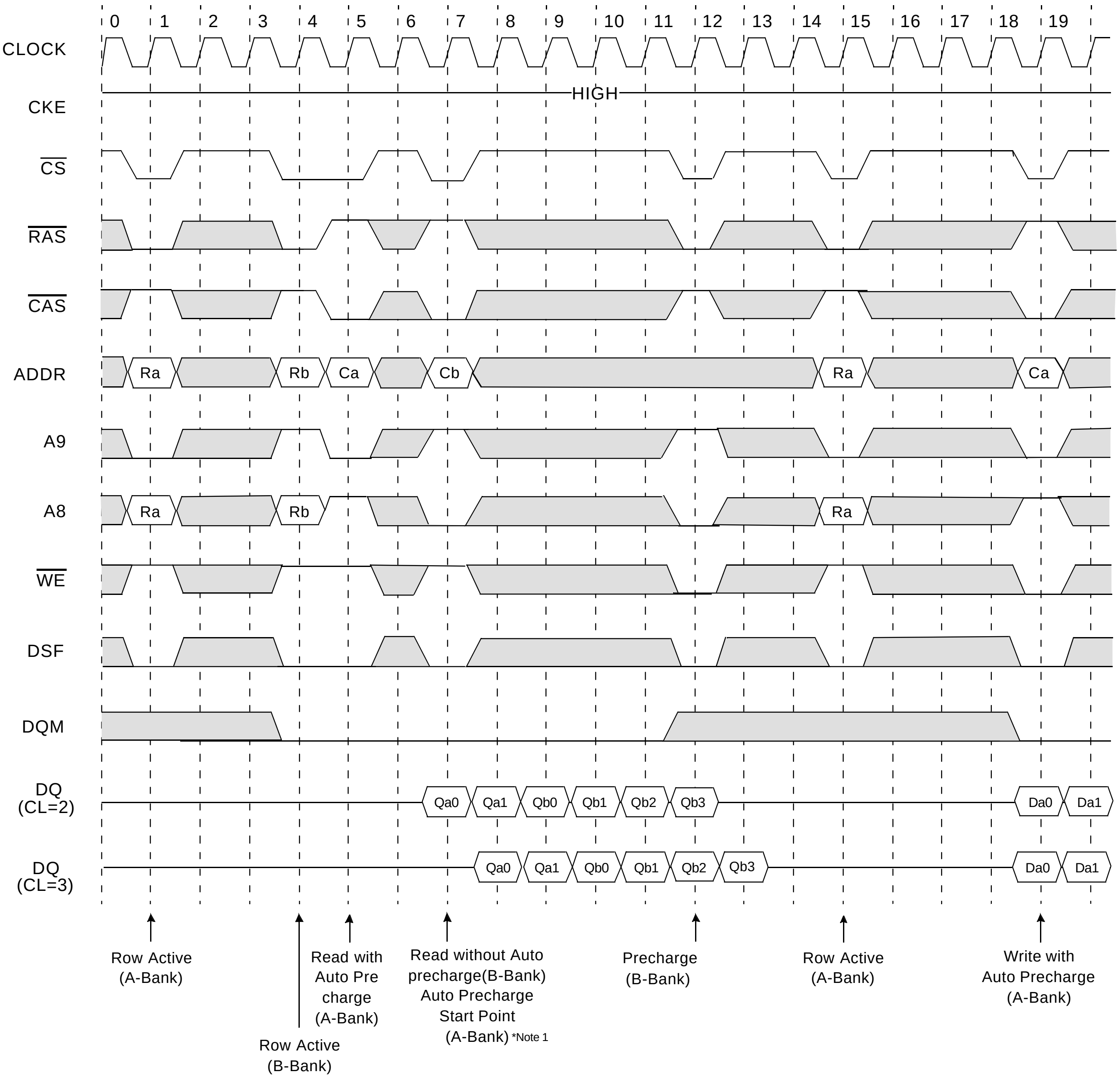
Read & Write Cycle with Auto Precharge I @Burst Length=4



***Note :** 1. t_{RCD} should be controlled to meet minimum t_{RAS} before internal precharge start.
(In the case of Burst Length=1 & 2, BRSW mode and Block write)

Downloaded from Elcodis.com electronic components distributor

Read & Write Cycle with Auto Precharge II @Burst Length=4

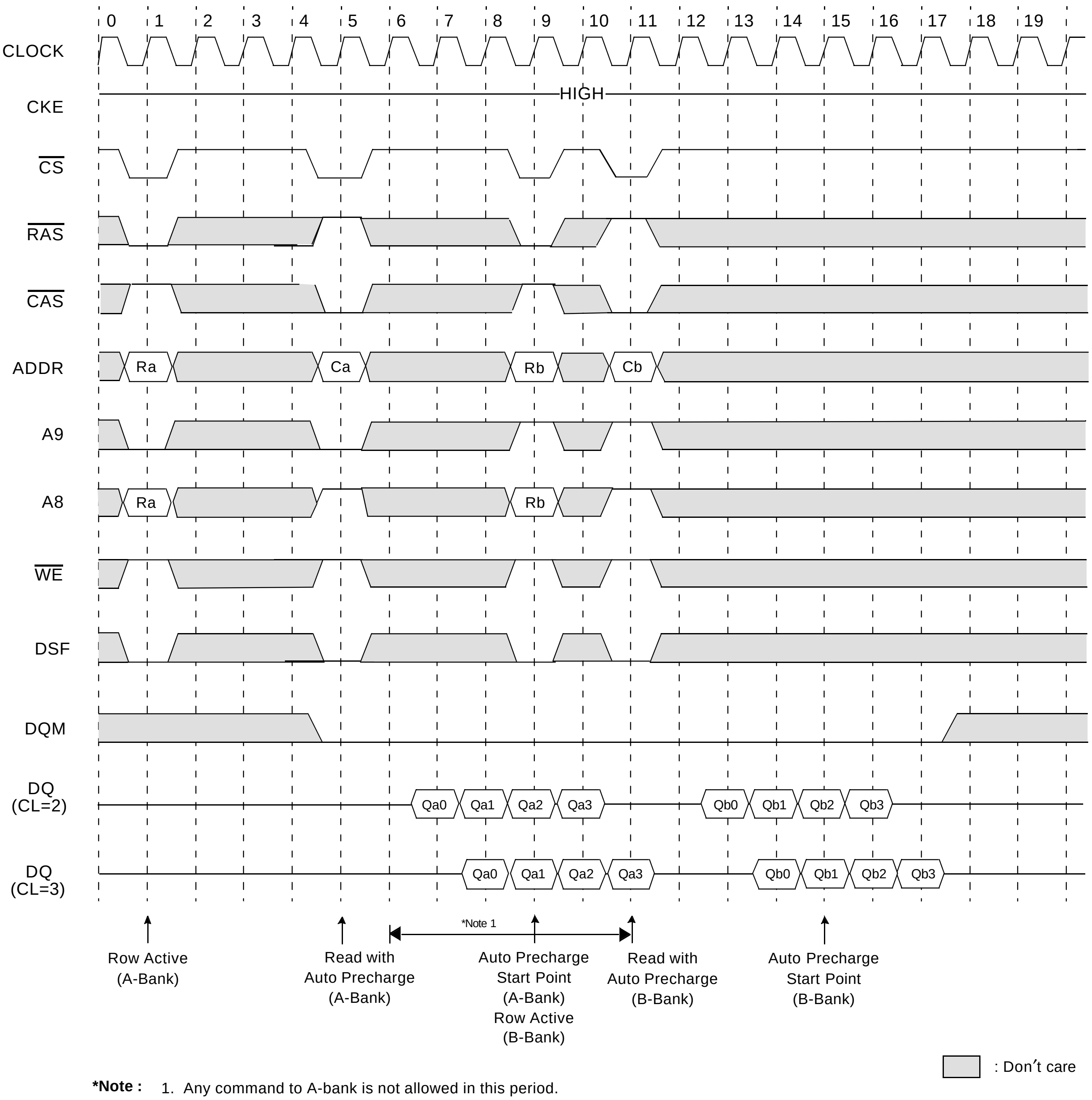


▨ : Don′t care

***Note:** 1. When Read(Write) command with auto precharge is issued at A-Bank after A and B Bank activation.
- if Read(Write) command without auto precharge is issued at B-Bank before A Bank auto precharge starts, A Bank auto precharge will start at B Bank read command input point .
- any command can not be issued at A Bank during tRP after A Bank auto precharge starts.

Downloaded from Elcodis.com electronic components distributor

Read & Write Cycle with Auto Precharge III @Burst Length=4

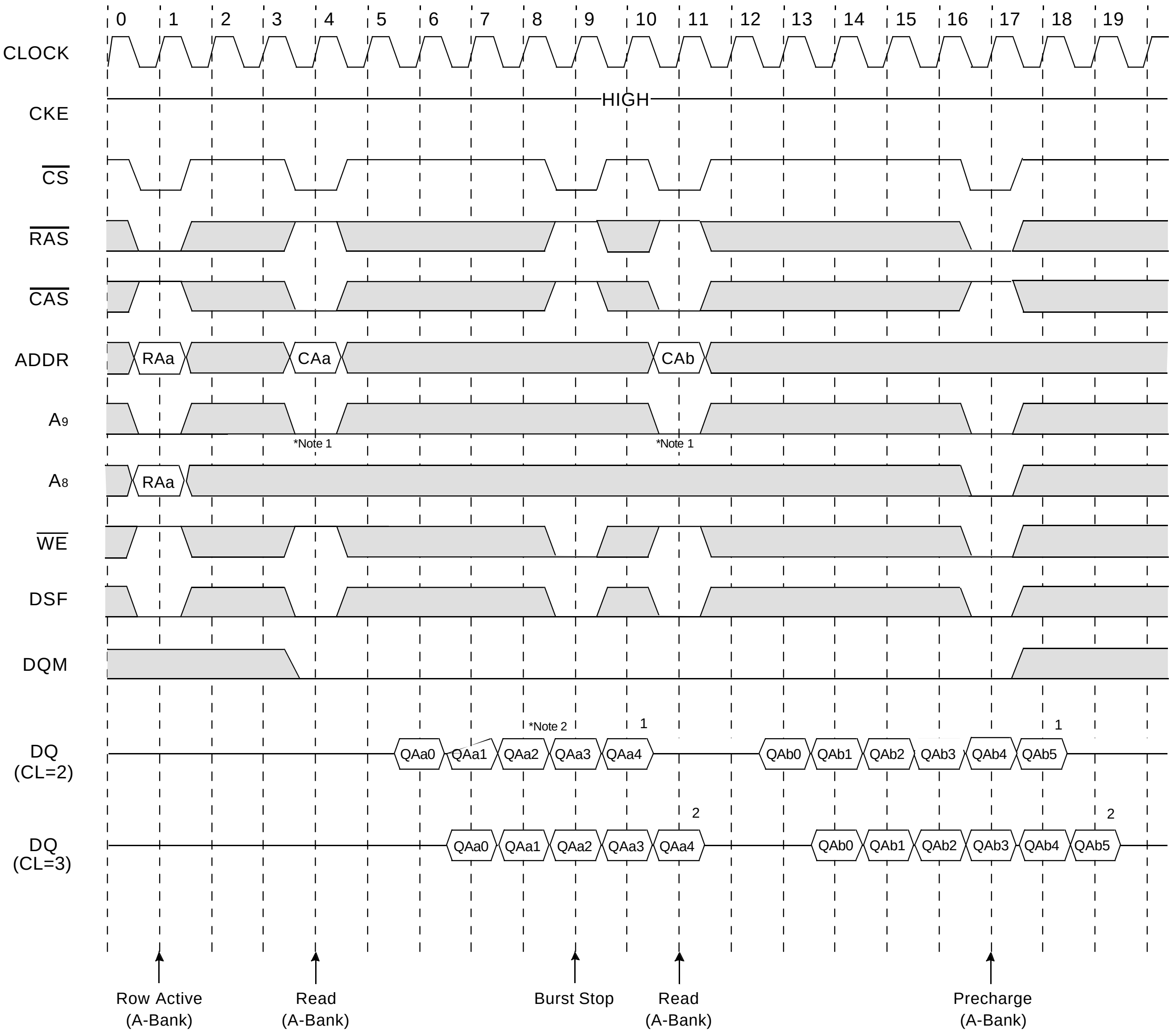


▭ : Don′t care

***Note :** 1. Any command to A-bank is not allowed in this period.
tRP is determined from at auto precharge start point

Downloaded from Elcodis.com electronic components distributor

Read Interrupted by Precharge Command & Read Burst Stop Cycle (@Full page Only)

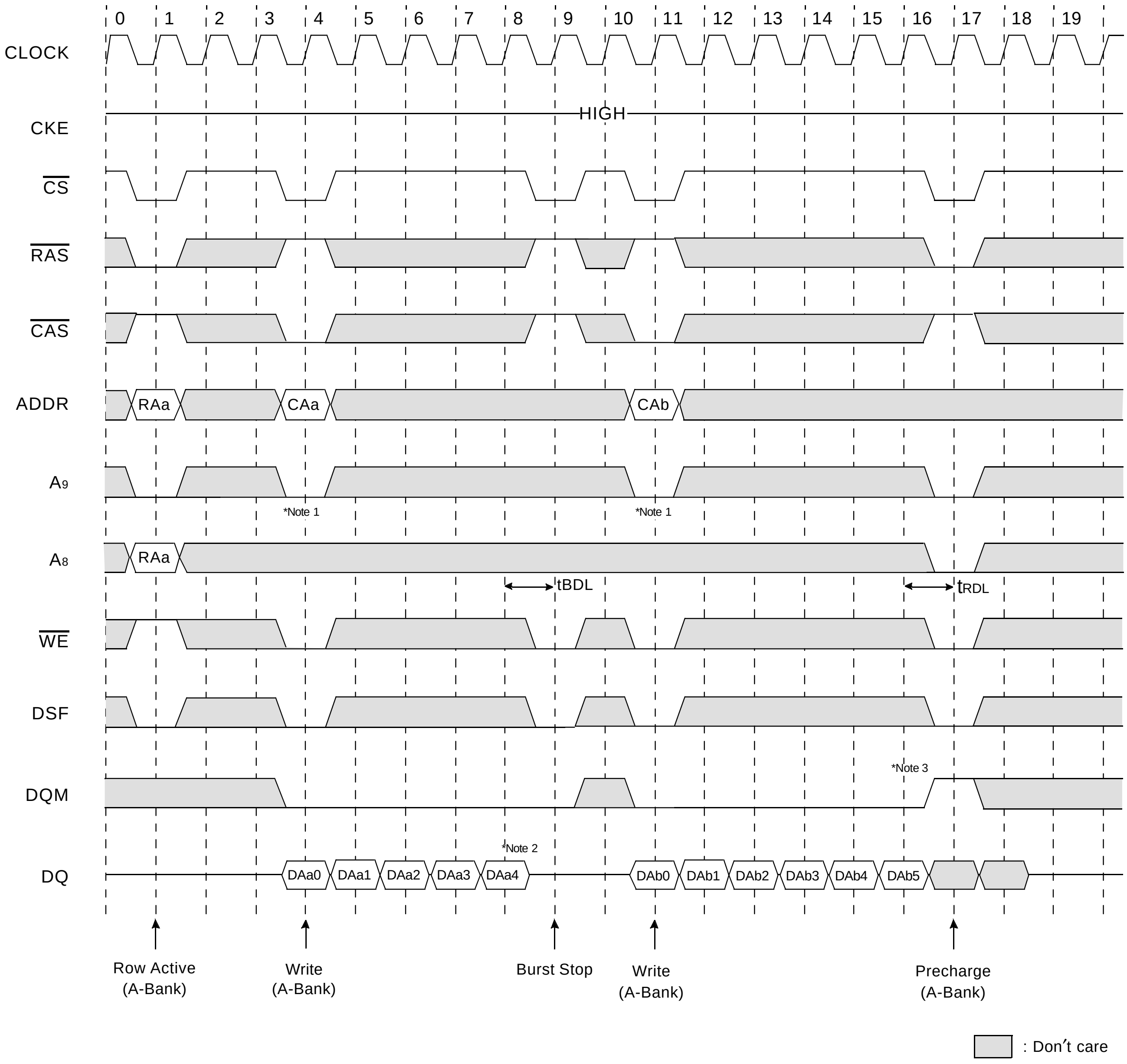


▭ : Don′t care

***Note :**
1. At full page mode, burst is wrap-around at the end of burst. So auto precharge is impossible.
2. About the valid DQ′s after burst stop, it is same as the case of $\overline{\text{RAS}}$ interrupt.
   Both cases are illustrated above timing diagram. See the label 1, 2 on them.
   But at burst write, Burst stop and $\overline{\text{RAS}}$ interrupt should be compared carefully.
   Refer the timing diagram of "Full page write burst stop cycle".
3. Burst stop is valid at full page mode.

Downloaded from Elcodis.com electronic components distributor

Write Interrupted by Precharge Command & Write Burst Stop Cycle (@ Full page Only)

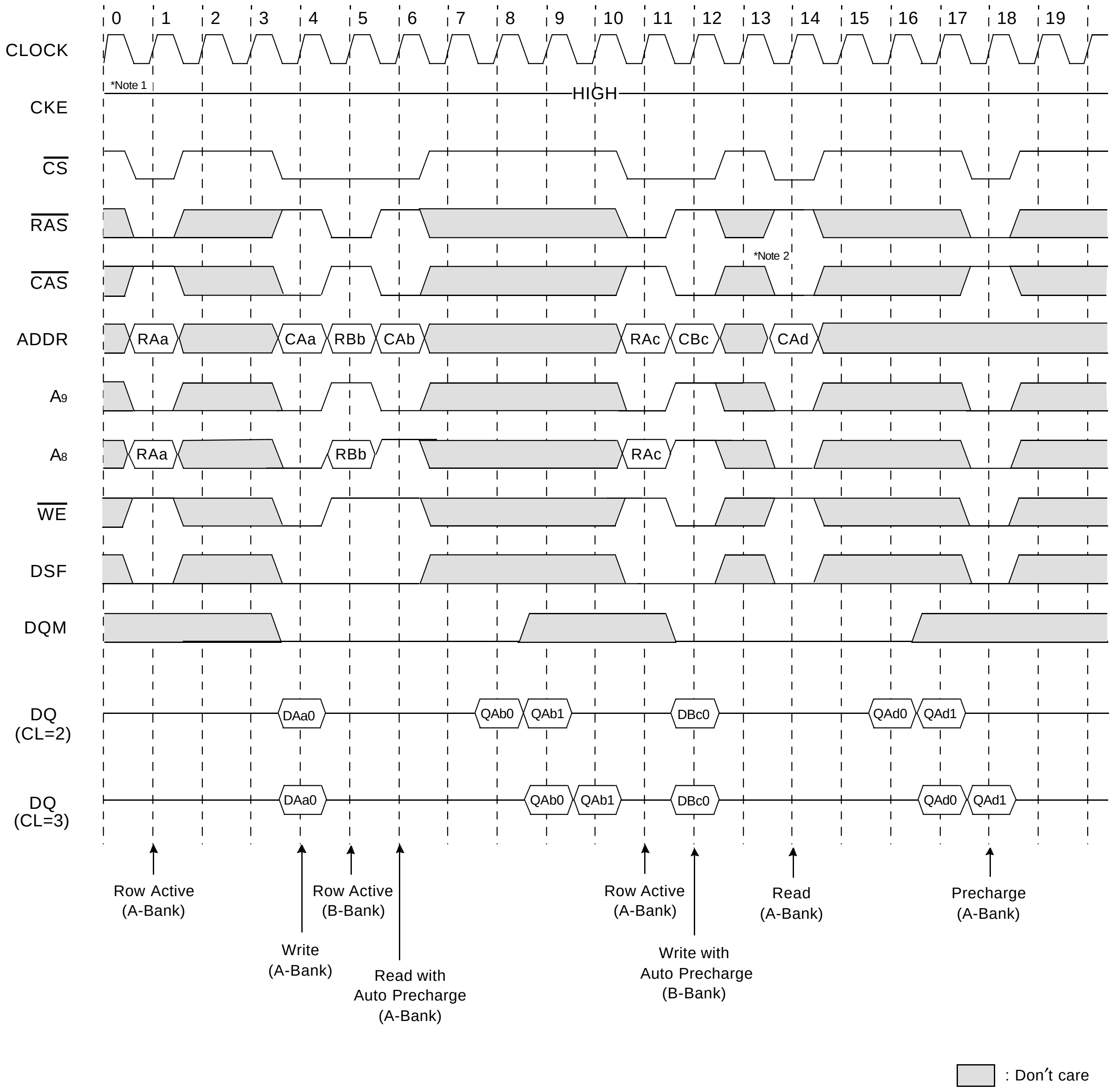


***Note :**

1. At full page mode, burst is wrap-around at the end of burst. So auto precharge is impossible.
2. Data-in at the cycle of burst stop command cannot be written into the corresponding memory cell.
   It is defined by AC parameter of tBDL (=1CLK).
3. Data-in at the cycle of interrupted by precharge cannot be written into the corresponding memory cell.
   It is defined by AC parameter of tRDL (=1CLK).
   DQM at write interrupted by precharge command is needed to ensure tRDL of 1CLK.
   DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst.
   Input data after Row precharge cycle will be masked internally.
4. Burst stop is valid only at full page burst length.

Downloaded from Elcodis.com electronic components distributor

Burst Read Single bit Write Cycle @Burst Length=2, BRSW

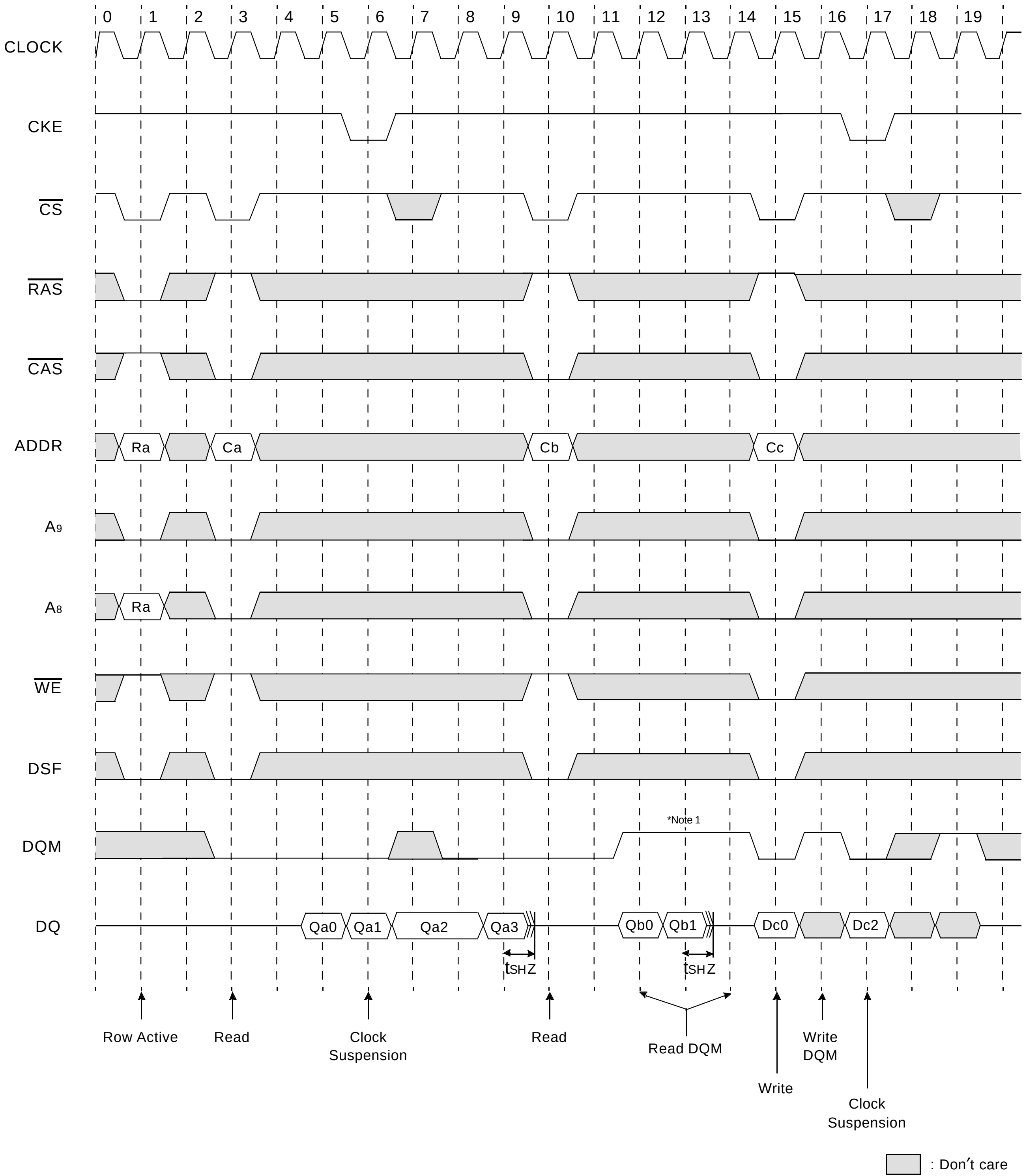


***Note :**

1. BRSW mode is enabled by setting A_9 "High" at MRS (Mode Register Set).
   At the BRSW Mode, the burst length at write is fixed to "1" regardless of programed burst length.
2. When BRSW write command with auto precharge is executed, keep it in mind that t_{RAS} should not be violated.
   Auto precharge is executed at the burst-end cycle, so in the case of BRSW write command,
   the next cycle starts the precharge.
3. WPB function is also possible at BRSW mode.

Downloaded from Elcodis.com electronic components distributor

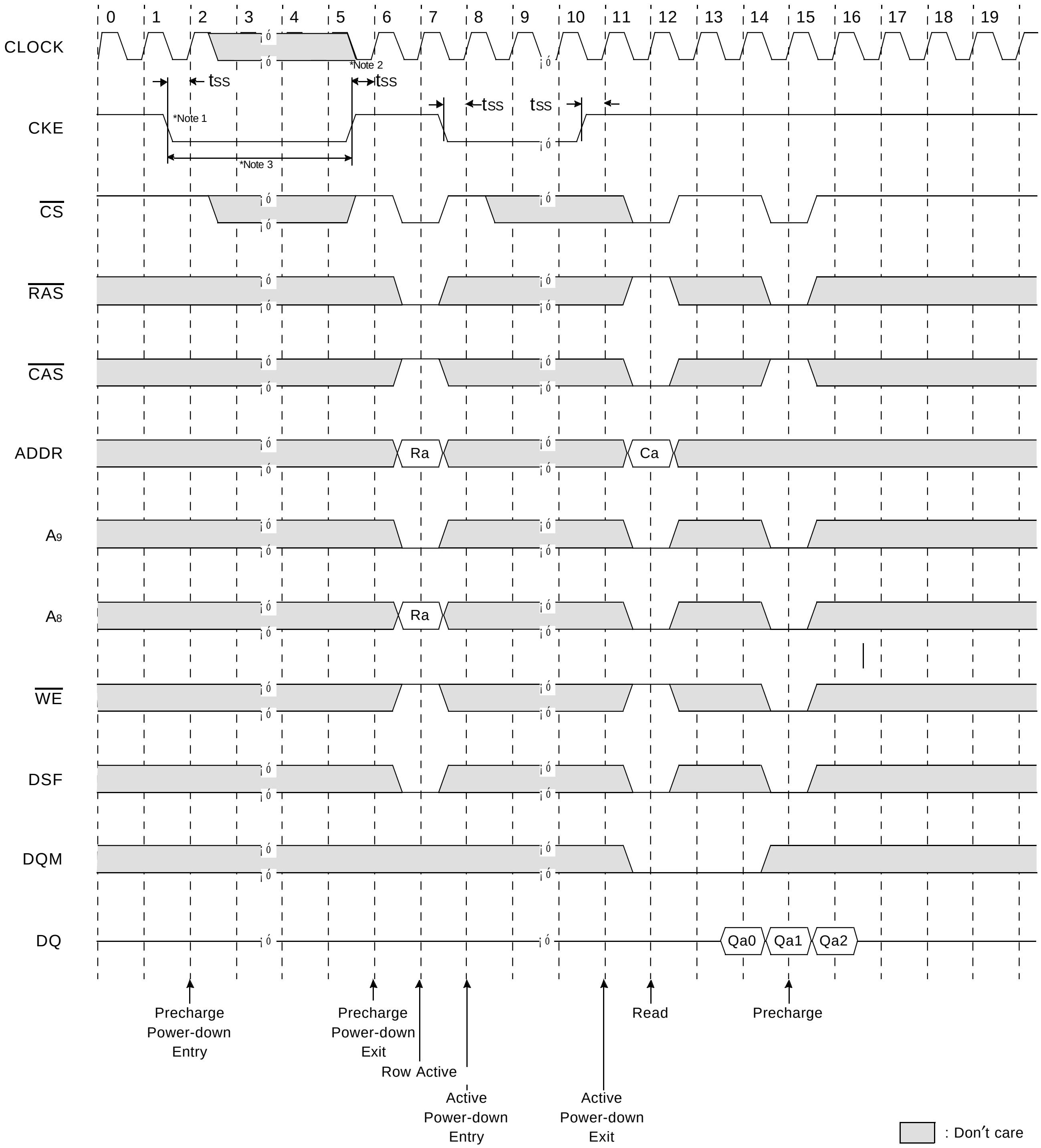
Clock suspension & DQM operation cycle @CAS Latency=2, Burst Length=4



***Note :** 1. DQM needed to prevent bus contention.

Downloaded from Elcodis.com electronic components distributor

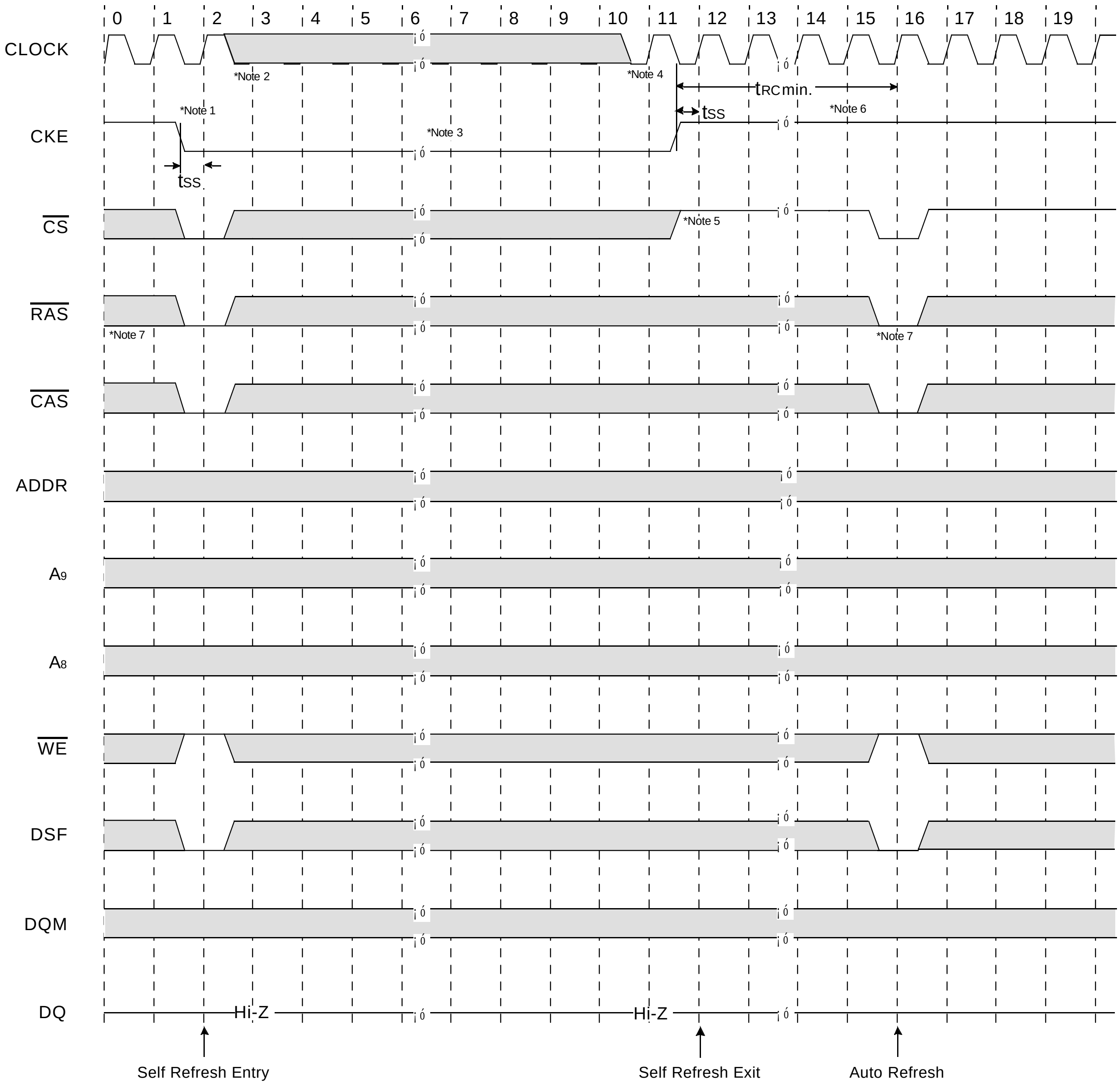
Active/Precharge Power Down Mode @CAS Lantency=2, Burst Length=4



***Note :**
1. All banks should be in idle state prior to entering precharge power down mode.
2. CKE should be set high at least "1CLK + tSS" prior to Row active command.
3. Cannot violate minimum refresh specification. (16ms)

Downloaded from Elcodis.com electronic components distributor

Self Refresh Entry & Exit Cycle



▨ : Don′t care

***Note :** **TO ENTER SELF REFRESH MODE**

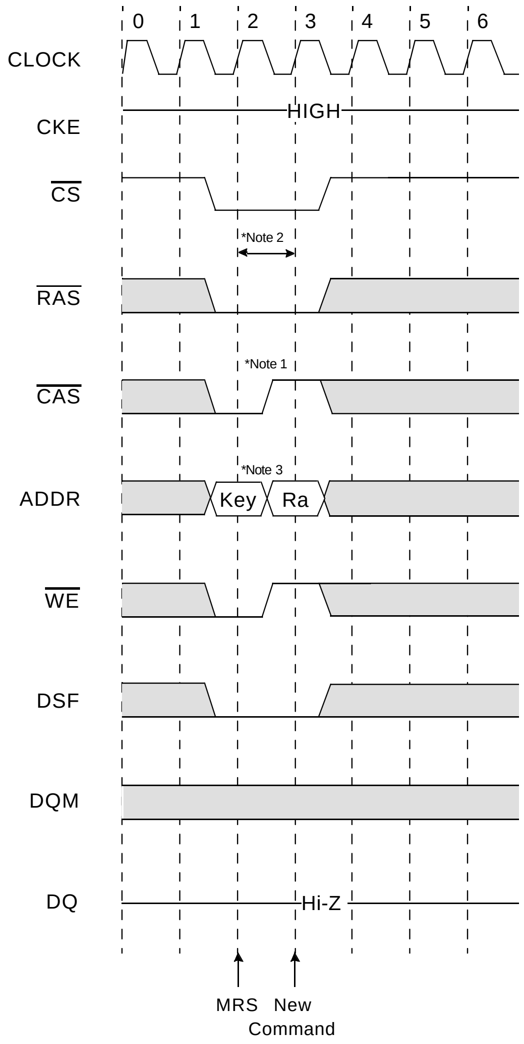
1. $\overline{\text{CS}}$, $\overline{\text{RAS}}$ & $\overline{\text{CAS}}$ with CKE should be low at the same clock cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don′t care except for CKE.
3. The device remains in self refresh mode as long as CKE stays "Low".
   cf.) Once the device enters self refresh mode, minimum t_{RAS} is required before exit from self refresh.

TO EXIT SELF REFRESH MODE

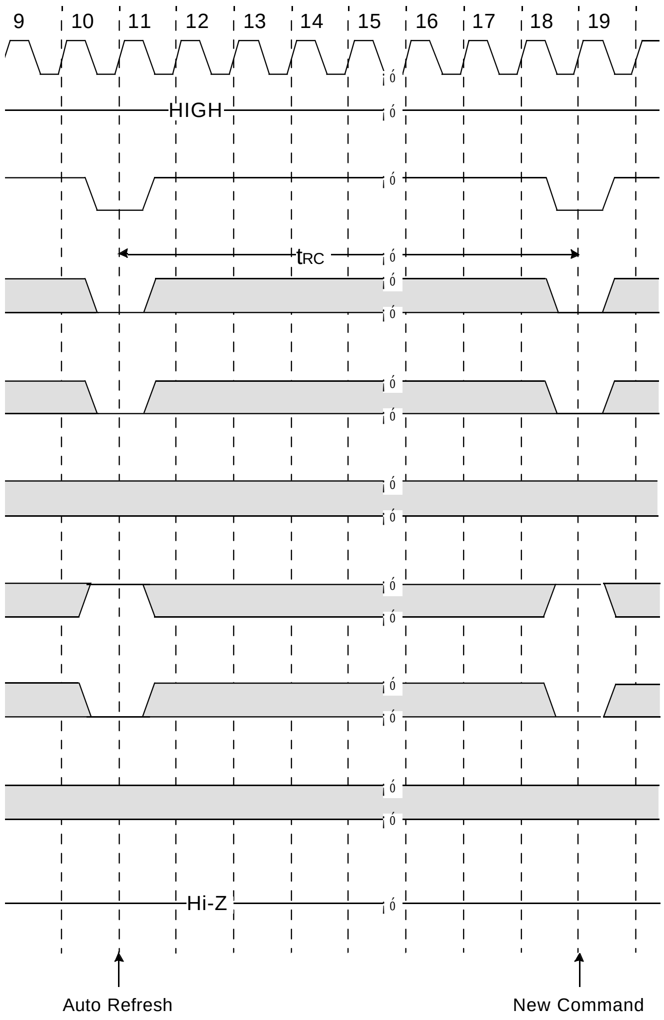
4. System clock restart and be stable before returning CKE high.
5. CS starts from high.
6. Minimum t_{RC} is required after CKE going high to complete self refresh exit.
7. 1K cycle of burst auto refresh is required before self refresh entry and after self refresh exit

Downloaded from Elcodis.com electronic components distributor

Mode Register Set Cycle



Auto Refresh Cycle



▨ : Don't care

* Both banks precharge should be completed before Mode Register Set cycle and auto refresh cycle.

MODE REGISTER SET CYCLE

***Note :**

1. CS, RAS, CAS, & WE activation and DSF of low at the same clock cycle with address key will set internal mode register.
2. Minimum 1 clock cycles should be met before new RAS activation.
3. Please refer to Mode Register Set table.

Downloaded from Elcodis.com electronic components distributor

FUNCTION TRUTH TABLE(TABLE 1)

Current State	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	DSF	BA (A_9)	ADDR	ACTION	NOTE
IDLE	H	X	X	X	X	X	X	NOP	
	L	H	H	H	X	X	X	NOP	
	L	H	H	L	X	X	X	ILLEGAL	2
	L	H	L	X	X	BA	CA	ILLEGAL	2
	L	L	H	H	L	BA	RA	Row Active ; Latch Row Address ; Non-IO Mask	
	L	L	H	H	H	BA	RA	Row Active ; Latch Row Address ; IO Mask	
	L	L	H	L	L	BA	PA	NOP	4
	L	L	H	L	H	X	X	ILLEGAL	
	L	L	L	H	L	X	X	Auto Refresh or Self Refresh	5
	L	L	L	H	H	X	X	ILLEGAL	
	L	L	L	L	L	OP Code		Mode Register Access	5
	L	L	L	L	H	OP Code		Special Mode Register Access	6
Row Active	H	X	X	X	X	X	X	NOP	
	L	H	H	H	X	X	X	NOP	
	L	H	H	L	X	X	X	ILLEGAL	2
	L	H	L	H	L	BA	CA,AP	Begin Read ; Latch CA ; Determine AP	
	L	H	L	H	H	X	X	ILLEGAL	
	L	H	L	L	L	BA	CA,AP	Begin Write ;Latch CA ; Determine AP	
	L	H	L	L	H	BA	CA,AP	Block Write ;Latch CA ; Determine AP	
	L	L	H	H	X	BA	RA	ILLEGAL	2
	L	L	H	L	L	BA	PA	Precharge	
	L	L	H	L	H	X	X	ILLEGAL	
	L	L	L	H	X	X	X	ILLEGAL	
	L	L	L	L	L	X	X	ILLEGAL	
	L	L	L	L	H	OP Code		Special Mode Register Access	6
Read	H	X	X	X	X	X	X	NOP(Continue Burst to End --> Row Active)	
	L	H	H	H	X	X	X	NOP(Continue Burst to End --> Row Active)	
	L	H	H	L	L	X	X	Term burst --> Row active	
	L	H	H	L	H	X	X	ILLEGAL	
	L	H	L	H	L	BA	CA,AP	Term burst ; Begin Read ; Latch CA ; Determine AP	3
	L	H	L	H	H	X	X	ILLEGAL	
	L	H	L	L	L	BA	CA,AP	Term burst ; Begin Write ; Latch CA ; Determine AP	3
	L	H	L	L	H	BA	CA.AP	Term burst ; Block Write ; Latch CA ; Determine AP	3
	L	L	H	H	X	BA	RA	ILLEGAL	2
	L	L	H	L	L	BA	PA	Term Burst ; Precharge timing for Reads	3
	L	L	H	L	H	X	X	ILLEGAL	
	L	L	L	X	X	X	X	ILLEGAL	
Write	H	X	X	X	X	X	X	NOP(Continue Burst to End --> Row Active)	
	L	H	H	H	X	X	X	NOP(Continue Burst to End --> Row Active)	
	L	H	H	L	L	X	X	Term burst --> Row active	
	L	H	H	L	H	X	X	ILLEGAL	
	L	H	L	H	L	BA	CA,AP	Term burst ; Begin Read ; Latch CA ; Determine AP	3
	L	H	L	H	H	X	X	ILLEGAL	
	L	H	L	L	L	BA	CA,AP	Term burst ; Begin Write ; Latch CA ; Determine AP	3
	L	H	L	L	H	BA	CA,AP	Term burst ; Block Write ; Latch CA ; Determine AP	3

Downloaded from Elcodis.com electronic components distributor

FUNCTION TRUTH TABLE(TABLE 1, Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	BA (A_9)	ADDR	ACTION	NOTE
Write	L	L	H	H	X	BA	RA	ILLEGAL	2
	L	L	H	L	L	BA	PA	Term Burst : Precharge timing for Writes	3
	L	L	H	L	H	X	X	ILLEGAL	
	L	L	L	X	X	X	X	ILLEGAL	
Read with Auto Precharge	H	X	X	X	X	X	X	NOP(Continue Burst to End --> Precharge)	
	L	H	H	H	X	X	X	NOP(Continue Burst to End --> Precharge)	
	L	H	H	L	X	X	X	ILLEGAL	
	L	H	L	H	X	BA	CA,AP	ILLEGAL	2
	L	H	L	L	X	BA	CA,AP	ILLEGAL	2
	L	L	H	X	X	BA	RA,PA	ILLEGAL	
	L	L	L	X	X	X	X	ILLEGAL	2
Write with Auto Precharge	H	X	X	X	X	X	X	NOP(Continue Burst to End --> Precharge)	
	L	H	H	H	X	X	X	NOP(Continue Burst to End --> Precharge)	
	L	H	H	L	X	X	X	ILLEGAL	
	L	H	L	H	X	BA	CA,AP	ILLEGAL	2
	L	H	L	L	X	BA	CA,AP	ILLEGAL	2
	L	L	H	X	X	BA	RA,PA	ILLEGAL	
	L	L	L	X	X	X	X	ILLEGAL	2
Precharging	H	X	X	X	X	X	X	NOP --> Idle after t_{RP}	
	L	H	H	H	X	X	X	NOP --> Idle after t_{RP}	
	L	H	H	L	X	X	X	ILLEGAL	
	L	H	L	X	X	BA	CA,AP	ILLEGAL	2
	L	L	H	H	X	BA	RA	ILLEGAL	2
	L	L	H	L	X	BA	PA	NOP --> Idle after t_{RP}	2
	L	L	L	X	X	X	X	ILLEGAL	4
Block Write Recovering	H	X	X	X	X	X	X	NOP --> Row Active after t_{BWC}	
	L	H	H	H	X	X	X	NOP --> Row Active after t_{BWC}	
	L	H	H	L	X	X	X	ILLEGAL	
	L	H	L	X	X	BA	CA,AP	ILLEGAL	2
	L	L	H	H	X	BA	RA	ILLEGAL	2
	L	L	H	L	X	BA	PA	Term Block Write : Precharge timing for Block Write	2
	L	L	L	X	X	X	X	ILLEGAL	2
Row Activating	H	X	X	X	X	X	X	NOP --> Row Active after t_{RCD}	
	L	H	H	H	X	X	X	NOP --> Row Active after t_{RCD}	
	L	H	H	L	X	X	X	ILLEGAL	
	L	H	L	X	X	BA	CA,AP	ILLEGAL	2
	L	L	H	H	X	BA	RA	ILLEGAL	2
	L	L	H	L	X	BA	PA	ILLEGAL	2
	L	L	L	X	X	X	X	ILLEGAL	2
Refreshing	H	X	X	X	X	X	X	NOP --> Idle after t_{RC}	
	L	H	H	X	X	X	X	NOP --> Idle after t_{RC}	
	L	H	L	X	X	X	X	ILLEGAL	
	L	L	H	X	X	X	X	ILLEGAL	
	L	L	L	X	X	X	X	ILLEGAL	

Downloaded from Elcodis.com electronic components distributor

FUNCTION TRUTH TABLE (TABLE 1, Continued)

ABBREVIATIONS

RA = Row Address(A_0~A_9)
NOP = No Operation Command
BA = Bank Address(A_{10})
CA = Column Address(A_0~A_7)
PA = Precharge All(A_9)
AP = Auto Precharge(A_9)

***Note :** 1. All entries assume that CKE was active(High) during the preceding clock cycle and the current clock cycle.
2. Illegal to bank in specified state ; Function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA(and PA).
5. Illegal if any banks is not idle.
6. Legal only if all banks are in idle or row active state.

FUNCTION TRUTH TABLE for CKE(TABLE 2)

Current State	CKE n-1	CKE n	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	DSF	ADDR	ACTION	NOTE
Self Refresh	H	X	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	X	Exit Self Refresh --> ABI after t_{RC}	7
	L	H	L	H	H	H	X	X	Exit Self Refresh --> ABI after t_{RC}	7
	L	H	L	H	H	L	X	X	ILLEGAL	
	L	H	L	H	L	X	X	X	ILLEGAL	
	L	H	L	L	X	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	X	NOP(Maintain Self Refresh)	
Both Bank Precharge Power Down	H	X	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	X	Exit Power Down --> ABI	8
	L	H	L	H	H	H	X	X	Exit Power Down --> ABI	8
	L	H	L	H	H	L	X	X	ILLEGAL	
	L	H	L	H	L	X	X	X	ILLEGAL	
	L	H	L	L	X	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	X	NOP(Maintain Power Down Mode)	
All Banks Idle	H	H	X	X	X	X	X	X	Refer to Table 1	
	H	L	H	X	X	X	X	X	Enter Power Down	9
	H	L	L	H	H	H	X	X	Enter Power Down	9
	H	L	L	H	H	L	X	X	ILLEGAL	
	H	L	L	H	L	X	X	X	ILLEGAL	
	H	L	L	L	H	H	L	RA	Row (& Bank) Active	
	H	L	L	L	L	H	L	X	Enter Self Refresh	9
	H	L	L	L	L	L	L	OP Code	Mode Register Access	
	H	L	L	L	L	L	H	OP Code	Special Mode Register Access	
	L	L	X	X	X	X	X	X	NOP	
Any State other than Listed Above	H	H	X	X	X	X	X	X	Refer to Operations in Table 1	
	H	L	X	X	X	X	X	X	Begin Clock Suspend next cycle	10
	L	H	X	X	X	X	X	X	Exit Clock Suspend next cycle	10
	L	L	X	X	X	X	X	X	Maintain clock Suspend	

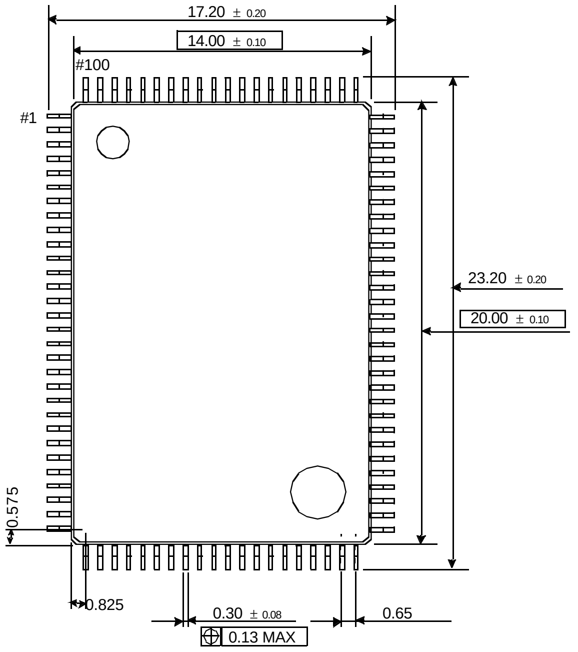
ABBREVIATIONS : ABI = All Banks Idle

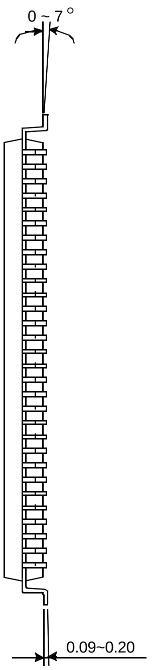
***Note :** 7. After CKE′s low to high transition to exist self refresh mode. And a time of t_{RC}(min) has to be elapse after CKE′s low to high transition to issue a new command.
8. CKE low to high transition is asynchronous as if restarts internal clock.
A minimum setup time "t_{SS} + one clock" must be satisfied before any command other than exit.
9. Power-down and self refresh can be entered only from the all banks idle state.
10. Must be a legal command.

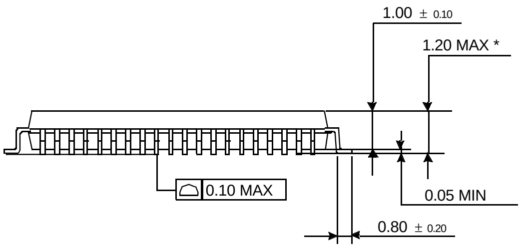
Downloaded from Elcodis.com electronic components distributor

PACKAGE DIMENSIONS (TQFP)

Dimensions in Millimeters







* All Package Dimensions of PQFP & TQFP are same except Height.
- PQFP (Height = 3.0mmMAX)
- TQFP (Height = 1.2mmMAX)

Downloaded from Elcodis.com electronic components distributor