# ISP1501

Hi-Speed Universal Serial Bus peripheral transceiver

**Rev. 02 — 21 November 2002** **Product data**

## 1. General description

The ISP1501 is a full-function transceiver designed to provide a Hi-Speed Universal Serial Bus (USB) analog front-end to Application-Specific Integrated Circuits (ASICs) and Field Programmable Gate Arrays (FPGAs) with a built-in USB Serial Interface Engine (SIE). A Hi-Speed USB transceiver is integrated to implement USB connectivity for high-speed peripherals. In addition, an Original USB transceiver provides backward compatibility with full-speed USB systems. A minimum number of external components is needed.

## 2. Features

- Complies with *Universal Serial Bus Specification Rev. 2.0*
- Legacy compliant Original USB full-speed transceiver interface
- Bus-powered capability with suspend mode
- Integrated parallel-to-serial converter (transmit) and serial-to-parallel converter (receive) for Hi-Speed USB data
- Hi-Speed USB data recovery upon receiving
- Hi-Speed USB data synchronization upon transmitting
- Integrated bit stuffing and de-stuffing for Hi-Speed USB data
- Non-Return-to-Zero Inverted (NRZI) encoding and decoding for Hi-Speed USB data
- Integrated Phase Locked Loop (PLL) oscillator using 12 MHz crystal
- Internal power-on reset
- Separate 3.3 V supplies for analog transceiver and digital I/Os minimizes crosstalk
- 3.3 V or 5 V tolerant digital input interface
- 16-bit bi-directional data bus allows FPGA verification, greatly reducing ASIC implementation risk
- Full industrial operating temperature range from –40 to +85 °C
- 6 kV in-circuit ESD protection; compliant with *IEC 61000-4-2* (level 3)
- Available in LQFP48 package.

## 3. Applications

- Scanner
- Digital still camera
- Printer, e.g.
  - Color printer
  - Multi-functional printer
- External storage device, e.g.
  - Portable hard disk
  - Zip® drive
  - Jaz® drive
  - Magneto-optical (MO) drive
  - Optical drive (CD-ROM, CD-RW, DVD).

## 4. Ordering information

**Table 1: Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| ISP1501BE | LQFP48 | plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm | SOT313-2 |

# 5. Block diagram

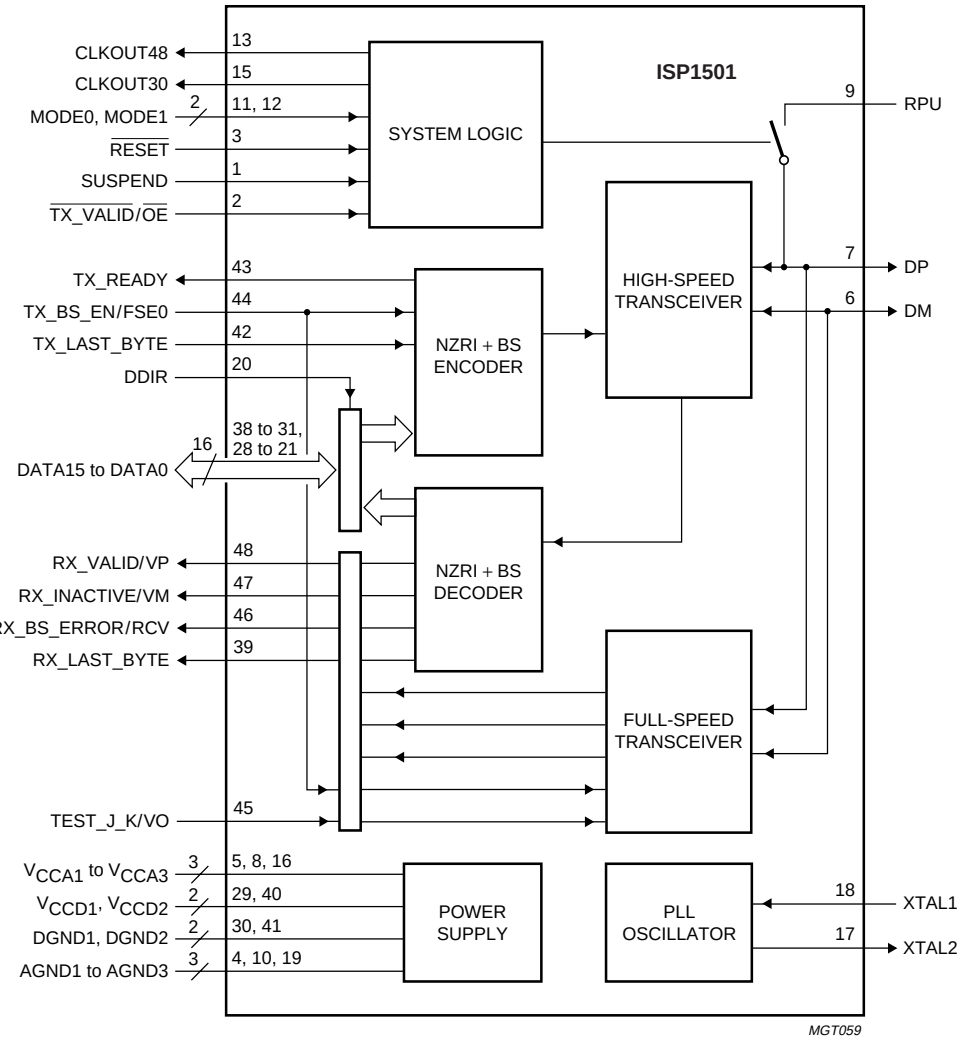



**Fig 1. Block diagram.**

# 6. Pinning information

## 6.1 Pinning

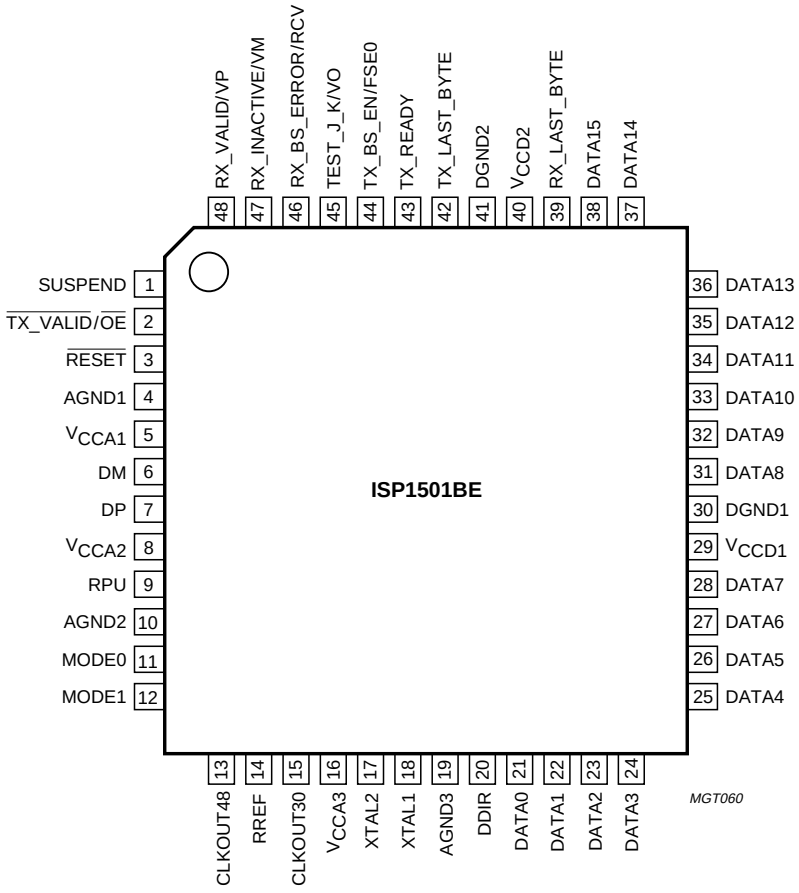



**Fig 2. Pin configuration LQFP48.**

## 6.2 Pin description

**Table 2: Pin description**

| Symbol[1] | Pin | Type | Description |
|---|---|---|---|
| SUSPEND | 1 | I | enables power saving mode for USB suspend state |
| $\overline{\text{TX\_VALID}}$/$\overline{\text{OE}}$ | 2 | I | pin function depends on operating mode (see Table 3):<br>**State = 0, 1 —** output enable for FS transceiver[2]<br>**State = 2, 3 —** transmission valid flag for HS transceiver[2] |
| $\overline{\text{RESET}}$ | 3 | I | reset input |
| AGND1 | 4 | - | analog ground 1 supply |
| $V_{CCA1}$ | 5 | - | analog supply voltage 1 (3.3 V) |
| DM | 6 | AI/O | USB D− connection (analog) with integrated 45 Ω series resistor |

**Table 2: Pin description** *...continued*

| Symbol[1] | Pin | Type | Description |
|---|---|---|---|
| DP | 7 | AI/O | USB D+ connection (analog) with integrated 45 Ω series resistor |
| $V_{CCA2}$ | 8 | - | analog supply voltage 2 (3.3 V) |
| RPU | 9 | AI | connection for external pull-up resistor (1.5 kΩ ± 5%) on USB D+; switched on via internal switch during the FS and HS chirp states |
| AGND2 | 10 | - | analog ground 2 supply |
| MODE0 | 11 | I | operating state and interface selection input 0; see Table 3 |
| MODE1 | 12 | I | operating state and interface selection input 1; see Table 3 |
| CLKOUT48 | 13 | O | 48 MHz clock output; clock is always running when input SUSPEND is logic 0; see Section 17 on application of this clock |
| RREF | 14 | AI | connection for external reference resistor (12 kΩ ± 1%) to analog ground supply |
| CLKOUT30 | 15 | O | clock output for Hi-Speed USB digital interface (30 MHz); clock is always running when input SUSPEND is logic 0 |
| $V_{CCA3}$ | 16 | - | analog supply voltage 3 (3.3 V) |
| XTAL2 | 17 | AO | crystal oscillator output (12 MHz) |
| XTAL1 | 18 | AI | crystal oscillator input (12 MHz) |
| AGND3 | 19 | - | analog ground 3 supply |
| DDIR | 20 | I | selects direction of 16-bit data bus DATA[15:0] |
| DATA0 | 21 | I/O | data bit 0; bi-directional, slew rate controlled output (5 ns) |
| DATA1 | 22 | I/O | data bit 1; bi-directional, slew rate controlled output (5 ns) |
| DATA2 | 23 | I/O | data bit 2; bi-directional, slew rate controlled output (5 ns) |
| DATA3 | 24 | I/O | data bit 3; bi-directional, slew rate controlled output (5 ns) |
| DATA4 | 25 | I/O | data bit 4; bi-directional, slew rate controlled output (5 ns) |
| DATA5 | 26 | I/O | data bit 5; bi-directional, slew rate controlled output (5 ns) |
| DATA6 | 27 | I/O | data bit 6; bi-directional, slew rate controlled output (5 ns) |
| DATA7 | 28 | I/O | data bit 7; bi-directional, slew rate controlled output (5 ns) |
| $V_{CCD1}$ | 29 | - | digital supply voltage 1 (3.3 V) |
| DGND1 | 30 | - | digital ground 1 supply |
| DATA8 | 31 | I/O | data bit 8; bi-directional, slew rate controlled output (5 ns) |
| DATA9 | 32 | I/O | data bit 9; bi-directional, slew rate controlled output (5 ns) |
| DATA10 | 33 | I/O | data bit 10; bi-directional, slew rate controlled output (5 ns) |
| DATA11 | 34 | I/O | data bit 11; bi-directional, slew rate controlled output (5 ns) |
| DATA12 | 35 | I/O | data bit 12; bi-directional, slew rate controlled output (5 ns) |
| DATA13 | 36 | I/O | data bit 13; bi-directional, slew rate controlled output (5 ns) |
| DATA14 | 37 | I/O | data bit 14; bi-directional, slew rate controlled output (5 ns) |
| DATA15 | 38 | I/O | data bit 15; bi-directional, slew rate controlled output (5 ns) |
| RX_LAST_BYTE | 39 | O | **logic 0 —** DATA[7:0] = valid data, DATA[15:8] = valid data<br>**logic 1 —** DATA[7:0] = valid data, DATA[15:8] = bit stuff error byte |
| $V_{CCD2}$ | 40 | - | digital supply voltage 2 (3.3 V) |

**Table 2: Pin description** *…continued*

| Symbol[1] | Pin | Type | Description |
|---|---|---|---|
| DGND2 | 41 | - | digital ground 2 supply |
| TX_LAST_BYTE | 42 | I | transmit last byte input; used in conjunction with TX_BS_EN to indicate different handling of the upper and lower data byte (see Table 7) |
| TX_READY | 43 | O | transmit ready output; a logic 1 means ISP1501 is ready to accept data on the next rising clock edge of CLKOUT30 |
| TX_BS_EN/FSE0 | 44 | I | pin function depends on operating state (see Table 3):<br>**State = 0, 1 —** a logic 1 forces single-ended zero (SE0) for FS transmitter<br>**State = 2, 3 —** a logic 1 enables bit stuffing for the HS transmitter |
| TEST_J_K/ VO | 45 | I | pin function depends on operating state (see Table 3):<br>**State = 0, 1 —** differential data for the FS transceiver input<br>**State = 2, 3 —** a logic 1 enables Hi-Speed USB test modes TEST_J and TEST_K; it also disables bit stuffing and NRZI for the HS receiver and transmitter |
| RX_BS_ERROR/ RCV | 46 | O | pin function depends on operating state (see Table 3):<br>**State = 0, 1 —** differential data at D+/D− receiver output<br>**State = 2, 3 —** a logic 1 signals a bit stuff error on receive data; the position of the erroneous byte is indicated by RX_LAST_BYTE |
| RX_INACTIVE/ VM | 47 | O | pin function depends on operating state (see Table 3):<br>**State = 0, 1 —** single-ended D− receiver output<br>**State = 2, 3 —** a logic 1 indicates HS line inactivity |
| RX_VALID/ VP | 48 | O | pin function depends on operating state (see Table 3):<br>**State = 0, 1 —** single-ended D+ receiver output<br>**State = 2, 3 —** valid data on falling clock edge at pin CLKOUT30 |

[1] Symbol names with an overscore (e.g. $\overline{\text{NAME}}$) indicate active LOW signals.

[2] FS: full-speed (Original USB); HS: high-speed (Hi-Speed USB).

# 7. Functional description

The ISP1501 supports both full-speed (FS) and high-speed (HS) USB physical layer for a Hi-Speed USB peripheral.

An adaptive termination circuit ensures a correct 45 Ω termination for DP and DM. Calibration is done at power-on and after any operating state change.

An internal bandgap reference circuit is used for generating the driver current and the biasing of the analog circuits. This circuit requires an external precision resistor (12 kΩ ± 1%) to analog ground.

A PLL oscillator using a 12 MHz crystal generates the internal clock of 480 MHz. From this signal, 30 MHz and 48 MHz clocks are derived for external use (available at pins CLKOUT30 and CLKOUT48, respectively).

An internal power-on-reset (POR) circuit monitors the digital supply and is used to start all circuits in the correct mode. An external reset can be applied via pin $\overline{\text{RESET}}$.

## 7.1 Full-speed (FS) transceiver

The full-speed (FS) transceiver interface is a serial interface. Access to this interface requires pins MODE1 and MODE0 to be set to either the disconnect state or the full-speed (FS) state. Bit stuffing/de-stuffing and NRZI encoding/decoding must be implemented on the external ASIC.

When pins MODE1 and MODE0 are in the disconnect or FS states, the FS transceiver is active and follows the protocol as specified in Table 5. The only difference between the disconnect and FS states is that the RPU resistor is disconnected when MODE[1:0] is in the disconnect state whereas the RPU resistor is connected to the DP line when MODE[1:0] is in the FS state.

To transmit FS USB traffic, pin $\overline{\text{OE}}$ is asserted by holding it at logic 0 (LOW) to enable the transmit driver. The USB bus will be driven to the USB bus state that corresponds to the logic conditions of FSE0 and VO. A logic 1 (HIGH) on pin FSE0 forces a USB SE0 bus state in which both the DP and DM lines are held to a voltage less than $V_{OL(max)}$ (see Table 13), regardless of VO. To force a USB J-state on the bus, FSE0 is de-asserted (set to logic 0) and VO is asserted (set to logic 1). The DP line will be held to a voltage greater than $V_{OH(min)}$ (see Table 13), and the DM line will be held to a voltage less than $V_{OL(max)}$.

To receive the FS USB traffic, the transmit driver needs to be disabled by the de-asserted pin $\overline{\text{OE}}$ by holding it at logic 1. VP and VM always reflect the state of DP and DM, respectively. An FS J-state (DP > $V_{IH(min)}$ and DM < $V_{IL(max)}$) on the USB bus will assert VP, de-assert VM and assert RCV. An FS K-state (DM > $V_{IH(min)}$ and DP < $V_{IL(max)}$) on the USB bus will de-assert VP, assert VM and de-assert RCV. An SE0 on the USB bus (DP and DM < $V_{IL(max)}$) will set VP and VM to LOW. RCV will be held in the same state as it was just before the SE0 condition occurred. In the suspend mode (SUSPND = HIGH), the differential receiver is inactive and output RCV is always LOW. Out-of-suspend ('K') signalling is detected via the single-ended receivers VP and VM. During suspend, the (D+, D-) lines are still driven to their

intended states without slew-rate control. This is permitted because driving during suspend is used to signal remote wake-up by driving a ‘K’ signal (one transition from idle to the ‘K’ state) for a period of 1 to 15 ms.

## 7.2 High-speed (HS) transceiver—transmit logic

The high-speed (HS) transceiver interface uses a 16-bit parallel bi-directional data interface. This HS module incorporates bit stuffing/de-stuffing and Non-Return-to-Zero-Inverted (NRZI) encoding/decoding logic. Access to the HS interface requires MODE[1:0] to be set to either the high-speed (HS) state or the high-speed (HS) chirp state.

When MODE[1:0] pins are in the HS or HS chirp states, the HS transceiver is active and follows the protocol as specified in Section 10.1, Section 10.2 and Section 10.3. One difference between the HS and HS chirp states is that the RPU resistor is disconnected when MODE[1:0] is in the HS state whereas the RPU resistor is connected to the DP line when MODE[1:0] is in the HS chirp state. Another difference between the HS and HS chirp state is that the 45 Ω terminations are disabled from the DP and DM lines in the HS chirp state.

The 16-bit data bus is a bi-directional bus. Pin DDIR must be set to logic 1 for clocking data into the 16-bit DATA[15:0] bus so that the payload is transmitted from the device to the host. If pin DDIR is set to logic 0, the 16-bit data bus is an output to the external ASIC. Any payload transferred from the host/hub to the transceiver is clocked out into the 16-bit data bus.

The transmit data is clocked on the rising edge of the 30 MHz clock output (CLKOUT30). All the handshake signals (TX_LAST_BYTE, TX_BS_EN and $\overline{\text{TX\_VALID}}$) are latched at the same time. These signals conform to the same set-up and hold times as specified in Section 17.1. Each set of latched data, including the 16-bit data bus and handshake signals, are qualified if $\overline{\text{TX\_VALID}}$ and TX_READY are asserted during latching. TX_READY transitions take place on the falling edge of the 30 MHz clock output.

For normal HS transmit, TEST_J_K is set to logic 0. The HS logic will process the 16-bit data with the latched TX_LAST_BYTE and TX_BS_EN signals according to Table 7, and the processed data is serially driven on the USB bus in HS signaling. When TEST_J_K is set to logic 1, the TX_BS_EN signal is ignored. The 16-bit input data will be serially driven on the bus in HS signaling with the NRZI and bit-stuffing disabled.

## 7.3 High-speed (HS) transceiver—receive logic

For receiving high-speed (HS) USB signals, the incoming differential signal from the USB cable is amplified before it is fed into a sampler circuit. In the normal receive mode, TEST_J_K is set to logic 0 and the over-sampled serial data is NRZI decoded and bit de-stuffed before being converted to 16-bit parallel words. The 16-bit data and other handshake signals (RX_BS_ERROR, RX_LAST_BYTE and RX_VALID) are latched on the falling edge of CLKOUT30 in accordance with the timings as specified in Table 18.

When TEST_J_K is set to logic 1, the sampled data from the differential amplifier will not be NRZI decoded and bit de-stuffed. All serial HS USB signals are passed-through and converted to 16-bit data on the parallel data bus. The handshake signals (RX_BS_ERROR, RX_LAST_BYTE and RX_VALID) are invalid.

### 7.4 High-speed (HS) transceiver—periphery circuit

To maintain a constant current driver for high-speed (HS) transmit and biasing of other analog circuits, an internal bandgap reference circuit and RREF resistor are used to form the reference current. This circuit requires an external precision resistor (12 kΩ ± 1%) from pin RF to the analog ground. A pull-up resistor of 1.5 kΩ ± 5% must be connected between pin RPU and $V_{CCA3}$. A 12 MHz crystal with an accuracy of less than ±500 ppm must be used between pins XTAL1 and XTAL2. Alternatively, an input clock (3.3 V, 12 MHz clock ±500 ppm, duty cycle between 40 and 60%) can also be used to drive pin XTAL1 (pin XTAL2 is left open).

## 8. Operating states

### 8.1 Interface and state selection

The MODE1 and MODE0 pins control the operating states of the ISP1501 and select the appropriate function of multiplexed pins (see Table 3).

**Table 3: Interface selection**

| MODE[1:0] | State | State name | Pin | Function |
|---|---|---|---|---|
| 00 | 0 | Disconnect | 2 | $\overline{OE}$ |
| | | | 44 | FSE0 |
| | | | 45 | VO |
| | | | 46 | RCV |
| | | | 47 | VM |
| | | | 48 | VP |
| 01 | 1 | Full-speed (FS) | 2 | $\overline{OE}$ |
| | | | 44 | FSE0 |
| | | | 45 | VO |
| | | | 46 | RCV |
| | | | 47 | VM |
| | | | 48 | VP |
| 10 | 2 | High-speed (HS) | 2 | $\overline{TX\_VALID}$ |
| | | | 44 | TX_BS_EN |
| | | | 45 | TEST_J_K |
| | | | 46 | RX_BS_ERROR |
| | | | 47 | RX_INACTIVE |
| | | | 48 | RX_VALID |

**Table 3: Interface selection** *...continued*

| MODE[1:0] | State | State name | Pin | Function |
|---|---|---|---|---|
| 11 | 3 | High-speed (HS) chirp | 2 | $\overline{\text{TX\_VALID}}$ |
| | | | 44 | TX_BS_EN |
| | | | 45 | TEST_J_K |
| | | | 46 | RX_BS_ERROR |
| | | | 47 | RX_INACTIVE |
| | | | 48 | RX_VALID |

## 8.2 State transitions

A Hi-Speed USB peripheral handles more than one electrical state under the USB specification. The ISP1501 accommodates the various states through the MODE[1:0] input pins. Table 4 summarizes the operating states.

**Table 4: Operating states**

| State | State name | Description |
|---|---|---|
| 0 | Disconnect | Legacy (full-speed) SIE interface; FS transceiver enabled; pull-up resistor on pin RPU disconnected |
| 1 | Full-speed (FS) | Legacy (full-speed) SIE interface; FS transceiver enabled; full-speed slew rate selected; pull-up resistor on pin RPU connected to pin DP |
| 2 | High-speed (HS) | High-speed SIE interface; HS transceiver enabled; FS transceiver on permanent SE0 to provide 45 Ω termination; pull-up resistor on pin RPU disconnected |
| 3 | High-speed (HS) chirp | High-speed SIE interface; HS transceiver enabled; FS transceiver disabled; pull-up resistor on pin RPU connected to pin DP |

### 8.2.1 Disconnect state

In the disconnect state (MODE[1:0] = 00), an external pull-up resistor on pin RPU is not connected to the DP line. The FS transceiver is enabled, and the legacy (Original USB) SIE interface is active (see Figure 3).

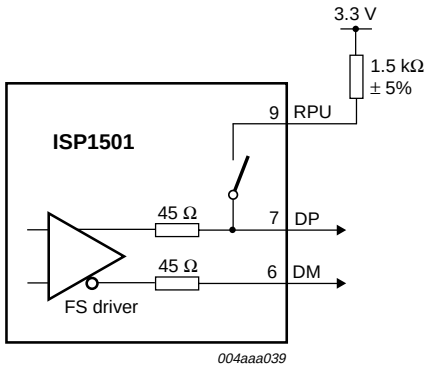



**Fig 3. Disconnect state.**

### 8.2.2 Full-speed (FS) state

In the full-speed (FS) state (MODE[1:0] = 01), an external pull-up resistor of 1.5 kΩ ± 5% is required on the DP line. This is implemented via the RPU resistor. The RPU resistor is internally connected to the DP line. The FS transceiver is enabled, and the legacy (Original USB) SIE interface is active (see Figure 4).

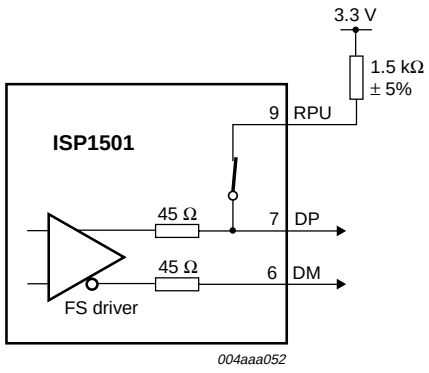



**Fig 4. Full-speed state.**

### 8.2.3 High-speed (HS) state

In the high-speed (HS) state, internal 45 Ω resistors on the DP and DM lines are connected to the ground. The pull-up resistor is disconnected. The HS transceiver is enabled, and the parallel interface and the HS-handshake signals are used (see Figure 5).

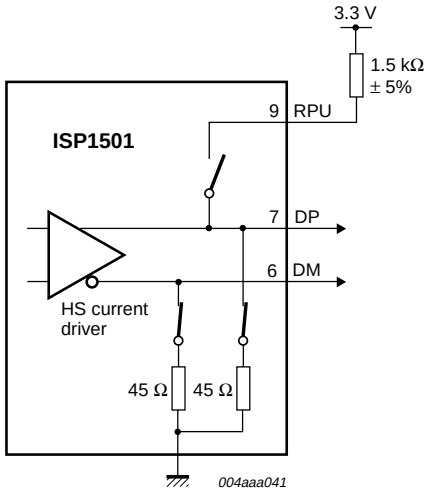



**Fig 5. High-speed state.**

### 8.2.4 High-speed (HS) chirp state

In the high-speed (HS) chirp state, 45 Ω terminations are disabled from the DP and DM lines. The pull-up resistor is connected on the DP line. The HS transceiver is enabled, and the parallel interface and HS handshake signals are in use (see Figure 6).

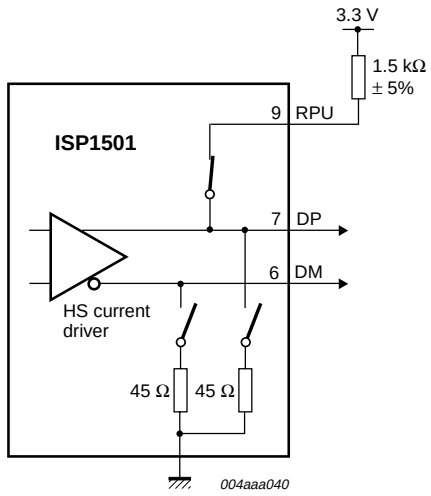
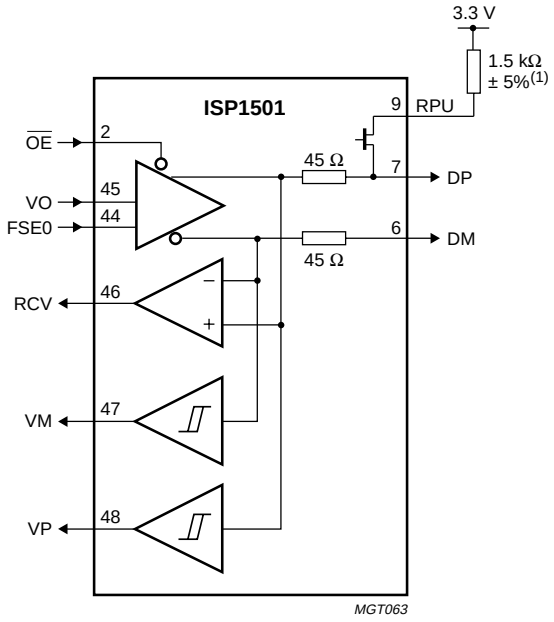



**Fig 6. High-speed chirp state.**

## 8.3 Reset

The output clocks are affected by pin $\overline{\text{RESET}}$ and may show a momentary change at $\overline{\text{RESET}}$. The ASIC may not transmit or receive data while the ISP1510 $\overline{\text{RESET}}$ is driven LOW.

# 9. Full-speed functionality




(1) Connected in FS state and HS chirp state.

**Fig 7. Full-speed transceiver functional diagram**

**Table 5: Full-speed driving function**

*$\overline{OE}$ = logic 0*

| FSE0 | VO | VP | VM | Differential data (DP, DM) |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | full-speed K state |
| 0 | 1 | 1 | 0 | full-speed J state |
| 1 | 0 | 0 | 0 | SE0 |
| 1 | 1 | 0 | 0 | SE0 |

**Table 6: Full-speed receiving function**

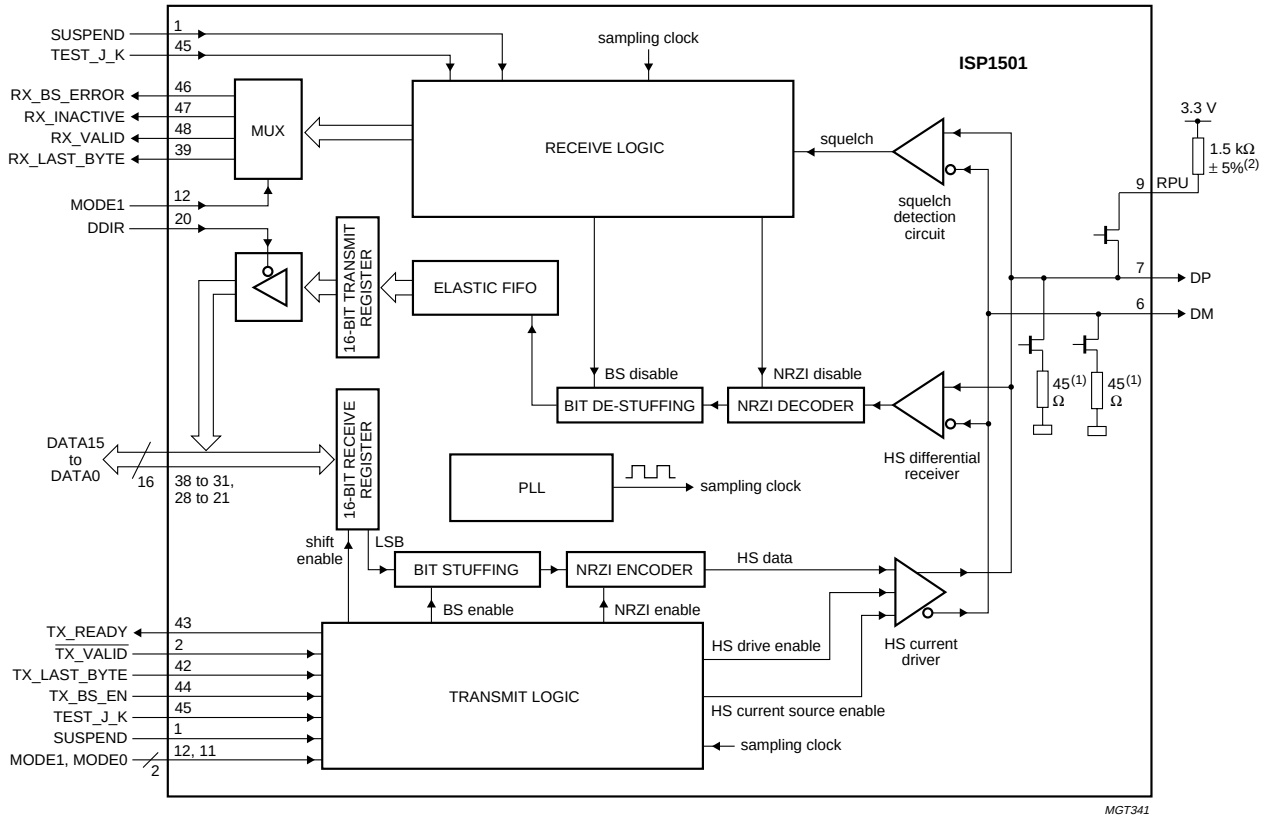
*$\overline{OE}$ = logic 1*

| Differential input | Single-ended input | | VP | VM | RCV[1] |
|---|---|---|---|---|---|
| $\Delta V = V_{DP} - V_{DM}$ | $V_{DP}$ | $V_{DM}$ | | | |
| $\Delta V$ > 200 mV | >2 V | <0.8 V | 1 | 0 | 1 |
| $\Delta V$ < –200 mV | <0.8 V | >2 V | 0 | 1 | 0 |
| $\lvert\Delta V\rvert$ < 200 mV | <0.8 V | <0.8 V | 0 | 0 | RCV*[2] |

[1] When a logic 1 is applied at input SUSPEND, output RCV is always made logic 0.

[2] RCV* denotes the signal level on output RCV just before the SE0 state occurs. This level is kept stable during the SE0 period.

# 10. High-speed functionality




(1) Implemented as part of the FS transceiver.

(2) Connected in FS state and HS chirp state.

**Fig 8. High-speed transceiver functional diagram.**

## 10.1 High-speed transmit

The ISP1501 must be set in high-speed state by setting MODE[1:0] = 02H. High-speed data propagate to the DP and DM pins when the 16-bit input data bus is driven. Driving pin DDIR to logic 1 switches the 16-bit data bus to input mode.

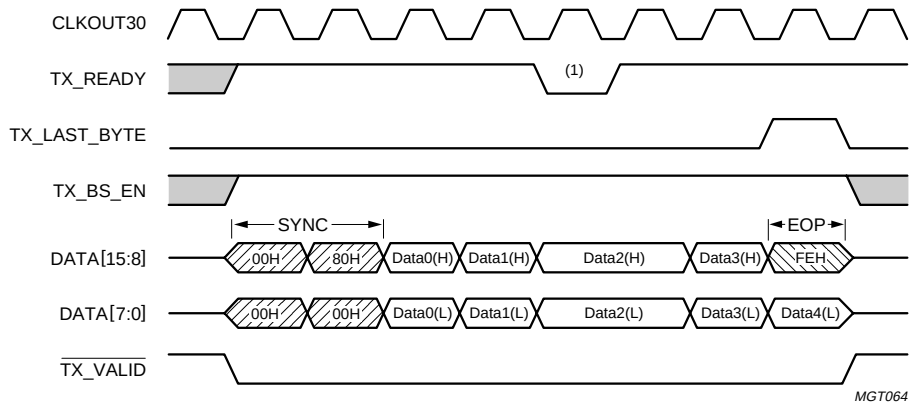
All data packets start with a 4-byte SYNC pattern and end with either a 1-byte or a 5-byte EOP (End of Packet). The SYNC pattern is a 32-bit pattern of KJKJKJKJ KJKJKJKJ KJKJKJKJ KJKJKJKK, which is to be sent by the SIE as 0000H, 8000H to the input. For a 1-byte EOP the HS pattern is generated with FEH. The 5-byte EOP starts with FEH, followed by four bytes of FFH.

**Remark:** All 16-bit data are sent LSB first.

When bit stuffing or the EOP finishes on an 8-bit boundary, the TX_BS_EN and TX_LAST_BYTE determine the behavior of the ISP1501 is shown in Table 7.

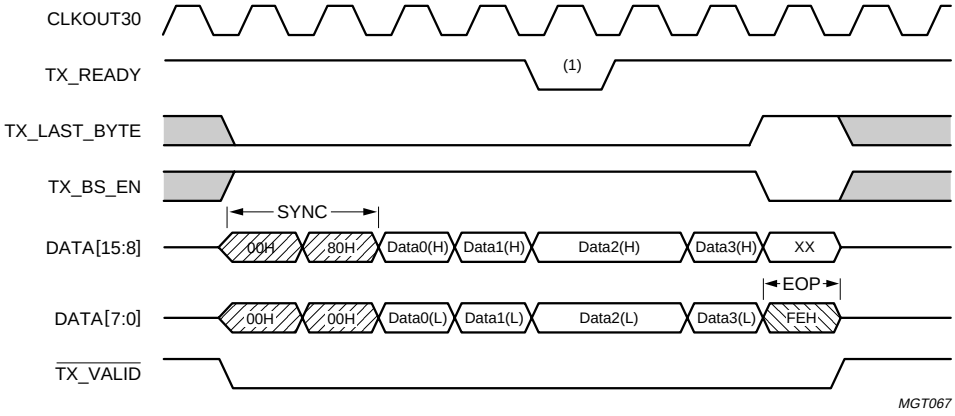
**Table 7: High-speed transmit conditions**

| TX_LAST_BYTE | TX_BS_EN | Condition |
|---|---|---|
| 0 | 0 | high and low bytes are both sent without bit stuffing |
| 0 | 1 | high and low bytes are both sent with bit stuffing |
| 1 | 0 | low byte is sent without bit stuffing; high byte is ignored |
| 1 | 1 | low byte is sent with bit stuffing; high byte without bit stuffing |



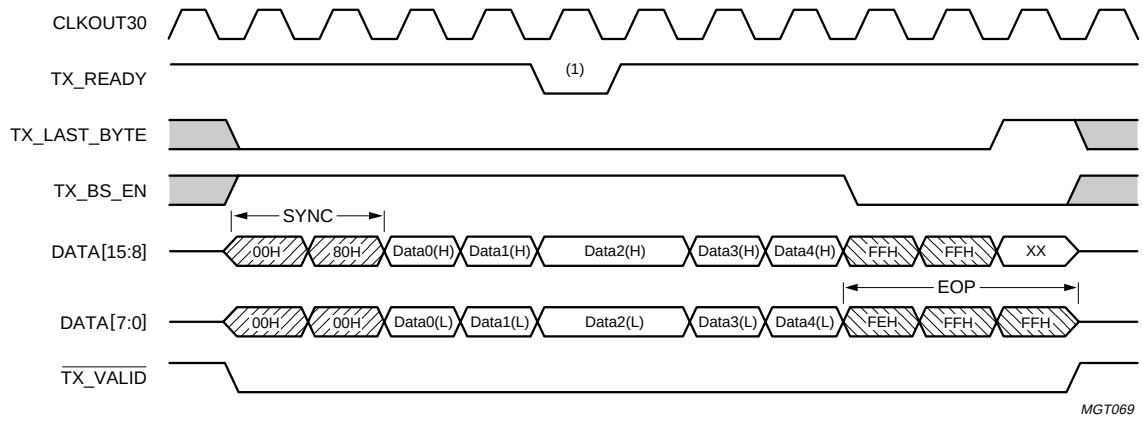

(1) TX_READY is only de-asserted during a transmission if the internal FIFO is full.

**Fig 9. HS transmit; single-byte EOP ending on 16-bit boundary.**



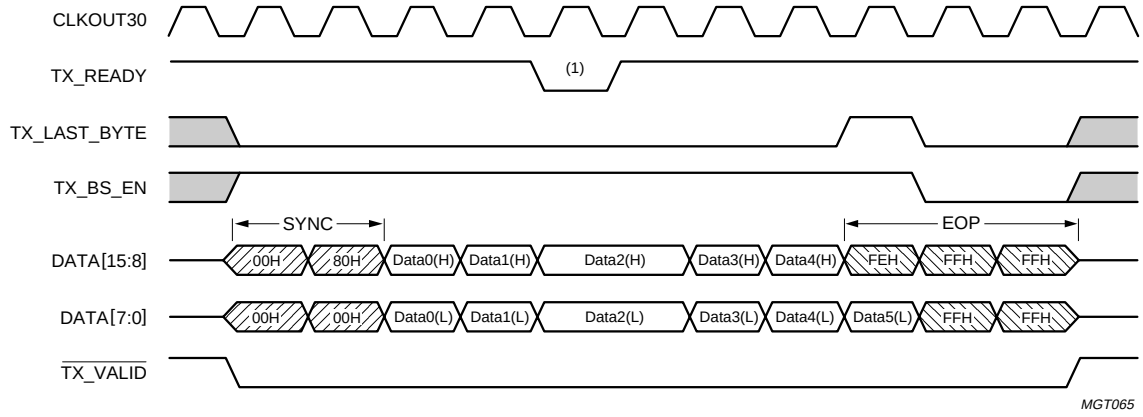

(1) TX_READY is only de-asserted during a transmission if the internal FIFO is full.

**Fig 10. HS transmit; single-byte EOP ending on 8-bit boundary.**




(1) TX_READY is only de-asserted during a transmission if the internal FIFO is full.

**Fig 11. HS transmit; 5-byte EOP ending on 8-bit boundary.**




(1) TX_READY is only de-asserted during a transmission if the internal FIFO is full.

**Fig 12. HS transmit; 5-byte EOP ending on 16-bit boundary**

## 10.2 High-speed receive

When ISP1501 is in high-speed state (MODE[1:0] = 02H), setting input DDIR to logic 0 allows the HS receiver to output data to the external 16-bit bus. As the length of the incoming EOP is not fixed, RX_LAST_BYTE and RX_BS_ERROR are encoded to differentiate between EOP arriving on an 8-bit or a 16-bit boundary. RX_VALID qualifies the data part of USB high-speed traffic. The SYNC pattern bytes are removed.

If the EOP arrives on the high byte, RX_VALID will qualify it, and RX_LAST_BYTE will be asserted. With these, the SIE will know that an EOP has occurred and can start deciphering the received packet.

If the EOP arrives on the low byte, RX_VALID goes LOW at the start of the EOP cycle. RX_BS_ERROR must be polled to determine whether an EOP has occurred.

**Table 8: High-speed receive conditions**

| RX_LAST_BYTE | RX_BS_ERROR | Condition |
|---|---|---|
| 0 | 0 | valid data on the high and low bytes; no bit stuff error |
| 0[1] | 1[1] | EOP on the low byte |
| 1 | 0 | EOP on the high byte; valid data on the low byte |
| 1 | 1 | illegal |

[1] This condition is only valid in the cycle immediately after pin RX_VALID goes LOW.

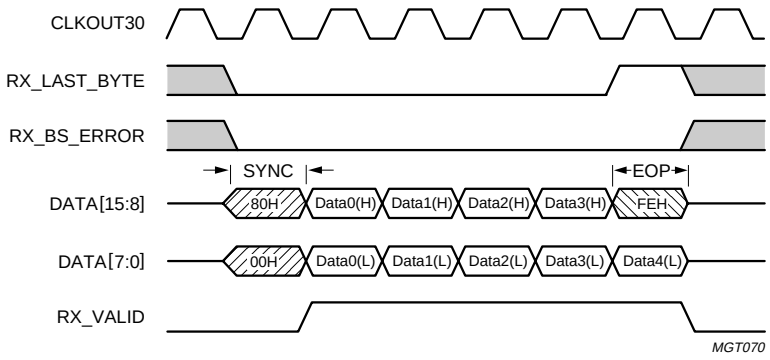



**Fig 13. HS receive timing; single-byte EOP starting on the high byte.**

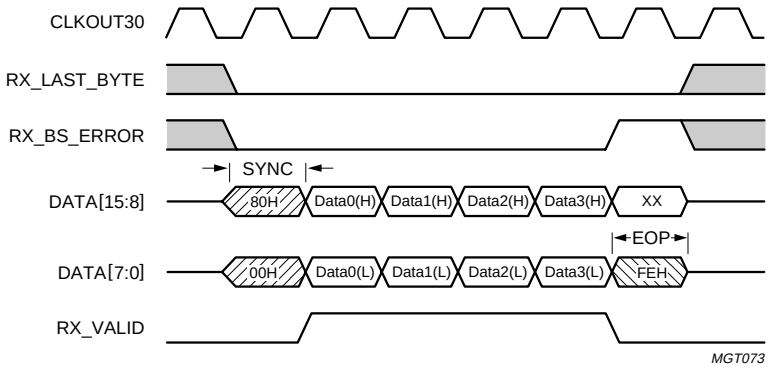



**Fig 14. HS receive timing; single-byte EOP starting on the low byte.**

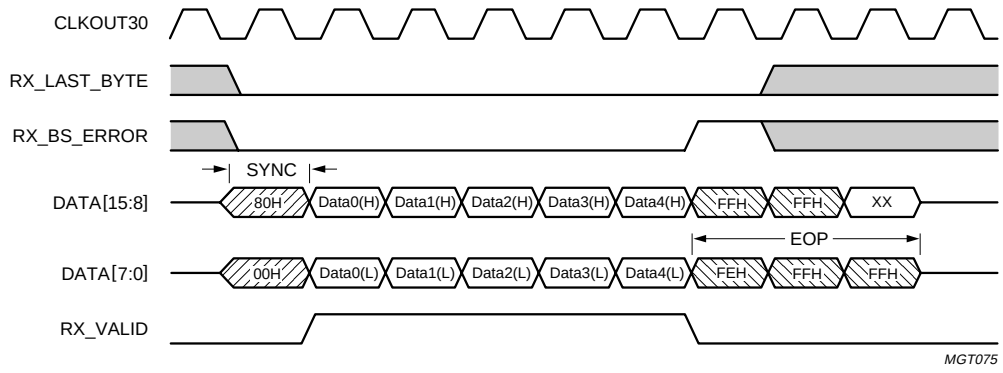



**Fig 15. HS receive timing; 5-bytes EOP starting on the low byte.**

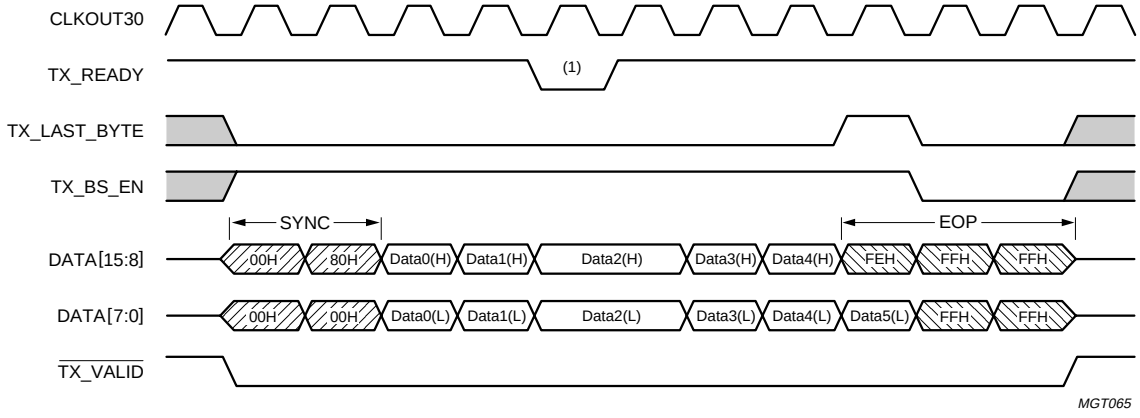


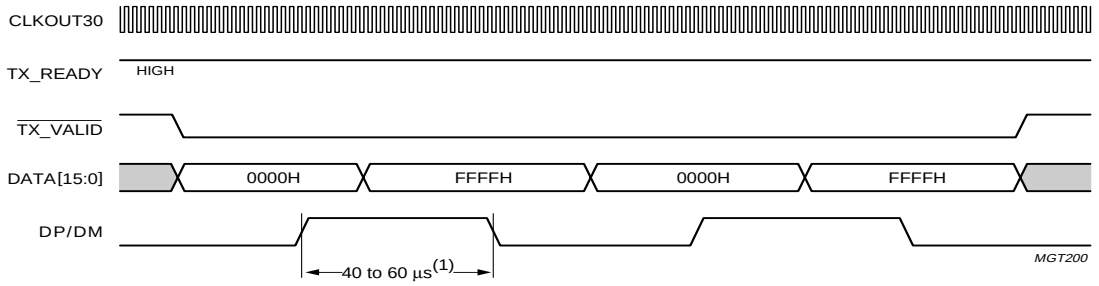

**Fig 16. HS receive timing; 5-bytes EOP starting on the high byte.**

The SYNC pattern will not appear on the data bus as an RX_VALID qualified data. The received SYNC value may differ from the expected 8000H.

The raw data is byte-aligned to the 16-bit data bus.

## 10.3 High-speed chirp

When the transceiver is configured to high-speed chirp state (MODE[1:0] = 03H), the internal termination resistors on DP and DM are deactivated (no SE0 is applied by the FS transceiver). Pin DP is connected to the pull-up resistor on pin RPU. No bit stuffing or NRZI encoding is performed on the data, regardless of the state of pin TX_BS_EN. The data is transmitted as soon as both $\overline{\text{TX\_VALID}}$ and TX_READY are asserted (see Figure 17).




(1) Time interval controlled by the SIE.

**Fig 17. HS chirp transmit timing.**

For HS chirp reception, the 16-bit data bus is in the bypass mode.

In the HS chirp mode, the receiver behaves like a simple serial to parallel converter. The transition on DP and DM may be mapped to anywhere within the 16-bit word boundary. Therefore, the output may not contain all 0s or 1s for one cycle. The SIE samples the 16-bit parallel data to check for the presence of extended JKJK states. RX_BS_ERROR no longer reflects a bit stuff error. The RX_VALID signal is used to qualify the data. The RX_INACTIVE signal is used in the HS chirp receive state.

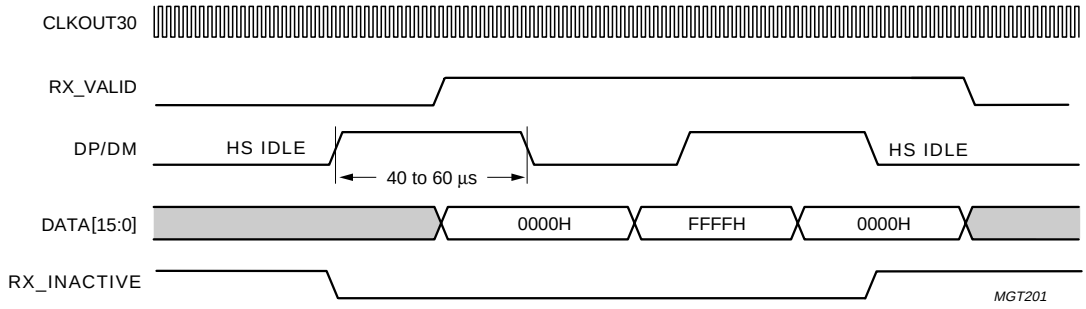



**Fig 18. HS chirp receive timing.**

## 10.4 High-speed transmit path delay

The total transmit path maximum delay is 8 HS bit times at 480 MHz.

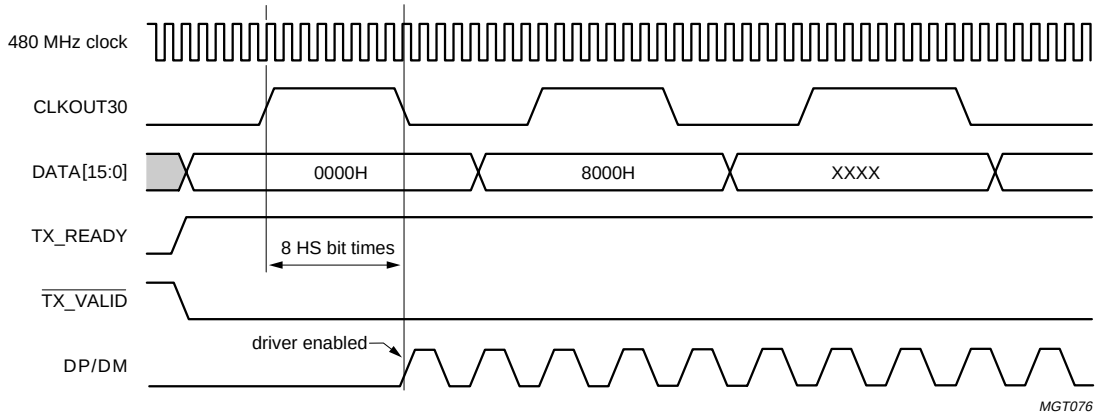



**Fig 19. HS transmit path delay.**

## 10.5 High-speed receive path delay

In the HS receive mode, the SYNC pattern is removed. As the preceding SYNC pattern may be trimmed, the delay from the appearance of the first bit of the SYNC pattern to the first valid data word on the DATA[15:0] bus is described here (see Figure 20, $t_A$ $t_B$ and $t_C$). The receive path delay is between 106 to 122 HS bit times.

However, to have an accurate measure of the bus turn-around time, the receive path delay is measured from the data on the DP and DM pins to the actual equivalent data on the 16-bit data bus (see Figure 20, $t_B$ and $t_C$).

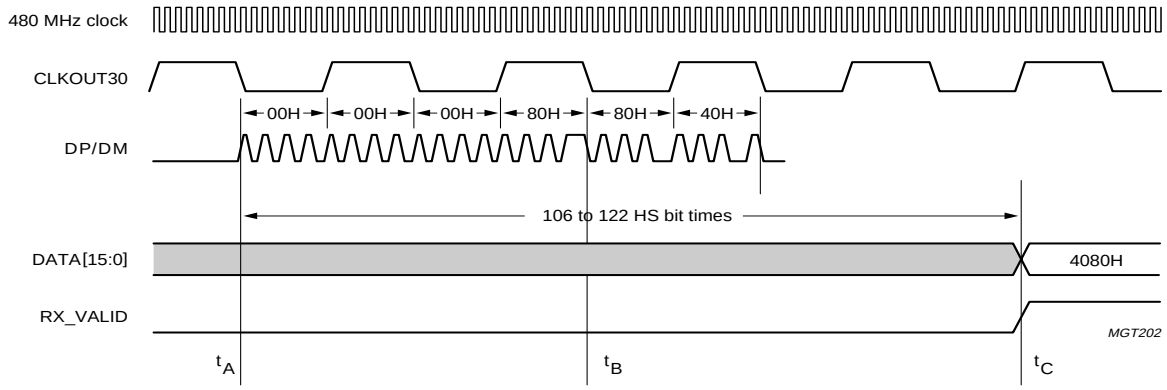



**Fig 20. HS receive path delay.**

# 11. Clocking

The CLKOUT30 and CLKOUT48 pins are free running clocks at 30 MHz and 48 MHz, respectively.

## 11.1 Power-up behavior

Both output clocks (CLKOUT30 and CLKOUT48) are held LOW (logic 0) at power-up for a period of up to 8192 oscillator cycles before they are enabled.

The time during which these output clocks are blocked depends on the start-up time of the external crystal. A total of 8192 oscillator clock ticks must be counted before enabling the output clocks. Therefore, the minimum timing from power-up to the time when CLKOUT30 and CLKOUT48 are available is 8192 x 83 ns = 680 µs.

## 11.2 Suspend behavior

When SUSPEND is driven from logic 0 to logic 1, output clocks will stop toggling because the internal PLL and the external crystal will also enter a power-down state. The clocks CLKOUT30 and CLKOUT48 can stop at either logic 0 or logic 1.

When SUSPEND is driven from logic 1 to logic 0, the external crystal and the PLL will start again. However, there is no blocking of output clocks. CLKOUT30 and CLKOUT48 may drift slightly from 30 MHz and 48 MHz, respectively until the PLL locks up.

## 11.3 Reset behavior

A pin reset will force the digital circuit that generates 30 MHz and 48 MHz from the HS PLL (480 MHz) to the initial state. Therefore, the output clock at 30 MHz and 48 MHz will be aligned after pin $\overline{\text{RESET}}$ is driven from logic 1 to logic 0 (falling edge). During that one instance, the alignment causes the clock period to change.

# 12. Termination calibration

The on-chip termination is calibrated after power-up and mode change to provide 45 Ω ± 10% termination resistance. The ISP1501 must not transmit or receive data during calibration.

## 12.1 Power-up behavior

This internal termination calibration occurs 21600 oscillator cycles after power-up. Similar to the clock blocking mechanism, the exact timing depends on the external crystal startup time. Therefore, the minimum timing from power-up to power-up termination calibration is 21600 x 83 ns = 1.8 ms.

## 12.2 Suspend behavior

Pin SUSPEND does not cause any termination calibration.

## 12.3 Reset behavior

Pin $\overline{\text{RESET}}$ does not cause any termination calibration.

## 12.4 Mode change behavior

A termination calibration occurs 4 μs after a mode change and lasts for 2 μs. RX_INACTIVE is asserted to facilitate calibration during this 2 μs period.

# 13. Limiting values

**Table 9: Absolute maximum ratings**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCA}$ | analog supply voltage | | –0.5 | +6.0 | V |
| $V_{CCD}$ | digital supply voltage | | –0.5 | +4.6 | V |
| $V_I$ | input voltage | | –0.5 | +6.0 | V |
| $I_{lu}$ | latch-up current | $-1.8\ V < V_I < +5.4\ V$ | - | 100 | mA |
| $V_{esd}$ | electrostatic discharge voltage[1] | $I_{LI} < 1\ \mu A$ | | | |
| | | pins DP, DM and ground pins | –4000 | +4000 | V |
| | | other pins | –2000 | +2000 | V |
| $T_{stg}$ | storage temperature | | –40 | +125 | °C |

[1] Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ resistor (Human Body Model).

# 14. Recommended operating conditions

**Table 10: Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CCA}$ | analog supply voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_{CCD}$ | digital supply voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_I$ | input voltage | | 0 | - | $V_{CCD}$ | V |
| $V_{I(AI/O)}$ | input voltage on analog I/O pins DP and DM | | 0 | - | 3.6 | V |
| $T_{amb}$ | ambient temperature | | –40 | - | +85 | °C |

# 15. Static characteristics

**Table 11: Static characteristics: supply pins**

*$V_{CCA} = V_{CCD} = 3.0$ to 3.6 V; $V_{AGND} = V_{DGND} = 0$ V; $T_{amb} = -40$ to $+85$ °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{CC}$ | operating supply current | full-speed transmitting and receiving at 12 MHz; 50 pF load on pins DP and DM | - | 25 | - | mA |
| | | high-speed receiving at 480 MHz | - | 60 | - | mA |
| | | high-speed transmitting at 480 MHz | - | 75 | - | mA |
| $I_{CC(susp)}$ | suspend supply current | in suspend mode with resistor on pin RPU disconnected | - | 100 | - | µA |

**Table 12: Static characteristics: digital pins**

*$V_{CCA}$ = $V_{CCD}$ = 3.0 to 3.6 V; $V_{AGND}$ = $V_{DGND}$ = 0 V; $T_{amb}$ = −40 to +85 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Input levels** | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | - | - | 0.8 | V |
| $V_{IH}$ | HIGH-level input voltage | | 2.0 | - | - | V |
| **Output levels** | | | | | | |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 100 µA | - | - | 0.15 | V |
| | | $I_{OL}$ = 4 mA | - | - | 0.4 | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH}$ = 100 µA | $V_{CCD}$ − 0.4 | - | - | V |
| | | $I_{OH}$ = 4 mA | $V_{CCD}$ − 0.4 | - | - | V |
| **Leakage current** | | | | | | |
| $I_{LI}$ | input leakage current | | - | - | ±1 | µA |

**Table 13: Static characteristics: analog I/O pins DP and DM)**

*$V_{CCA}$ = $V_{CCD}$ = 3.0 to 3.6 V; $V_{AGND}$ = $V_{DGND}$ = 0 V; $T_{amb}$ = −40 to +85 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Original USB transceiver (FS)** | | | | | | |
| Input levels (differential receiver) | | | | | | |
| $V_{DI}$ | differential input sensitivity | $\|V_{I(DP)} - V_{I(DM)}\|$ | 0.2 | - | - | V |
| $V_{CM}$ | differential common mode voltage | includes $V_{DI}$ range | 0.8 | - | 2.5 | V |
| Input levels (single-ended receivers) | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | - | - | 0.8 | V |
| $V_{IH}$ | HIGH-level input voltage | | 2.0 | - | - | V |
| $V_{hys}$ | hysteresis voltage | | 0.4 | - | 0.7 | V |
| Output levels | | | | | | |
| $V_{OL}$ | LOW-level output voltage | pull-up on DP; $R_L$ = 1.5 kΩ to + 3.6 V | 0 | - | 0.3 | V |
| $V_{OH}$ | HIGH-level output voltage | pull-down on DP, DM; $R_L$ = 15 kΩ to GND | 2.8 | - | 3.6 | V |
| **Hi-Speed USB transceiver (HS)** | | | | | | |
| Input levels (differential receiver) | | | | | | |
| $V_{HSSQ}$ | high-speed squelch detection threshold (differential) | squelch detected | - | - | 100 | mV |
| | | no squelch detected | 150 | - | - | mV |
| $V_{HSDSC}$ | high-speed disconnect detection threshold (differential) | disconnect detected | 625 | - | - | mV |
| | | disconnect not detected | - | - | 525 | mV |
| $V_{HSDI}$ | high-speed differential input sensitivity | $\|V_{I(DP)} - V_{I(DM)}\|$ | 300 | - | - | mV |
| $V_{HSCM}$ | high-speed data signaling common mode voltage range | | −50 | - | +500 | mV |
| Output levels | | | | | | |
| $V_{HSOI}$ | high-speed idle level output voltage (differential) | | −10 | - | +10 | mV |
| $V_{HSOL}$ | high-speed LOW-level output voltage (differential) | | −10 | - | +10 | mV |

**Table 13: Static characteristics: analog I/O pins DP and DM)** *...continued*

*$V_{CCA}$ = $V_{CCD}$ = 3.0 to 3.6 V; $V_{AGND}$ = $V_{DGND}$ = 0 V; $T_{amb}$ = −40 to +85 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{HSOH}$ | high-speed HIGH-level output voltage (differential) | | | 360 | - | 440 | mV |
| $V_{CHIRPJ}$ | chirp-J output voltage (differential) | | [1] | 700 | - | 1100 | mV |
| $V_{CHIRPK}$ | chirp-K output voltage (differential) | | [1] | −900 | - | −500 | mV |
| **Leakage current** | | | | | | | |
| $I_{LZ}$ | OFF-state leakage current | | | - | - | ±1 | µA |
| **Capacitance** | | | | | | | |
| $C_{IN}$ | transceiver capacitance | pin to GND | | - | - | 20 | pF |
| **Resistance** | | | | | | | |
| $Z_{DRV2}$ | driver output impedance for Hi-Speed USB and Original USB | steady-state drive | [2] | 40.5 | 45 | 49.5 | Ω |
| $Z_{INP}$ | input impedance | | | 10 | - | - | MΩ |
| **Termination** | | | | | | | |
| $V_{TERM}$ | termination voltage for pull-up resistor on pin RPU | | [3] | 3.0 | - | 3.6 | V |

[1] HS termination resistor disabled, pull-up resistor connected. Only during reset, when both hub and device are high-speed capable.

[2] Includes internal matching resistors on both pins DP and DM. This tolerance range complies to Hi-Speed USB.

[3] In suspend mode the minimum voltage is 2.7 V.

# 16. Dynamic characteristics

**Table 14: Dynamic characteristics: analog I/O pins (DP/DM)**

*$V_{CCA}$ = $V_{CCD}$ = 3.0 to 3.6 V; $V_{AGND}$ = $V_{DGND}$ = 0 V; $T_{amb}$ = −40 to +85 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Driver characteristics** | | | | | | |
| Full-speed mode | | | | | | |
| $t_{FR}$ | rise time | $C_L$ = 50 pF; 10% to 90% of $\|V_{OH} - V_{OL}\|$; see Figure 21 | 4 | - | 20 | ns |
| $t_{FF}$ | fall time | $C_L$ = 50 pF; 90% to 10% of $\|V_{OH} - V_{OL}\|$; see Figure 21 | 4 | - | 20 | ns |
| FRFM | differential rise/fall time matching ($t_{FR}/t_{FF}$) | excluding the first transition from Idle state | 90 | - | 111.1 | % |
| $V_{CRS}$ | output signal crossover voltage | excluding the first transition from Idle state; see Figure 22 | 1.3 | - | 2.0 | V |
| High-speed mode | | | | | | |
| $t_{HSR}$ | high-speed differential rise time | | 500 | - | - | ps |
| $t_{HSF}$ | high-speed differential fall time | | 500 | - | - | ps |
| **Driver timing** | | | | | | |
| Full-speed mode | | | | | | |
| $t_{PLH(drv)}$ | driver propagation delay (VO, FSE0 to DP, DM) | LOW-to-HIGH; see Figure 24 | - | - | 15 | ns |
| $t_{PHL(drv)}$ | | HIGH-to-LOW; see Figure 24 | - | - | 15 | ns |

**Table 14: Dynamic characteristics: analog I/O pins (DP/DM)** *...continued*

*$V_{CCA}$ = $V_{CCD}$ = 3.0 to 3.6 V; $V_{AGND}$ = $V_{DGND}$ = 0 V; $T_{amb}$ = −40 to +85 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{PHZ}$ | driver disable delay ($\overline{OE}$ to DP, DM) | HIGH-to-OFF; see Figure 22 | - | - | 10 | ns |
| $t_{PLZ}$ | | LOW-to-OFF; see Figure 22 | - | - | 10 | ns |
| $t_{PZH}$ | driver enable delay ($\overline{OE}$ to DP, DM) | OFF-to-HIGH; see Figure 22 | - | - | 15 | ns |
| $t_{PZL}$ | | OFF-to-LOW; see Figure 22 | - | - | 15 | ns |
| High-speed mode (Template 1, *Universal Serial Bus Specification Rev. 2.0*) | | | | | | |
| - | driver waveform requirements | eye pattern of Template 1; see Figure 26 and Table 15 [1] | | | | |
| **Receiver timing full-speed mode** | | | | | | |
| Differential receiver | | | | | | |
| $t_{PLH(rcv)}$ | receiver propagation delay (DP, DM to RCV) | LOW-to-HIGH; see Figure 23 | - | - | 15 | ns |
| $t_{PHL(rcv)}$ | | HIGH-to-LOW; see Figure 23 | - | - | 15 | ns |
| Single-ended receiver | | | | | | |
| $t_{PLH(se)}$ | single-ended propagation delay (DP, DM to VP, VM) | LOW-to-HIGH; see Figure 23 | - | - | 15 | ns |
| $t_{PHL(se)}$ | | HIGH-to-LOW; see Figure 23 | - | - | 15 | ns |
| **Receiver timing high-speed mode** | | | | | | |
| Template 4, *Universal Serial Bus Specification Rev. 2.0* | | | | | | |
| - | data source jitter and receiver jitter tolerance | eye pattern of Template 4; see Figure 27 and Table 16 [1] | | | | |

[1] Characterized only, not tested in production. Limits guaranteed by design.

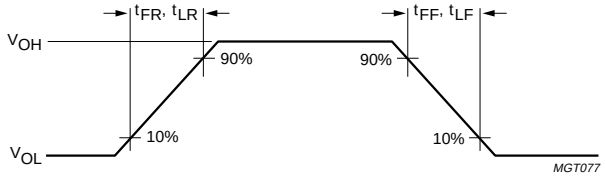



**Fig 21. Rise and fall times (FS and LS mode).**

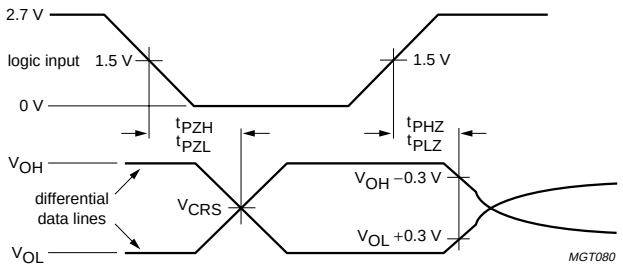



**Fig 22. Timing of $\overline{OE}$ to DP, DM.**

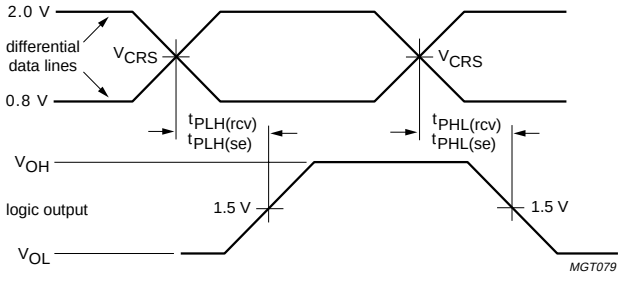



**Fig 23. Timing of DP, DM to RCV, VP, VM.**

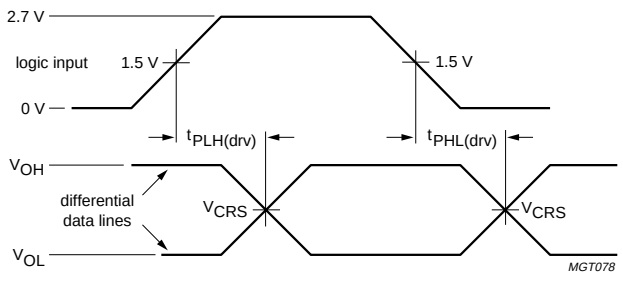



**Fig 24. Timing of VO, FSE0 to DP, DM.**

## 16.1 High-speed signals

High-speed USB signals are characterized using eye patterns. For measuring the eye patterns 4 test points have been defined (see Figure 25). The *Universal Serial Bus Specification Rev. 2.0* defines the eye patterns in several 'templates'. For ISP1501 only Templates 1 and 4 are relevant.

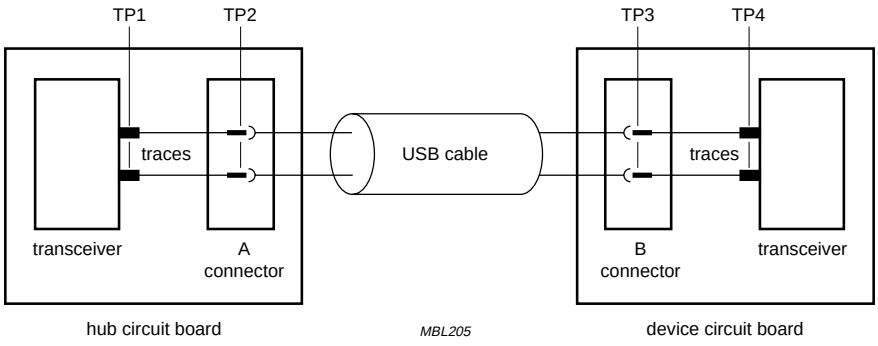



**Fig 25. Eye pattern measurement planes.**

### 16.1.1 Template 1 (transmit waveform)

The eye pattern in Figure 26 defines the transmit waveform requirements for a hub (measured at TP2) or a device without a captive cable (measured at TP3).
**Remark:** Captive cables have a vendor-specific connector to the peripheral (hardwired or detachable) and a USB "A" connector on the other side. For hot plugging, the vendor-specific connector must meet the same performance requirements as a USB "B" connector.
The corresponding signal levels and timings are given in Table 15. Timings are given as a percentage of the unit interval (UI), which represents the nominal bit duration $T_{PERIOD}$ for a 480 Mbit/s transmission rate.

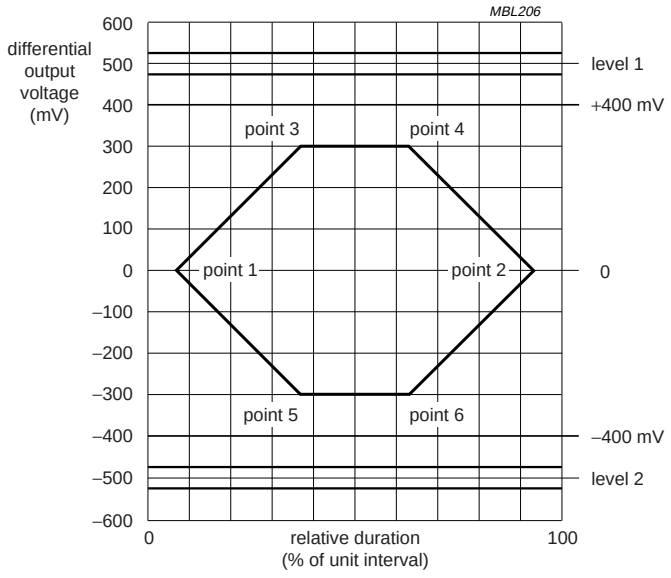



**Fig 26. Template 1 eye pattern (transmit waveform).**

**Table 15: Template 1 eye pattern definition**

| Name | Differential voltage on pins DP and DM (mV) | Relative duration (% of unit interval) |
|---|---|---|
| Level 1 | +525[1]<br>+475[2] | n.a. |
| Level 2 | –525[1]<br>–475[2] | n.a. |
| Point 1 | 0 | 7.5 |
| Point 2 | 0 | 92.5 |
| Point 3 | +300 | 37.5 |
| Point 4 | +300 | 62.5 |
| Point 5 | –300 | 37.5 |
| Point 6 | –300 | 62.5 |

[1] In the unit interval following a transition.

[2] In all other cases.

### 16.1.2 Template 4 (receive waveform)

The eye pattern defined in Table 16 defines the receiver sensitivity requirements for a hub (signal applied at test point TP2) or a device without a captive cable (signal applied at test point TP3). The corresponding signal levels and timings are given in Table 16. Timings are given as a percentage of the unit interval (UI), which represents the nominal bit duration $T_{PERIOD}$ for a 480 Mbit/s transmission rate.

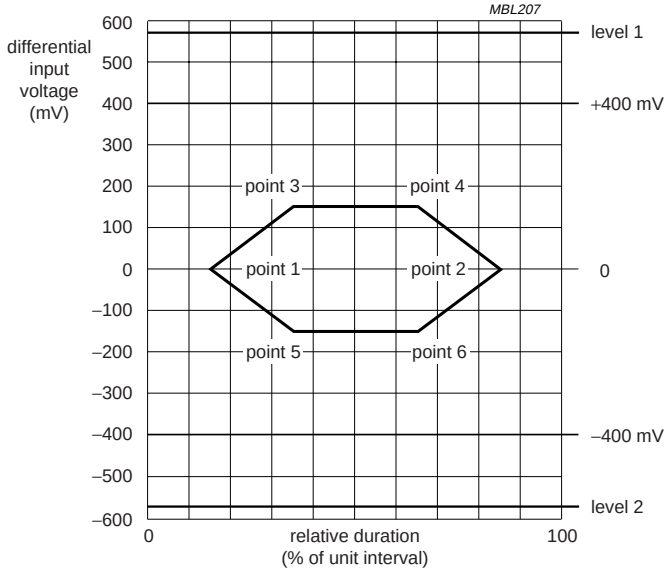



**Fig 27. Template 4 eye pattern (receive waveform).**

**Table 16: Template 4 eye pattern definition**

| Name | Differential voltage on pins DP and DM (mV) | Relative duration (% of unit interval) |
|---|---|---|
| Level 1 | +575 | n.a. |
| Level 2 | –575 | n.a. |
| Point 1 | 0 | 15 |
| Point 2 | 0 | 85 |
| Point 3 | +150 | 35 |
| Point 4 | +150 | 65 |
| Point 5 | –150 | 35 |
| Point 6 | –150 | 65 |

# 17. Parallel digital interface timing

## 17.1 High-speed transmit timing

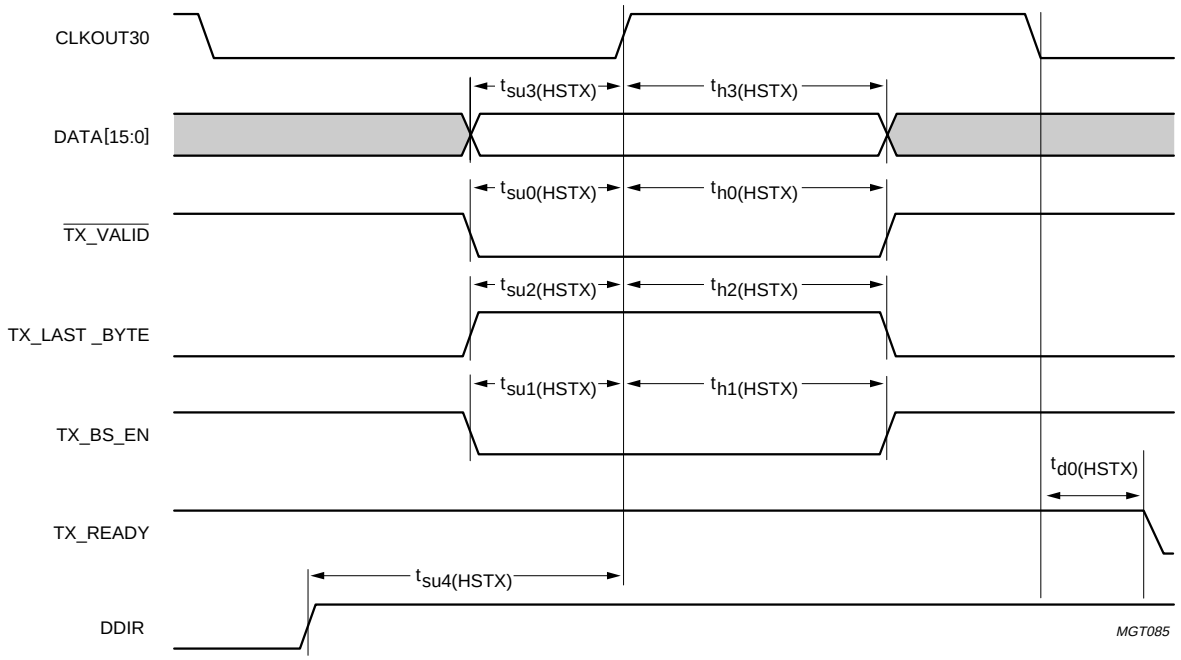



**Fig 28. Parallel digital interface timing: high-speed transmit.**

**Table 17: High-speed transmit timing**

*CLKOUT30 duty cycle = 50%; see Figure 28.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{su3(HSTX)}$ | data set-up time to rising clock edge | | 6.6 | - | - | ns |
| $t_{h3(HSTX)}$ | data hold time after rising clock edge | | 0.1 | - | - | ns |
| $t_{su0(HSTX)}$ | $\overline{TX\_VALID}$ set-up time to rising clock edge | | 6.6 | - | - | ns |
| $t_{h0(HSTX)}$ | $\overline{TX\_VALID}$ hold time after rising clock edge | | 0.1 | - | - | ns |
| $t_{su2(HSTX)}$ | TX_LAST_BYTE set-up time to rising clock edge | | 6.6 | - | - | ns |
| $t_{h2(HSTX)}$ | TX_LAST_BYTE hold time after rising clock edge | | 0.1 | - | - | ns |
| $t_{su1(HSTX)}$ | TX_BS_EN set-up time to rising clock edge | | 6.6 | - | - | ns |
| $t_{h1(HSTX)}$ | TX_BS_EN hold time after rising clock edge | | 0.1 | - | - | ns |
| $t_{su4(HSTX)}$ | DDIR switching time before rising clock edge | | 11 | - | - | ns |
| $t_{d0(HSTX)}$ | TX_READY output delay after falling clock edge | | - | - | 6.9 | ns |

## 17.2 High-speed receive timing

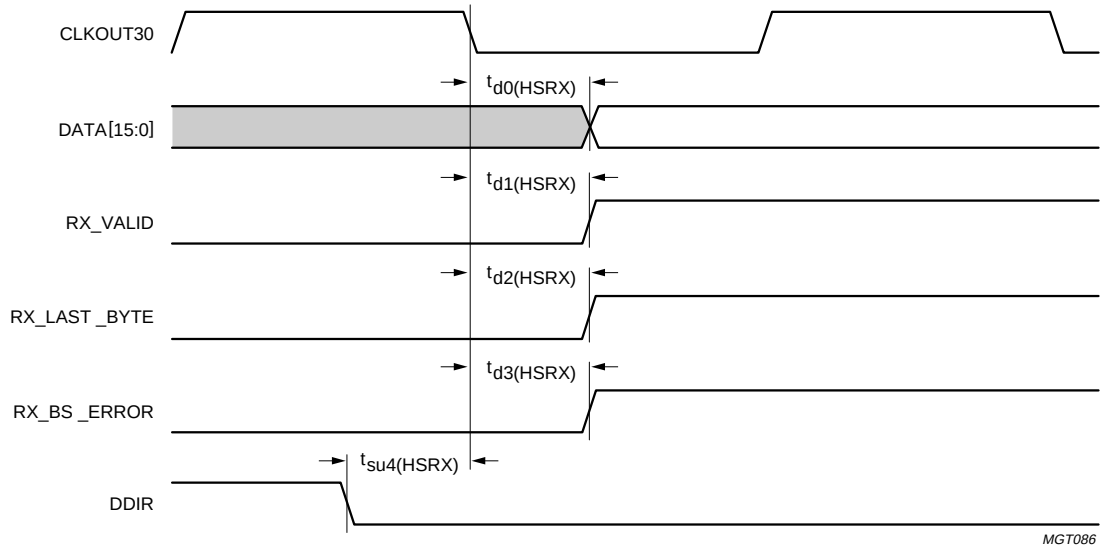


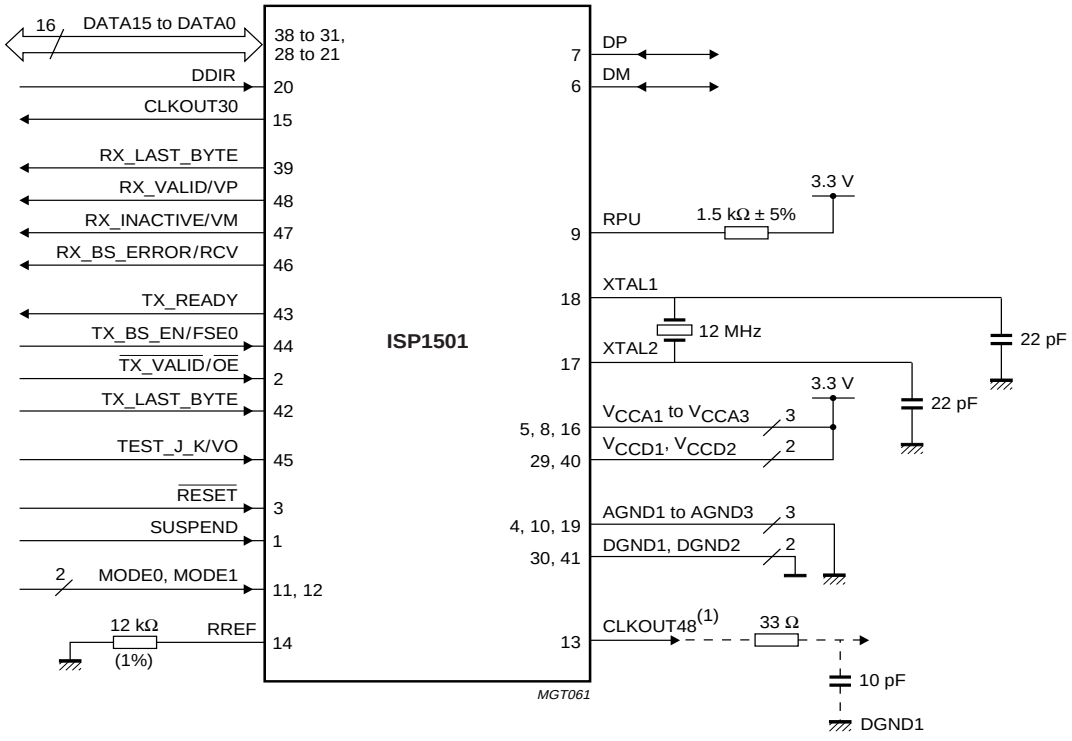

**Fig 29. Parallel digital interface timing: high-speed receive.**

**Table 18: High-speed receive timing**

*CLKOUT30 duty cycle = 50%; see Figure 29.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{d0(HSRX)}$ | received data output delay after falling clock edge | | - | - | 6.8 | ns |
| $t_{d1(HSRX)}$ | RX_VALID delay after falling clock edge | | - | - | 6.8 | ns |
| $t_{d2(HSRX)}$ | RX_LAST_BYTE delay after falling clock edge | | - | - | 6.8 | ns |
| $t_{d3(HSRX)}$ | RX_BS_ERROR delay after falling clock edge | | - | - | 6.8 | ns |
| $t_{su4(HSRX)}$ | DDIR switching time after rising clock edge | | - | - | 11 | ns |

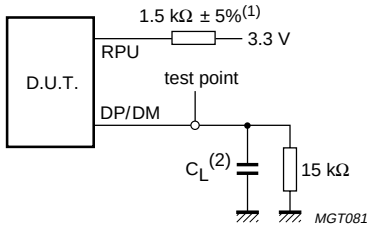
# 18. Application information




(1) The 48 MHz output clock might cause EMC problems unless care is taken during PCB design. If this clock is not used in the ASIC, leave this pin unconnected to the PCB. Connect a 33 Ω series resistor and a 10 pF capacitor to this pin if it is used in the ASIC.

**Fig 30. Application diagram.**

# 19. Test information




(1) Internally connected to pin DP; FS operating state (see Table 4).

(2) $C_L$ = 50 pF for FS.

**Fig 31. FS test circuit.**

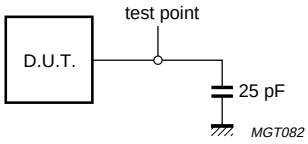
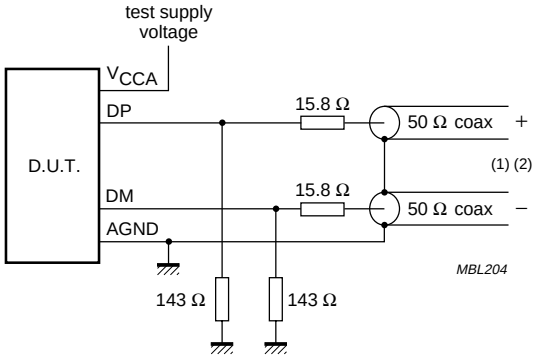



**Fig 32. Load for VM, VP and RCV in FS mode.**



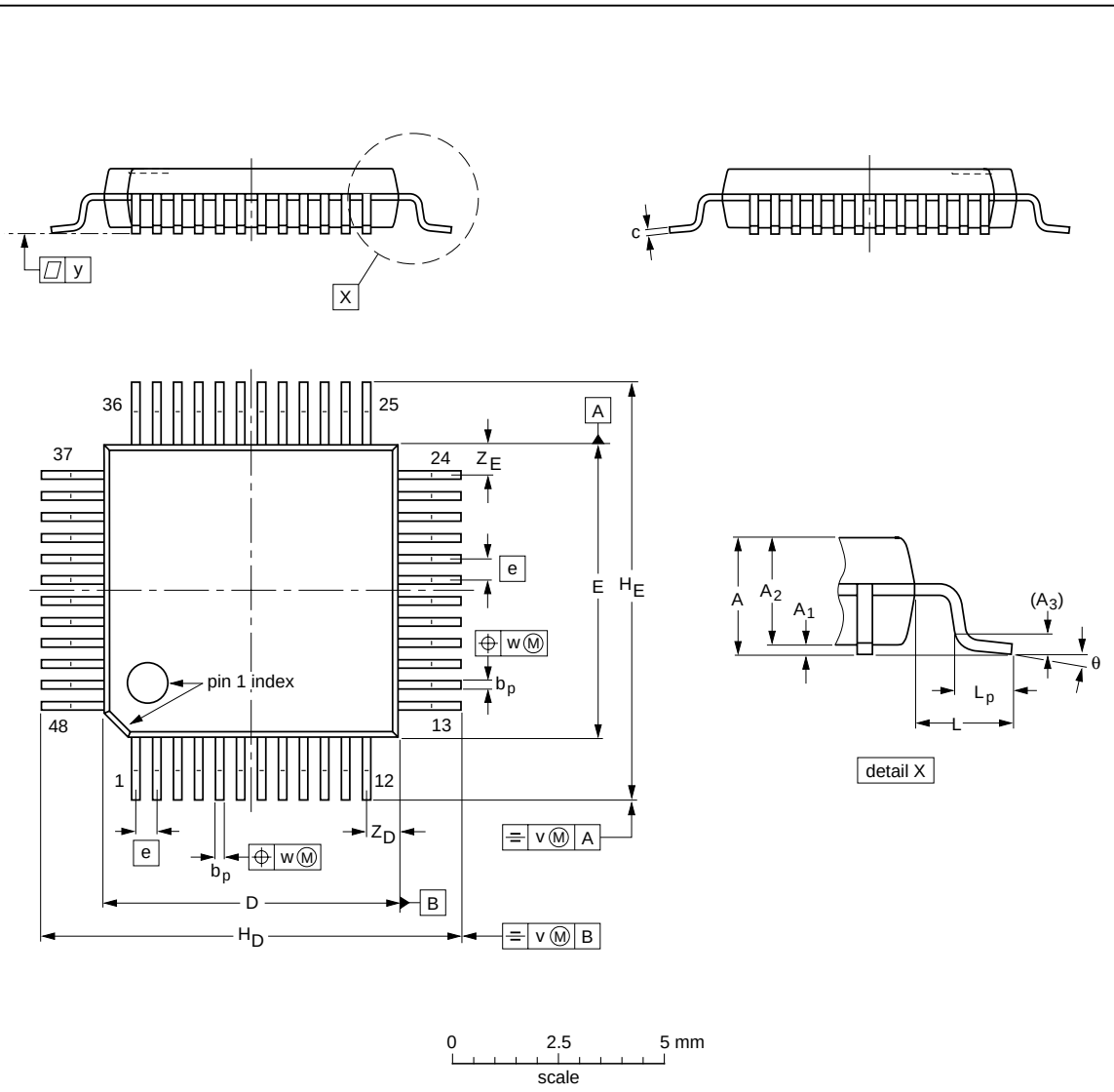

(1) Transmitter: connected to 50 Ω inputs of a high-speed differential oscilloscope.

(2) Receiver: connected to 50 Ω outputs of a high-speed differential data generator.

**Fig 33. High-speed transmitter/receiver test circuit.**

## 20. Package outline

**LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm** **SOT313-2**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_D$ | $H_E$ | L | $L_p$ | v | w | y | $Z_D^{(1)}$ | $Z_E^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.60 | 0.20<br>0.05 | 1.45<br>1.35 | 0.25 | 0.27<br>0.17 | 0.18<br>0.12 | 7.1<br>6.9 | 7.1<br>6.9 | 0.5 | 9.15<br>8.85 | 9.15<br>8.85 | 1.0 | 0.75<br>0.45 | 0.2 | 0.12 | 0.1 | 0.95<br>0.55 | 0.95<br>0.55 | $7^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT313-2 | 136E05 | MS-026 | | | | ~~99-12-27~~<br>00-01-19 |

**Fig 34. Package outline.**

# 21. Soldering

## 21.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

## 21.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C small/thin packages.

## 21.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

## 21.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## 21.5 Package related soldering information

**Table 19: Suitability of surface mount IC packages for wave and reflow soldering methods**

| Package[1] | Soldering method | |
|---|---|---|
| | Wave | Reflow[2] |
| BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA | not suitable | suitable |
| DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS | not suitable[3] | suitable |
| PLCC[4], SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended[4][5] | suitable |
| SSOP, TSSOP, VSO | not recommended[6] | suitable |

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[4] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[5] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[6] Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

# 22. Revision history

**Table 20: Revision history**

| Rev | Date | CPCN | Description |
|---|---|---|---|
| 02 | 20021121 | | **Product data (9397 750 10025); supersedes Objective specification of ISP1501-01 of July 14th, 2000.**<br>Modifications:<br>• Globally changed USB 2.0 and USB 1.1 to Hi-Speed USB and Original USB, respectively.<br>• Globally changed XI and XO to XTAL1 and XTAL2, respectively.<br>• Section 8.3: changed the second sentence.<br>• Section 12.4: changed the second sentence.<br>• Figure 28: changed RX_READY.<br>• Table 17: in the $t_{d0(HSTX)}$ parameter description, changed rising to falling.<br>• Figure 30: added 33 Ω series resistor and 10 pF capacitor to CLKOUT48. Also modified the table note.<br>• Table 2: updated the pin description for pin 13.<br>• Added Section 8.3.<br>• Added Section 12.<br>• Figure 30: added a figure note.<br>• Table 11 $I_{CC(susp)}$ removed the max value and added typ value as 100 μA.<br>• In Section 1, expanded USB.<br>• Globally changed BS_EN to TX_BS_EN.<br>• Globally changed the external precision resistor from 12.2 kΩ ± 1% to 12 kΩ ± 1%.<br>• Globally added ±5% to the external pull-up resistor at RPU.<br>• Globally made TX_VALID active LOW.<br>• Globally changed CLOCKOUT (pin 15) to CLKOUT30 and TEST (pin 13) to CLKOUT48.<br>• Made the following changes in Section 2:<br>– In the fifth and sixth features, changed USB to Hi-Speed USB<br>– In the seventh and eighth features, added for Hi-Speed USB data<br>– Added the feature 3.3 V or 5 V tolerant digital input interface<br>– Changed the feature on ESD protection.<br>• In Figure 1, moved the product title name “ISP1501” to the top right corner.<br>• Made the following changes in Table 2:<br>– Pin 9 description, added 1.5 kΩ ± 5% as the external pull-up resistor. In addition, added HS chirp state at the end of the description<br>– Pin 13 description, changed to “48 MHz output clock; clock is always running when...”<br>– Changed the first statement in the description for pin 15<br>– Modified the pin description for pin 20<br>– Pin 39: modified the pin description<br>– Pin 42: modified the pin description<br>– Pin 43 description, changed it to ISP1501 to make the description clearer |

**Table 20: Revision history**…*continued*

| Rev | Date | CPCN | Description |
|---|---|---|---|
| 02 | 20021121 | | **Product data (9397 750 10025); supersedes Objective specification of ISP1501-01 of July 14th, 2000.**<br>Modifications (continued):<br>• Made the following changes in Table 2<br>– Corrected typo for pin 44 (FES0 changed to FSE0). Also, changed the description for State = 2, 3<br>– Pin 45 description, changed the description for State = 0, 1<br>– Pin 48 description: changed the description for State = 2, 3.<br>• Made the following changes in Section 7:<br>– Removed the first three paragraphs<br>– Added the first sentence “The ISP1501 supports both full-speed (FS) and high-speed (HS) USB physical layer.”<br>– Swapped the second and third paragraph<br>– Added Section 7.1 through Section 7.4<br>• In Section 8.2 first paragraph, removed “and Figure 3 shows the state transition diagram.” Also, removed paragraphs 2 through 7 and the state transition diagram.<br>• In Table 4, added “to provide 45 Ω terminations” to the state 2 description.<br>• Changed Section 8.3 to Section 8.2.1. Also, removed the second sentence and added Figure 3.<br>• Added Section 8.2.2 through Section 8.2.4.<br>• In Figure 8, added transistors on the DP and DM lines. Added RPU on DP, added table note 2 and changed the pin order from 11, 12 to 12, 11 for MODE1 and MODE0.<br>• In Section 10.1 second paragraph, rephrased the second sentence.<br>• In Table 7 and Table 8, changed “high and low byte” to “high and low bytes”.<br>• In Figure 11, changed the Hex value for DATA[7:0] from 80H to 00H.<br>• In Figure 12, changed the Hex value for DATA[7:0] from 80H to 00H.<br>• In Section 10.2:<br>– First paragraph: added the last sentence<br>– Third paragraph: rephrased the first sentence<br>– Second last paragraph: rephrased the second sentence<br>– Last paragraph: removed the last sentence.<br>• In Table 8, changed text in the second and fourth rows of the condition column.<br>• Changed figure title in Figure 13, Figure 14, Figure 15 and Figure 16.<br>• In Figure 17, added a figure note.<br>• In Section 10.3, changed content in the second paragraph.<br>• In Section 10.4 first sentence, changed 37 bits to 8 HS bit times. Also, changed the same in Figure 19.<br>• In Figure 20, changed clock cycles to HS bit times.<br>• In Section 10.5, changed content in the second sentence. Added reference to Figure 20 in the two paragraphs. Also, added the last sentence to the first paragraph.<br>• In Figure 7, switched the location of the DP and DM lines. Also, added RPU on DP.<br>• In Table 6, added table notes 3 and 4. |

**Table 20: Revision history**…*continued*

| Rev | Date | CPCN | Description |
|---|---|---|---|
| **02** | **20021121** | | **Product data (9397 750 10025); supersedes Objective specification of ISP1501-01 of July 14th, 2000.**<br>Modifications (continued):<br>• Added Section 11.<br>• In Table 9, changed $I_{LI}$ to <1 μA. Removed table note 2 and changed $V_{esd}$.<br>• In Table 11, added typical values in all rows and removed the maximum values.<br>• In Table 13, added the minimum value for $V_{OL}$ as 0.<br>• In Table 14, removed content related to the low-speed mode.<br>• Separated Figure 23 and Figure 24 from Figure 21 and Figure 22.<br>• In Table 17, changed the order of the timing symbols to match their order in Figure 28. Also, changed the value of $t_{SU4(HSTX)}$ to 11 ns.<br>• Made the following changes to Figure 28:<br>– $\overline{TX\_VALID}$: changed the symbols $t_{SU2(HSTX}$) and $t_{H2(HSTX)}$ to $t_{SU0(HSTX)}$ and $t_{H0(HSTX)}$<br>– TX_LAST_BYTE: changed $t_{SU0(HSTX)}$ and $t_{H0(HSTX)}$ to $t_{SU2(HSTX)}$ and $t_{H2(HSTX)}$<br>– Changed the width of the CLKOUT30 signal.<br>• In Figure 29, changed the symbol for DDIR from $t_{SU0(HSRX)}$ to $t_{SU4(HSRX)}$.<br>• In Table 18, changed the parameter text for $t_{SU4(HSRX)}$, removed the value in the min field and added 11 ns in the max field. Also, made $t_{SU4(HSRX)}$ as the last row.<br>• In Figure 30:<br>– Added 22 pF to XTAL1 and XTAL2<br>– Removed n.c. from pin 13<br>– Changed 12.2 kΩ ± 1% to 12 kΩ ± 1%.<br>• In Figure 31, changed the content of figure note 1. Also, added figure note 2. |
| **01** | **20000714** | | **Objective data; initial version.** |

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|---|---|---|---|
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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