Data Sheet | January 2001 | File Number 4860.2

2.4GHz RF/IF Converter and Synthesizer

The ISL3685 is a monolithic SiGe half duplex RF/IF transceiver designed to operate in the 2.4GHz ISM band. The receive chain features a low noise, gain selectable amplifier (LNA) followed by a down-converter mixer. An up-converter mixer and a high performance preamplifier compose the transmit chain. The remaining circuitry comprises a high frequency Phase Locked Loop (PLL) synthesizer with a three wire programmable interface for local oscillator applications.

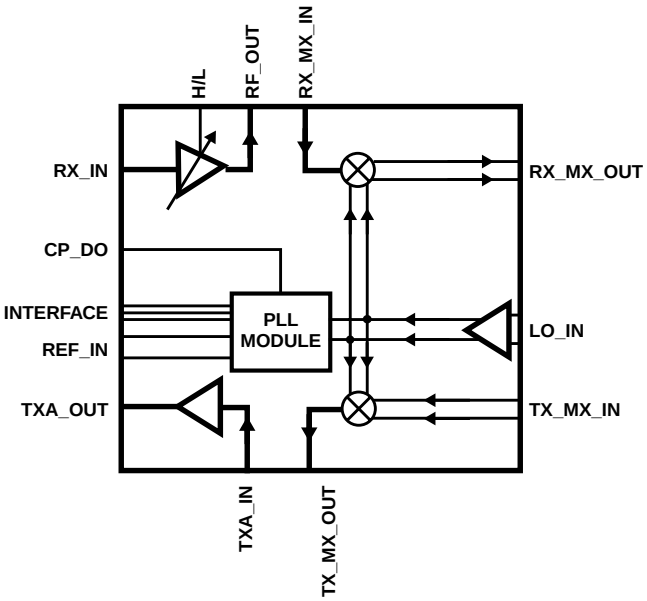
A reduced filter count is realized by multiplexing the receive and transmit IF paths and by sharing a common differential matching network. Furthermore, both transmit and receive RF amplifiers can be directly connected to mixers as bandwidth characteristics attenuate image frequencies. The inherent image rejection of both the transmit and receive functions allows this economic advantage.

The ISL3685 is housed in a 44 lead MLFP package well suited for PCMCIA board and MINI PCI applications.

Ordering Information

PART NUMBER	TEMP RANGE (^{o}C)	PACKAGE	PKG. NO
ISL3685IR	-40 to 85	44 Ld MLFP	L44.7x7
ISL3685IR96	-40 to 85	Tape and Reel	

Simplified Block Diagram



Features

- Highly Integrated
- Multiplexed RX/TX IF Path prescribes Single IF Filter
- Programmable Synthesizer
- Gain Selectable LNA
- Power Management/Standby Mode
- Single Supply 2.7V to 3.3V Operation

Cascaded LNA/Mixer (High Gain)

- Gain 25dB
- SSB Noise Figure. 3.7dB
- Input IP3. . . . . -12dBm
- IF Frequency . . . . . .280MHz to 600MHz

Cascaded LNA/Mixer (Low Gain)

- Gain . . . . . -9dB
- Input P1dB . . . . . +2.5dBm
- IF Frequency . . . . . .280MHz to 600MHz

Cascaded Mixer/Preamplifier

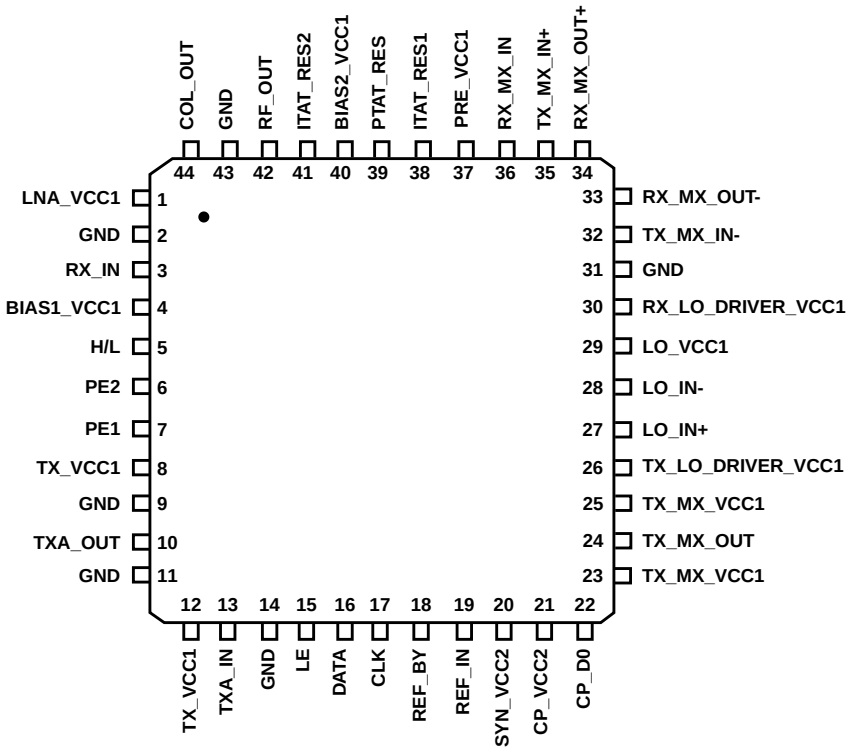
- Transmit Cascaded Mixer/Preamplifier Gain 25dB
- SSB Noise Figure. 10dB
- Output P1dB. 4dBm
- IF Frequency . . . . . .280MHz to 600MHz

Applications

- IEEE802.11 1Mbps and 2Mbps Standard
- Systems Targeting IEEE802.11, 11Mbps Standard
- Wireless Local Area Networks
- PCMCIA Wireless Transceivers
- ISM Systems
- TDMA Packet Protocol Radios
- MINI PCI Wireless Transceivers

Pinout

ISL3685
(MLF)
TOP VIEW



Pin Description

PIN	NAME	DESCRIPTION
1	LNA_VCC1	Low Noise Amplifier Positive Power Supply.
3	RX_IN	Low Noise Amplifier RF Input, internally DC coupled and requires an external blocking capacitor. A shunt capacitor to ground matches the input for return loss and optimum NF.
4	BIAS1_VCC1	Bias Positive Power Supply for the LNA and Preamplifier.
5	H/L	High or Low Gain Select, controls the LNA high and low gain modes.
6	PE2	This pin along with pin PE1 and bit M(0) of PLL_PE determine which of various operational modes will be active. Please refer to the Power Enable Truth Table.
7	PE1	This pin along with pin PE2 and bit M(0) of PLL_PE determine which of various operational modes will be active. Please refer to the Power Enable Truth Table.
8	TX_VCC1	Transmit Amplifier Positive Power Supply, requires a high quality decoupling capacitor and a short return path.
10	TXA_OUT	Transmit Amplifier Output, internally matched to 50Ω, requires an external DC blocking capacitor.
12	TX_VCC1	Transmit Amplifier Positive Power Supply.
13	TXA_IN	Transmit Amplifier Input, internally AC coupled.
15	LE	Synthesizer Latch Enable, the serial interface is active when LE is low and the serial data is latched into defined registers on the rising edge of LE.
16	DATA	Synthesizer Serial Data Input, clocked in on the rising edge of the serial clock, MSB first.
17	CLK	Synthesizer Clock, DATA is clocked in on the rising edge of the serial clock, MSB first.
18	REF_BY	Synthesizer Reference Frequency Input Bypass, internally DC coupled and requires an external bypass to ground when REF_IN is used as a Single Ended input, requires an external AC coupling capacitor when used as a differential input.

Pin Description (Continued)

PIN	NAME	DESCRIPTION
19	REF_IN	Synthesizer Reference Frequency Input, internally DC coupled and requires an external AC coupling capacitor.
20	SYN_VCC2	Synthesizer Positive Power Supply.
21	CP_VCC2	Synthesizer Charge Pump Positive Power Supply.
22	CP_DO	Synthesizer Charge Pump Output, feeds the PLL loop filter.
23	TX_MX_VCC1	Transmit Mixer Positive Power Supply.
24	TX_MX_OUT	Transmit Mixer RF output, internal AC coupled and internally matched to 50Ω.
25	TX_MX_VCC1	Transmit Mixer Positive Power Supply.
26	TX_LO_Driver_ VCC1	Transmit LO Driver Positive Power Supply.
27	LO_IN+	Local Oscillator Positive Input, internally AC coupled, internally matched to 50Ω when the LO is driven single ended and the LO_IN- is grounded.
28	LO_IN-	Local Oscillator Negative Input, internally AC coupled, differential or single ended capability, ground externally for single ended operation.
29	LO_VCC1	LO Buffer Positive Power Supply.
30	RX_LO_DRIVER _VCC1	Receiver LO Driver Positive Power Supply.
32	TX_MX_IN-	Transmit Mixer Negative Input, internally DC coupled, high impedance input. Designed to share a common IF matching network/IF SAW filter with the receive mixer. Care should be exercised regarding the PC board layout to avoid interference and noise pickup. Layout symmetry and management of PC board parasitics is also critical for maximizing the bandwidth of the IF matching network.
33	RX_MX_OUT-	Receive Mixer Negative Output, open collector, high impedance output. Designed to share a common IF matching network/IF SAW filter with the transmit mixer. Care should be exercised regarding the PC board layout to avoid interference and noise pickup. Layout symmetry and management of PC board parasitics is also critical for maximizing the bandwidth of the IF matching network.
34	RX_MX_OUT+	Receive Mixer Positive Output, open collector, high impedance output. Designed to share a common IF matching network/IF SAW filter with the transmit mixer. Care should be exercised regarding the PC board layout to avoid interference and noise pickup. Layout symmetry and management of PC board parasitics is also critical for maximizing the bandwidth of the IF matching network.
35	TX_MX_IN+	Transmit Mixer Positive Input, internally DC coupled, high impedance input. Designed to share a common IF matching network/IF SAW filter with the receive mixer. Care should be exercised regarding the PC board layout to avoid interference and noise pickup. Layout symmetry and management of PC board parasitics is also critical for maximizing the bandwidth of the IF matching network.
36	RX_MX_IN	Receive Mixer RF Input, internally DC coupled and requires external AC coupling as well as RF matching. The recommend network consists of a 3.3pF series capacitor followed by a small series inductance of 1.4nH and then a 1.2nH shunt inductor. The series inductance is best implemented on the PC board using a narrow transmission line inductor.
37	PRE_VCC1	PLL Prescaler Positive Power Supply.
38	ITAT_RES1	Connection to external resistor sets the receive and transmit mixers tail currents, independent of Absolute Temperature.
39	PTAT_RES	Connection to external resistor sets the receive and transmit mixers tail currents, proportional of Absolute Temperature.
40	BIAS2_VCC1	Bias Positive Power Supply for the receive and transmit mixers.
41	ITAT_RES2	Connection to external resistor sets the LNA and Preamplifier bias currents, independent of Absolute Temperature.
42	RF_OUT	Low Noise Amplifier RF Output, internally AC coupled and internally matched to 50Ω.
44	COL_OUT	LNA Collector Output, requires a bypass capacitance which is resonant with the PC board parasitics. A small resistance (20Ω) in series with the main PC board V_{CC} bus is recommended to provide isolation from other V_{CC} bypass capacitors. This ensures the image rejection performance of the LNA is maintained.
All Others	GND	Circuit Ground Pins (Quantity 6 each).

Absolute Maximum Ratings

Supply Voltage 3.6V
V_{CC} to V_{CC} Decouple . . . . . -0.3 to +0.3V
Any GND to GND . . . . . -0.3 to +0.3V

Operating Conditions

Temperature Range . . . . . -40 to 85^{o}C
Supply Voltage Range . . . . . 2.7V to 3.3V

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (^{o}C/W)
MLFP Package 25
Maximum Junction Temperature (Plastic Package) . . . . . 150^{o}C
Maximum Storage Temperature Range . . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C
(MLF - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Intersil TB379.

General Electrical Specifications 25^{o}C, V_{CC} = 2.7V Unless Otherwise Specified

PARAMETER	MIN	TYP	MAX	UNITS
Supply Voltage	2.7	-	3.3	V
Receive Total Supply Current (LNA in High Gain)	-	32	38	mA
Receive Total Supply Current (LNA in Low Gain)	-	25	32	mA
Transmit Total Supply Current	-	41	45	mA
Standby Total Supply Current (PLL and LO Buffers Active)	-	6.5	10	mA
TX/RX Power Down Supply Current (Note 2)	-	-	100	µA
TX/RX/Power Down Time (Note 3)	-	1	10	µs
RX/TX, TX/RX Switching Time (Note 3)	-	0.2	1	µs
CMOS Low Level Input Voltage	-	-	0.3*V_{DD}	V
CMOS High Level Input Voltage, Any V_{DD}/V_{CC}	0.7*V_{DD}	-	3.6	V
CMOS High or Low Level Input Current	-3.0	-	+3.0	µA

NOTES:

2. Standby current is measured after a long elapsed time (20 seconds).
3. TX/RX/TX switching time and power Down/Up time are dependent on external components.

Cascaded LNA/Mixer AC Electrical Specifications

Assumes a direct connection between the LNA and Mixer, IF = 374MHz, LO = 2075MHz at -6dBm, V_{CC} = 2.7 Unless Otherwise Specified, 25^{o}C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
RF Frequency Range		2400	-	2500	MHz
IF Frequency Range		280	374	600	MHz
LO Frequency Range		1800	-	2220	MHz
LO Input Drive Level	Single End or Differential	-10	-6	0	dBm
Power/Voltage Gain	High Gain Mode	21.5	25	29	dB
Noise Figure SSB		-	3.7	5.0	dB
Input IP3		-17.5	-12	-	dBm
Input P1dB		-27.5	-23	-	dBm
Power/Voltage Gain	Low Gain Mode	-11	-9	-1	dB
Noise Figure		-	25	-	dB
Output IM3 at -12dBm Input Tones		-	-58	-40	dBc
Input P1dB		-1	-	-	dBm

Cascaded LNA/Mixer AC Electrical Specifications

Assumes a direct connection between the LNA and Mixer, IF = 374MHz, LO = 2075MHz at -6dBm, V_{CC} = 2.7 Unless Otherwise Specified, 25°C **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
LNA Input 50Ω VSWR with Match Network	High Gain Mode	-	-	2.0:1	-
	Low Gain Mode	-	-	2.0:1	-
LO VSWR (Direct)	LO = Single End	-	-	2.0:1	-
Differential IF Output Load	Shared with TX	-	200	-	Ω
IF Output Capacitance (Single Ended)		-	1.2	-	pF
IF Output Resistance (Single Ended)		-	5.5	-	kΩ
LO to LNA Input Feedthrough (Cascaded, no Filter)		-	-65	-50	dBm
Gain Switching Speed at Full Scale - High to Low	±1dB settling	-	0.03	0.1	µs
Gain Switching Speed at Full Scale - Low to High	±1dB settling	-	0.25	0.3	µs
Image Rejection (Cascaded, No Filter)	With Matching Network	-	14	-	dB

Cascaded Transmit Mixer AC Electrical Specifications

Assumes a direct connection between the Mixer and Preamplifier, F = 374MHz, LO = 2075MHz at -6dBm, VCC = 2.7 Unless Otherwise Specified, 25°C.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
RF Frequency Range		2400	-	2500	MHz
IF Frequency Range		280	374	600	MHz
LO Frequency Range		1800	-	2220	MHz
Power Conversion Gain	200Ω In, 50Ω Out	21	25	29	dB
SSB Noise Figure		-	10	15	dB
Output IP3		+12	+14	-	dBm
Output P1dB		+2.8	+4	-	dBm
LO Input Drive Level	Same as RX	-10	-6	0	dBm
LO to Transmit Amp. Output Feedthrough (Cascaded, No Filter)		-	-25	-	dBm
Preamplifier Output 50Ω VSWR		-	-	3.0:1	-
LO 50Ω VSWR	LO = Single End	-	1.4:1	2.0:1	-
Differential IF Input Load	Shared with RX	-	200	-	Ω
IF Input Capacitance (Single Ended)		-	1.1	-	pF
IF Input Resistance (Single Ended)		-	0.7	-	kΩ

Phase Lock Loop Electrical Specifications (See Notes 4 through 12)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating LO Frequency (32/33 Prescaler)		1800	-	2220	MHz
Operating LO Frequency (64/65 Prescaler)		1800	-	3500	MHz
Reference Oscillator Frequency		-	-	50	MHz
Selectable Prescaler Ratios (P)		32/33	-	64/65	-
Swallow Counter Divide Ratio (A Counter)		0	-	127	-
Programmable Counter Divide Ratio (B Counter)		3	-	2047	-
Reference Counter Divide Ratio (R Counter)		3	-	32767	-
Reference Oscillator Sensitivity, Single or Differential Sine Inputs		0.5	-	V_{CC}	V_{PP}

Phase Lock Loop Electrical Specifications (See Notes 4 through 12) **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Oscillator Sensitivity, CMOS Inputs, Single Ended or Complementary		-	CMOS	-	Note 7
Reference Oscillator Duty Cycle	CMOS Inputs	40	-	60	%
Charge Pump Sink/Source Current/Tolerance	250µA Selection ±25%	0.18	0.25	0.32	mA
Charge Pump Sink/Source Current/Tolerance	500µA Selection ±25%	0.375	0.50	0.625	mA
Charge Pump Sink/Source Current/Tolerance	750µA Selection ±25%	0.56	0.75	0.94	mA
Charge Pump Sink/Source Current/Tolerance	1mA Selection ±25%	0.75	1.0	1.25	mA
Charge Pump Sink/Source Mismatch		-	-	15	%
Charge Pump Output Compliance	Charge Pump $V_{CC} = V_{CC2}$	0.5	-	V_{CC2}-0.5	V
Charge Pump Supply Voltage		2.7	-	3.6	V
Serial Interface Clock Width	High Level t_{CWH}	20	-	-	ns
	Low Level t_{CWL}	20	-	-	ns
Serial Interface Data/Clk Set-Up Time t_{CS}		20	-	-	ns
Serial Interface Data/Clk Hold Time t_{CH}		10	-	-	ns
Serial Interface Clk/LE Set-Up Time t_{ES}		20	-	-	ns
Serial Interface LE Pulse Width t_{EW}		20	-	-	ns

NOTES:

4. The Serial data is clocked on the Rising Edge of the serial clock, MSB first. The serial Interface is active when LE is LOW. The serial Data is latched into defined registers on the rising edge of LE.
5. As long as power is applied, all register settings will remain stored, including the power down state. The system may then come in and out of the power down state without requiring the registers to be rewritten.
6. CMOS Reference Oscillator input levels are given in the General Electrical Specification section.

POWER ENABLE TRUTH TABLE

PE1	PE2	PLL_PE (SERIAL BUS)	STATUS
0	0	1	Power Down State, PLL in Save Mode, Active Serial Interface
1	1	1	Receive State
1	0	1	Transmit State
0	1	1	PLL Inactive, Inactive RX, TX, Active Serial Interface
X	X	0	PLL Disabled, Disabled PLL Registers, Active Serial Interface

NOTE:

7. PLL_PE is controlled via the serial interface, and can be used to disable the synthesizer. The actual synthesizer control is a logic AND function of PLL_PE and the result of the logic OR function of PE1 and PE2. PE1 and PE2 directly control the power enable functionality of the LO buffers.

PLL Synthesizer Table

	REGISTER DEFINITION																			
SERIAL BITS	LSB 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	MSB
R Counter	0	0	R(0)	R(1)	R(2)	R(3)	R(4)	R(5)	R(6)	R(7)	R(8)	R(9)	R(10)	R(11)	R(12)	R(13)	R(14)	X (Don't Care)		
A/B Counter	0	1	A(0)	A(1)	A(2)	A(3)	A(4)	A(5)	A(6)	B(0)	B(1)	B(2)	B(3)	B(4)	B(5)	B(6)	B(7)	B(8)	B(9)	B(10)
Operational Mode	1	0	M(0)	0	M(2)	M(3)	M(4)	M(5)	M(6)	M(7)	M(8)	0	0	0	0	M(13)	M(14)	M(15)	X	X

Reference Frequency Counter/Divider

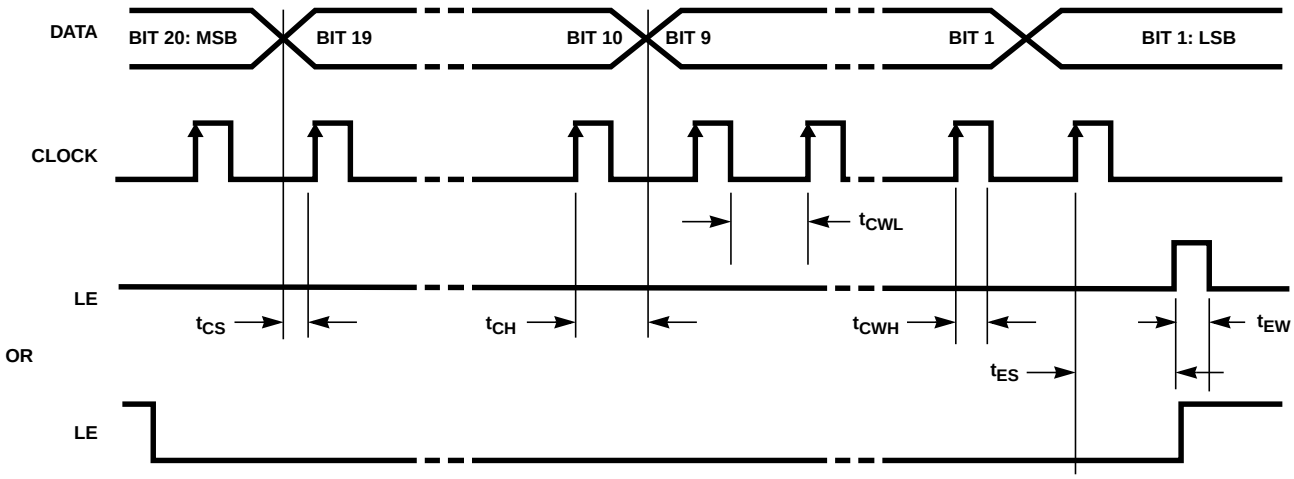
BIT	DESCRIPTION
R(0-14)	Least significant bit R(0) to most significant bit R(14) of the divide by R counter. The Reference signal frequency is divided down by this counter and is compared with a divided LO by a phase detector.

LO Frequency Counters/Dividers

BIT	DESCRIPTION
A(0-6)	Least significant bit A(0) to most significant bit A(6) of a 7-bit Swallow counter and LSB B(0) to MSB B(10) of the 11-bit divider. The LO frequency is divided down by [P*B+A], where P is the Prescaler divider set by bit M(2). This divided signal frequency is compared by a phase detector with the divided Reference signal.
B(0-11)	

Operational Modes

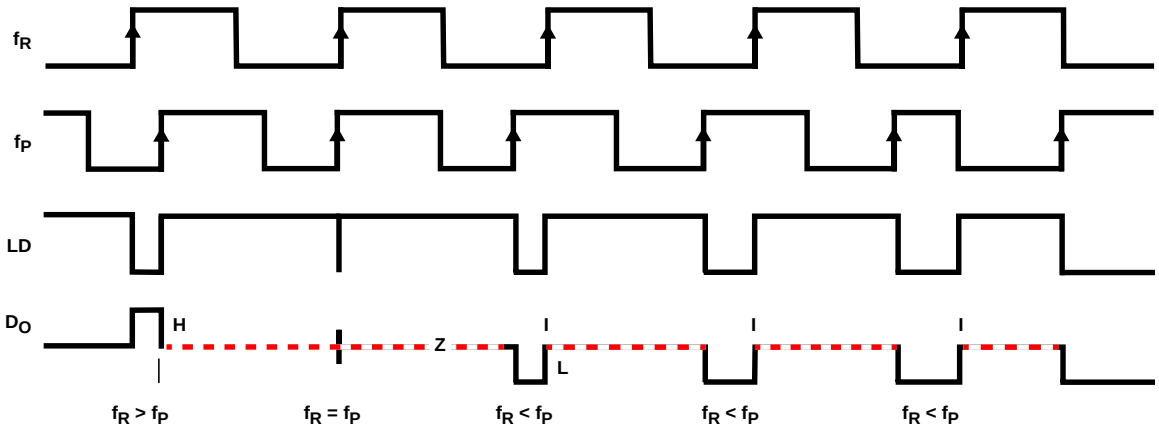
BIT	DESCRIPTION				
M(0)	(PLL_PE), Phase Lock Loop Power Enable. 1 = Enable, 0 = Power Down. Serial port always on.				
M(2)	Prescaler Select. 0 = 32/33, 1 = 64/65.				
M(3) M(4)	Charge Pump Current Setting		**M(4)**	**M(3)**	**OUTPUT SINK/SOURCE**
			0	0	0.25mA
			0	1	0.50mA
			1	0	0.75mA
			1	1	1.00mA
M(5) M(6)	Charge Pump Sign	**M(6)**	**M(5)**		
		0	0	Source if LO/ [P*B+A] < Ref/R	
		0	1	Source if LO/ [P*B+A] > Ref/R	
M(7) M(8) M(13)	LD Pin Multiplex Operation	**M(13)**	**M(8)**	**M(7)**	**OUTPUT AT PIN LD**
		0	0	X	Lock Detect Operation
		0	1	X	Short to GND
		1	0	X	Serial Register Read Back
		1	1	0	Ref. Divided by R Waveform
		1	1	1	LO Divided by [P*B+A] Waveform
M(14) M(15)	Charge Pump Operation/Test	**M(15)**	**M(14)**	**OPERATION/TEST**	
		0	0	Normal Operation	
		0	1	Charge Pump Constant Current Source	
		1	0	Charge Pump Constant Current Sink	
		1	1	High Impedance State	



NOTES:

8. Parenthesis data indicates programmable reference divider data.
9. Data shifted into register on clock rising edge.
10. Data is shifted in MSB first.

FIGURE 1. SERIAL DATA INPUT TIMING

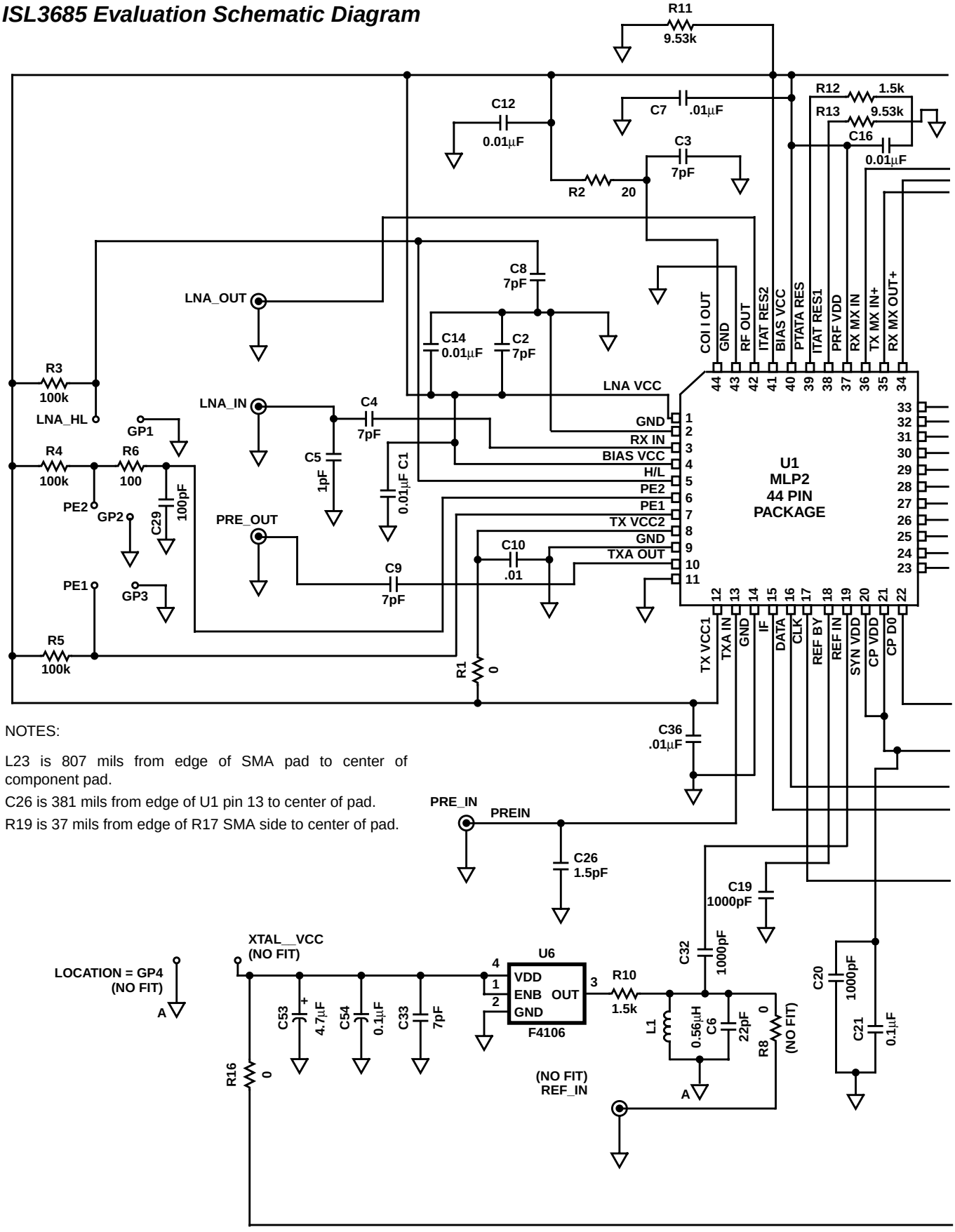


NOTES:

11. Phase difference detection range: -2π to $+2\pi$.
12. The minimum width pump up and pump down current pulses occur at the D_O pin when the loop is locked.

FIGURE 2. PHASE COMPARATOR AND INTERNAL CHARGE PUMP CHARACTERISTICS

ISL3685 Evaluation Schematic Diagram



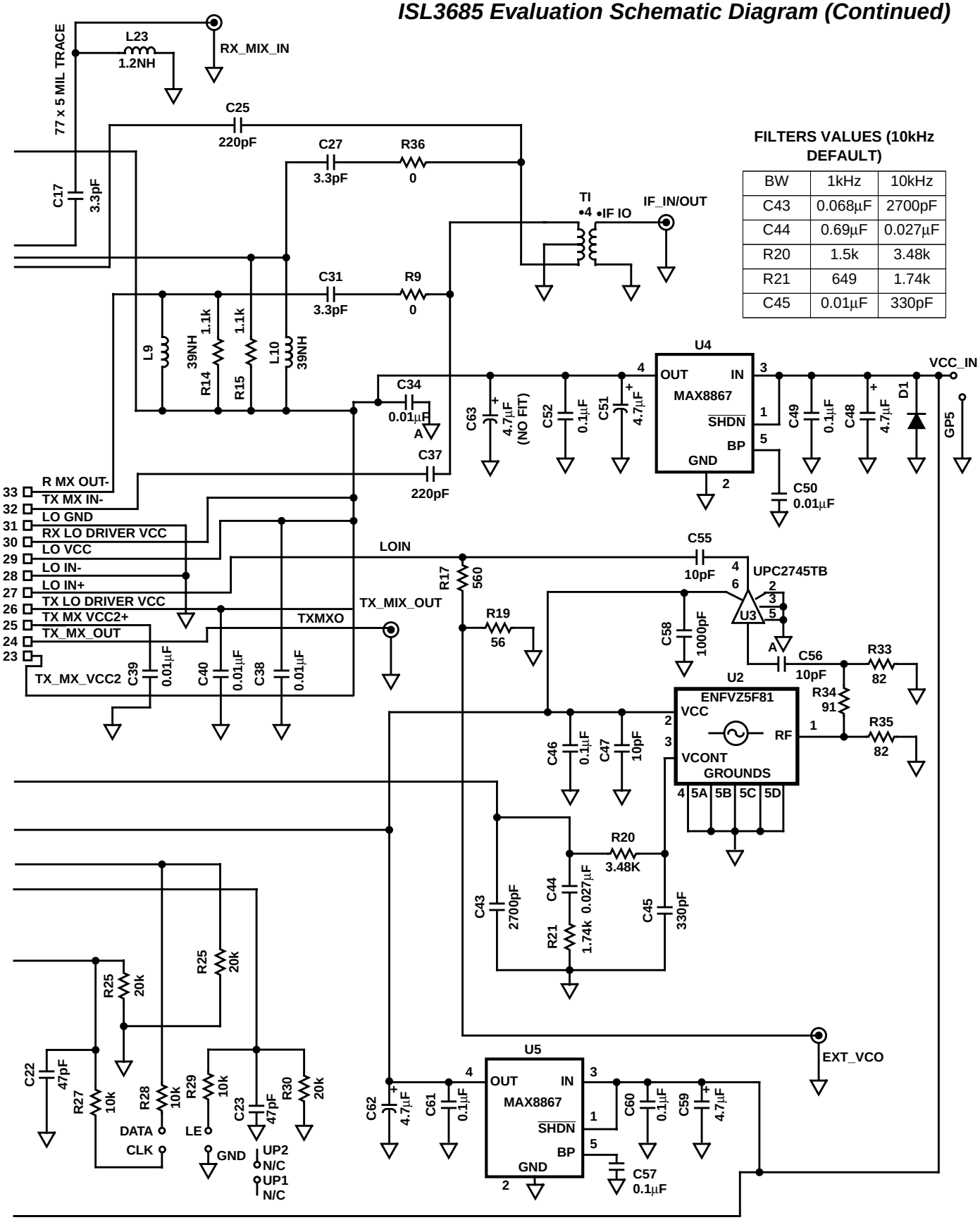
NOTES:

L23 is 807 mils from edge of SMA pad to center of component pad.

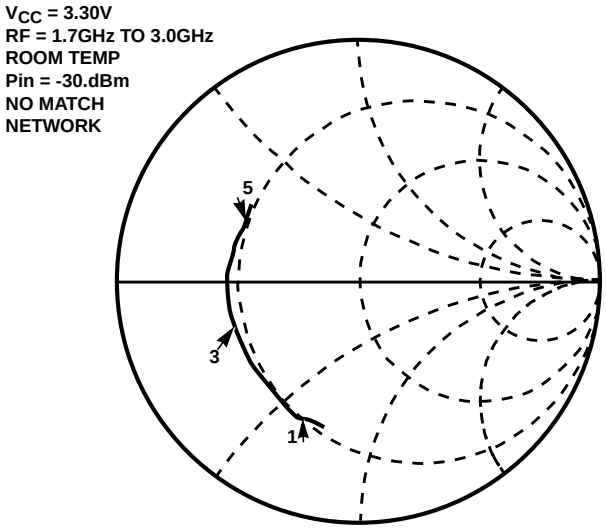
C26 is 381 mils from edge of U1 pin 13 to center of pad.

R19 is 37 mils from edge of R17 SMA side to center of pad.

ISL3685 Evaluation Schematic Diagram (Continued)

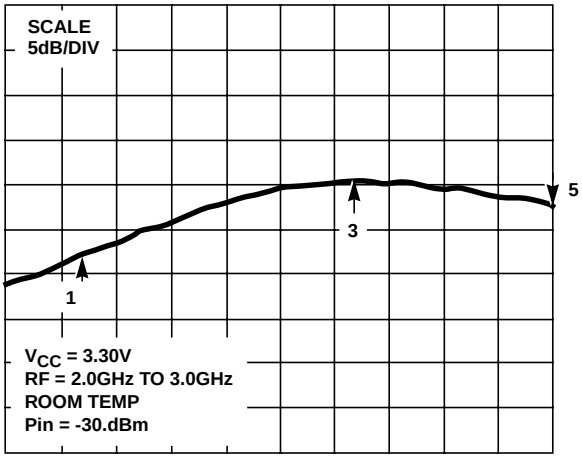


Typical Performance Curves



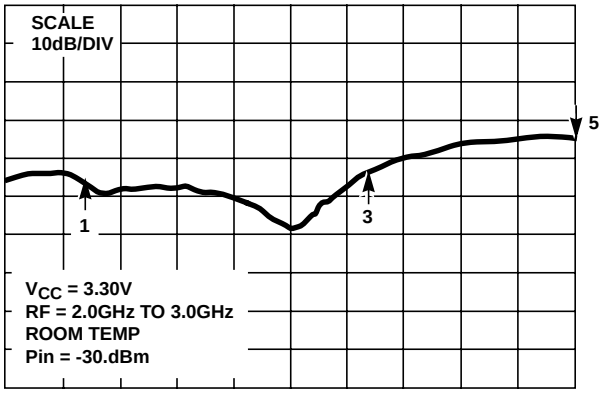
Marker 1 = 1.7GHz, Real = 16.7Ω, Imaginary = -31.8Ω
Marker 3 = 2.45GHz, Real = 15.0Ω, Imaginary = -8.0Ω
Marker 5 = 3.0GHz, Real = 16.5Ω, Imaginary = 10.5Ω

FIGURE 3. S11 LNA in HIGH GAIN



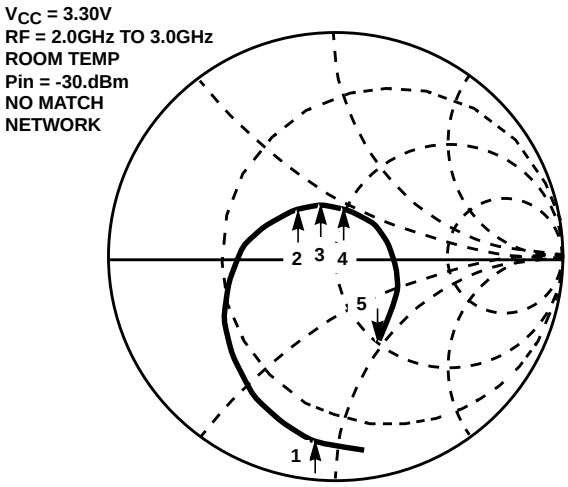
Marker 1 = 1.7GHz, 7.0dB
Marker 3 = 2.45GHz, 15.3dB
Marker 5 = 3.0GHz, 12.5dB

FIGURE 4. S21 LNA in HIGH GAIN



Marker 1 = 1.7GHz, -46.4dB
Marker 3 = 2.45GHz, -44.1dB
Marker 5 = 3.0GHz, -35.4dB

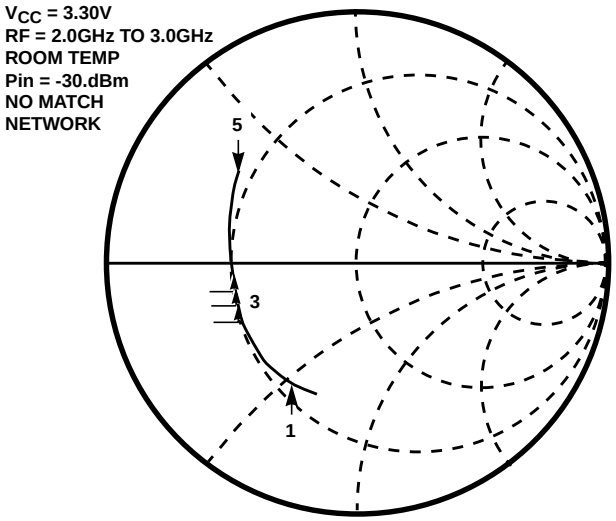
FIGURE 5. S12 LNA in HIGH GAIN



Marker 1 = 1.7GHz, Real = 8.2Ω, Imaginary = -43.5Ω
Marker 3 = 2.45GHz, Real = 39.4Ω, Imaginary = 19.4Ω
Marker 5 = 3.0GHz, Real = -50.6Ω, Imaginary = -45.4Ω

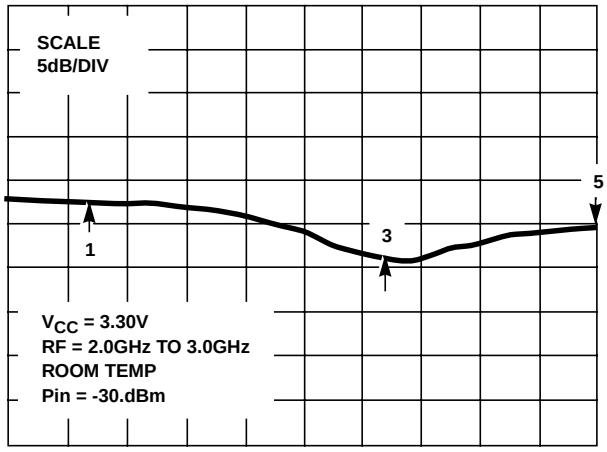
FIGURE 6. S22 LNA in HIGH GAIN

Typical Performance Curves (Continued)



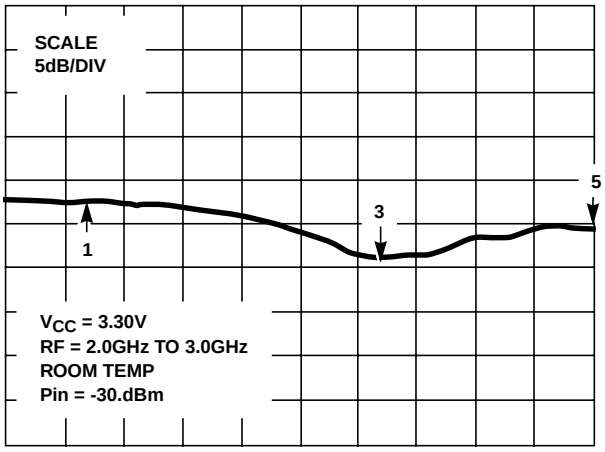
Marker 1 = 1.7GHz, Real = 19.2Ω, Imaginary = -26.1Ω
Marker 3 = 2.45GHz, Real = 16.7Ω, Imaginary = -2.1Ω
Marker 5 = 3.0GHz, Real = 14.1Ω, Imaginary = 15.0Ω

FIGURE 7. S11 LOW GAIN LNA



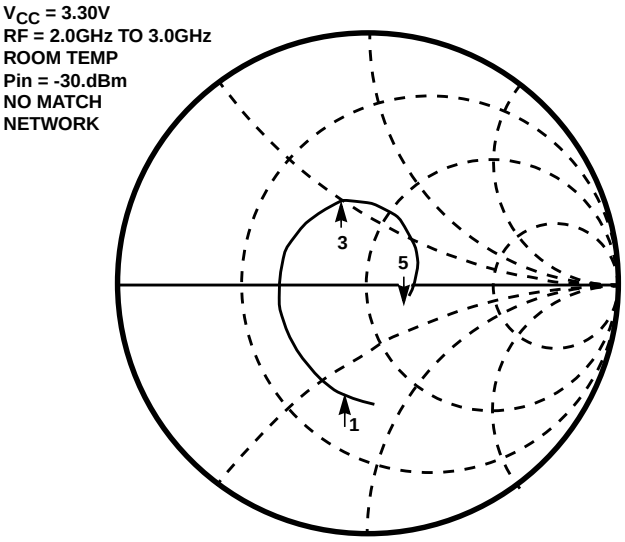
Marker 1 = 1.7GHz, -12.4dB
Marker 3 = 2.45GHz, -18.9dB
Marker 5 = 3.0GHz, -15.4dB

FIGURE 8. S21 LOW GAIN LNA



Marker 1 = 1.7GHz, -12.4dB
Marker 3 = 2.45GHz, -18.9dB
Marker 5 = 3.0GHz, -15.7dB

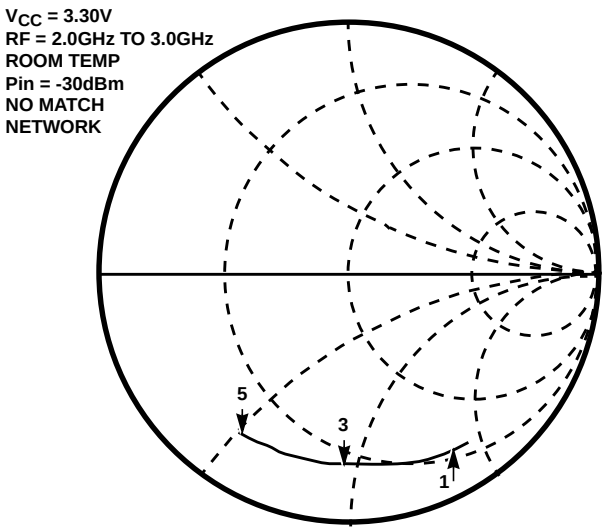
FIGURE 9. S12 LOW GAIN LNA



Marker 1 = 1.7GHz, Real = 28.2Ω, Imaginary = -31.7Ω
Marker 3 = 2.45GHz, Real = 32.5Ω, Imaginary = 24.2Ω
Marker 5 = 3.0GHz, Real = 64.7Ω, Imaginary = -12.8Ω

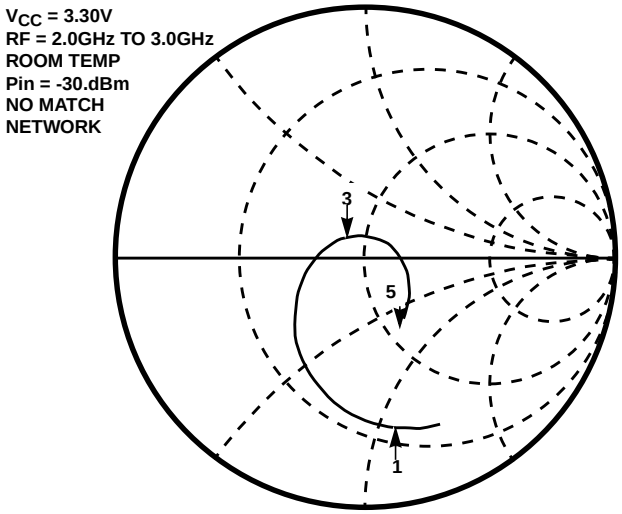
FIGURE 10. S22 LOW GAIN LNA

Typical Performance Curves (Continued)



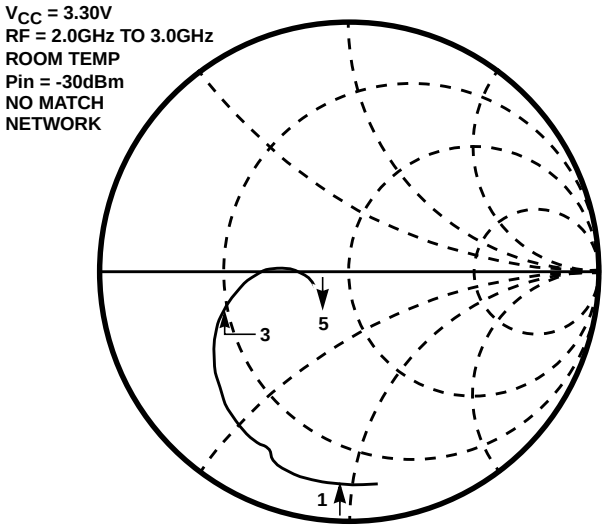
Marker 1 = 1.7GHz, Real = 18.6Ω, Imaginary = -84.7Ω
Marker 3 = 2.45GHz, Real = 13.0Ω, Imaginary = -46.8Ω
Marker 5 = 3.0GHz, Real = 8.0Ω, Imaginary = -25.3Ω

FIGURE 11. S11 RX MIXER



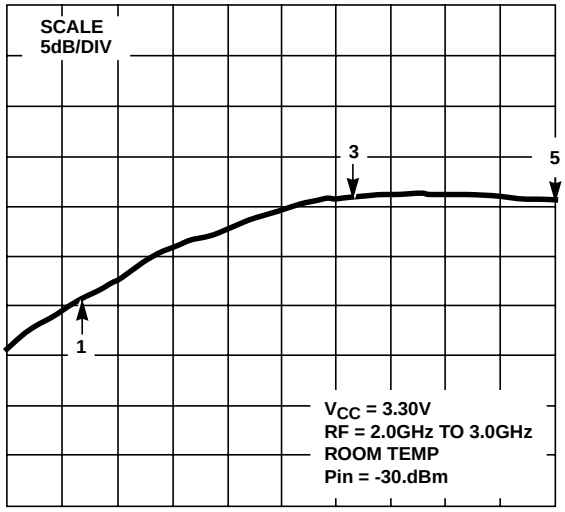
Marker 1 = 1.7GHz, Real = 21.0Ω, Imaginary = -54.8Ω
Marker 3 = 2.45GHz, Real = 42.1Ω, Imaginary = 6.4Ω
Marker 5 = 3.0GHz, Real = 54.4Ω, Imaginary = -34.6Ω

FIGURE 12. S22 TX_MIX_OUT



Marker 1 = 1.7GHz, Real = 7.8Ω, Imaginary = -47.0Ω
Marker 3 = 2.45GHz, Real = 15.4Ω, Imaginary = 7.53Ω
Marker 5 = 3.0GHz, Real = 37.9Ω, Imaginary = -12.5Ω

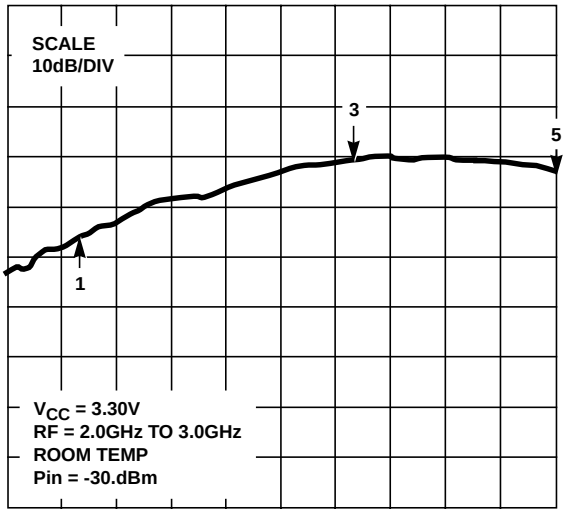
FIGURE 13. S11 TX PREAMP



Marker 1 = 1.7GHz, 5.6dB
Marker 3 = 2.45GHz, 15.6dB
Marker 5 = 3.0GHz, 15.3dB

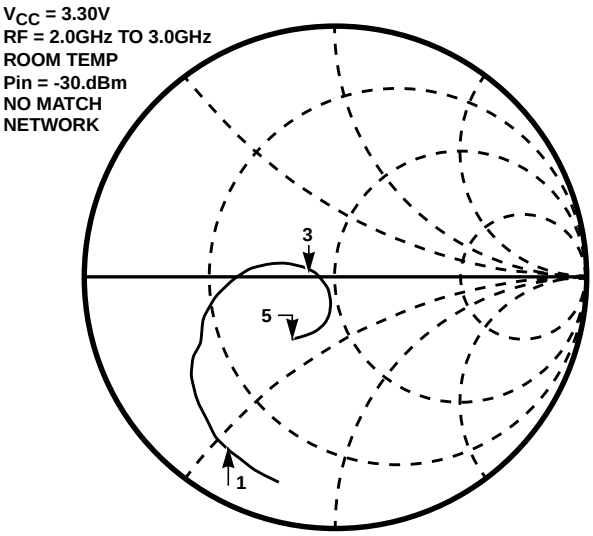
FIGURE 14. S21 TX PREAMP

Typical Performance Curves (Continued)



Marker 1 = 1.7GHz, -46.2dB
Marker 3 = 2.45GHz, -30.7dB
Marker 5 = 3.0GHz, -32.8dB

FIGURE 15. S12 TX PREAMP



Marker 1 = 1.7GHz, Real = 7.2Ω, Imaginary = -27.1Ω
Marker 3 = 2.45GHz, Real = 39.5Ω, Imaginary = 2.7Ω
Marker 5 = 31.8Ω, Real = 31.8Ω, Imaginary = -17.2Ω

FIGURE 16. S22 TX PREAMP

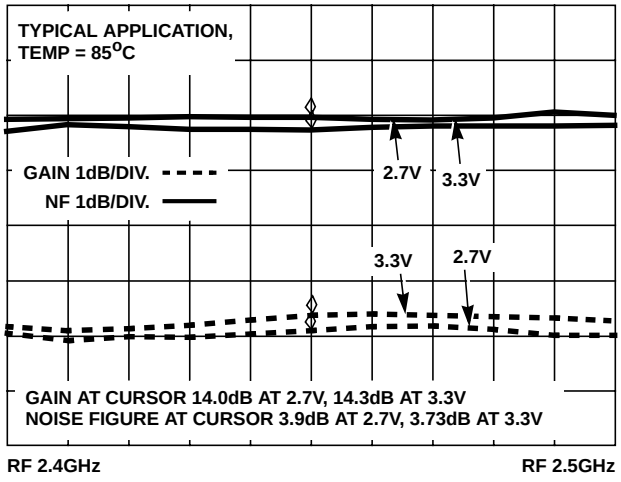


FIGURE 17. LNA HIGH SETTING, GAIN AND NF

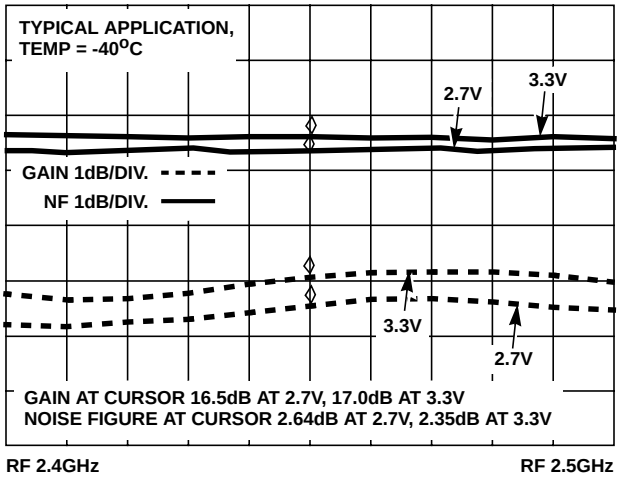


FIGURE 18. LNA HIGH SETTING GAIN AND NF

Typical Performance Curves (Continued)

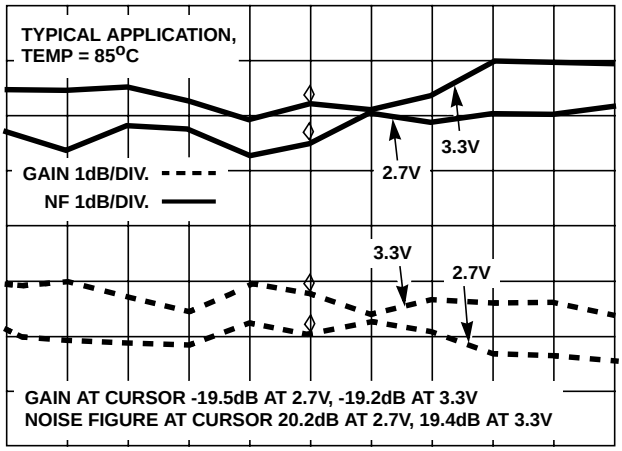


FIGURE 19. LNA LOW SETTING GAIN AND NF

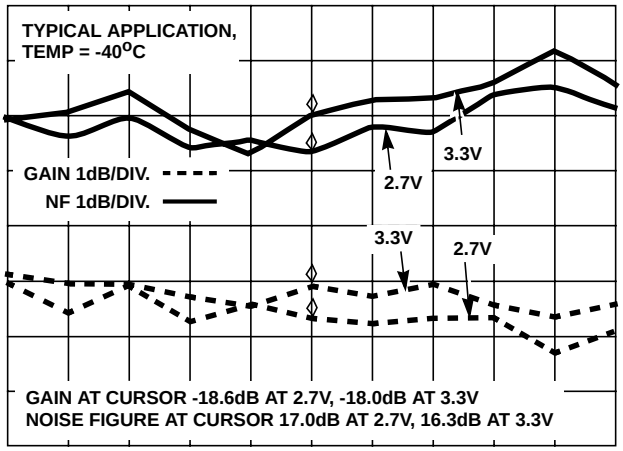


FIGURE 20. LNA LOW SETTING GAIN AND NF

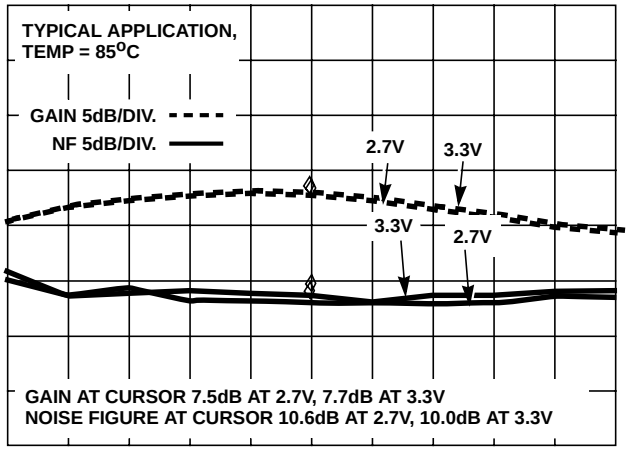


FIGURE 21. RX MIXER GAIN AND NF

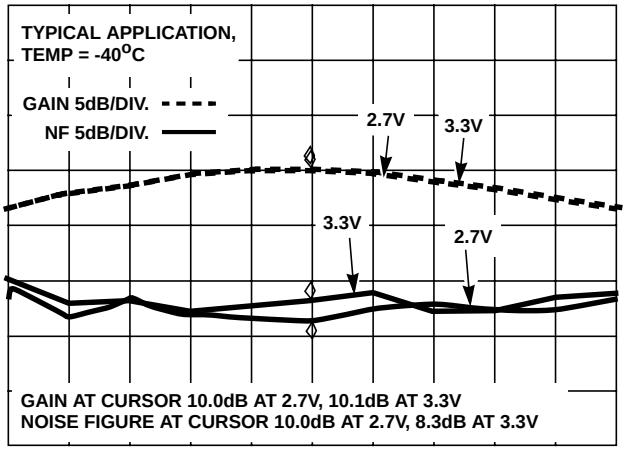


FIGURE 22. RX MIXER GAIN AND NF

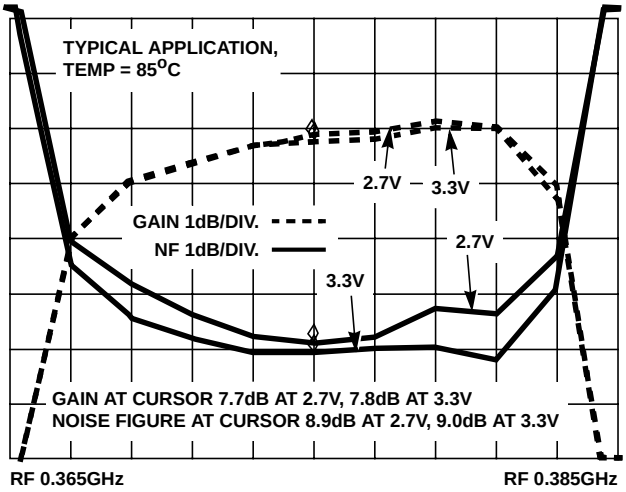


FIGURE 23. TX MIXER GAIN AND NF

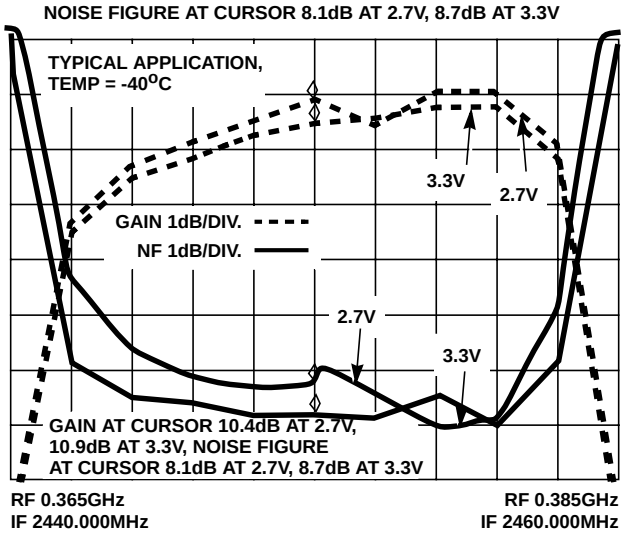


FIGURE 24. TX MIXER GAIN AND NF

Typical Performance Curves (Continued)

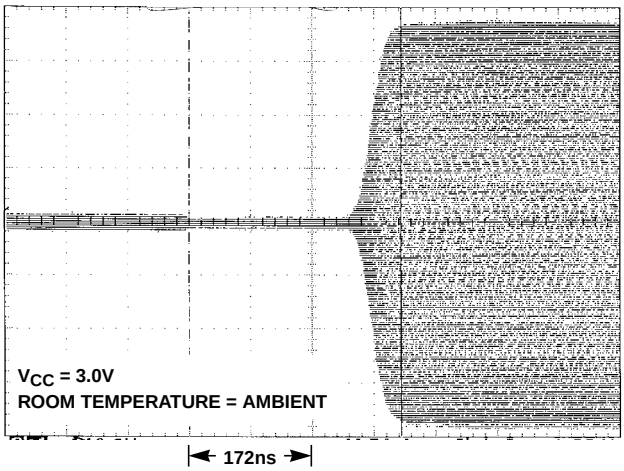


FIGURE 25. GAIN SWITCHING SPEED AT FULL SCALE LNA LOW TO HIGH AT BASEBAND

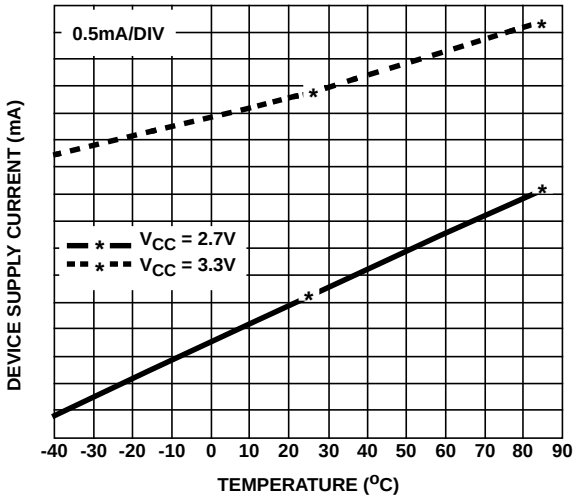


FIGURE 26. RECEIVE TOTAL SUPPLY CURRENT (LNA IN HIGH GAIN)

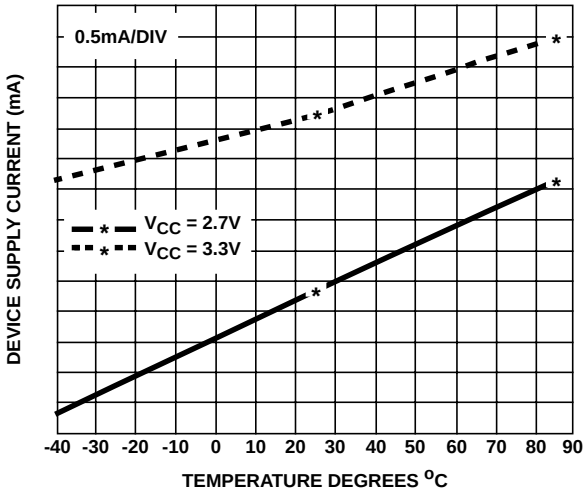


FIGURE 27. RECEIVE TOTAL SUPPLY CURRENT (LNA IN LOW GAIN)

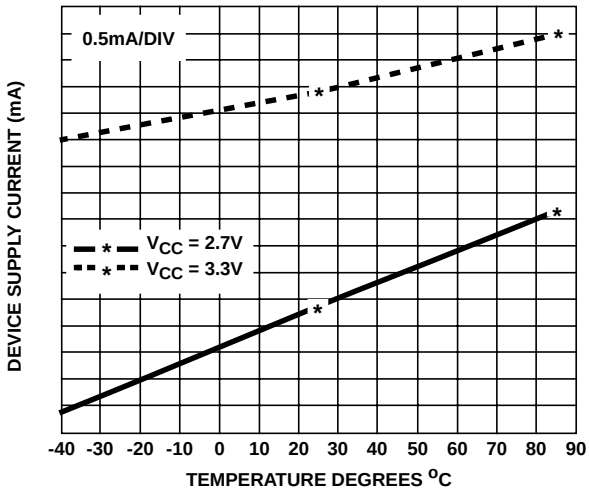


FIGURE 28. TRANSMIT TOTAL SUPPLY CURRENT

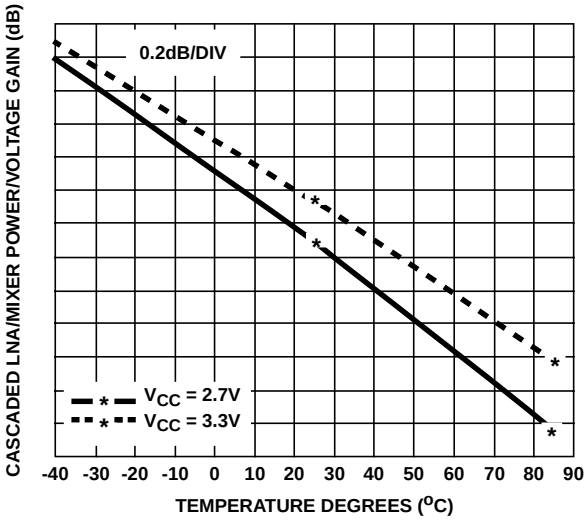


FIGURE 29. POWER/VOLTAGE GAIN HIGH GAIN MODE

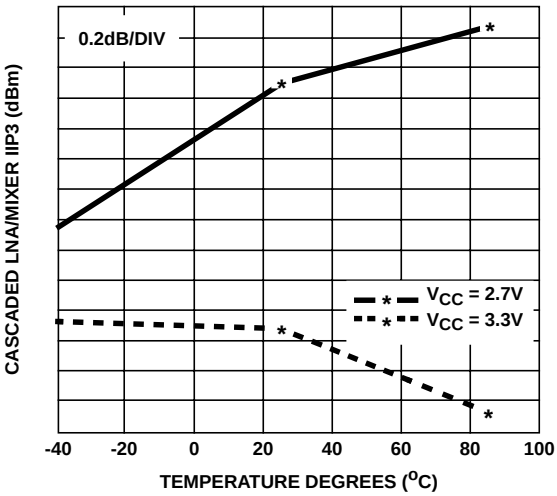


FIGURE 30. INPUT IP3 HIGH GAIN MODE

Typical Performance Curves (Continued)

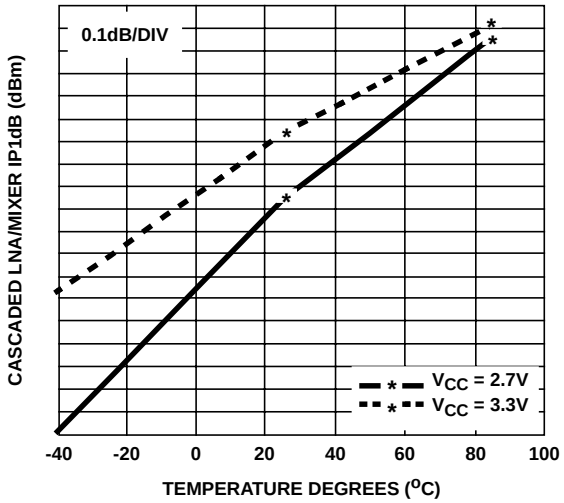


FIGURE 31. INPUT P1dB HIGH GAIN MODE

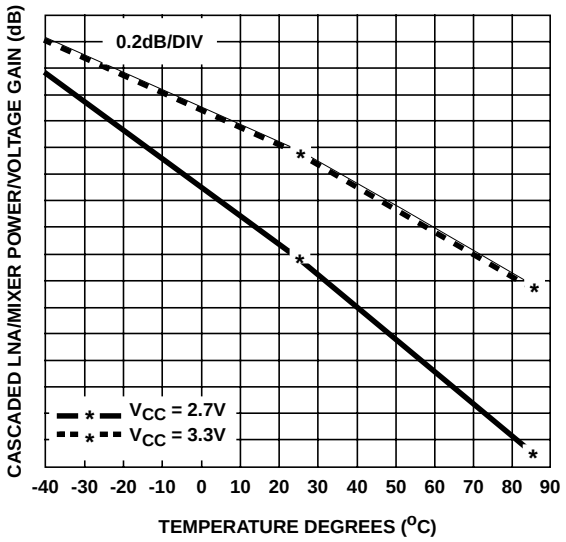


FIGURE 32. POWER/VOLTAGE GAIN LOW GAIN MODE

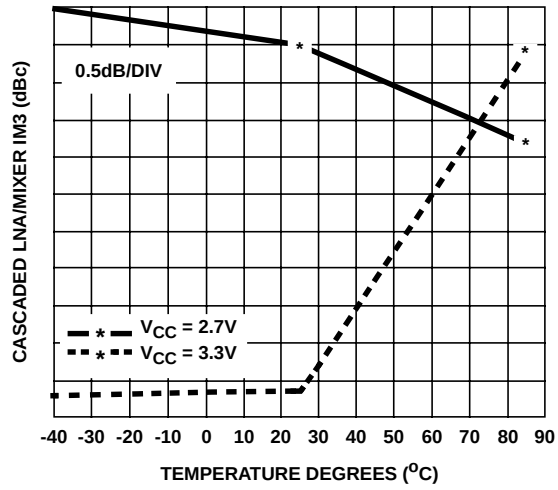


FIGURE 33. RX OUTPUT IM3 AT -5dBm INPUT TONES

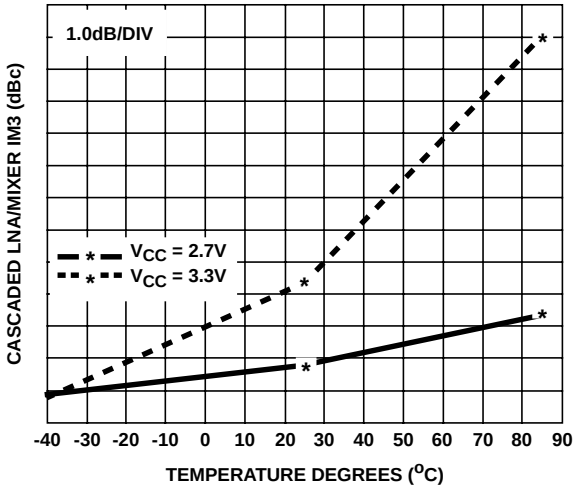


FIGURE 34. RX OUTPUT IM3 AT -12dBm INPUT TONES

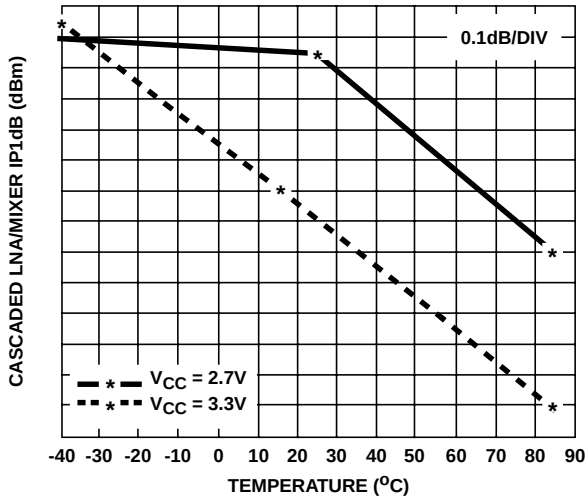


FIGURE 35. INPUT P1dB LOW GAIN MODE

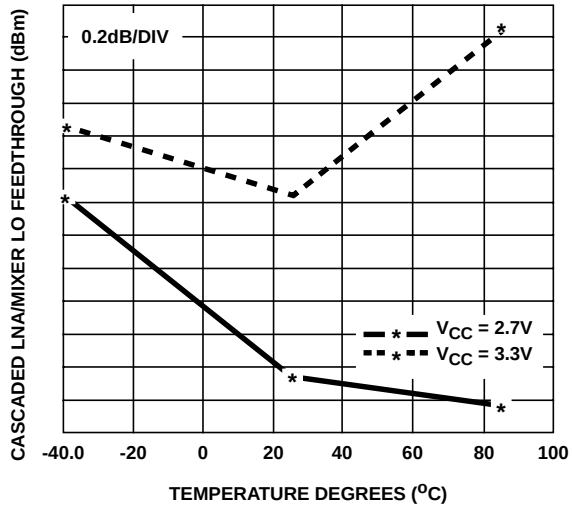


FIGURE 36. LO TO LNA INPUT FEEDTHROUGH (CASCADED, NO FILTER)

Typical Performance Curves (Continued)

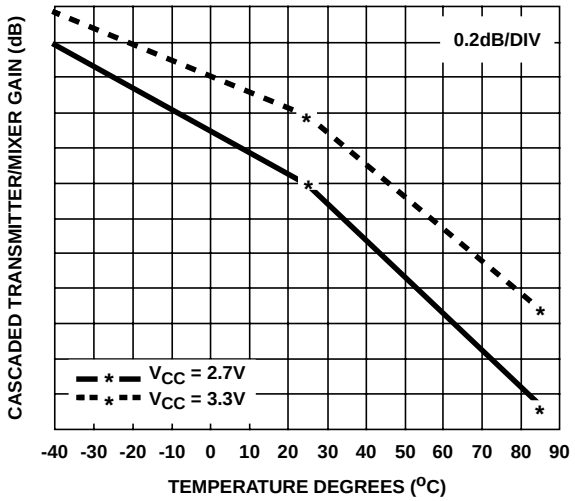


FIGURE 37. POWER CONVERSION GAIN

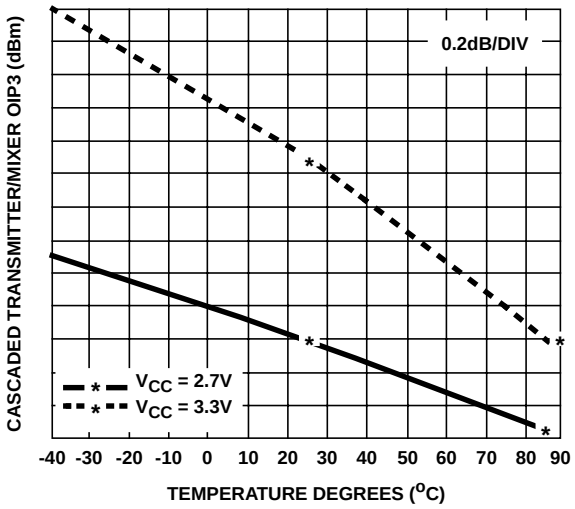


FIGURE 38. OUTPUT IP3

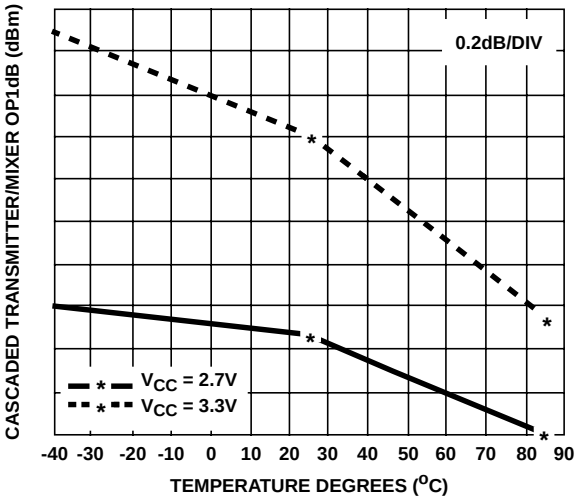


FIGURE 39. OUTPUT P1dB

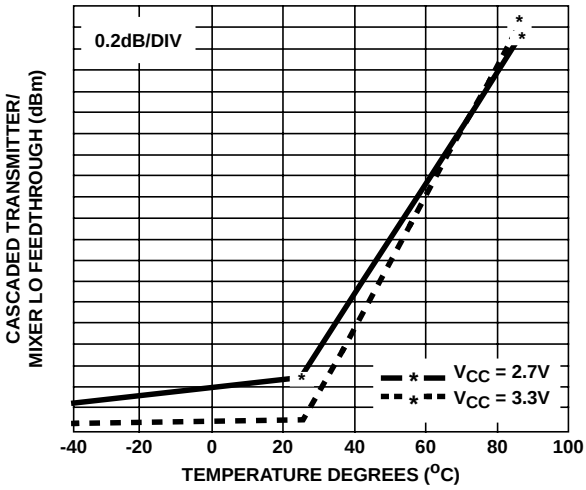
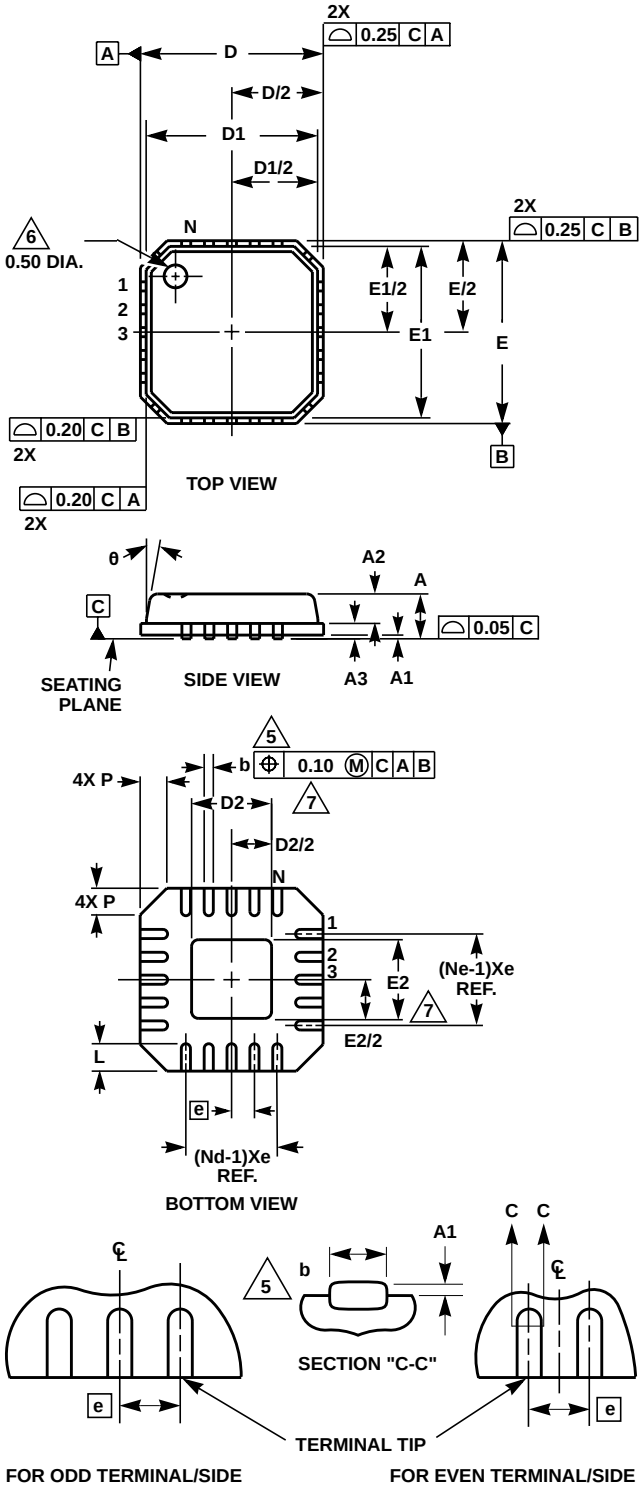


FIGURE 40. LO TO TRANSMIT AMP OUTPUT FEEDTHROUGH (CASCADED, NO FILTER)

Micro Lead Frame Plastic Package (MLFP)



L44.7x7

44 LEAD MICRO LEAD FRAME PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220-VKKD-1 ISSUE A)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.039	-	1.00	
A1	-	0.002	-	0.05	
A2	-	0.031	-	0.80	
A3	0.008 REF		0.20 REF		
b	0.007	0.012	0.18	0.30	5
D	0.275 BSC		7.00 BSC		
D1	0.265 BSC		6.75 BSC		
D2	-	0.130	-	3.30	7
E	0.275 BSC		7.00 BSC		
E1	0.265 BSC		6.75 BSC		
E2	-	0.130	-	3.30	7
e	0.019 BSC		0.50 BSC		
L	0.019	0.029	0.50	0.75	
N	44		44		2
Nd	11		11		3
Ne	11		11		3
P	0.009	0.024	0.24	0.60	
θ	-	12	-	12	

Rev. 1 8/00

NOTES:

1. Dimensioning and tolerancing per ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd is the number of terminals in the X direction, and Ne is the number of terminals in the Y direction.
4. Controlling dimension: Millimeters. Converted dimensions to inches are not necessarily exact. Angles are in degrees.
5. Dimension b applies to the plated terminal and is measured between 0.20mm and 0.25mm from the terminal tip.
6. The Pin #1 identifier exists on the top surface as an indentation mark in the molded body.
7. Dimensions D2 and E2 are the maximum exposed pad dimensions for improved grounding and thermal performance.