PRELIMINARY DATA SHEET

SDA 9400 SCARABAEUS

Scan Rate Converter using Embedded DRAM Technology Units

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MICRONAS

Document Change Note

DS[1]	Date	Section/ Page	Changes compared to previous issue	Department
	12.01.99		Changes to the previous issue Version 03, Edition 05/98 are marked with a change bar	HL IV CE
	05.05.99	page 86	ESD CDM model added, -1.5 kV, ..., 1,5 kV	IV CE
	26.04.00	all	**Preliminary Data Sheet Version 01, Edition 04/00** update new logo, removal of change bars	CNP HN PD

1)... DS = Document state, compares to block 4 of document number

1 General description

The SDA 9400 is a new component of the Micronas MEGAVISION® IC set in a 0.35 µm embedded DRAM technology (frame memory embedded). The SDA 9400 is pin compatible to the SDA 9401 (field memory embedded). The SDA 9400 comprises all main functionalities of a digital featurebox in one monolithic IC.

The scan rate conversion to 100/120 Hz interlaced (50/60 Hz progressive) is based on a motion adaptive algorithm. The scan rate converted picture can be vertically expanded. The SDA 9400 has a freerunning mode, therefore features like scan rate conversion to e.g. 70, 75 Hz with joint lines or multiple picture display (e.g. tuner scan) are possible.

Due to the frame based signal processing, the noise reduction has been greatly improved. Furthermore separate motion detectors for luminance and chrominance have been implemented. For automatic controlling of the noise reduction parameters a noise measurement algorithm is included, which measures the noise level in the picture or in the blanking period. In addition a spatial noise reduction is implemented, which reduces the noise even in the case of motion. The input signal can be compressed horizontally and vertically with a certain number of factors. Therefore split screen is supported.

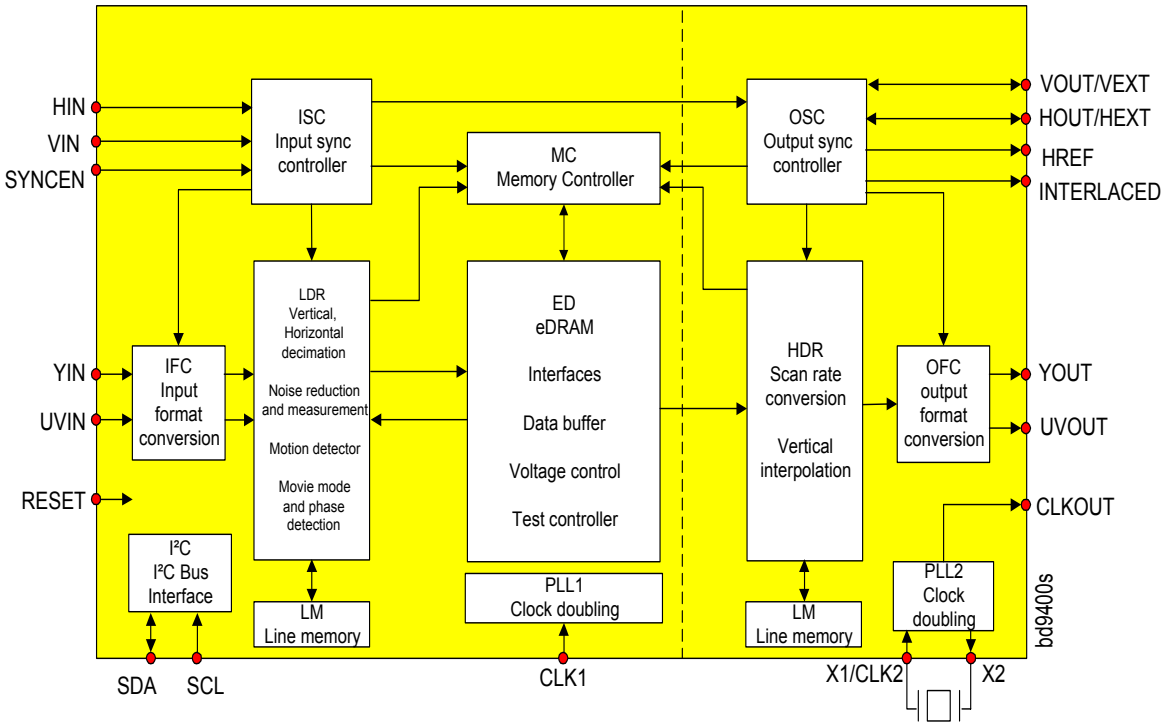
Beside these additional functions like coloured background, windowing and flashing are implemented.

2 Features

- **Two input data formats**
  - 4:2:2 luminance and chrominance parallel (2 x 8 wires)
  - ITU-R 656 data format (8 wires)
- **Two different representations of input chrominance data**
  - 2‘s complement code
  - Positive dual code
- **Flexible input sync controller**
- **Flexible compression of the input signal**
  - Digital vertical compression of the input signal (1.0, 1.25, 1.5, 1.75, 2.0, 3.0, 4.0)
  - Digital horizontal compression of the input signal (1.0, 2.0, 4.0)
- **Noise reduction**
  - Motion adaptive spatial and temporal noise reduction (3D-NR)
  - Temporal noise reduction for luminance frame based or field based
  - Temporal noise reduction for chrominance field based
  - Separate motion detectors for luminance and chrominance
  - Flexible programming of the temporal noise reduction parameters
  - Automatic measurement of the noise level (5 bit value, readable by I²C bus)
- **3-D motion detection**
  - High performance motion detector for scan rate conversion
  - Global motion detection flag (readable by I²C bus)
  - Movie mode and phase detector (readable by I²C bus)

- **TV mode detection by counting line numbers (PAL, NTSC, readable by I²C bus)**
- **Embedded memory**
  - 5 Mbit embedded DRAM core for field memories
  - 192 kbit embedded DRAM core for line memories
- **Flexible clock and synchronization concept**
  - Decoupling of the input and output clock system possible
- **Scan rate conversion**
  - Motion adaptive 100/120 Hz interlaced scan conversion
  - Motion adaptive 50/60 Hz progressive scan conversion
  - Simple static interlaced and progressive conversion modes for 100/120 Hz interlaced or 50/60 Hz progressive scan conversion: e.g. ABAB, AABB, AA*B*B, AAAA, BBBB, AB, AA*
  - Simple progressive scan conversion with joint lines: 50 Hz -> 60, 70, 75 Hz progressive 60 Hz -> 70, 75 Hz progressive
  - Large area and line flicker reduction
- **Flexible digital vertical expansion of the output signal (1.0, ... [1/32] ... , 2.0)**
- **Flexible output sync controller**
  - Flexible positioning of the output signal
  - Flexible programming of the output sync raster
  - External synchronization by backend IC possible (e.g. split screen for one TV channel with joint lines and one PC VGA channel)
- **Signal manipulations**
  - Insertion of coloured background
  - Vertical and/or horizontal windowing with four different speed factors
  - Flash generation (for supervising applications, motion flag readable by I²C bus)
  - Still frame or field
  - Support of split screen applications
  - Multiple picture display - Tuner scan (4 and 16 times for 4:3, 12 times for 16:9 tubes)
  - Support of multi picture display with PIP or front-end processor with integrated scaler (e.g. 9 times display of PIP pictures, picture tracking, random pictures, still-in-moving picture, moving-in-still picture)
- **I²C-bus control (400 kHz)**
- **P-MQFP-64 package**
- **3.3 V ± 5% supply voltage**

3 Block diagram



The SDA 9400 contains the blocks, which will be briefly described below:

ISC - Flexible input sync controller

IFC - Input format conversion

LDR - Low data rate processing (noise reduction and measurement, vertical compression, horizontal compression, motion detector for scan rate conversion, movie mode and phase detector)

MC - Memory controller

OSC - Flexible output sync controller

OFC - Output format conversion

HDR - High data rate processing (scan rate conversion, vertical expansion)

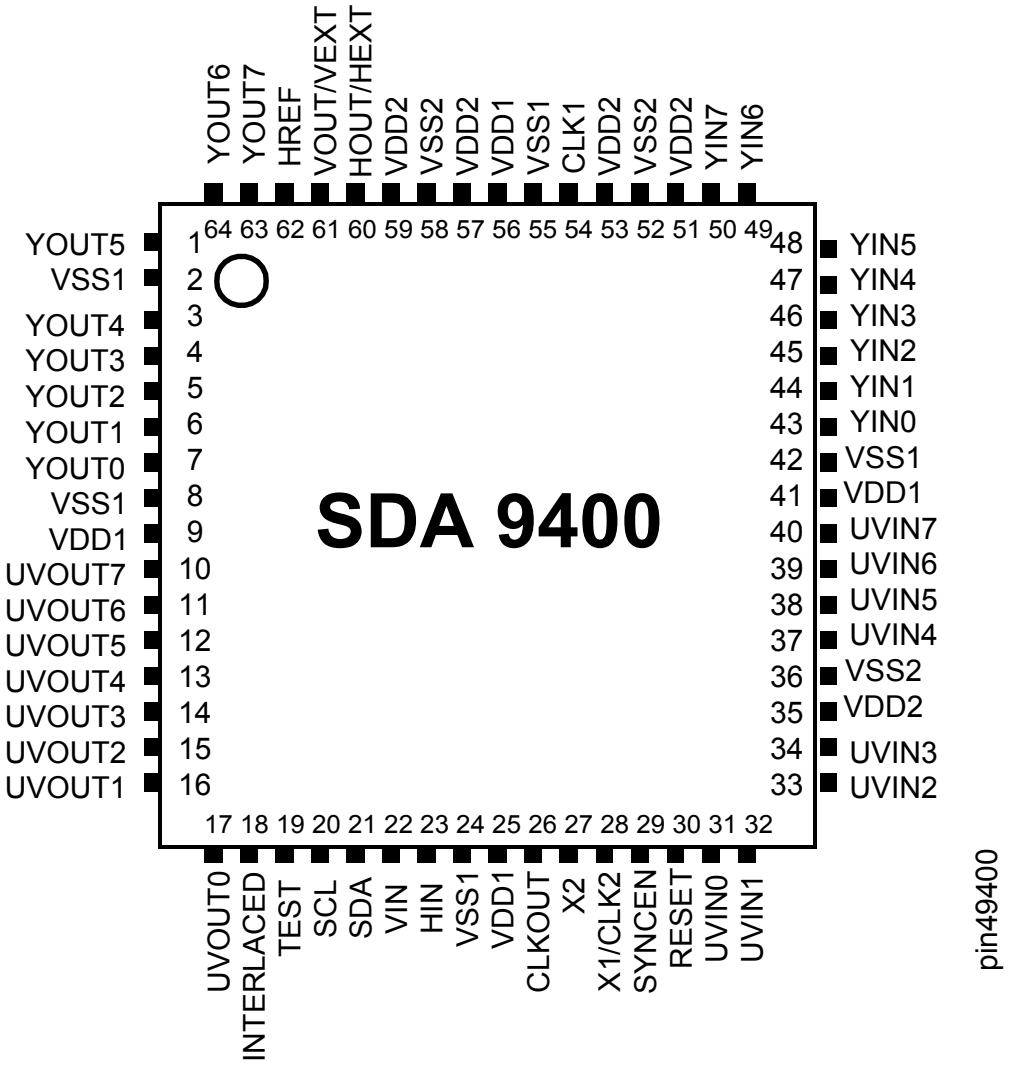
I²C - I²C bus interface

PLL1/2 - PLL for frequency doubling

LM - Line memory core

ED - eDRAM core

4 Pin configuration



5 Pin description

Pin No.	Name	Type	Description
2,8,24,42,55	VSS1	S	Supply voltage (V_{SS} = 0 V)
9,25,41,56	VDD1	S	Supply voltage (V_{DD} = 3.3 V)
36,52,58	VSS2	S	Supply voltage (V_{SS} = 0 V)
35,51,53,57, 59	VDD2	S	Supply voltage (V_{DD} = 3.3 V)
43,..,50	YIN0...7	I/TTL	Data input Y (see input data format)
31,..,34;37,..., 40	UVIN0...7	I/TTL PD	Data input UV (for 4:2:2 parallel, see input data format) (for CCIR 656, see input data format)
30	RESET	I/TTL	System reset. The RESET input is low active. In order to ensure correct operation a **"**Power On Reset**"** must be performed. The RESET pulse must have a minimum duration of two clock periods of the system clock CLK1.
23	HIN	I/TTL PD	H-Sync input (only for full CCIR 656)
22	VIN	I/TTL PD	V-Sync input (only for full CCIR 656)
29	SYNCEN	I/TTL	Synchronization enable input
21	SDA	I/O	I^2C-Bus data line (5V ability)
20	SCL	I	I^2C-Bus clock line (5V ability)
54	CLK1	I/TTL	System clock 1
17,..,10	UVOUT0...7	O/TTL	Data output UV (see output data format)
7,..,3;1;64;63	YOUT0...7	O/TTL	Data output Y (see output data format)
62	HREF	O/TTL	Horizontal active video output
61	VOUT/ VEXT	I/O/ TTL	EXSYN=0 (I²C-bus parameter): V-Sync output EXSYN=1: External V-Sync input for output part
60	HOUT/ HEXT	I/O/ TTL	EXSYN=0 (I²C-bus parameter): H-Sync output EXSYN=1: External H-Sync input for output part
18	INTERLACED	O/TTL	Interlace signal for AC coupled vertical deflection
28	X1 / CLK2	I/TTL	Crystal connection / System clock 2
27	X2	O/ANA	Crystal connection
26	CLKOUT	O/TTL	Clock output (depends on I²C parameters CLK11EN, CLK21EN, FREQR, see also *Clock concept* on Page 37)
19	TEST	I/TTL	Test input, connect to V_{SS} for normal operation

S: supply, I: input, O: output, TTL: digital (TTL)

ANA: analog PD: pull down

6 System description

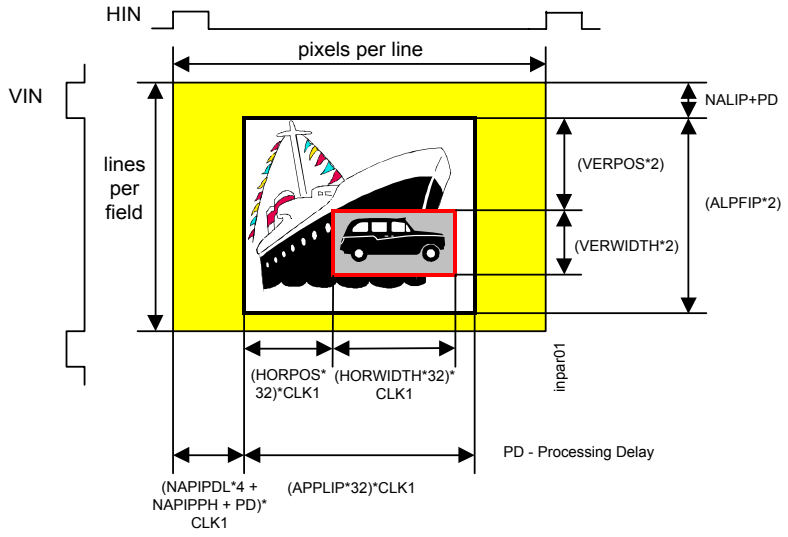
6.1 Input sync controller (ISC)

Input signals

Signals	Pin number	Description
HIN	23	horizontal synchronization signal (polarity programmable, I²C bus parameter 01h HINPOL, default: high active)
VIN	22	vertical synchronization signal (polarity programmable, I²C bus parameter 01h VINPOL, default: high active)
SYNCEN	29	enable signal for HIN and VIN signal, low active (see also *Input format conversion (IFC)* on page 15)

The input sync controller derives framing signals from the H- and V-Sync for the input data processing. The framing signals depend on different parameters and mark the active picture area.

Input parameter



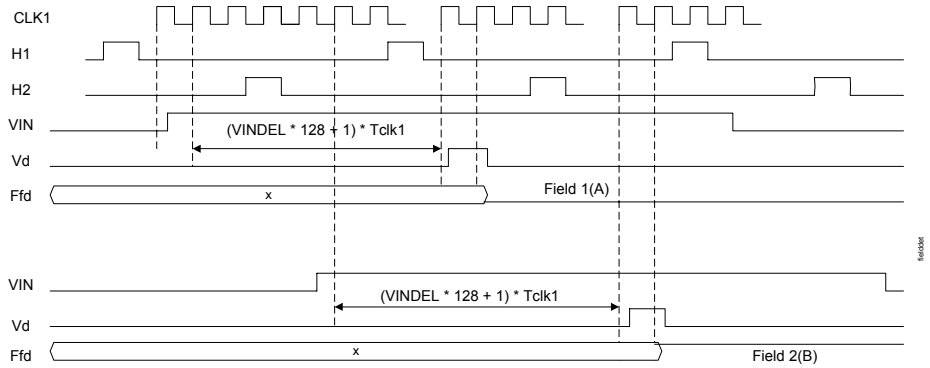
The distance between the incoming H-syncs in system clocks of clk1 must be even.

Input write parameter

Parameter [Default value]	Subaddress	Description
NALIP [20]	02h	Not Active Line InPut defines the number of lines from the V-Sync to the first active line of the field
ALPFIP [144]	03h	Active Lines Per Field InPut defines the number of active lines
NAPLIP NAPIPDL [0] NAPIPPH [0]	00h, 04h	Not Active Pixels Per Line InPut defines the number of pixels from the H-Sync to the first active pixel of the line. The number of pixels is a combination of NAPIPDL and NAPIPPH.
APPLIP [45]	05h	Active Pixels Per Line InPut defines the number of active pixels
PIMODE 1: on 0: off [0]	00h	Picture Insert MODE allows the insertion of an arbitrary picture with the horizontal and vertical width defined by VERWIDTH and HORWIDTH at the position defined by VERPOS and HORPOS
VERPOS [0]	08h	VERtical POSition defines the number of lines from the first active line to the first active line of an inserted picture
VERWIDTH [0]	07h	VERtical WIDTH defines the number of lines (vertical width) of an inserted picture
HORPOS [0]	0Ah	HORizontal POSition defines the number of pixels from the first active pixel to the first active pixel of an inserted picture
HORWIDTH [0]	09h	HORizontal WIDTH defines the number of pixels (horizontal width) of an inserted picture

Inside of the SDA 9400 a field detection block is necessary for the detection of an odd (A) or even (B) field. Therefore the incoming H-Sync H1 (delayed HIN signal, delay depends on NAPIPDL and NAPIPPH) is doubled (H2 signal). Depending on the phase position of the rising edge of the VIN signal an A (rising edge between H1 and H2) or B (rising edge between H2 and H1) field is detected. For proper operation of the field detection block, the VIN must be delayed depending on the delay of the HIN signal (H1). The figure below explains the field detection process and the functionality of the VINDEL parameter (inside the SDA 9400 the delayed VIN signal is called Vd and the detected field signal is called Ffd).

Field detection and VIN delay



Input write parameter

Parameter [Default value]	Subaddress	Description
VINDEL [0]	01h	Delay of the incoming V-Sync VIN (must be adjusted depending on the delay of the HIN signal)
FIEINV 1: Field A=1 0: Field A=0 [0]	00h	Inversion of the internal field polarity
VCRMODE 1: on 0: off [1]	00h	In case of non standard interlaced signals (VCR, Play-Stations) a filtering of the internal field signal has to be done (should also be used for normal TV signals)

In case of non-standard signals the field order is indeterminate (e.g. AAA... , BBB... , AAABAAAB..., etc.). Therefore a special filtering algorithm is implemented, which can be switched on by the parameter VCRMODE. It is recommended to set the parameter VCRMODE=1. In other case (VCRMODE=0) an additional internal signal VTSEQ is generated. This signal goes high (VTSEQ=1), if at least the last two fields were identical. Due to the fixed storage places of the fields in the internal memory block, this information is necessary for the scan rate conversion processing (see also *Output sync controller (OSC)* on page 40, it is recommended in case of VCRMODE=0 to choose an adaptive operation mode).

The OPDEL parameter is used to adjust the outgoing V-Sync VOUT in relation to the incoming delayed V-Sync VIN. In case of 50 Hz to 100 Hz interlaced scan rate conversion the OPDEL parameter should be greater than half the number of lines of a field plus the internal processing delay (8 lines).

Input write parameter

Parameter [Default value]	Subaddress	Description
OPDEL [170]	06h	Delay (in number of lines) of the internal V-Sync (delayed VIN) to the outgoing V-Sync (VOUT)

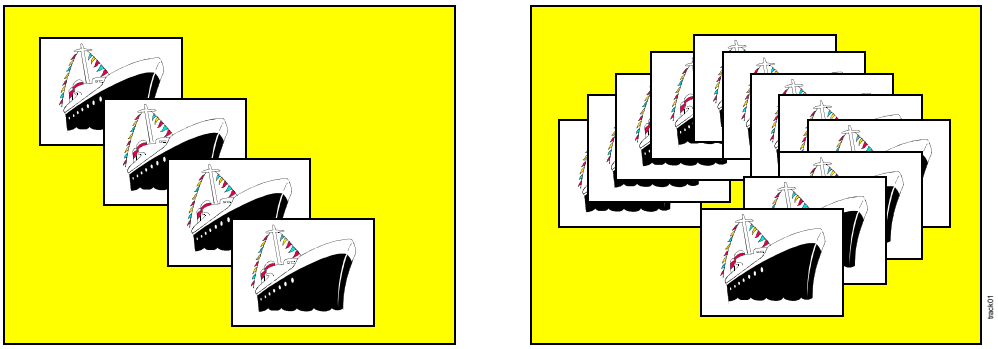
The internal line counter is used to determine the information about the standard of the incoming signal.

Input read parameter

Parameter	Subaddress	Description
TVMODE	33h	TV standard of the incoming signal: 1: NTSC 0: PAL

The figure below shows applications of the picture insert mode. For this feature an additional PIP circuit (e.g. SDA 9388, SDA 9488/89) is necessary. Together with the PIP IV circuit (SDA 9488/89) also split screen applications like double window are possible. In the picture insert mode motion adaptive scan rate conversion modes (e.g. Soft Mix I) are not supported (see also *Operation mode generator* on page 46). The compression of the inserted picture has also be done by the external PIP or front-end processor.

Picture insert mode: application examples picture tracking, random pictures



6.2 Input format conversion (IFC)

Input signals

Signals	Pin number	Description
YIN0...7	43, 44, 45, 46, 47, 48, 49, 50	luminance input
UVIN0...7	31, 32, 33, 34, 37, 38, 39, 40	chrominance input

The SDA 9400 accepts at the input side the sample frequency relations of Y : (B-Y) : (R-Y): 4:2:2 and CCIR 656. In case of CCIR 656 three modes are supported (FORMAT=11 means full CCIR 656 support, including H-, V-Sync and Field signal, FORMAT=01 means only data processing, H- and V-Sync have to be added separately according PAL/NTSC norm, FORMAT=10 means only data processing, H- and V-sync have to be added separately according CCIR656-PAL/NTSC norm). The representation of the samples of the chrominance signal is programmable as positive dual code (unsigned, parameter TWOIN=0) or two's complement code (TWOIN=1, see also *I²C bus format* on page 64, I²C bus parameter 00h). Inside the SDA 9400 all algorithms assume positive dual code.

Input data formats

Data Pin	**CCIR 656 FORMAT = 1X**			**FORMAT = 01**	**4:2:2 Parallel FORMAT = 00**	
YIN7	U_{07}	Y_{07}	V_{07}	Y_{17}	Y_{07}	Y_{17}
YIN6	U_{06}	Y_{06}	V_{06}	Y_{16}	Y_{06}	Y_{16}
YIN5	U_{05}	Y_{05}	V_{05}	Y_{15}	Y_{05}	Y_{15}
YIN4	U_{04}	Y_{04}	V_{04}	Y_{14}	Y_{04}	Y_{14}
YIN3	U_{03}	Y_{03}	V_{03}	Y_{13}	Y_{03}	Y_{13}
YIN2	U_{02}	Y_{02}	V_{02}	Y_{12}	Y_{02}	Y_{12}
YIN1	U_{01}	Y_{01}	V_{01}	Y_{11}	Y_{01}	Y_{11}
YIN0	U_{00}	Y_{00}	V_{00}	Y_{10}	Y_{00}	Y_{10}
UVIN7					U_{07}	V_{07}
UVIN6					U_{06}	V_{06}
UVIN5					U_{05}	V_{05}
UVIN4					U_{04}	V_{04}
UVIN3					U_{03}	V_{03}
UVIN2					U_{02}	V_{02}
UVIN1					U_{01}	V_{01}
UVIN0					U_{00}	V_{00}

X_{ab}: X: signal component a: sample number b: bit number

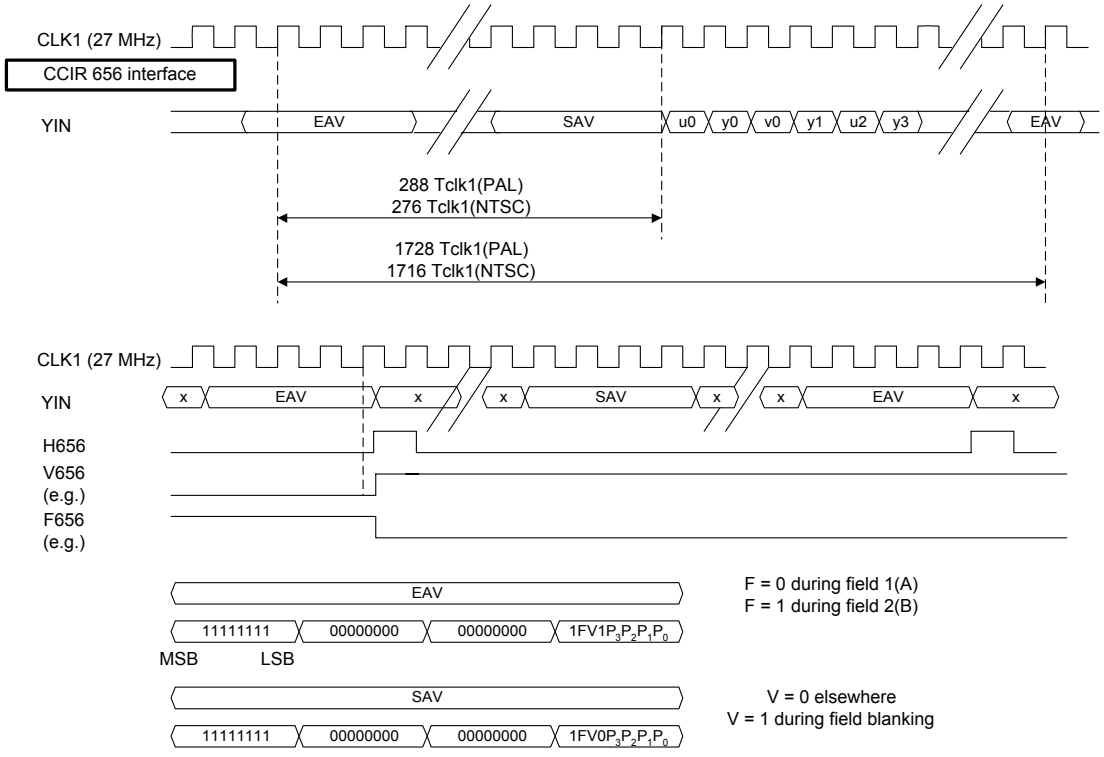
Input sync formats

FORMAT	HIN	VIN	YIN	UVIN
00	PAL/NTSC	PAL/NTSC	4:2:2	4:2:2
01 (CCIR 656 only data)	PAL/NTSC	PAL/NTSC	CCIR 656	x
10	CCIR 656	CCIR 656	CCIR 656	x
11 (full CCIR 656)	x	x	CCIR 656	x

The amplitude resolution for each input signal component is 8 bit, the maximum clock frequency is 27 MHz. Consequently the SDA 9400 is dedicated for application in high quality digital video systems.

The figure below shows the generation of the internal H- and V-syncs in case of full CCIR 656 mode. The H656 sync is generated after the EAV. The V656 and F656 signals change synchronously with the EAV timing reference code.

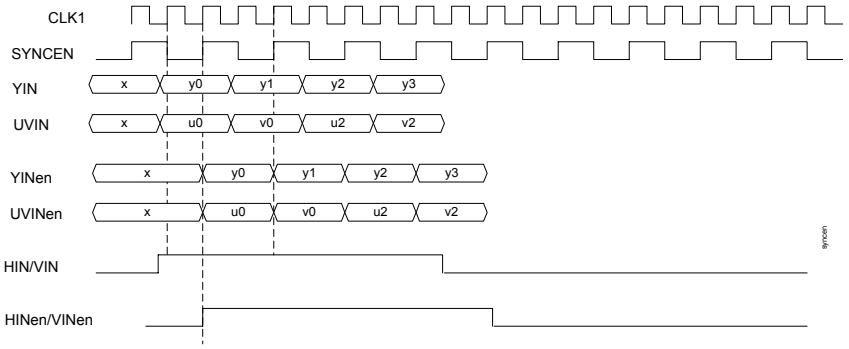
Explanation of 656 format



The figure below explains the functionality of the SYNCEN signal. The SDA 9400 needs the SYNCEN (synchronization enable) signal, which is used to gate the YIN, UVIN as well as the HIN and the VIN signal. This is implemented for front-ends which are working with 13.5 MHz and a large

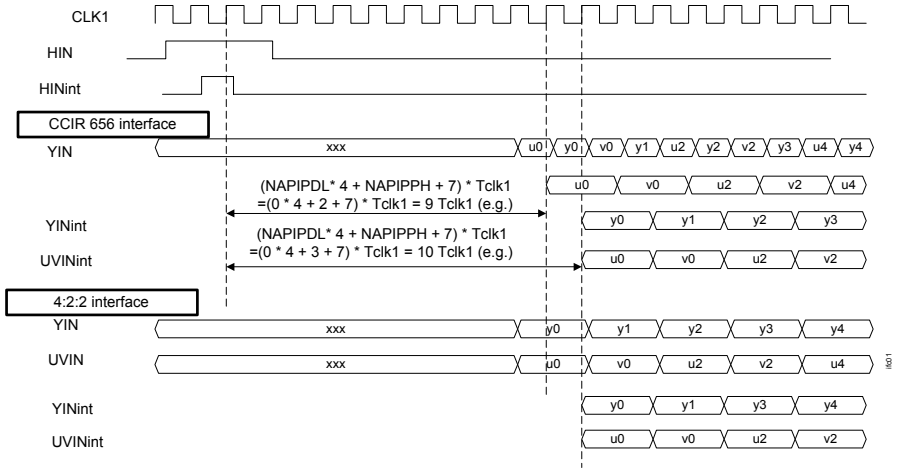
output delay time for YIN, UVIN, HIN and VIN (e.g. Micronas VPC32XX, output delay: 35 ns). For this application the half system clock CLK1 (13.5 MHz) from the front-end should be provided at this pin. In case the front-end is working at 27.0 MHz with sync signals having delay times smaller than 25 ns, this input can be set to low level (SYNCEN=V_{SS}) (e.g. Micronas SDA 9206, output delay: 25 ns). Thus the signals YIN, UVIN, HIN and VIN are sampled with the CLK1 system clock when the SYNCEN input is low.

SYNCEN signal



The figure below shows the input timing and the functionality of the NAPIPDL and NAPIPPH parameter in case of CCIR 656 and 4:2:2 parallel data input format for one example. The signals HINint, YINint and UVint are the internal available sampled input signals.

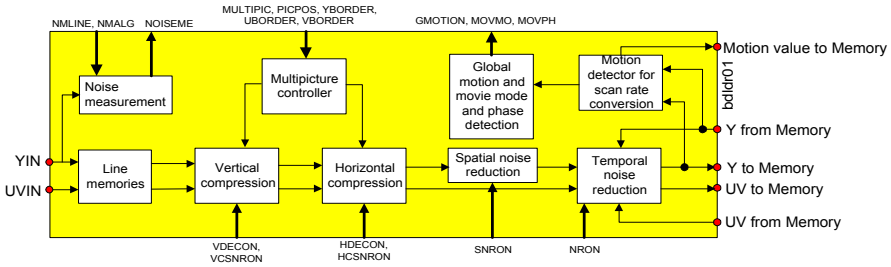
Input timing



6.3 Low data rate processing

The next figure shows the block diagram of the low data rate processing block. The input signal can be vertically and horizontally compressed by a limited number of factors. In case of multipicture mode the internal Multipicture controller will use both compression blocks to control the different modes. Furthermore the input signal can be processed by different noise reduction algorithms to reduce the noise in the signal. A motion detector calculates motion values for a motion adaptive scan rate conversion processing. The movie mode and phase detector determines the information, whether the input signal is a camera scene or movie scene. The global motion detector derives a one bit signal, which indicates that the input signal is a still picture or a moving picture. The noise measurement block determines the noise level of the input signal.

Block diagram of low data rate processing



The different blocks and the corresponding parameters will be described now in more detail.

6.3.1 Vertical compression

The vertical compression compresses the incoming signal vertically by a constant factor given by the parameter VDECON. For the Y and UV signal different filter characteristics are used. The vertical compression can be switched off. For the multipicture modes the factors VDECON 2, 3 and 4 are necessary. Different filter characteristics are used for the factors 3 and 4. High quality vertical compression for double window applications is possible, because the filter characteristic is optimized for the factor 1.5.

The table below shows the relation between the parameter VDECON and the compression factor.

Input write parameter: VDECON

VDECON (1Ch)	
0	Vertical compression off
1	Factor 1.25
2	Factor 1.5
3	Factor 1.75
4	Factor 2.0
5	Factor 3.0
6	Factor 4.0
7	not defined

Inside the SDA 9400 the number of active lines per field depends on the chosen vertical compression factor VDECON (see also *Output sync controller (OSC)* on page 40).

6.3.2 Horizontal compression

The horizontal compression compresses the incoming signal horizontally by a constant factor. For the Y and UV signal the same filter characteristics are used. The horizontal compression can be switched off.

The table below shows the relation between the parameter HDECON and the compression factor.

Input write parameter: HDECON

HDECON (1Ch)	
00	no horizontal compression
01	factor 2
10	factor 4
11	not defined

The APPLIP (Active Pixels Per Line Input, see also *Input sync controller (ISC)* on page 11) value defines the length of an active line. Inside the SDA 9400 the number of active pixels per line is APPL (Active Pixels Per Line) and its value depends on the chosen horizontal compression factor HDECON. The table below explains the connection between APPL and APPLIP (see also *Output sync controller (OSC)* on page 40).

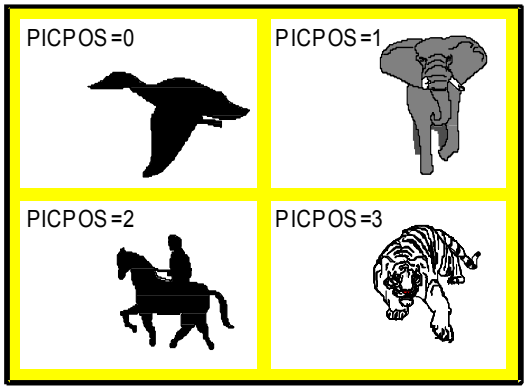
Connection between APPL and APPLIP

Mode	APPL
no horizontal compression (HDECON = ’00’)	APPLIP
horizontal compression, Factor 2 (HDECON = ’01’)	(APPLIP + 1) / 2
horizontal compression, Factor 4 (HDECON = ’10’)	(APPLIP + 3) / 4
MULTIPIC > ’0’ (dominant, see also *Multipicture display* on page 20)	45

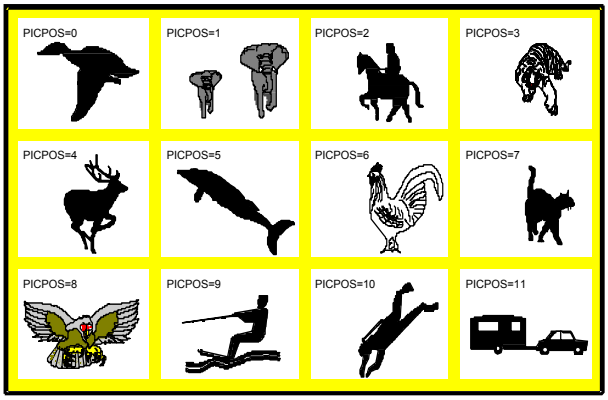
6.3.3 Multipicture display

The figures below show the different “multi picture modes” as they are represented on the display.

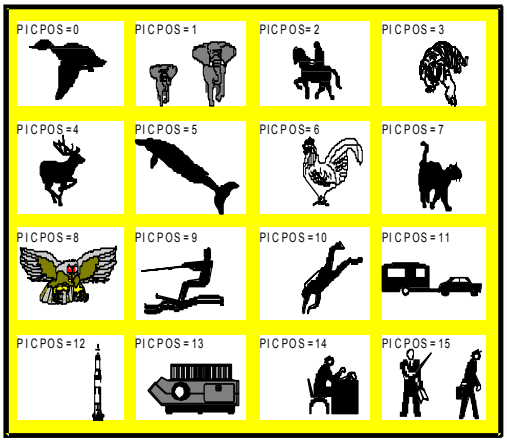
Fourfold multi picture



Twelvefold multi picture



Sixteenfold multi picture



The three different “multi picture modes” can be selected by the parameter MULTIPIC. MULTIPIC=0 defines normal operation without compression. The table below explains the performed compressions depending on the “multi picture mode” and the corresponding aspect ratio of the display.

Input write parameter: MULTIPIC

MULTIPIC (1Bh)	Horizontal compression	Vertical compression	Aspect ratio of the display
00 (Multi Picture Off)	normal operation, no compression		
01 (fourfold)	2 : 1	2 : 1	4 : 3
10 (twelvefold)	4 : 1	3 : 1	16 : 9
11 (sixteenfold)	4 : 1	4 : 1	4 : 3

To get a “multi picture display” the following executions must be performed:
Entering a “multi picture mode” is defined by transmitting a value MULTIPIC>0. This value of MULTIPIC must not be equal to the previous value of MULTIPIC. During the following two fields the memory will be completely filled with a constant colour defined by the parameters YBORDER, UBORDER, VBORDER. This colour is identical to the background and the borders of the multi picture display. The same procedure is performed when the “multi picture mode” changes from a value MULTIPIC>0 to another value MULTIPIC>0. Beginning with the following field the compressed input picture is written at the position PICPOS addressed via I²C-bus. The user has to address all possible positions PICPOS one after the other to build a complete multi picture display. In sequence, the background colour is replaced by the small pictures. The not overwritten areas of the background colour form the borders of the multi picture display.

The pictures can be taken from the same source (’Shots of a Sequence’) or from different sources (’Tuner Scanning’). The actual addressed picture is moving until “Freeze mode” is activated.

Before entering “multi picture mode” the “H-and-V-freerunning mode” (see also *Output sync controller (OSC)* on page 40) should be activated via the I²C bus bits HOUTFR and VOUTFR, especially when “Tuner Scanning” will be performed. The “H-and-V-freerunning mode” avoids synchronization problems of the display during changing the tuner channel.

The values of ALPFIP (Active Lines Per Field Input, see also *Input sync controller (ISC)* on page 11), and ALPFOP (Active Lines Per Field Output, see also *Output sync controller (OSC)* on page 40) must be set to 144 or 121, respectively. Only these standard signals corresponding to PAL and NTSC systems are supported. A mixture of PAL and NTSC signals is also possible.

Input write parameter

Parameter	Subaddress	Description
MULTIPIC	1Bh	Defines the multi picture modes
PICPOS	1Bh	Position of the picture in the multi picture mode (only valid for MULTIPIC>0)
YBORDER	17h	Y background value
UBORDER	18h	U background value

Parameter	Subaddress	Description
VBORDER	18h	V background value
FREEZE 1: on 0: off	1Bh	Freeze mode (frozen picture)

The 100 Hz conversion mode should be AABB, AAAA or BBBB for DC coupled deflection units and AA*B*B, AAAA or BBBB for AC coupled deflection units as explained in the following table. For progressive conversion the A+A* or B+B* modes are recommended. Motion values are not calculated in “multi picture mode”. A*, B* mean raster interpolated fields (not motion adaptive, see also *Operation mode generator* on page 46).

Interlaced and progressive conversion in multi picture mode

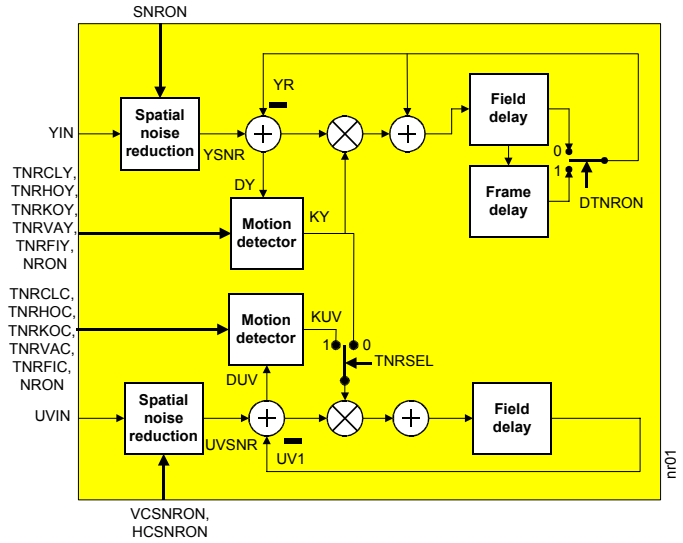
STOPMODE	RMODE	Raster Sequence	Comment
0000 (ABAB mode I interlaced)	0	αβαβ (100/120 Hz)	Motion blur possible
0001 (AA*B*B mode I interlaced)	0	αβαβ (100/120 Hz)	reduced vertical resolution
0010 (AABB mode I interlaced)	0	ααββ (100/120 Hz)	recommended
0100 (Multipicture mode I, AAAA)	0	αβαβ (100/120 Hz)	recommended
0101 (Multipicture mode II, BBBB)	0	αβαβ (100/120 Hz)	recommended
0110 (AAAA mode)	0	αααα (100/120 Hz)	recommended
0111 (BBBB mode)	0	ββββ (100/120 Hz)	recommended
0000, 0100, 0110 (AB modeI, progressive)	1	α+β, α+β (50/60 Hz)	Motion blur possible
0001, 0101 (AA* mode I-II, progressive)	1	α+β, α+β (50/60 Hz)	recommended
0111 (B*B mode, progressive)	1	α+β, α+β (50/60 Hz)	recommended

The borders are fixed to a width of 16 pixels in horizontal direction. In vertical direction the border widths are also fixed, the number of lines, however, depends on the TV standard of the input and the display.

6.3.4 Noise reduction

The figure below shows a block diagram of the spatial and temporal motion adaptive noise reduction (first order IIR filter). The spatial noise reduction of the luminance differs from the spatial noise reduction of the chrominance. The structure of the temporal motion adaptive noise reduction is the same for the luminance as for the chrominance signal.

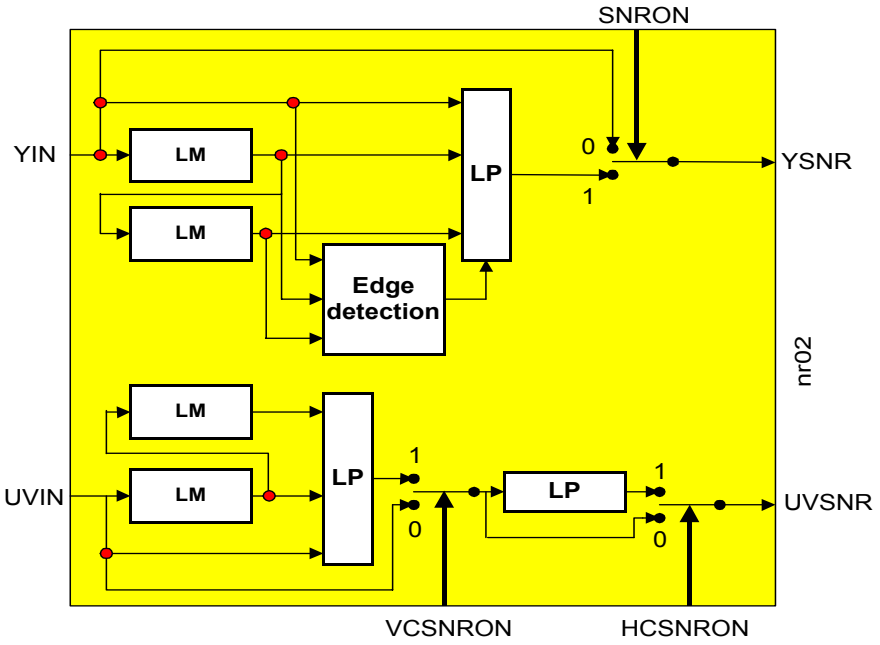
Block diagram of noise reduction



6.3.4.1 Spatial noise reduction

Normally a spatial noise reduction reduces the resolution due to the low pass characteristic of the used filter. Therefore the spatial noise reduction of the SDA 9400 works adaptive on the picture content. The low pas filter process is only executed on a homogeneous area. That's why an edge detection controls the low pass filter process and depending on the result of the edge detection the pixels for the low pass filter are chosen. The next figure shows a block diagram of the spatial noise reduction. For the UV signal only a simple spatial noise reduction algorithm (vertical and/or horizontal low pass filtering) is implemented.

Block diagram of spatial noise reduction



Input write parameter

Parameter	Subaddress	Description
SNRON 1: on 0: off	1Dh	Spatial noise reduction of luminance signal
VCSNRON 1: on 0: off	1Dh	Vertical spatial noise reduction of chrominance
HCSNRON 1: on 0: off	1Dh	Horizontal spatial noise reduction of chrominance

In case of VDECON>0 or HDECON>0 or MULTIPIC>0 (see also *Vertical compression* on page 18, see also *Horizontal compression* on page 19, see also *Multipicture display* on page 20) spatial noise reduction is not possible.

6.3.4.2 Motion adaptive temporal noise reduction

The equation below describes the behaviour of the temporal adaptive noise reduction filter. The same equation is valid for the chrominance signal. Depending on the motion in the input signal, the K-factor Ky (Kuv) can be adjusted between 0 (no motion) and 15 (motion) by the motion detector. The K-factor for the chrominance filter can be either Ky (output of the luminance motion detector, TNRSEL=0) or Kuv (output of the chrominance motion detector, TNRSEL=1). For the luminance

signal the delay of the feed back path can be either a field delay (DTNRON=0) or a frame delay (DTNRON=1) (block diagram of noise reduction).

Equation for temporal noise reduction (luminance signal)

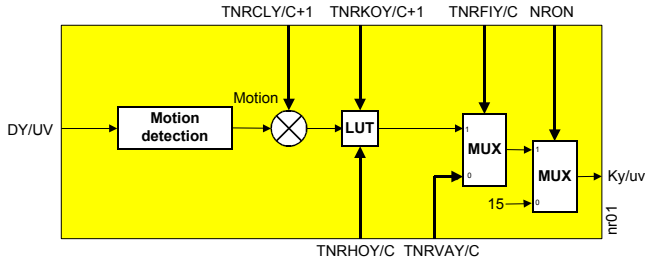
$$YOUT = \left(\frac{1+Ky}{16}\right)(YSNR - YR) + YR$$

Equation for temporal noise reduction (chrominance signal)

$$UVOUT = \left(\frac{1+K}{16}\right)(UVSNR - UV1) + UV1; K = (Ky; Kuv)$$

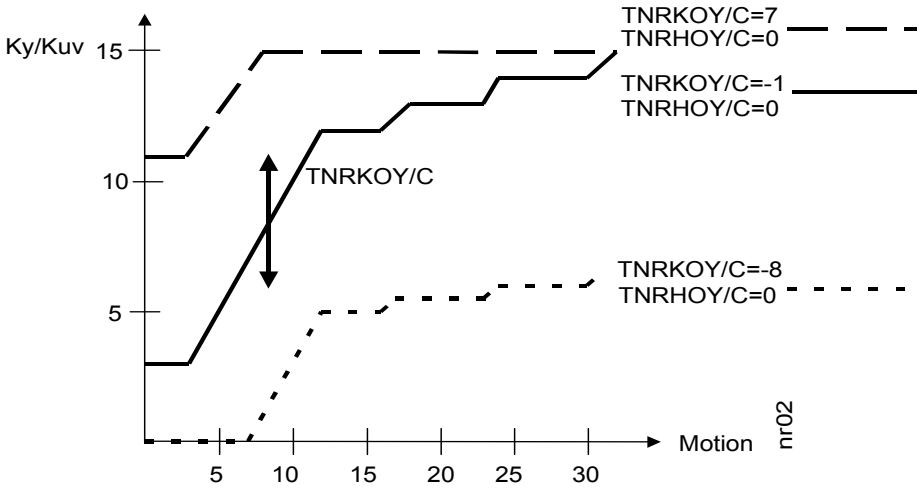
The next figure shows the motion detector in more detail. Temporal noise reduction can be switched off by NRON (NRON=0). The parameter TNRFIY/C switches between a fixed noise reduction K-factor TNRVAY/C (TNRFIY/C=0) or a motion adaptive noise reduction K-factor (TNRFIY/C=1).

Block diagram of motion detector

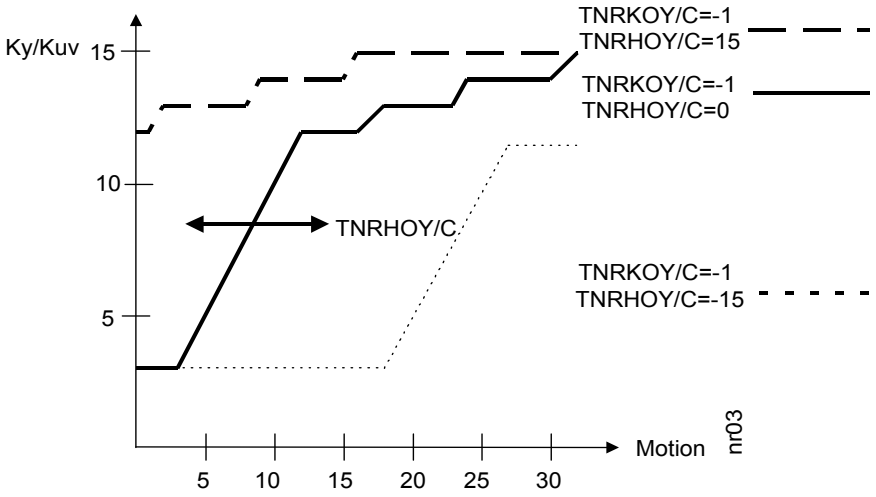


In case of adaptive noise reduction the K-factor depends on the detected “Motion” (see figure above). The “Motion”-Ky/Kuv characteristic curve (LUT) is fixed inside the SDA 9400, but the characteristic curve can be changed by two parameters: TNRHOY/C and TNRKOY/C. TNRHOY/C shifts the curve horizontally and TNRKOY/C shifts the curve vertically. For a fixed characteristic curve, the sensitivity of the motion detector is adjustable by TNRCLY/C.

LUT for motion detection I



LUT for motion detection II



Parameter TNRVAY/C

Parameter	0 (minimum value)	15 (maximum value)
TNRVAY/C	strong noise reduction (not motion adaptive, Ky/K=0)	no noise reduction (not motion adaptive, Ky/K=15)

Parameter TNRHOY/C and TNRKOY/C

Parameter	Range
TNRHOY/C	-32, ... , 31
TNRKOY/C	-8, ..., 7

Parameter TNRCLY

Parameter	0 (minimum value)	15 (maximum value)
TNRCLY/C	maximum sensitivity for motion -> strong noise reduction	minimum sensitivity for motion -> weak noise reduction

Input write parameter

Parameter	Subaddress	Description
TNRSEL 1: separate 0: luminance motion detector	1Dh	Switch for motion detection of temporal noise reduction of chrominance signal
DTNRON 1: frame 0: field	1Dh	Delay for temporal noise reduction of luminance signal
TNRFIY/C 1: off 0: on	21h/22h	Switch for fixed K-factor value defined by TNRVAY/C
TNRVAY/C	20h	Fixed K-factor for temporal noise reduction of luminance/chrominance
TNRHOY/C	21h/22h	Horizontal shift of the motion detector characteristic
TNRKOY/C	1Fh	Vertical shift of the motion detector characteristic
TNRCLY/C	1Eh	Classification of temporal noise reduction

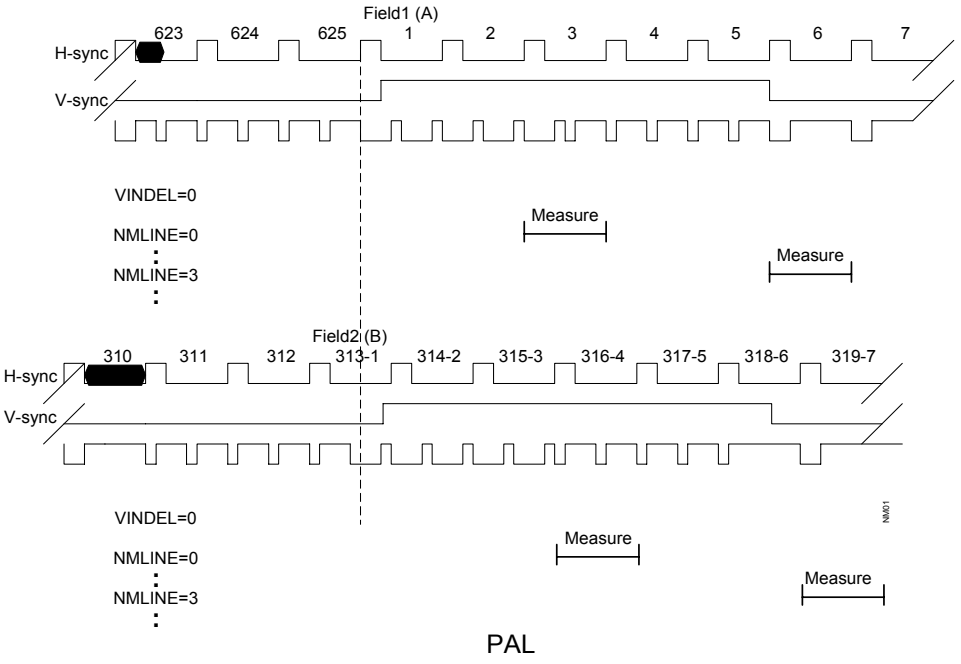
6.3.5 Noise measurement

The noise measurement algorithm can be used to change the parameters of the temporal noise reduction processing depending on the actual noise level of the input signal. This is done by the I²C-bus controller which reads the NOISEME value, and sends depending on this value different parameter sets to the temporal noise reduction registers of the SDA 9400. The NOISEME value can be interpreted as a linear curve from no noise (0) to strong noise (30). Value 31 indicates an overflow status and can be handled in different ways: strong noise or measurement failed.

Two measurement algorithms are included, which can be chosen by the parameter NMALG. In case NMALG=1 the noise is measured during the vertical blanking period in the line defined by NMLINE. For NMALG=0 the noise is measured during the first active line. In both cases the value is determined by averaging over several fields.

The figure below shows an example for the noise measurement. The NMLINE parameter determines the line, which is used in the SDA 9400 for the measurement. In case of VINDEL=0 and NMLINE=0 line 3 of the field A and line 316 of the field B is chosen. In case of VINDEL=0 and NMLINE=3 line 6 of the field A and line 319 of the field B is chosen.

Example of noise measurement



PAL

Input write parameter

Parameter	Subaddress	Description
NMALG	1Dh	Noise measurement algorithm 1: measurement during vertical blanking period (measure line can be defined by NMLINE) 0: measurement in the first active line
NMLINE	28h	Line for noise measurement (only valid for NMALG=1)

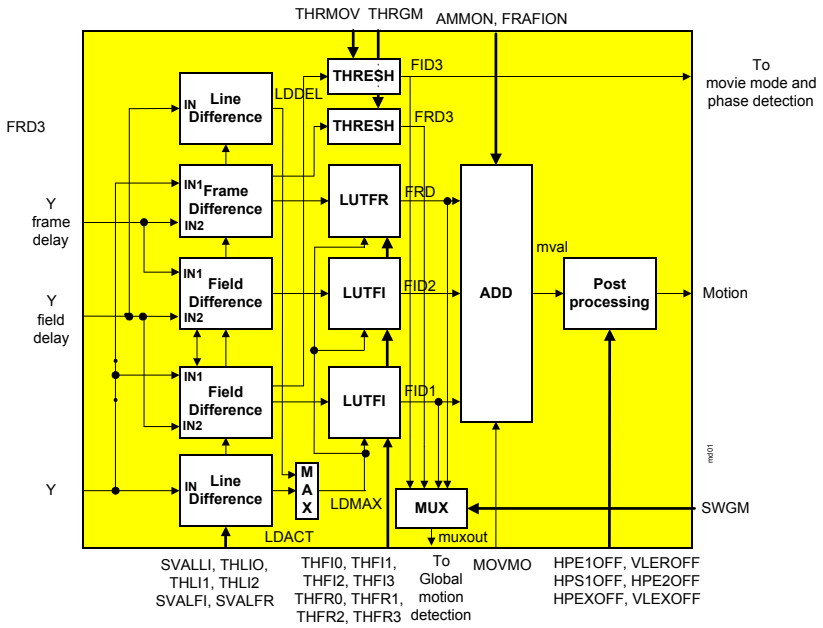
Input read parameter

Parameter	Subaddress	Description
NOISEME	32h	Noise level of the input signal: 0 (no noise), ... , 30 (strong noise) [31 (strong noise or measurement failed)]
NMSTATUS	33h	Signals a new value for NOISEME 1: a new value can be read 0: current noise measurement not finalized (see also *I²C bus format* on page 64)

6.3.6 Motion detection for scan rate conversion

The motion detection for scan rate conversion results in a motion value for each pixel. The motion values are stored within the main memory block, read out at the high data rate and used for the scan rate conversion. The motion detection works on luminance data. In case of VDECON>0 or HDECON>0 the motion detection for scan rate conversion is disabled. The diagram below shows the block diagram of the motion detection. Separate line, field and frame differences are calculated. The result of the differences are fed to separate look up tables. The result FRD of the LUTFR (look up table frame) depends on the frame difference and the line difference (LDMAX). The result of the LUTFI (look up table field) FID1 or FID2 depends on the field difference and the line difference. These three values FRD, FID1 and FID2 determine the motion value mval. The final motion value “Motion” is generated by the postprocessing block. It is possible to alternate the behaviour of the motion detection selecting different parameters, which will be described in detail for each block afterwards.

Block diagram motion detection



Input write parameter

Parameter [Default value]	Subaddress	Description
SVALLI [1]	28h	Sensitivity of line difference
THLI2, THLI1, THLI0 [12, 8, 4]	29h, 2Ah	Threshold of line difference

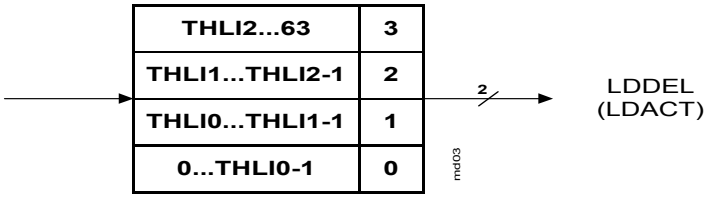
Parameter [Default value]	Subaddress	Description
SVALFI [2]	2Fh	Sensitivity of field difference
THFI3, THFI2, THFI1, THFI0 [28,18,16,8]	2Ah, 2Bh, 2Ch, 2Dh	Threshold of field difference
SVALFR [0]	2Fh	Sensitivity of frame difference
THFR3, THFR2, THFR1, THFR0 [10,6,4,3]	2Dh, 2Eh, 2Fh	Threshold of frame difference
SWGM [1]	31h	Switch for global motion detection
THRGM [8]	31h	Threshold of frame difference for global motion detection
THRMOV [8]	30h	Threshold of field difference for movie mode detection

The maximum line difference LDMAX of the output signals LDACT and LDDEL controls the look up tables LUTFR/LUTFI in the frame and field difference signal processing path. In this way the sensitivity of the field and frame differences are adapted to the picture contents. The sensitivity of the line difference block can be changed by the SVALLI parameter. The line difference will be quantised to a two bit value. The thresholds are programmable by the parameters THLI2, THLI1 and THLI0.

Parameter SVALLI

Parameter	0 (minimum value)	3 (maximum value)
SVALLI	maximum sensitivity line difference	minimum sensitivity line difference

Parameter THLI2, THLI1, THLI0



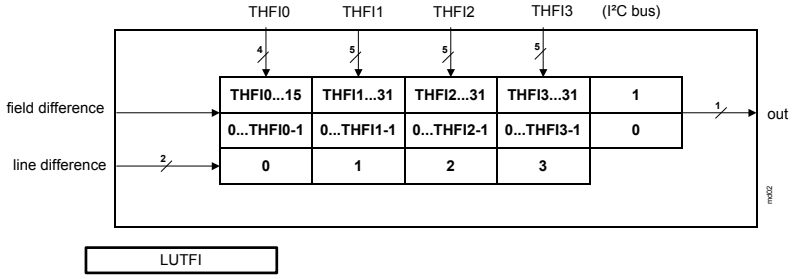
The motion detection calculates two field difference signals and one frame difference signal. The sensitivity of the field difference can be changed by the parameter SVALFI, and the sensitivity of the frame difference can be changed by the parameter SVALFR.

Parameter SVALFI and SVALFR

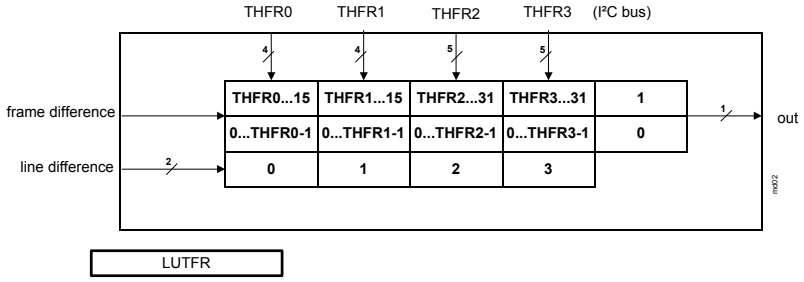
Parameter	0 (minimum value)	3 (maximum value)
SVALFI, SVALFR	maximum sensitivity field/frame difference	minimum sensitivity field/frame difference

The output values of the field and frame difference blocks are mapped to 1 bit signals by three look up tables. The thresholds of the look up tables are programmable. THFI3, THFI2, THFI1, THFI0 control both look up tables for the field differences LUTFI. THFR3, THFR2, THFR1, THFR0 control the look up table for the frame difference LUTFR. The thresholds are selected by the corresponding line difference signals LDACT and LDDEL, respectively as described before.

Parameter THFI3, THFI2, THFI1, THFI0



Parameter THFR3, THFR2, THFR1, THFR0



The output of the look up table LUTFI FID1, the output of the LUTFR FRD, the output of the threshold FID3 and the output of the threshold FRD3 are fed to a multiplexer. The output of the multiplexer is fed to the global motion detection block. The multiplexer can be switched using the I²C bus parameter SWGM. The output of the threshold FID3 is in addition fed to the movie mode and phase detection block (see also *Global motion, movie mode and phase detection* on page 33). The FID3 and FRD3 signal are also one bit signals. Both signals are independent of the parameters described up to now. The FID3 signal depends only on the threshold THRMOV and the FRD3 signal depends only on the threshold THRGM. So it is possible to optimise the movie mode and global

motion detector independent of the settings of the motion detection for scan rate conversion.

Parameter THMOV

FID3	
1	Field difference > THRMOV
0	otherwise

Parameter THRGM

FRD3	
1	Frame difference > THRGM
0	otherwise

Parameter SWGM

muxout	SWGM
FID3	11
FID1	10
FRD3	01
FRD	00

The ADD block combines the outputs of the field and frame differences to a single one bit data stream mval. The combination can be influenced by the parameters AMMON and FRAFION. The output value MOVMO of the movie mode detection block also controls the value mval when the automatic movie mode detection is activated by setting AMMON=1X.

With deactivated automatic movie mode detection (MSB of AMMON=0) FRAFION determines which differences are switched to the output mval. FRAFION=0 means that only the frame difference FRD is used, FRAFION=1 supplies all three differences.

With activated automatic movie mode detection (MSB of AMMON=1) and detected camera mode (MOVMO=0) FRAFION controls mval as described before. If movie mode is detected (MOVMO=1) the LSB of AMMON controls the output mval instead of FRAFION. LSB of AMMON=0 supplies the frame difference and LSB of AMMON=1 sets the output to constant zero.

Behaviour of ADD block

AMMON	MOVMO	FRAFION	mval
0X	X	0	FRD
0X	X	1	FRD + FID1 + FID2
10	1	X	FRD
11	1	X	0

AMMON	MOVMO	FRAFION	mval
1X	0	0	FRD
1X	0	1	FRD + FID1 + FID2

Input write parameter

Parameter	Subaddress	Description
AMMON	1Ch	Automatic movie mode for the motion detection for scan rate conversion
FRAFION	1Ch	Frame or field based motion value for scan rate conversion

The postprocessing block has the task to delete isolated groups of set motion flags (erosion) and to homogenize the motion areas in horizontal and vertical direction that correspond to a moving object (extension, smearing). The table below shows the several parameters in sequence. They can be switched off (1) or on (0). It is recommended to enable all parameters.

Input write parameter

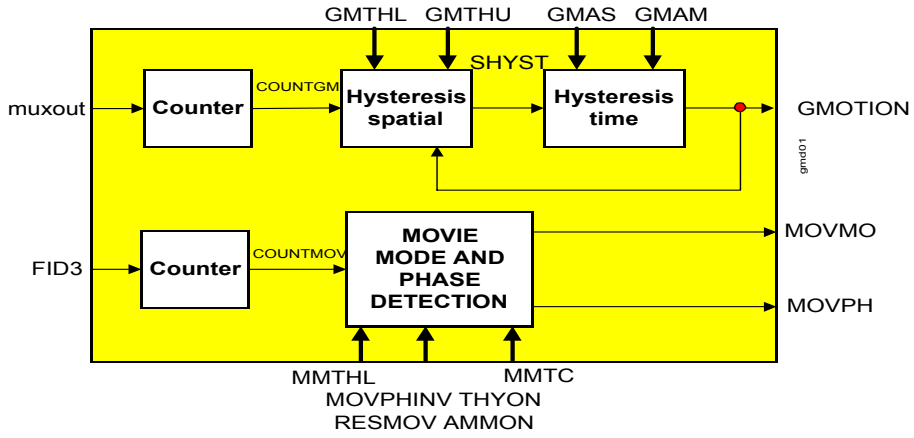
Parameter	Subaddress	Description
HPE1OFF	21h	Horizontal pixel erosion 1
VLEROFF	22h	Vertical line erosion
HPS1OFF	23h	Horizontal pixel smearing 1
HPE2OFF	24h	Horizontal pixel erosion 2
HPEXOFF	25h	Horizontal pixel extension
VLEXOFF	26h	Vertical line extension

6.3.7 Global motion, movie mode and phase detection

The global motion detection is used to generate a global motion value GMOTION. GMOTION is a one bit signal and can be read out by the I²C-bus. GMOTION equal zero means, the complete picture is still, GMOTION equal one means, there is motion in the picture. This value can also be used internal to switch between different scan rate conversion algorithms (see also *Output sync controller (OSC)* on page 40).

Furthermore a movie mode (MOVMO) and phase (MOVPH) detector is included. MOVMO and MOVPH are one bit signals and can be read out by I²C-bus or can be used internal to influence the motion detection for scan rate conversion as well as the scan rate conversion itself (see also *Output sync controller (OSC)* on page 40). The diagram below shows the block diagram of the global motion, movie mode and phase detection algorithm.

Block diagram of global motion, movie mode and phase detection



The muxout and FID3 values (Field difference 1, see also *Motion detection for scan rate conversion* on page 29) are accumulated during each incoming field. After accumulation the value COUNTGM is compared with a threshold TH. It is assumed, that the whole picture is moving, if the accumulated value is greater than the threshold (SHYST=1). Otherwise it will be assumed, that the picture is still (SHYST=0). The threshold TH itself depends on the actual GMOTION value. This is a kind of spatial hysteresis. If the actual GMOTION value is zero, then TH is equal GMTHU. In the other case that GMOTION is one, TH is equal GMTHL.

Behaviour spatial hysteresis

SHYST	
1	COUNT >= TH
0	COUNT < TH

TH	GMOTION
64 * GMTHU	0
64 * GMTHL	1

The time hysteresis block generates the final GMOTION value. The GMOTION value will only changed, if at least the last GMAM/GMAS fields had the same SHYST value.

Behaviour of time hysteresis

GMOTION(T)	
0	last GMAS fields, SHYST were 0

GMOTION(T)	
1	last GMAM fields, SHYST were 1
GMOTION(T-1)	otherwise

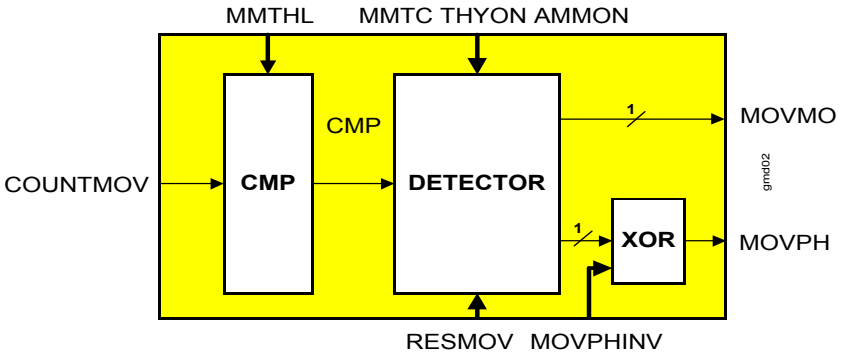
The COUNTMOV value is used in movie mode and phase detector to generate the MOVMO and the MOVPH signal. Movie mode means, that the signal source was a movie (24 Hz progressive), which was translated into a (50 Hz) interlaced signal. Therefore two consecutive fields have the same motion phase. Normally field An and field Bn belong to the same phase. But it is also possible, depending on the translation process, that field Bn-1 and field An belong to the same motion phase. In case of movie mode it is better to switch to an ABAB mode, therefore the information about movie mode and the movie mode phase is important. This information will be used in the motion detection block for scan rate conversion to switch the motion values to zero or to frame difference (depends on the automatic movie mode parameter) or to force the display raster to $\alpha\beta\alpha\beta$ in one of the adaptive operation modes (eg. Field mixer mode). The phase is necessary for the right order of the fields at the output (ABAB mode or BABA mode) (see also *Operation mode generator* on page 46).

COUNTMOV is the result of the accumulation of the FID3 value during one field. This value can be used for the detection of the movie mode. If this value is smaller than a given threshold TH (programmable by the parameter MMTH), both fields may belong to the same phase. The result of the comparison is stored in CMP (see block diagram of movie mode and phase detection below). The difference of the COUNTMOV value of the actual field and the COUNTMOV value of the previous field can be used to switch adaptive the threshold for the movie mode detection. The final MOVMO as well as the MOVPH value is determined by comparison of the results from the last 2*(MMTC+1) CMP values.

If THYON = 0 (Temporal hysteresis off, I²C bus parameter), the time to switch from camera mode to movie mode and vice versa is the same: 2*(MMTC+1) fields. If THYON = 1 (Temporal hysteresis on), the time to switch from camera mode to movie mode differs from the time to switch from movie mode to camera mode. In case THYON = 1 the time to switch from camera to movie mode is 2*(MMTC+1) fields and the time to switch from movie mode to camera is (MMTC+1). So camera mode is preferred.

To reset the movie mode detector e.g. after tuner change, the I²C bus parameter RESMOV exists. If the parameter RESMOV = 1, the MOVMO is set to camera mode (MOVMO=0) and the time hysteresis queue is reset too. RESMOV = 0 means normal behaviour of the movie mode and movie phase detection block.

Block diagram of movie mode and phase detection



The movie mode detection block contains a fall back circuit. This fall back circuit can be enabled by the I²C bus parameter AMMON. If AMMON is set to zero, the fall back counter is disabled. In all other cases the fall back counter is enabled. If the fall back counter is enabled, the failures of the movie mode detector will be counted. So if a certain threshold is reached, the MOVMO will be forced to camera mode.

Behaviour CMP block

CMP	
1	COUNT >= TH
0	COUNT < TH

TH	
32 * MMTH	ABS(COUNT(T)-COUNT(T-1)) < 64* MMTH
64 * MMTH	ABS(COUNT(T)-COUNT(T-1)) >= 64* MMTH

Behaviour of detector block

MOVMO	
1	Movie mode: last 2*(MMTC+1) CMP values were sequence of 0 and 1 or 1 and 0 (e.g. 101010 or 010101)
0	Camera mode: last 2*(MMTC+1) CMP values were 1

MOVPH	
1	field An and field Bn-1 belong to the same phase
0	field An and field Bn belong to the same phase

Input write parameter

Parameter	Subaddress	Description
GMTHU	23h	Global motion detection: upper spatial hysteresis threshold
GMTHL	24h	Global motion detection: lower spatial hysteresis threshold
GMAS	25h	Global motion detection: amount of still pictures
GMAM	26h	Global motion detection: amount of moving pictures

Parameter	Subaddress	Description
MMTC	25h, 26h	Movie mode detection time constant
MMTHL	27h	Movie mode detection threshold
MOVPHINV 1: enabled 0: disabled	1Dh	Inversion of the movie phase signal
THYON	30h	Time hysteresis for movie mode detection on/off: 1: on (camera->movie: 2*(MMTC+1); movie->camera: (MMTC+1)) 0: off (camera<->movie: 2*(MMTC+1))
RESMOV	30h	Reset of movie mode detection time hysteresis queue 1: Reset: MOVMO=0 (camera mode) 0: no reset

Input read parameter

Parameter	Subaddress	Description
GMOTION	33h	Global motion flag: 1 - motion, 0 - still
MOVMO	33h	Movie mode flag: 1 - movie mode, 0 - camera mode
MOVPH	33h	Movie mode phase: field An and field Bn-1 belong to the same phase field An and field Bn belong to the same phase
MDSTATUS	33h	Signals a new value for GMOTION, MOVMO, MOVPH or TVMODE 1: a new value can be read 0: non of the parameters has changed its value (see also *I²C bus format* on page 64)

6.4 Clock concept

Input signals

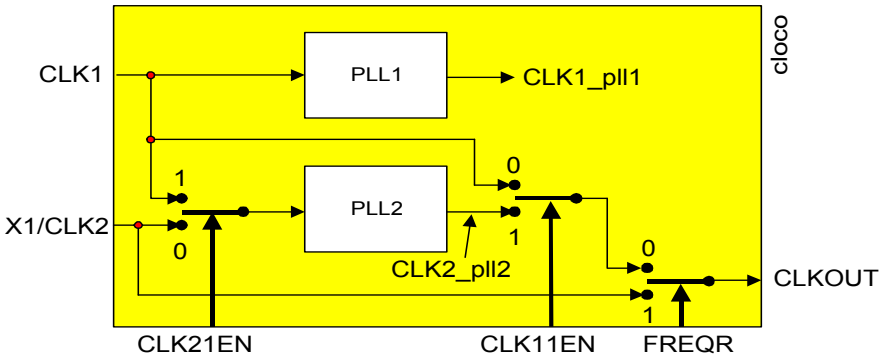
Signals	Pin number	Description
CLK1	54	System clock 1 input
X1/CLK2	28	System clock 2 input

Output signals

Signals	Pin number	Description
CLKOUT	26	Clock output

The SDA 9400 supports different clock concepts. In chapter 10 (see also *Application information* on page 90) a typical application of the circuit is shown. The front-end clock is connected to CLK1 input. The CLKOUT pin is connected to the back-end and the X1/CLK2 input is connected to a crystal oscillator. The next figure explains the different clock switches, which may be used for the separate modes (see also page 39, “Ingenious configurations of the HOUT and VOUT generator”).

Clock concept



Clock concept switching matrix

CLK11EN (19h)	CLK21EN (19h)	FREQR (1Bh)	CLKOUT
0	1	0	CLK1
0	0	0	not allowed
X	1	1	not allowed
1	X	0	CLK2_pll2
X	0	1	X1/CLK2

Clock	FREQR	Used in block
CLK1_pll1	X	ISC, IFC, LDR, ED, MC, LM, I²C
CLK2_pll2	0	OSC, HDR, ED, MC, LM, OFC
X1/CLK2	1	OSC, HDR, ED, MC, LM, OFC

Input write parameter

Parameter	Subaddress	Description
PLL1OFF 1: off 0: on	02h	PLL 1 on or off
PLL1RA	09h,0Ah	PLL range, only for test purposes
PLL2OFF 1: off 0: on	16h	PLL 2 on or off
PLL2RA	19h	PLL range, only for test purposes
CLKOUTON 1: enabled 0: disabled	16h	Output of system clock

6.5 Output sync controller (OSC)

Input signals

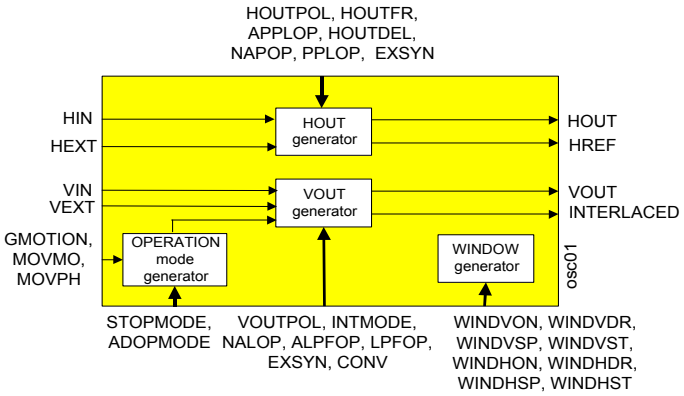
Signals	Pin number	Description
HEXT	60	horizontal synchronization signal for external synchronization (polarity programmable, I²C bus parameter 14h HOUTPOL, default: high active, EXSYN=1)
VEXT	61	vertical synchronization signal for external synchronization (polarity programmable, I²C bus parameter 14h VOUTPOL, default: high active, EXSYN=1)

Output signals

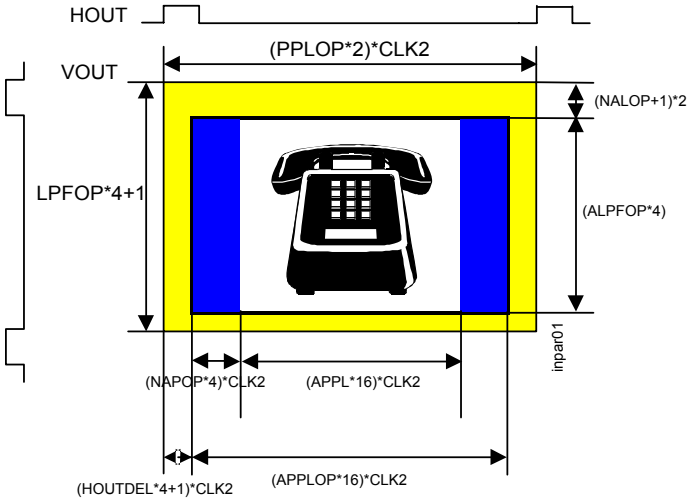
Signals	Pin number	Description
HOUT	60	horizontal synchronization signal (polarity programmable, I²C bus parameter 14h HOUTPOL, default: high active, EXSYN=0)
VOUT	61	vertical synchronization signal (polarity programmable, I²C bus parameter 14h VOUTPOL, default: high active, EXSYN=0)
HREF	62	horizontal active video output
INTERLACED	18	interlaced signal (can be used for AC coupled deflection circuits)

The output sync controller generates horizontal and vertical synchronization signals for the scan rate converted output signal. The figures below show the block diagram of the OSC and the existing parameters.

Block diagram of OSC



Output parameter



Output write parameter

Parameter [Default value]	Subaddress	Description
NALOP [22]	0Bh	Not Active Line OutPut defines the number of lines from the V-Sync to the first active line of the output frame
ALPFOP [144]	0Ch	Active Lines Per Field OutPut defines the number of active lines per output frame
LPFOP [156]	0Dh	Lines Per Frame OutPut defines the number of lines per output frame (only valid for VOUTFR=1)
HOUTDEL [4]	0Fh	HOUT DELay defines the number of pixels from the H-Sync to the first active pixel

Parameter [Default value]	Subaddress	Description
NAPOP [0]	0Eh	Not Active Pixel OutPut defines the number of not active pixels (e.g. coloured border values)
APPLOP [45]	10h	Active Pixels Per Line OutPut defines the number of pixels per line including border pixels
APPL	internal	Active Pixels Per Line defines the number of active pixels (see also *Horizontal compression* on page 19, APPLIP)
PPLOP [432]	11h, 12h	Pixel Per Line OutPut defines the number of pixels between two consecutive H-Syncs (only valid for HOUTFR=1)

The next paragraphs describe the HOUT and VOUT generator in more detail. Both generators have a so called “locked-mode” and “freerunning-mode”. Not all combinations of the modi make sense. The table below shows ingenious configurations.

Ingenious configurations of the HOUT and VOUT generator

Mode	EXSYN	HOUTFR	VOUTFR	CLK11EN	CLK21EN	FREQR	CONV
“H-and-V-locked”	0	0	0	1	1	0	by I²C-bus
“H-freerunning-V-locked”	0	1	0	1	0	0	by I²C-bus
“H-and-V-freerunning”	0	1	1	1	0	0 or 1	0
External synchronization	1	0	0	1	0	0 or 1	0

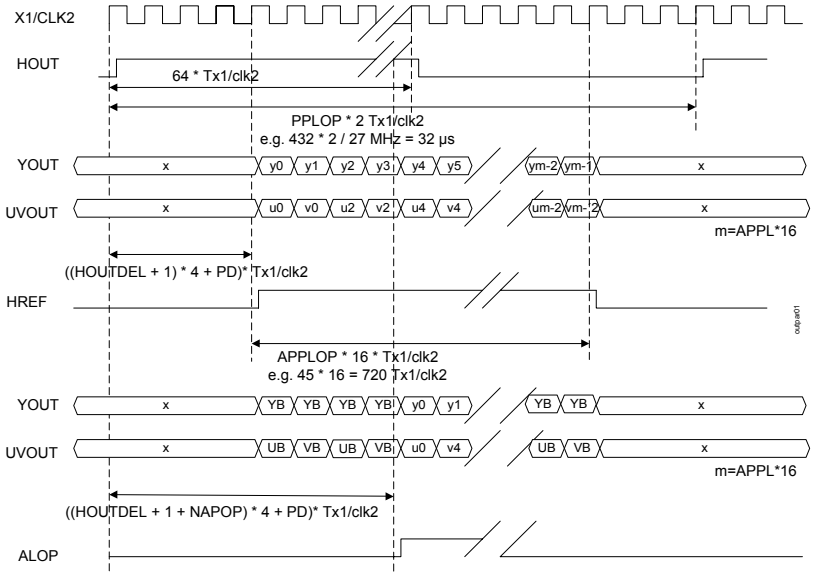
6.5.1 HOUT generator

The HOUT generator has two operation modes, which can be selected by the parameter HOUTFR. The HOUT signal is active high (HOUTPOL=0) for 64 clock cycles (X1/CLK2). In the freerunning-mode the HOUT signal is generated depending on the PPLOP parameter. In the locked-mode the HOUT signal is locked on the incoming H-Sync signal HIN. In case of external synchronization (EXSYN=1), no HOUT signal is generated. The SDA 9400 needs in this case an external H-Sync (HEXT). The polarity of the HEXT signal as well as of the HOUT signal is programmable by the parameter HOUTPOL. In case of external synchronization the HOUT generator has to be set into the locked-mode (see also *Output sync controller (OSC)* on page 40).

The HREF signal marks the active part of a line. The figure below shows the timing relation of the HOUT and the HREF signal. The distance is programmable by the parameter HOUTDEL. PD means processing delay of the internal data processing (PD=36 X1/CLK2 clocks). The length of the active part is determined by the parameter APPLOP. If the number of the active pixels (internal parameter APPL, see also *Horizontal compression* on page 19) is smaller than the number of the displayed pixels (e.g. displaying a 4:3 source on a 16:9 screen), a coloured border can be defined using the NAPOP parameter. The border colour is defined by the parameters YBORDER,

UBORDER and VBORDER. To avoid transition artifacts of digital filters the number of active pixels per line (parameter APPL) can be symmetrically reduced using the CAPP parameter. The figure below shows also the internal signal ALOP, which marks the active pixels of the line.

Timing diagram of output signals



Output write parameter

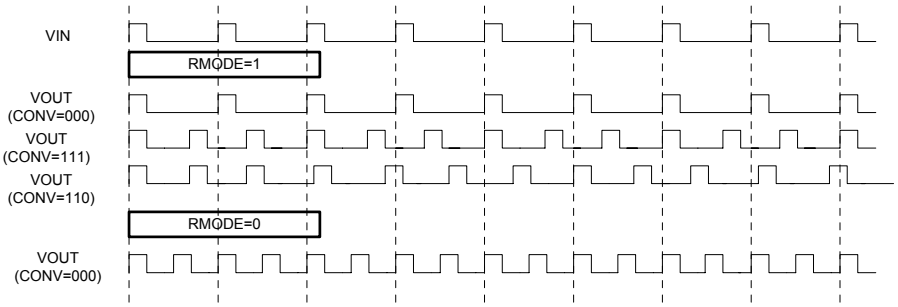
Parameter	Subaddress	Description
HOUTFR 1: freerun 0: locked mode	14h	HOUT generator mode select
EXSYN 1: on 0: off	14h	External synchronization select
YBORDER	17h	Y border value (four MSB of the 8 bit colour)
UBORDER	18h	U border value (four MSB of the 8 bit colour)
VBORDER	18h	V border value (four MSB of the 8 bit colour)
CAPP 00: k = 0 01: k = 8 10: k = 16 11: k = 24	10h	Reducing factor for the Active Pixels Per Line Value (APPL) Number of active pixels per line = 16 * APPL - 2*k

6.5.2 VOUT generator

The VOUT generator has two operation modes, which can be selected by the parameter VOUTFR. The VOUT signal is active high (VOUTPOL=0) for two output lines. In the freerunning-mode the VOUT signal is generated depending on the LPFOP parameter.

In the locked-mode the VOUT signal is synchronized by the incoming V-Sync signal VIN (means the internal VIN delayed by the parameter OPDEL, see also *Input sync controller (ISC)* on page 11). Furthermore the CONV parameter defines, how many V-Syncs VIN have to be suppressed for synchronization. In the freerunning-mode the CONV parameter has to be set to CONV=0. Both the CONV and RMODE parameter (raster mode 1: progressive, 0: interlaced) determine the scan rate conversion mode. The figure below shows some examples. If CONV=000 and RMODE=1, then for each incoming V-sync signal VIN an outgoing V-sync signal VOUT has to be generated (e.g. 50 Hz interlaced to 50 Hz progressive scan rate conversion). If CONV=000 and RMODE=0, then during one incoming V-Sync signal, two VOUT pulses have to be generated (e.g. 50 Hz interlaced to 100 Hz interlaced scan rate conversion). If CONV=111 and RMODE=1, then during two incoming VIN signals, three VOUT pulses have to be generated. That means every second VIN is not used to synchronize the output V-Sync raster on the incoming V-Sync raster. If CONV=110 and RMODE=1, then during five incoming VIN signals, seven VOUT pulses have to be generated.

Examples for VOUT generation depending on parameter CONV and RMODE



Output write parameter: CONV, RMODE

CONV		RMODE = 0	RMODE = 1	Factor	MODE
	Input syncs	Output syncs	Output syncs		e.g.
000	1	2	1	1.0	50->100 Hz interlaced, 50-> 50 Hz progressive
001	8	18	9	1.125 (9/8)	
010	7	16	8	1.14 (8/7)	
011	6	14	7	1.16 (7/6)	60->140 Hz interlaced, 60->70 Hz progressive
100	5	12	6	1.2 (6/5)	50->120 interlaced, 50->60 Hz progressive
101	4	10	5	1.25 (5/4)	60->150 Hz interlaced, 60->75 Hz progressive

CONV		RMODE = 0	RMODE = 1	Factor	MODE
110	5	14	7	1.4 (7/5)	50-> 140 Hz interlaced, 50->70 Hz progressive
111	2	6	3	1.5 (3/2)	50->150 Hz interlaced 50->75 Hz progressive

In case of external synchronization (EXSYN=1), no VOUT signal is generated. The SDA 9400 needs in this case an external V-Sync (VEXT). The polarity of the VEXT signal as well as of the VOUT signal is programmable by the parameter VOUTPOL. In case of external synchronization the VOUT generator has to be set to the locked-mode (see also *Output sync controller (OSC)* on page 40).

The VOUT signal has a delay of two CLKOUT clocks to the HOUT signal or in case of interlaced a delay of a half line plus two CLKOUT clocks.

Output write parameter

Parameter	Subaddress	Description
VOUTFR 1: freerun 0: locked mode	14h	VOUT generator mode select
EXSYN 1: on 0: off	14h	External synchronization select
CONV	15h	CONV defines the scan rate conversion mode
RMODE 1: progressive 0: interlaced	14h	Raster mode

Switching from H-and-V-freerunning to H-and-V-locked mode

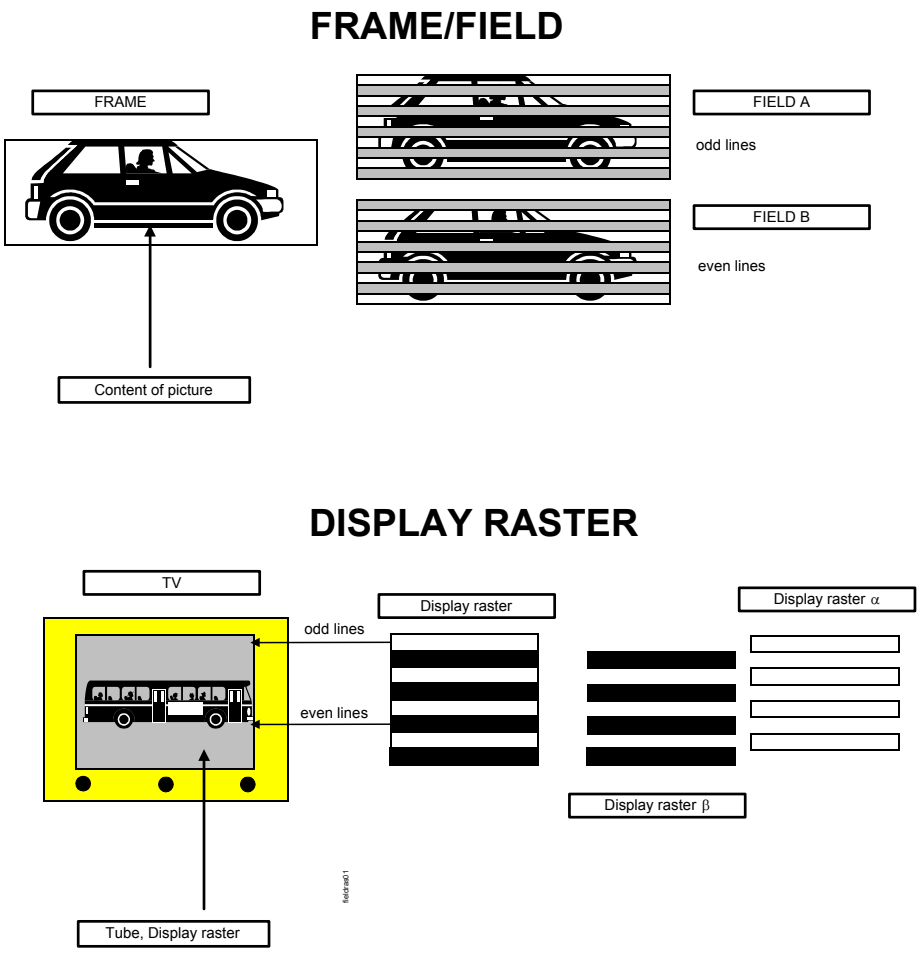
In H-and-V-freerunning mode, generally, the phase of the generated synchronization raster has no correlation to the input raster. A hard switch from the H-and-V-freerunning mode to the H-and-V-locked mode therefore would cause visible synchronization artefacts. To avoid these problems the SDA 9400 enlarges the line and the field lengths of the output sync signals HOUT and VOUT in a defined procedure to enable an unvisible synchronization of the freerunning output to the input.

For vertical synchronization the maximum synchronization time is 260 ms for interlaced and 520 ms for progressive display modes. Horizontal synchronization is performed in a maximum time of 50 ms. To get the best performance it is recommended to change at first the vertical and after the mentioned delay times the horizontal mode from free running to locked.

6.5.3 Operation mode generator

The VOUT generator determines the VOUT signal. For proper operation of the VOUT generator information about the raster sequence is necessary. The parameter STOPMODE (Static operation mode) and the parameter ADOPMODE (Adaptive operation mode) define the raster sequence and the scan rate conversion algorithm. The figure below explains the used wording for the following explanations.

Explanations of field and display raster



The interlaced input signal (e.g. 50 Hz PAL or 60 Hz NTSC) is composed of a field A (odd lines) and a field B (even lines).

A^n - Input signal, field A at time n,

B^n - Input signal, field B at time n

The field information describes the picture content. The output signal, which could contain different picture contents (e.g. field A, field B) can be displayed with the display raster α or β.

(A^n,α) - Output signal, field A at time n, displayed as raster α,

(A^n,β) - Output signal, field A at time n, displayed as raster β,

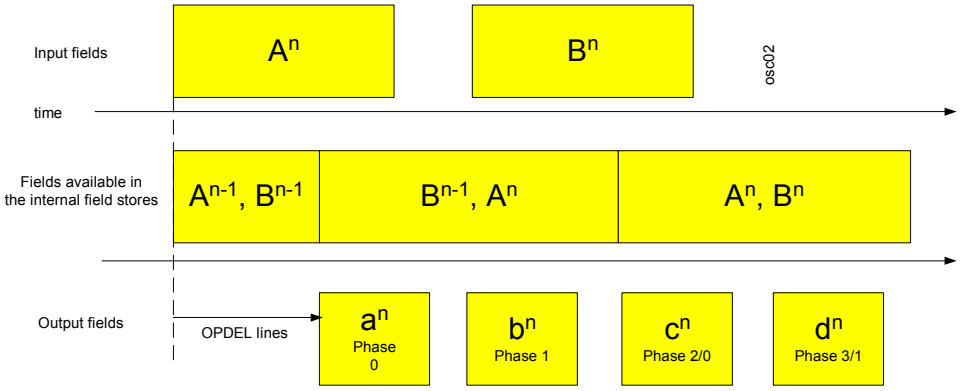
((A^*)^n,β) - Output signal, field A raster interpolated into field B at time n, displayed as raster β

(A^n B^{n-1},α+β) – Output signal, frame AB at time n, progressive

The table below describes the different scan rate conversion algorithms and the corresponding raster sequences (see also *Principles of scan rate conversion* on page 55). The delay between the input field and the corresponding output fields depends on the OPDEL parameter and the default value for the delay is an half input field.

The INTERLACED signal can be used for AC-coupled deflections. Depending on the parameter INTMODE the value of this signal will be generated. The table below shows also the definition of this signal.

Explanation of operation mode timing



Static operation modes (only valid for ADOPMODE=0)

		Input field A		Input field B		
STOPMODE	**Scan rate conversion algorithm**	**Output field a^n phase 0**	**Output field b^n phase 1**	**Output field c^n phase 2/0**	**Output field d^n phase 3/1**	**RMODE**
0000	ABAB mode I interlaced	B^{n-1},β INTMODE(3)	A^n,α INTMODE(0)	B^n,β INTMODE(1)	A^n,α INTMODE(2)	0
0001	AA*B*B mode I interlaced	(A^*)^n,β INTMODE(3)	A^n,α INTMODE(0)	B^n,β INTMODE(1)	(B^*)^n,α INTMODE(2)	0
0010	AABB mode I interlaced	A^n,α INTMODE(0)	A^n,α INTMODE(0)	B^n,β INTMODE(1)	B^n,β INTMODE(1)	0
0011	Micronas Soft mix I (motion adaptive mode interlaced)	B^{n-1},β or (A^*)^n,β INTMODE(3)	A^n,α INTMODE(0)	B^n,β INTMODE(1)	A^n,α or (B^*)^n,α INTMODE(2)	0
0100	Multipicture mode I	A^n,β INTMODE(0)	A^n,α INTMODE(0)	A^n,β INTMODE(0)	A^n,α INTMODE(0)	0

		Input field A		Input field B		
STOPMODE	**Scan rate conversion algorithm**	**Output field a^n phase 0**	**Output field b^n phase 1**	**Output field c^n phase 2/0**	**Output field d^n phase 3/1**	**RMODE**
0101	Multipicture mode II	B^{n-1},β INTMODE(1)	B^{n-1},α INTMODE(1)	B^n,β INTMODE(1)	B^n,α INTMODE(1)	0
0110	AAAA mode	A^n,α INTMODE(0)	A^n,α INTMODE(0)	A^n,α INTMODE(0)	A^n,α INTMODE(0)	0
0111	BBBB mode	B^{n-1},β INTMODE(0)	B^{n-1},β INTMODE(0)	B^n,β INTMODE(0)	B^n,β INTMODE(0)	0
1000	ABAB mode II interlaced	A^n,α INTMODE(0)	B^{n-1},β INTMODE(1)	A^n,α INTMODE(2)	B^n,β INTMODE(3)	0
1001	AA*B*B mode II interlaced	$(B^*)^{n-1},\alpha$ INTMODE(2)	B^{n-1},β INTMODE(1)	A^n,α INTMODE(0)	$(A^*)^n,\beta$ INTMODE(3)	0
1010	AABB mode II interlaced	B^{n-1},β INTMODE(1)	B^{n-1},β INTMODE(1)	A^n,α INTMODE(0)	A^n,α INTMODE(0)	0
1011	Micronas Soft mix II (motion adaptive mode interlaced)	B^{n-1},β INTMODE(1)	A^n,α INTMODE(0)	B^n,β or $(A^*)^n,\beta$ INTMODE(3)	A^n,α or $(B^*)^n,\alpha$ INTMODE(2)	0
1100	Micronas Soft mix III (motion adaptive mode interlaced)	A^n,α INTMODE(0)	B^{n-1},β or $(A^*)^n,\beta$ INTMODE(3)	A^n,α or $(B^*)^n,\alpha$ INTMODE(2)	B^n,β INTMODE(1)	0
11xx	not defined	x	x	x	x	0
0000, 0100, 0110	AB mode progressive	$(A^n B^{n-1}, \alpha+\beta)$		$(A^n B^n, \alpha+\beta)$		1
0001	AA* mode I progressive	$(A^n A^{*n}, \alpha+\beta)$		$(B^{*n} B^n, \alpha+\beta)$		1
0010	not defined	x	x	x	x	1
0011	Micronas soft mix (motion adaptive mode progressive)	$(A^n B^{n-1}$ or$A^n A^{*n}, \alpha+\beta)$		$(A^n B^n$ or$B^{*n} B^n, \alpha+\beta)$		1
0101	AA* mode II progressive	$(A^n A^{*n}, \alpha+\beta)$		$(A^n A^{*n}, \alpha+\beta)$		1
0111	B*B mode progressive	$(B^{n-1} B^{*n-1}, \alpha+\beta)$		$(B^n B^{*n}, \alpha+\beta)$		1
1000	Test Mode (motion adaptive mode interlaced, DL)	$(A^n B^{n-1}$ or $A^n A^{*n}$, $\alpha+\beta$/ $\alpha+\beta)$		$(A^n B^n$ or $B^{*n} B^n$, $\alpha+\beta$/ $\alpha+\beta)$		1

		Input field A		Input field B		
STOPMODE	Scan rate conversion algorithm	Output field a^n phase 0	Output field b^n phase 1	Output field c^n phase 2/0	Output field d^n phase 3/1	RMODE
1xxx	not defined	x	x	x	x	1

For STOPMODE=0011 (Micronas soft mix I) the high performance motion detector is used to switch motion adaptive pixel by pixel between different algorithms. This scan rate conversion method results in a high performance line flicker reduction (see also *Principles of scan rate conversion* on page 55).

The table below shows all possible display raster sequences for the different static operation modes and the lines per field value between two consecutive output V-Syncs. It is assumed, that in case of freerunning-mode LPFOP=156 and in the locked mode the number of lines of the incoming field is 312.5.

Display raster sequence for RMODE=1 (progressive)

Display raster sequence	1. to 2.	2. to 3. (1.)
α+β	625	625

Display raster sequence for RMODE=0 (interlaced)

Display raster sequence	1. to 2.	2. to 3.	3. to 4.	4. to 5.(1.)
αααα	312	313	312	313
αβαβ	312.5	312.5	312.5	312.5
ββββ	313	312	313	312
βαβα	312.5	312.5	312.5	312.5
ααββ	312	312.5	313	312.5
ββαα	313	312.5	312	312.5
α+β/α+β (test mode only)	625,5	624,5	625,5	624,5

All static operation modes can be influenced by the I²C bus parameters FIXSHR, MEDON, CSMOFF and PSMOFF. Some fields are raster interpolated. Two raster interpolation methods are implemented, which can be switched using the I²C parameter MEDON.

Output write parameter: MEDON

MEDON	Raster interpolation method
0	linear filter
1	median filter

In addition a temporal mixing of the different fields can be switched on using the parameters FIXSHR, CSMOFF, PSMOFF. Temporal mixing may be used for better line flicker reduction performance.

Output write parameter: CSMOFF, PSMOFF, FIXSHR

CSMOFF	PSMOFF	FIXSHR	
x	x	1	Fixed temporal mixing on, independent of motion detector for scan rate conversion
0	0	0	Temporal mixing on for all static operation modes, depending on motion detection for scan rate conversion
0	1	0	Temporal mixing on for all static operation modes, but only raster interpolated fields, depending on motion detection for scan rate conversion
1	0	0	Temporal mixing on for all static operation modes, but only for not raster interpolated fields, depending on motion detection for scan rate conversion
1	1	0	Temporal mixing off

The adaptive operation modes (ADOPMODE) define a dynamic switch between different static operation modes controlled by several internal signals. The start point of all modes is the actual chosen STOPMODE as described before. The tables below shows the different adaptive operation modes. The internal used control signals are GMOTION, MOVMO and MOVPH (see also *Global motion, movie mode and phase detection* on page 33). Furthermore the internal control signal VTSEQ exists. In case of parameter VCRMODE=1, VTSEQ is still zero. If VCRMODE=0, VTSEQ can be equal one (see also *Input sync controller (ISC)* on page 11). In this cases the scan rate conversion is forced to a simple field based scan rate conversion algorithm. All internal control signals GMOTION, MOVMO and MOVPH are also readable by the I²C-bus interface.

Adaptive operation modes (RMODE = 0 (interlaced)):

ADOPMODE: off

ADOPMODE=000	MOVMO	MOVPH	GMOTION	VTSEQ
no adaptive mode, operation defined by STOPMODE	x	x	x	x

ADOPMODE: Still picture mode

ADOPMODE=001	MOVMO	MOVPH	GMOTION	VTSEQ
ABAB mode I interlaced	x	x	0	0
STOPMODE	x	x	1	0
AABB mode I interlaced	x	x	x	1

ADOPMODE: Field mixer mode I

ADOPMODE=010	MOVMO	MOVPH	GMOTION	VTSEQ
STOPMODE	x	x	0	0
AABB mode I interlaced	x	x	1	0
AABB mode I interlaced	x	x	x	1

ADOPMODE: Field mixer mode II

ADOPMODE=011	MOVMO	MOVPH	GMOTION	VTSEQ
STOPMODE	x	x	0	0
AABB mode I interlaced	x	x	1	0
AA*B*B mode I interlaced	x	x	x	1

ADOPMODE: Movie mode I

ADOPMODE=100	MOVMO	MOVPH	GMOTION	VTSEQ
STOPMODE	0	x	x	0
ABAB mode I interlaced	1	0	x	0
ABAB mode II interlaced	1	1	x	0

ADOPMODE=100	MOVMO	MOVPH	GMOTION	VTSEQ
AA*B*B mode I interlaced	x	x	x	1

ADOPMODE: Movie mode II

ADOPMODE=101	MOVMO	MOVPH	GMOTION	VTSEQ
STOPMODE	0	x	x	0
ABAB mode I interlaced	1	0	x	0
ABAB mode II interlaced	1	1	x	0
AABB mode I interlaced	x	x	x	1

ADOPMODE: Field mixer mode I and movie mode

ADOPMODE=110	MOVMO	MOVPH	GMOTION	VTSEQ
STOPMODE	0	x	0	0
AABB mode I interlaced	0	x	1	0
ABAB mode I interlaced	1	0	x	0
ABAB mode II interlaced	1	1	x	0
AABB mode I interlaced	x	x	x	1

ADOPMODE: Field mixer mode II and movie mode

ADOPMODE=111	MOVMO	MOVPH	GMOTION	VTSEQ
STOPMODE	0	x	0	0
AABB mode I interlaced	0	x	1	0
ABAB mode I interlaced	1	0	x	0
ABAB mode II interlaced	1	1	x	0
AA*B*B mode I interlaced	x	x	x	1

Basic adaptive operation mode (RMODE = 1 (progressive)):

ADOPMODE: off

ADOPMODE=000	MOVMO	MOVPH	GMOTION	VTSEQ
no adaptive mode, operation defined by STOPMODE	x	x	x	x

ADOPMODE: VCRMODE off

ADOPMODE=001	MOVMO	MOVPH	GMOTION	VTSEQ
STOPMODE	x	x	x	0
AA* MODE I progressive	x	x	x	1

Example for explanation of the adaptive operation modes:

ADOPMODE=2: Field mixer mode I

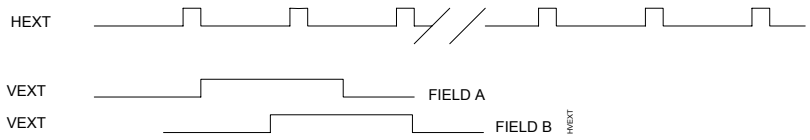
In this case the scan rate conversion algorithm is only controlled by the signal GMOTION. If GMOTION=0, the scan rate algorithm is defined by the parameter STOPMODE (e.g. Micronas field mixer algorithm). If GMOTION=1 the scan rate conversion algorithm is changed to the simple AABB mode I interlaced. The behaviour in this case is like the Micronas FIELD MIXER circuit SDA9270.

Recommended operation mode combinations

MODE	STOPMODE	ADOP MODE	CSMOFF	PSMOFF	MEDON	FIXSHR	Comment
1	0011 SoftMix I	000	1	1	0	0	corresponds to former SDA 9272 (VIP),
2	0011 SoftMix I	010	1	1	0	0	Mode 1 plus global fall back mode AABB activated
3	0011 SoftMix I	110	1	1	0	0	Mode 2 plus movie mode fall back ABAB activated
4	1011 SoftMix II	000	0	0	0	0	corresponds to former SDA 9270 (FieldMixer)
5	1011 SoftMix II	010	0	0	0	0	Mode 4 plus global fall back mode activated
6	1011 SoftMix II	110	0	0	0	0	Mode 5 plus movie mode fall back ABAB activated

The STOPMODE parameter has in case of external synchronization a different meaning (EXSYN=1). The STOPMODE parameter defines, which input display raster the OSC block expects and which output pictures the SDA 9400 generates. In case of interlaced signals the field information is also necessary. The SDA 9400 will detect the information itself. If the VEXT signal has a rising edge in the first half of the line period a field A is detected, otherwise a field B. The SDA 9400 recognizes only the rising edge of the VEXT and the HEXT signal. Therefore the length of the external signals are not relevant.

Field detection by external synchronization



Static operation modes for external synchronization

STOPMODE	Scan rate conversion algorithm	Output field phase 0	Output field phase 1	RMODE
0000	AB mode interlaced	A^n	B^n	0
0100	AA mode	A^n	A^n	0
0101	BB mode	B^n	B^n	0
0000	AB mode progressive	AB^n	AB^n	1

If STOPMODE=0, then the SDA 9400 expects an external interlaced signal with the raster sequence $\alpha\beta\alpha\beta$ and the SDA 9400 generates an output picture sequence ABAB.

Output write parameter

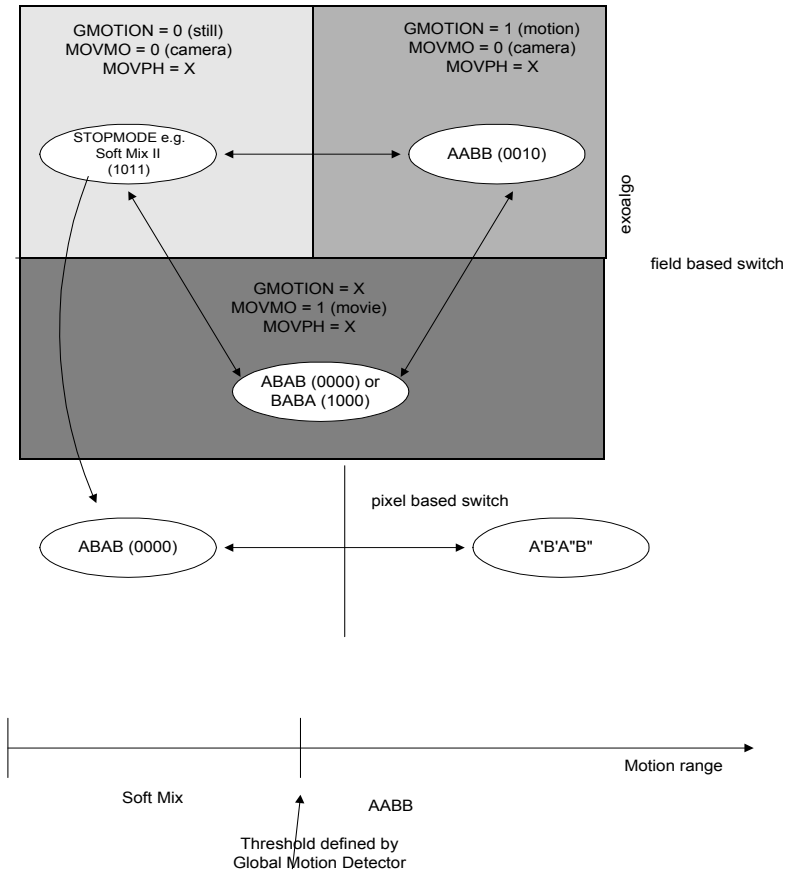
Parameter	Subaddress	Description
INTMODE	13h, 14h	Free programmable INTERLACED signal for AC-coupled deflection stages
STOPMODE	12h	Static operation modes
ADOPMODE	12h	Adaptive operation modes
MEDON	17h	Raster interpolation filter method
FIXSHR	17h	Fixed temporal mixing
CSMOFF	19h	Temporal mixing
PSMOFF	19h	Temporal mixing

6.5.4 Principles of scan rate conversion

The scan rate conversion algorithm concept is based on the assumption that the video input signal can be in camera mode (two consecutive fields belong not to the same motion phase) or movie mode (means two consecutive fields belong to the same motion phase). The camera mode material can be further separated. The separation is based on the motion range of the picture content, which is displayed. For the different source materials optimised scan rate conversion methods exist. Movie mode material should be displayed in ABAB or BABA mode depending on the movie mode phase. For camera mode material the optimised scan rate conversion method depends on the picture content. That means for still areas the ABAB scan rate conversion method is optimal (best line flicker reduction) and for moving areas or objects AABB scan rate conversion method is well suited. Normally camera material can contain both types of areas or objects. That's why a high performance 3-D motion detector is included, which analyzes the picture content and assigns each pixel to a still or moving area (object). Depending on the assignment of the 3-D motion detector different optimised scan rate conversion methods will be used. Due to the fact that the switch between these methods is soft, the algorithm is called Soft Switch. Depending on the motion range, which can be individually defined by the thresholds of the global motion detector block, the Soft Mix method may be switched to the scan rate conversion method AABB. This display method is best for camera mode material, if the motion range is as high that line flickering is not visible any more.

The figure below shows the algorithm concept in more detail. The global motion detector can be used to separate the whole motion range in two areas. The separation point depends on the parameter setting and can be changed individually. If the motion range exceeds the separation point, the AABB method is applied. Otherwise the e.g. Soft Mix method is used as the scan rate conversion method. In case of movie mode ABAB or BABA is applied. The switching is automatically done if one of the adaptive modes (I²C bus parameter ADOPMODE) is used.

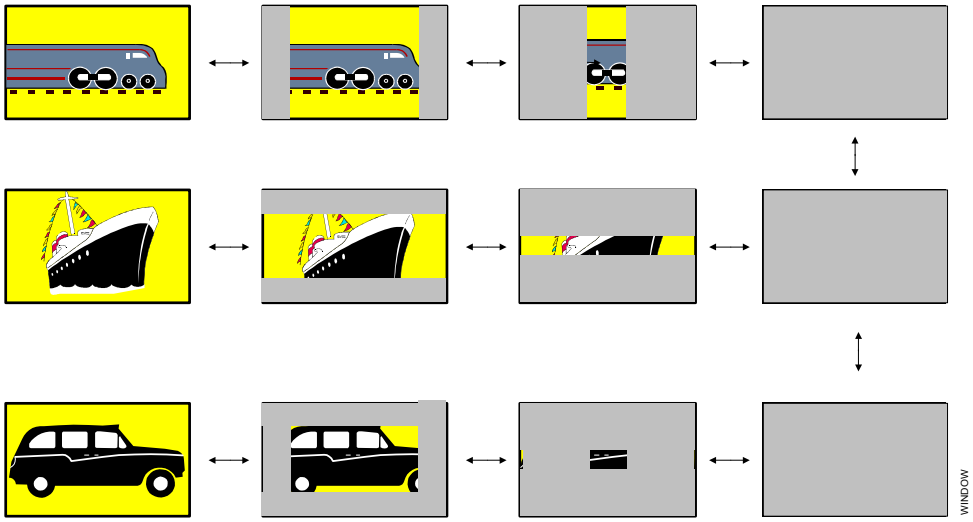
Principles of scan rate conversion



6.5.5 Window generator

The figures below show the functionality of the horizontal and/or vertical window function. The actual TV display can be overwritten with a constant value (defined by YBORDER, UBORDER, VBORDER), which is called “closing” or the constant value can be overwritten with the actual TV signal, which is called “opening”. For the generation some parameters exist, which will be explained in more detail afterwards.

Examples for window feature



The feature can be enabled by the parameter WINDHON/WINDVON. The parameter WINDHST/ WINDVST defines the status of the window (opened or closed). Closed means, that only a constant value is displayed, opened means, that the full TV is displayed. The parameter WINDHDR/ WINDVDR defines, what can be done with the window (open the window, close the window).

Output write parameter: WINDHST/WINDVST and WINDHDR/WINDVDR

WINDHST/ WINDVST	Description	WINDHDR/ WINDVDR	Description
0	Window is closed	0	open the window
0	Window is closed	1	window remains closed
1	Window is opened	0	window remains open
1	Window is opened	1	close the window

With each enabling of the window function by the WINDHON/WINDVON parameter, the status of the window will be as defined by the table above, that means the WINDHST/WINDVST parameter is only once interpreted after enabling the window function. To change afterwards the status from “window is close” to “window is open” or vice versa only the WINDHDR/WINDVDR has to be

toggled. If for example the status WINDHST/WINDVST=0 and the WINDHDR/WINDVDR=0 the window is closed and will be open after enabling the feature by setting the parameter WINDHON/ WINDVON=1. To close the window only the parameter WINDHDR/WINDVDR has to be set to 1. Again to open the window WINDHDR/WINDVDR has to be set to 0.

For example:

After switching on the TV set, the customer should see the window closed and afterwards the window should be opened. Therefore the WINDHST/WINDVST has to be set to “0”, the WINDHDR/ WINDVDR has to be set to “1” and the WINDHON/WINDVON has to be set to “1”. So the customer will see first a screen with a colour defined by the I²C parameters YBORDER, UBORDER and VBORDER. Then the WINDHDR/WINDVDR has to be set to “0”, that means the window will be open and the customer will see the chosen TV channel.

The speed of closing or opening the window can be defined by the parameter WINDHSP/ WINDVSP. The tables below explain the using of these parameters.

Output write parameter: WINDHSP

windhsp	freerun mode	locked mode	time to close/ open (e.g. 720 active pixel, 10ms per output field)
00	pplop/256	distance/512	~4s
01	pplop/128	distance/256	~2s
10	pplop/64	distance/128	~1s
11	pplop/32	distance/64	~0.5s

Distance: Number of pixels in system clocks X1/CLK2 between two output H-Syncs

time to close = time(field) * number of active pixels / (distance/512)

e.g. time to close = 10 ms * 720 / (864/512) = 4,26 s

time to close = time(field) * number of active pixels / (pplop/128)

Output write parameter: WINDVSP

windvsp	freerun mode	locked mode	time to close/ open (e.g. 576 active lines, 10ms per output field)
00	lpfop/128	lpfip/256	~5s
01	lpfop/64	lpfip/128	~2s
10	lpfop/32	lpfip/64	~1s
11	lpfop/16	lpfip/32	~0.5s

LPFIP: Lines per field of the input signal - amount of lines between two input V-Syncs
time to close = time(field(interlaced)/frame(progressive)) * number of active lines / (lpfip/256)
e.g. time to close = 10 ms * 576 / (312/256) = 4.7 s
time to close = time(field) * number of active lines / (lpfop/128)

Output write parameter

Parameter	Subaddress	Description
WINDVON 1: on 0: off	15h	Vertical window feature on or off
WINDVDR 1: close window 0: open window	15h	Direction of the vertical window feature
WINDVST 1: window is opened 0: window is closed	15h	Status of the vertical window feature after enabling the window feature
WINDVSP	15h	Speed of the vertical window feature
WINDHON 1: on 0: off	16h	Horizontal window feature on or off
WINDHDR 1: close window 0: open window	16h	Direction of the horizontal window feature
WINDHST 1: window is opened 0: window is closed	16h	Status of the horizontal window feature after enabling the window feature
WINDHSP	16h	Speed of the horizontal window feature
FLASHON 1: on 0: off	17h	Flash of the TV signal (after each output V-Sync the TV signal or the constant background value defined by YBORDER, UBORDER, VBORDER is displayed)

6.6 Output format conversion (OFC)

Output signals

Signals	Pin number	Description
YOUT0...7	7, 6, 5, 4, 3, 1, 64, 63	luminance output
UVOUT0...7	17, 16, 15, 14, 13, 12, 11, 10	chrominance output

The SDA 9400 supports at the output side only the sample frequency relations of Y : (B-Y) : (R-Y):

4:2:2. The representation of the samples of the chrominance signal is programmable as positive dual code (unsigned, parameter TWOOUT=0) or two's complement code (TWOOUT=1, see also *I²C bus format* on page 64, I²C bus parameter 17h).

Output data format

Data Pin	4:2:2 Parallel	
YOUT7	Y_{07}	Y_{17}
YOUT6	Y_{06}	Y_{16}
YOUT5	Y_{05}	Y_{15}
YOUT4	Y_{04}	Y_{14}
YOUT3	Y_{03}	Y_{13}
YOUT2	Y_{02}	Y_{12}
YOUT1	Y_{01}	Y_{11}
YOUT0	Y_{00}	Y_{10}
UVOUT7	U_{07}	V_{07}
UVOUT6	U_{06}	V_{06}
UVOUT5	U_{05}	V_{05}
UVOUT4	U_{04}	V_{04}
UVOUT3	U_{03}	V_{03}
UVOUT2	U_{02}	V_{02}
UVOUT1	U_{01}	V_{01}
UVOUT0	U_{00}	V_{00}

X_{ab}: X: signal component a: sample number b: bit number

6.7 High data rate processing (HDR)

The output signal can be vertically expanded. The expansion as well as the different scan rate conversion algorithms are processed in the HDR block. For the vertical expansion line memories are used. If the operation frequency X1/CLK2 is higher than 27 MHz plus 10%, the line memories will not work correctly any more. In this case only simple processing will be possible. Simple processing means, that the vertical expansion must be disabled. To force simple processing the parameter FREQR is used. Furthermore all static operation modes are disabled, which needs the interpolation into another raster position like Micronas soft mix mode.

Output write parameter: FREQR

FREQR	X1/CLK2	Vertical expansion
0	<= 27 MHZ + 10%	depends on VERINT

FREQR	X1/CLK2	Vertical expansion
1	> 27 MHZ + 10%	off

The table below defines the internal expansion factor ZOOM depending on the RMODE, FREQR and VERINT parameter.

Output write parameter: VERINT

FREQR	VERINT	RMODE	ZOOM
0	I²C-bus parameter	0	2*(VERINT+1)
0	I²C-bus parameter	1	(VERINT+1)
1	x	0	128
1	x	1	64

The reachable expansion factors are listed in the table below in case of VDECON=0 and VDECON=2 (vertical compression of the input signal with factor 1.0 and 1.5).

Examples of reachable expansion factors

	100/120 Hz interlaced RMODE=0 CONV=0	50/60 Hz progressive RMODE=1 CONV=0	real vertical expansion factor	real vertical expansion factor
VERINT	ZOOM	ZOOM	VDECON=0	VDECON=2
63	128	64	1.00	0.75
62	126	63	1.02	0.76
61	124	62	1.03	0.77
60	122	61	1.05	0.79
59	120	60	1.07	0.80
58	118	59	1.08	0.81
57	116	58	1.10	0.83
56	114	57	1.12	0.84
55	112	56	1.14	0.86
54	110	55	1.16	0.87
53	108	54	1.19	0.89
52	106	53	1.21	0.91
51	104	52	1.23	0.92
50	102	51	1.25	0.94
49	100	50	1.28	0.96
48	98	49	1.31	0.98
47	96	48	1.33	1.00

	100/120 Hz interlaced RMODE=0 CONV=0	50/60 Hz progressive RMODE=1 CONV=0	real vertical expansion factor	real vertical expansion factor
VERINT	ZOOM	ZOOM	VDECON=0	VDECON=2
46	94	47	1.36	1.02
45	92	46	1.39	1.04
44	90	45	1.42	1.07
43	88	44	1.45	1.09
42	86	43	1.49	1.12
41	84	42	1.52	1.14
40	82	41	1.56	1.17
39	80	40	1.60	1.20
38	78	39	1.64	1.23
37	76	38	1.68	1.26
36	74	37	1.73	1.30
35	72	36	1.78	1.33
34	70	35	1.83	1.37
33	68	34	1.88	1.41
32	66	33	1.94	1.45
31	64	32	2.00	1.50
30	62	31	2.06	1.55
29	60	30	2.13	1.60
28	58	29	2.21	1.66
27	56	28	2.29	1.71
26	54	27	2.37	1.78
25	52	26	2.46	1.85
24	50	25	2.56	1.92
23	48	24	2.67	2.00
22	46	23	2.78	2.09
21	44	22	2.91	2.18
20	42	21	3.05	2.29
19	40	20	3.20	2.40
18	38	19	3.37	2.53
17	36	18	3.56	2.67
16	34	17	3.76	2.82
15	32	16	4.00	3.00
14	30	15	4.27	3.20
13	28	14	4.57	3.43
12	26	13	4.92	3.69
11	24	12	5.33	4.00
10	22	11	5.82	4.36
9	20	10	6.40	4.80
8	18	9	7.11	5.33
7	16	8	8.00	6.00
6	14	7	9.14	6.86
5	12	6	10.67	8.00
4	10	5	12.80	9.60
3	8	4	16.00	12.00

	100/120 Hz interlaced RMODE=0 CONV=0	50/60 Hz progressive RMODE=1 CONV=0	real vertical expansion factor	real vertical expansion factor
VERINT	**ZOOM**	**ZOOM**	**VDECON=0**	**VDECON=2**
2	6	3	21.33	16.00
1	4	2	32.00	24.00
0	2	1	64.00	48.00

The parameter VPAN can be used to select the start line of the expansion. To expand the upper part of the incoming signal with the factor 2.0, VPAN should be set to zero. To expand the lower part, VPAN should be equal to 144. That means in case of VPAN=0 the first used line is line 1 and in case of VPAN=144 the first used line is line 144.

Dependent on the parameter VERINT a certain number of input lines of the input field is required. Therefore not all VPAN values are allowed. The formula below can be used to calculate the maximum allowed VPAN value depending on the chosen VERINT value.

Calculation of maximum VPAN value

$$VPANmax = \left\lfloor 2 \times ALPFOP \times \left(1 - \frac{(VERINT + 1)}{64}\right) \right\rfloor$$

Floor symbol means: take only integer part of x

$$\lfloor x \rfloor$$

Output write parameter

Parameter	Subaddress	Description
VERINT	13h	Vertical expansion factor
VPAN	1Ah	Vertical adjustment of the output picture
FREQR	1Bh	Frequency range select

6.8 I²C bus

6.8.1 I²C bus slave address

Write Adress: BCh

1	0	1	1	1	1	0	0

Read Adress: BDh

1	0	1	1	1	1	0	1

6.8.2 I²C bus format

The SDA 9400 I²C bus interface acts as a slave receiver and a slave transmitter and provides two different access modes (write, read). All modes run with a subaddress auto increment. The interface supports the normal 100 kHz transmission speed as well as the high speed 400 kHz transmission.

write:

S	1	0	1	1	1	1	0	0	A	Subaddress	A	Data Byte	A	*****	A	P

S: Start condition
A: Acknowledge
P: Stop condition
NA: Not Acknowledge

read:

S	1	0	1	1	1	1	0	0	A	Subaddress	A	S	1	0	1	1	1	1	0	1	A	Data Byte	A

Data Byte	NA	P

The transmitted data are internally stored in registers. The master has to write a don't care byte to the subaddress FFh (store command) to make the register values available for the SDA 9400. To have a defined time step, where the data will be available, the data are made valid with the incoming V-sync VIN or with the next OPSTART pulse, which is an internal signal and indicates the start of a new output cycle. The subaddresses, where the data are made valid with the VIN signal are indicated in the overview of the subaddresses with „VI", where the data are made valid with the OPSTART are indicated with „OS". The I²C parameter VISTATUS and OSSTATUS (subaddress 33h) reflect the state of the register values. If these bits are read as '0', then the store command was sent, but the data aren't made available yet. If these bits are '1' then the data were made valid and a new write or read cycle can start. The bits VISTATUS and OSSTATUS may be checked before writing or reading new data, otherwise data can be lost by overwriting.

Furthermore the bits NMSTATUS (status of noise measurement: NOISEME) and MDSTATUS (status of motion detection parameters: GMOTION, MOVMO, MOVPH, TVMODE) exist. NMSTATUS signalizes a new value for NOISEME. So if NMSTATUS is read as '0' the current noise measurement has not been finalized. If the NMSTATUS is read as '1' a new noise measurement

value can be read. MDSTATUS signalizes at least a change of one of the parameters: GMOTION, MOVMO, MOVPH, TVMODE. So if MDSTATUS is read as ’0’ none of the parameters has changed its value. If the MDSTATUS is read as ’1’ at least one of the parameters has changed its value.

After switching on the IC, all bits of the SDA 9400 are set to defined states. Particularly :

Subaddress	Default value	R/W	Take over	Subaddress	Default value	R/W	Take over
00	11h	W	VI	1B	00h	W	VI
01	00h	W	VI	1C	01h	W	VI
02	50h	W	VI	1D	0Bh	W	VI
03	90h	W	VI	1E	FFh	W	VI
04	00h	W	VI	1F	00h	W	VI
05	B4h	W	VI	20	FFh	W	VI
06	AAh	W	VI	21	02h	W	VI
07	00h	W	VI	22	02h	W	VI
08	00h	W	VI	23	88h	W	VI
09	00h	W	VI	24	86h	W	VI
0A	00h	W	VI	25	ECh	W	VI
0B	16h	W	OS	26	84h	W	VI
0C	90h	W	OS	27	18h	W	VI
0D	9Ch	W	OS	28	22h	W	VI
0E	00h	W	OS	29	31h	W	VI
0F	04h	W	OS	2A	09h	W	VI
10	B4h	W	OS	2B	C9h	W	VI
11	B0h	W	OS	2C	42h	W	VI
12	D8h	W	OS	2D	14h	W	VI
13	3Fh	W	OS	2E	64h	W	VI
14	00h	W	OS	2F	38h	W	VI
15	00h	W	OS	30	90	W	VI
16	04h	W	OS	31	50	W	VI
17	14h	W	OS	32		R	
18	88h	W	OS	33		R	
19	0Ch	W	OS	34...FE	not used		
1A	00h	W	OS	FF		W	

R/W: R - Read register; W - Write Register; R/W - Read and Write Register;
Take over: VI - take over with VIN; OS- take over with OPSTART

Reading the “Read only” register 32h must be followed by reading the “Read only” register 33h.

6.8.3 I²C bus commands

Subadd. (Hex.)	Data Byte							
	D7	D6	D5	D4	D3	D2	D1	D0
00	FORMAT1 ISC/IFC	FORMAT0 ISC/IFC	FIEINV ISC	VCRMODE ISC	PIMODE ISC	NAPIPPH1 ISC	NAPIPPH0 ISC	TWOIN ISC/IFC
01	VINDEL5 ISC	VINDEL4 ISC	VINDEL3 ISC	VINDEL2 ISC	VINDEL1 ISC	VINDEL0 ISC	VINPOL ISC	HINPOL ISC
02	NALIP5 ISC	NALIP4 ISC	NALIP3 ISC	NALIP2 ISC	NALIP1 ISC	NALIP0 ISC	PLL1OFF PLL1	REFRESH MC
03	ALPFIP7 ISC	ALPFIP6 ISC	ALPFIP5 ISC	ALPFIP4 ISC	ALPFIP3 ISC	ALPFIP2 ISC	ALPFIP1 ISC	ALPFIP0 ISC
04	NAPIPDL7 ISC	NAPIPDL6 ISC	NAPIPDL5 ISC	NAPIPDL4 ISC	NAPIPDL3 ISC	NAPIPDL2 ISC	NAPIPDL1 ISC	NAPIPDL0 ISC
05	APPLIP5 ISC	APPLIP4 ISC	APPLIP3 ISC	APPLIP2 ISC	APPLIP1 ISC	APPLIP0 ISC	x	x
06	OPDEL7 ISC	OPDEL6 ISC	OPDEL5 ISC	OPDEL4 ISC	OPDEL3 ISC	OPDEL2 ISC	OPDEL1 ISC	OPDEL0 ISC
07	VERWIDTH7 ISC	VERWIDTH6 ISC	VERWIDTH5 ISC	VERWIDT4 ISC	VERWIDTH3 ISC	VERWIDTH2 ISC	VERWIDTH1 ISC	VERWIDTH0 ISC
08	VERPOS7 ISC	VERPOS6 ISC	VERPOS5 ISC	VERPOS4 ISC	VERPOS3 ISC	VERPOS2 ISC	VERPOS1 ISC	VERPOS0 ISC
09	HORWIDTH5 ISC	HORWIDTH4 ISC	HORWIDTH3 ISC	HORWIDTH2 ISC	HORWIDTH1 ISC	HORWIDT0 ISC	PLL1RA1 PLL1	PLL1RA0 PLL1
0A	HORPOS5 ISC	HORPOS4 ISC	HORPOS3 ISC	HORPOS2 ISC	HORPOS1 ISC	HORPOS0 ISC	PLL1RA3 PLL1	PLL1RA2 PLL1
0B	NALOP7 OSC	NALOP6 OSC	NALOP5 OSC	NALOP4 OSC	NALOP3 OSC	NALOP2 OSC	NALOP1 OSC	NALOP0 OSC
0C	ALPFOP7 OSC	ALPFOP6 OSC	ALPFOP5 OSC	ALPFOP4 OSC	ALPFOP3 OSC	ALPFOP2 OSC	ALPFOP1 OSC	ALPFOP0 OSC
0D	LPFOP7 OSC	LPFOP6 OSC	LPFOP5 OSC	LPFOP4 OSC	LPFOP3 OSC	LPFOP2 OSC	LPFOP1 OSC	LPFOP0 OSC
0E	NAPOP7 OSC	NAPOP6 OSC	NAPOP5 OSC	NAPOP4 OSC	NAPOP3 OSC	NAPOP2 OSC	NAPOP1 OSC	NAPOP0 OSC
0F	HOUTDEL7 OSC	HOUTDEL6 OSC	HOUTDEL5 OSC	HOUTDEL4 OSC	HOUTDEL3 OSC	HOUTDEL2 OSC	HOUTDEL1 OSC	HOUTDEL0 OSC
10	APPLOP5 OSC	APPLOP4 OSC	APPLOP3 OSC	APPLOP2 OSC	APPLOP1 OSC	APPLOP0 OSC	CAPP1 OSC	CAPP0 OSC
11	PPLOP7 OSC	PPLOP6 OSC	PPLOP5 OSC	PPLOP4 OSC	PPLOP3 OSC	PPLOP2 OSC	PPLOP1 OSC	PPLOP0 OSC
12	PPLOP8 OSC	STOPMODE3 OSC	STOPMODE2 OSC	STOPMODE1 OSC	STOPMODE0 OSC	ADOPMOD2 OSC	ADOPMOD1 OSC	ADOPMOD0 OSC
13	INTMODE3 OSC	INTMODE2 OSC	VERINT5 OSC	VERINT4 OSC	VERINT3 OSC	VERINT2 OSC	VERINT1 OSC	VERINT0 OSC
14	INTMODE1 OSC	INTMODE0 OSC	EXSYN OSC	RMODE OSC	VOUTFR OSC	HOUTFR OSC	VOUTPOL OSC	HOUTPOL OSC
15	WINDVON OSC	WINDVDR OSC	WINDVST OSC	WINDVSP1 OSC	WINDVSP0 OSC	CONV2 OSC	CONV1 OSC	CONV0 OSC

16	WINDHON OSC	WINDHDR OSC	WINDHST OSC	WINDHSP1 OSC	WINDHSP0 OSC	CLKOUTON PLL2	PLL2OFF PLL2	x
17	YBORDER3 OFC/LDR	YBORDER2 OFC/LDR	YBORDER1 OFC/LDR	YBORDER0 OFC/LDR	FLASHON OFC	TWOOUT OFC	FIXSHR HDR	MEDON HDR
18	UBORDER3 OFC/LDR	UBORDER2 OFC/LDR	UBORDER1 OFC/LDR	UBORDER0 OFC/LDR	VBORDER3 OFC/LDR	VBORDER2 OFC/LDR	VBORDER1 OFC/LDR	VBORDER0 OFC/LDR
19	PLL2RA3 PLL2	PLL2RA2 PLL2	PLL2RA1 PLL2	PLL2RA0 PLL2	CLK21EN PLL2	CLK11EN PLL2	CSMOFF HDR	PSMOFF HDR
1A	VPAN7 MC	VPAN6 MC	VPAN5 MC	VPAN4 MC	VPAN3 MC	VPAN2 MC	VPAN1 MC	VPAN0 MC
1B	MULTIPIC1 LDR/ISC	MULTIPIC0 LDR/ISC	PICPOS3 LDR/MC	PICPOS2 LDR/MC	PICPOS1 LDR/MC	PICPOS0 LDR/MC	FREEZE MC	FREQR MC/OSC/HD
1C	VDECON2 LDR	VDECON1 LDR	VDECON0 LDR	HDECON1 LDR/ISC	HDECON0 LDR/ISC	AMMON1 LDR	AMMON0 LDR	FRAFION LDR
1D	NRON LDR/MC	SNRON LDR	VCSNRON LDR	HCSNRON LDR	DTNRON LDR	MOVPHINV LDR	TNRSEL LDR	NMALG LDR
1E	TNRCLY3 LDR	TNRCLY2 LDR	TNRCLY1 LDR	TNRCLY0 LDR	TNRCLC3 LDR	TNRCLC2 LDR	TNRCLC1 LDR	TNRCLC0 LDR
1F	TNRKOY3 LDR	TNRKOY2 LDR	TNRKOY1 LDR	TNRKOY0 LDR	TNRKOC3 LDR	TNRKOC2 LDR	TNRKOC1 LDR	TNRKOC0 LDR
20	TNRVAY3 LDR	TNRVAY2 LDR	TNRVAY1 LDR	TNRVAY0 LDR	TNRVAC3 LDR	TNRVAC2 LDR	TNRVAC1 LDR	TNRVAC0 LDR
21	TNRHOY5 LDR	TNRHOY4 LDR	TNRHOY3 LDR	TNRHOY2 LDR	TNRHOY1 LDR	TNRHOY0 LDR	TNRFIY LDR	HPE1OFF LDR
22	TNRHOC5 LDR	TNRHOC4 LDR	TNRHOC3 LDR	TNRHOC2 LDR	TNRHOC1 LDR	TNRHOC0 LDR	TNRFIC LDR	VLEROFF LDR
23	GMTHU6 LDR	GMTHU5 LDR	GMTHU4 LDR	GMTHU3 LDR	GMTHU2 LDR	GMTHU1 LDR	GMTHU0 LDR	HPS1OFF LDR
24	GMTHL6 LDR	GMTHL5 LDR	GMTHL4 LDR	GMTHL3 LDR	GMTHL2 LDR	GMTHL1 LDR	GMTHL0 LDR	HPE2OFF LDR
25	GMAS4 LDR	GMAS3 LDR	GMAS2 LDR	GMAS1 LDR	GMAS0 LDR	MMTC3 LDR	MMTC2 LDR	HPEXOFF LDR
26	GMAM4 LDR	GMAM3 LDR	GMAM2 LDR	GMAM1 LDR	GMAM0 LDR	MMTC1 LDR	MMTC0 LDR	VLEXOFF LDR
27	MMTHL6 LDR	MMTHL5 LDR	MMTHL4 LDR	MMTHL3 LDR	MMTHL2 LDR	MMTHL1 LDR	MMTHL0 LDR	x
28	NMLINE4 LDR	NMLINE3 LDR	NMLINE2 LDR	NMLINE1 LDR	NMLINE0 LDR	SVALLI1 LDR	SVALLI0 LDR	x
29	THLI25 LDR	THLI24 LDR	THLI23 LDR	THLI22 LDR	THLI21 LDR	THLI20 LDR	THLI14 LDR	THLI13 LDR
2A	THLI12 LDR	THLI11 LDR	THLI10 LDR	THLI03 LDR	THLI02 LDR	THLI01 LDR	THLI00 LDR	THFI34 LDR
2B	THFI33 LDR	THFI32 LDR	THFI31 LDR	THFI30 LDR	THFI24 LDR	THFI23 LDR	THFI22 LDR	THFI21 LDR
2C	THFI20 LDR	THFI14 LDR	THFI13 LDR	THFI12 LDR	THFI11 LDR	THFI10 LDR	THFI03 LDR	THFI02 LDR
2D	THFI01 LDR	THFI00 LDR	THFR34 LDR	THFR33 LDR	THFR32 LDR	THFR31 LDR	THFR30 LDR	THFR24 LDR
2E	THFR23 LDR	THFR22 LDR	THFR21 LDR	THFR20 LDR	THFR13 LDR	THFR12 LDR	THFR11 LDR	THFR10 LDR

2F	THFR03 LDR	THFR02 LDR	THFR01 LDR	THFR00 LDR	SVALFI1 LDR	SVALFI0 LDR	SVALFR1 LDR	SVALFR0 LDR
30	THYON	RESMOV	THRMOV4 LDR	THRMOV3 LDR	THRMOV2 LDR	THRMOV1 LDR	THRMOV0 LDR	x
31	SWGM1	SWGM0	THRGM4 LDR	THRGM3 LDR	THRGM2 LDR	THRGM1 LDR	THRGM0 LDR	x
32	NOISME4 LDR	NOISME3 LDR	NOISEME2 LDR	NOISEME1 LDR	NOISEME0 LDR	VERSION2	VERSION1	VERSION0
33	GMOTION LDR	MOVMO LDR	MOVPH LDR	TVMODE LDR	VISTATUS	OSSTATUS	MDSTATUS	NMSTATUS
FF	x	x	x	x	x	x	x	x

x = don’t care

ISC - Input sync controller block
IFC - Input format conversion block
OSC - Output sync controller block
OFC - Output format conversion block
LDR - Low data rate block
HDR - High data rate block
MC - Memory controller
PLL1 - Clock doubling block 1
PLL2 - Clock doubling block 2

6.8.4 Detailed description

Default values are underlined.

Subaddress 00		
Bit	**Name**	**Function**
D7...D6	FORMAT	Input format: 11: full CCIR 656 10: CCIR 656 only data, H- and V-sync according CCIR656 01: CCIR 656 only data, H- and V-sync according PAL/NTSC 00: 4:2:2
D5	FIEINV	Field polarity inversion: 1: Field A=1, Field B=0 0: Field A=0, Field B=1
D4	VCRMODE	Input filtering of the incoming field signal: 1: on 0: off
D3	PIMODE	Picture insert mode (see VERWIDTH, VERPOS, HORWIDTH, HORPOS): 1: on 0: off
D2...D1	NAPIPPH (LSBs of NAPLIP)	Number of not active pixels from external HIN to the input data in system clocks of CLK1: Number(HIN to input data) = (NAPIPDL*4+NAPIPPH+8) [NAPIPPH = 0]
D0	TWOIN	Chrominance input format: 1: 2's complement input (-128...127) 0: unsigned input (0...255) inside the SDA 9400 the data are always processed as unsigned data

Subaddress 01		
Bit	**Name**	**Function**
D7...D2	VINDEL	VIN input delay: Delay(VIN to internal V-sync) = (128 * VINDEL + 1)*Tclk1 [VINDEL = 0]
D1	VINPOL	VIN polarity: 1: low active 0: high active
D0	HINPOL	HIN polarity: 1: low active 0: high active

Subaddress 02		
Bit	**Name**	**Function**
D7...D2	NALIP	Number of not active lines per field in the input data stream: Not active lines = NALIP+3 [NALIP= 20]
D1	PLL1OFF	PLL1 switch: 1: off 0: on
D0	REFRESH	Internal refresh: 1: on 0: off

Subaddress 03		
Bit	**Name**	**Function**
D7...D0	ALPFIP	Number of active lines per field in the input data stream: Active lines = ALPFIP * 2 [ALPFIP=144]

Subaddress 04		
Bit	**Name**	**Function**
D7...D0	NAPIPDL (MSBs of NAPLIP)	Number of not active pixels from HIN to the input data in system clocks of CLK1: Number(HIN to input data) = (4 * NAPIPDL + NAPIPPH + 8) [NAPIPDL= 0]

Subaddress 05		
Bit	**Name**	**Function**
D7...D2	APPLIP	Number of active pixels per line in the input data stream in system clocks of CLK1: Active pixels = APPLIP*32 [APPLIP = 45] Inside the SDA 9400 the number of active pixels per line is APPL*32, with APPL = APPLIP, MULITPIC = 0 and HDECON = 0 (APPLIP + 1)/2, MULTIPIC = 0 and HDECON = 1 (APPLIP + 3)/4, MULTIPIC = 0 and HDECON = 2 45, MULTIPIC > 0
D1...D0	x	x

Subaddress 06		
Bit	**Name**	**Function**
D7...D0	OPDEL	Output processing delay (in number of lines): Delay(VIN to VOUT) = (OPDEL + 1) * Tline [OPDEL = 170]

Subaddress 07		
Bit	**Name**	**Function**
D7...D0	VERWIDTH	Vertical width of inserted picture in input lines: Vertical width = (2 * VERWIDTH) [VERWIDTH = 0]

Subaddress 08		
Bit	**Name**	**Function**
D7...D0	VERPOS	Vertical position of inserted picture in input lines: Vertical position = (2 * VERPOS) + NALIP + 3 [VERPOS = 0]

Subaddress 09		
Bit	**Name**	**Function**
D7...D2	HORWIDTH	Horizontal width of inserted picture in system clocks of CLK1: Horizontal width = (32 * HORWIDTH) [HORWIDTH = 0]
D1...D0	PLL1RA(1...0)	PLL1 range, only for test purposes [PPL1RA=0]

Subaddress 0A		
Bit	**Name**	**Function**
D7...D2	HORPOS	Horizontal position of inserted picture in system clocks of CLK1: Horizontal position = (32 * HORPOS) + (4 * NAPIPDL + NAPIPPH + 8) [HORPOS = 0]
D1...D0	PLL1RA(3...2)	PLL1 range, only for test purposes [PPL1RA=0]

Subaddress 0B		
Bit	**Name**	**Function**
D7...D0	NALOP	Number of not active lines per frame in the output data stream: Not active lines = 2 * (NALOP + 1) [NALOP= 22]

Subaddress 0C		
Bit	**Name**	**Function**
D7...D0	ALPFOP	Number of active lines per output frame: Active lines = 4 * ALPFOP [ALPFOP= 144]

Subaddress 0D		
Bit	**Name**	**Function**
D7...D0	LPFOP	Number of lines per output frame (only valid for VOUTFR=1): Number of lines = 4 * LPFOP + 1 [LPFOP = 156]

Subaddress 0E		
Bit	**Name**	**Function**
D7...D0	NAPOP	Number of not active pixels (coloured border values) from external HREF to the first active pixel of the output data stream in system clocks of X1/ CLK2: Distance(HREF to output data) = (4 * NAPOP) [NAPOP = 0]

Subaddress 0F		
Bit	**Name**	**Function**
D7...D0	HOUTDEL	HOUT delay: Delay(HOUT to HREF) = (4 * (HOUTDEL + 1) + 36) *Tx1/clk2 [HOUTDEL = 4]

Subaddress 10		
Bit	**Name**	**Function**
D7...D2	APPLOP	Number of active pixels per line (including coloured border values and data) in the output data stream in system clocks of X1/CLK2 (length of HREF): Active pixels = 16 * APPLOP [APPLOP = 45]
D1...D0	CAPP	Reduces the active pixels per line (APPL) at the output side: Active pixels per line at the output side in system clocks of X1/CLK2 = 16 * APPL - 2 * k k = 24: CAPP = 11 16: CAPP = 10 8: CAPP = 01 0: CAPP = 00

Subaddress 11		
Bit	**Name**	**Function**
D7...D0	PPLOP(7...0)	Number of pixels between two output H-syncs HOUT (only valid for HOUTFR=1) in system clocks of X1/CLK2 (Bit 7 to 0): Number of pixels = 2 * PPLOP [PPLOP = 432]

Subaddress 12		
Bit	**Name**	**Function**
D7	PPLOP(8)	Number of pixels between two output H-syncs HOUT (only valid for HOUTFR=1) in system clocks of X1/CLK2 (Bit 8): Number of pixels = 2 * PPLOP [PPLOP = 432]
D6...D3	STOPMODE	Static operation modes (see also *Operation mode generator* on page 46): 1011: Soft Mix II (interlaced)
D2...D0	ADOPMODE	Dynamic operation modes (see also *Operation mode generator* on page 46): 000: no adaptive operation mode: operation mode defined by STOP-MODE

Subaddress 13		
Bit	**Name**	**Function**
D7...D6	INTMODE(3...2)	Free programmable INTERLACED signal for AC coupled deflection stages (Bit 3 and Bit 2) [INTMODE3...2 = 0]
D5...D0	VERINT	Vertical expansion factor (see also *High data rate processing (HDR)* on page 60): 63: no vertical expansion : 47: vertical expansion with factor 1.5 : 31: vertical expansion with factor 2 :

Subaddress 14		
Bit	**Name**	**Function**
D7...D6	INTMODE(1...0)	Free programmable INTERLACED signal for AC coupled deflection stages (Bit 1 and Bit 0) [INTMODE1...0 = 0]
D5	EXSYN	External synchronization (only valid for HOUTFR=0 and VOUTFR=0): 1: on 0: off
D4	RMODE	Raster mode: 1: progressive 0: interlaced
D3	VOUTFR	VOUT generator: 1: freerunning mode 0: locked mode
D2	HOUTFR	HOUT generator 1: freerunning mode 0: locked mode
D1	VOUTPOL	VOUT (EXSYN=0), VEXT (EXSYN=1) polarity: 1: low active 0: high active
D0	HOUTPOL	HOUT (EXSYN=0), HEXT (EXSYN=1) polarity: 1: low active 0: high active

Subaddress 15		
Bit	**Name**	**Function**
D7	WINDVON	Vertical window: 1: on 0: off
D6	WINDVDR	1: close the vertical window 0: open the vertical window
D5	WINDVST	Status of vertical window after entering vertical window mode: 1: window is opened 0: window is closed
D4...D3	WINDVSP	Speed of vertical window (see also *Window generator* on page 57): 11: very fast 10: fast 01: medium 00: slow
D2...D0	CONV	Defines scan rate conversion mode (only valid for VOUTFR=0, see also *VOUT generator* on page 44): 000: 100/120 interlaced (RMODE=0), 50/60 Hz progressive (RDMODE=1)

Subaddress 16		
Bit	**Name**	**Function**
D7	WINDHON	Horizontal window: 1: on 0: off
D6	WINDHDR	1: close the horizontal window 0: open the horizontal window
D5	WINDHST	Status of horizontal window after entering horizontal window mode: 1: window is opened 0: window is closed
D4...D3	WINDHSP	Speed of horizontal window (see also *Window generator* on page 57): 11: very fast 10: fast 01: medium 00: slow
D2	CLKOUTON	Output of system clock CLKOUT: 1: enabled 0: disabled
D1	PLL2OFF	PLL2 switch: 1: off 0: on
D0	x	x

Subaddress 17		
Bit	**Name**	**Function**
D7...D4	YBORDER	Y border value (Yborder(3) Yborder(2) Yborder(1) Yborder(0) 0 0 0 0 = 00010000 = 16), YBORDER defines the 4 MSB's of a 8 bit value
D3	FLASHON	Flash of output picture: 1: on 0: off
D2	TWOOUT	Chrominance output format: 1: 2's complement input (-128...127) 0: unsigned input (0...255) inside the SDA 9400 the data are always processed as unsigned data
D1	FIXSHR	Fixed temporal filtering on: 1: on 0: off
D0	MEDON	Used filter type for raster interpolation: 1: Median 0: Linear

Subaddress 18		
Bit	**Name**	**Function**
D7...D4	UBORDER	U border value (Uborder(3) Uborder(2) Uborder(1) Uborder(0) 0 0 0 0 = 10000000 = 128), UBORDER defines the 4 MSB's of a 8 bit value
D3...D0	VBORDER	V border value (Vborder(3) Vborder(2) Vborder(1) Vborder(0) 0 0 0 0 = 10000000 = 128), VBORDER defines the 4 MSB's of a 8 bit value

Subaddress 19		
Bit	**Name**	**Function**
D7...D4	PLL2RA	PLL2 range, only for test purposes [PPL2RA=0]
D3	CLK21EN	PLL2 input signal (see also *Clock concept* on page 37): 1: external CLK1 0: external X1/CLK2
D2	CLK11EN	Internal clock switch for CLKOUT (see also *Clock concept* on page 37): 1: PLL2 output 0: external CLK1
D1	CSMOFF	Temporal mixing I: 1: off 0: on

Subaddress 19		
Bit	**Name**	**Function**
D0	PSMOFF	Temporal mixing II: 1: off 0: on

Subaddress 1A		
Bit	**Name**	**Function**
D7...D0	VPAN	Vertical adjustment of the output picture [VPAN = 0]

Subaddress 1B		
Bit	**Name**	**Function**
D7...D6	MULTIPIC	Multipicture modes: 11: sixteenfold 10: twelvefold 01: fourfold 00: off (In case of MULTIPIC>0, spatial and temporal noise reduction as well as the motion detection for scan rate conversion are disabled)
D5...D2	PICPOS	Position for the picture in the multipicture mode (only valid for MULTIPIC > 0, see also *Multipicture display* on page 20) [PICPOS = 0]
D1	FREEZE	Freeze mode (frozen picture): 1: on 0: off
D0	FREQR	Frequency of system clock X1/CLK2: 1: X1/CLK2 > 27 MHZ + 10% 0: X1/CLK2 <= 27 MHz + 10%

Subaddress 1C		
Bit	**Name**	**Function**
D7...D5	VDECON	Vertical decimation of the input data stream: 111: not used 110: factor 4.0 101: factor 3.0 100: factor 2.0 011: factor 1.75 010: factor 1.5 001: factor 1.25 000: off (In case of VDECON>0, spatial noise reduction as well as the motion detection for scan rate conversion are disabled)
D4...D3	HDECON	Horizontal decimation of the input data stream: 11: not used 10: factor 4.0 01: factor 2.0 00: off (In case of HDECON>0, spatial noise reduction as well as the motion detection for scan rate conversion are disabled)
D2...D1	AMMON	Automatic movie mode for the motion detection for the scan rate conversion: In case of movie mode, the motion detection for scan rate conversion will be automatically switched to 11: no motion 10: only frame difference 0X: off
D0	FRAFION	Motion detection for the scan rate conversion: 1: based on frame difference and field difference 0: based only on frame difference (In case of AMMON>1 and no movie mode, the motion detection for scan rate conversion is still defined by FRAFION)

Subaddress 1D		
Bit	**Name**	**Function**
D7	NRON	Temporal noise reduction of luminance and chrominance: 1: enabled 0: disabled
D6	SNRON	Spatial noise reduction of luminance: 1: enabled 0: disabled
D5	VCSNRON	Vertical spatial noise reduction of chrominance: 1: enabled 0: disabled

Subaddress 1D		
Bit	**Name**	**Function**
D4	HCSNRON	Horizontal spatial noise reduction of chrominance: 1: enabled 0: disabled
D3	DTNRON	Temporal noise reduction of luminance: 1: frame based 0: field based
D2	MOVPHIN	Inversion of the MOVPH signal: 1: enabled 0: disabled
D1	TNRSEL	Motion detection of temporal noise reduction of chrominance: 1: separate motion detector 0: luminance motion detector
D0	NMALG	Noise measurement algorithm: 1: measurement during vertical blanking period (line can be defined by NMLINE) 0: measurement in the active picture (first active line)

Subaddress 1E		
Bit	**Name**	**Function**
D7...D4	TNRCLY	Temporal noise reduction of luminance: classification 1111: slight noise reduction : 0000: strong noise reduction
D3...D0	TNRCLC	Temporal noise reduction of chrominance: classification 1111: slight noise reduction : 0000: strong noise reduction

Subaddress 1F		
Bit	**Name**	**Function**
D7...D4	TNRKOY	Temporal noise reduction of luminance: Vertical shift of the motion detector characteristic [TNRKOY=0]
D3...D0	TNRKOC	Temporal noise reduction of chrominance: Vertical shift of the motion detector characteristic [TNRKOC=0]

Subaddress 20		
Bit	**Name**	**Function**
D7...D4	TNRVAY	Fixed K-factor for temporal noise reduction of luminance [TNRVAY = 15]
D3...D0	TNRVAC	Fixed K-factor for temporal noise reduction of chrominance [TNRVAC = 15]

Subaddress 21		
Bit	**Name**	**Function**
D7...D2	TNRHOY	Temporal noise reduction of luminance: Horizontal shift of the motion detector characteristic [TNRHOY=0]
D1	TNRFIY	Fixed K-factor switch for temporal noise reduction of luminance: 1: off 0: on
D0	HPE1OFF	Horizontal pixel erosion 1 of motion detection for scan rate conversion: 1: off 0: on

Subaddress 22		
Bit	**Name**	**Function**
D7...D2	TNRHOC	Temporal noise reduction of chrominance: Horizontal shift of the motion detector characteristic [TNRHOC=0]
D1	TNRFIC	Fixed K-factor switch for temporal noise reduction of chrominance: 1: off 0: on
D0	VLEROFF	Vertical line erosion of motion detection for scan rate conversion: 1: off 0: on

Subaddress 23		
Bit	**Name**	**Function**
D7...D1	GMTHU	Global motion detection spatial hysteresis: upper threshold [GMTHU =68]
D0	HPS1OFF	Horizontal pixel smearing 1 of motion detection for scan rate conversion: 1: off 0: on

Subaddress 24		
Bit	**Name**	**Function**
D7...D1	GMTHL	Global motion detection spatial hysteresis: lower threshold [GMTHL =67]
D0	HPE2OFF	Horizontal pixel erosion 2 of motion detection for scan rate conversion: 1: off 0: on

Subaddress 25		
Bit	**Name**	**Function**
D7...D3	GMAS	Global motion detection amount of still pictures [GMAS = 29]
D2...D1	MMTC(3...2)	Movie mode detection time constant [MMTC3...2 = 2]
D0	HPEXOFF	Horizontal pixel extension of motion detection for scan rate conversion: 1: off 0: on

Subaddress 26		
Bit	**Name**	**Function**
D7...D3	GMAM	Global motion detection amount of moving pictures [GMAM = 16]
D2...D1	MMTC(1...0)	Movie mode detection time constant [MMTC1...0 = 2]
D0	VLEXOFF	Vertical line extension of motion detection for scan rate conversion: 1: off 0: on

Subaddress 27		
Bit	**Name**	**Function**
D7...D1	MMTHL	Movie mode detection threshold [MMTHL = 12]
D0	x	x

Subaddress 28		
Bit	**Name**	**Function**
D7...D3	NMLINE	Line for noise measurement (only valid for NMALG=1) [NMLINE = 4]
D2...D1	SVALLI	Sensitivity of line difference in the motion detection for scan rate conversion: 11: factor 32 (minimum) 10: factor 16 01: factor 8 00: factor 4 (maximum)
D0	x	x

Subaddress 29		
Bit	**Name**	**Function**
D7...D2	THLI2	Threshold 2 of line difference in the motion detection for scan rate conversion [THLI2 = 12]
D1...D0	THLI1(4...3)	Threshold 1 (Bit 4 and Bit 3) of line difference in the motion detection for scan rate conversion [THLI14...3 = 1]

Subaddress 2A		
Bit	**Name**	**Function**
D7...D5	THLI1(2...0)	Threshold 1 (Bit 2, Bit 1 and Bit 0) of line difference in the motion detection for scan rate conversion [THLI12...0 = 0]
D4...D1	THLI0	Threshold 0 of line difference in the motion detection for scan rate conversion [THLI0 = 4]
D0	THFI3(4)	Threshold 3 (Bit 4) of field difference in the motion detection for scan rate conversion [THFI34 = 1]

Subaddress 2B		
Bit	**Name**	**Function**
D7...D4	THFI3(3...0)	Threshold 3 (Bit 3, Bit 2,Bit 1and Bit 0) of field difference in the motion detection for scan rate conversion [THFI33...0 = 12]
D3...D0	THFI2(4...1)	Threshold 2 (Bit 4, Bit3, Bit 2 and Bit 1) of field difference in the motion detection for scan rate conversion [THFI24...1 = 9]

Subaddress 2C		
Bit	**Name**	**Function**
D7	THFI2(0)	Threshold 2 (Bit 0) of field difference in the motion detection for scan rate conversion [THFI20 = 0]
D6...D2	THFI1	Threshold 1 of field difference in the motion detection for scan rate conversion [THFI1 = 16]
D1...D0	THFI0(3...2)	Threshold 0 (Bit 3 and Bit 2) of field difference in the motion detection for scan rate conversion [THFI03...2 = 2]

Subaddress 2D		
Bit	**Name**	**Function**
D7...D6	THFI0(1...0)	Threshold 0 (Bit 1 and Bit 0) of field difference in the motion detection for scan rate conversion [THFI01...0 = 0]
D5...D1	THFR3	Threshold 3 of frame difference in the motion detection for scan rate conversion [THFR3 = 10]
D0	THFR2(4)	Threshold 2 (Bit 4) of frame difference in the motion detection for scan rate conversion [THFR24 = 0]

Subaddress 2E		
Bit	**Name**	**Function**
D7...D4	THFR23...0	Threshold 2 (Bit 3, Bit2, Bit1 and Bit 0) of frame difference in the motion detection for scan rate conversion [THFR23...0 = 6]
D3...D0	THFR1	Threshold 1 of frame difference in the motion detection for scan rate conversion [THFR1 = 4]

Subaddress 2F		
Bit	**Name**	**Function**
D7...D4	THFR0	Threshold 0 of frame difference in the motion detection for scan rate conversion [THFR0 = 3]
D3...D2	SVALFI	Sensitivity of field difference in the motion detection for scan rate conversion: 11: factor 8 (minimum) 10: factor 4 01: factor 2 00: factor 1 (maximum)

Subaddress 2F		
Bit	**Name**	**Function**
D1...D0	SVALFR	Sensitivity of frame difference in the motion detection for scan rate conversion: 11: factor 8 (minimum) 10: factor 4 01: factor 2 00: factor 1 (maximum)

Subaddress 30		
Bit	**Name**	**Function**
D7	THYON	Time hysteresis for movie mode detection on/off: 1: on (camera->movie: 2*(MMTC+1); movie->camera: (MMTC+1) 0: off (2*(MMTC+1))
D6	RESMOV	Reset of movie detection time hysteresis queue 1: Reset: movmo=0 (camera mode) 0: no reset
D5...D1	THRMOV	Threshold of field difference in the motion detection for movie mode detection [THRMOV = 8]
D0	x	x

Subaddress 31		
Bit	**Name**	**Function**
D7...D6	SWGM	Switch for global motion detection 11: field difference not influenced by motion detection for src 10: field difference, influenced by motion detection for src 01: frame difference, not influenced by motion detection for src 00: frame difference, influenced by motion detection for src
D5...D1	THRGM	Threshold of frame difference in the motion detection for global motion detection [THRGM = 8]
D0	x	x

Subaddress 32		
Bit	**Name**	**Function**
D7...D3	NOISEME	Noise level of the input signal: 0 (no noise), ..., 30 (strong noise) [31 (strong noise or measurement failed)]

Subaddress 32		
Bit	**Name**	**Function**
D2...D0	VERSION	Version of SDA 94XX family: 000: SDA 9400 001: SDA 9401 010: SDA 9402

Subaddress 33		
Bit	**Name**	**Function**
D7	GMOTION	Global motion detection: motion value 1: motion in the picture 0: no motion in the picture
D6	MOVMO	Movie mode detection: 1: movie mode 0: camera mode
D5	MOVPH	Movie phase detection: 1: A^n and B^{n-1} have the same phase 0: B^n and A^n and have the same phase
D4	TVMODE	TV mode of the input signal 1: NTSC 0: PAL
D3	VISTATUS	Status bit for subaddresses, which will be made valid by VIN 1: New write or read cycle can start 0: No new write or read cycle can start
D2	OSSTATUS	Status bit for subaddresses, which will be made valid by OPSTART 1: New write or read cycle can start 0: No new write or read cycle can start
D1	MDSTATUS	Status bit for motion detection parameters: 1: One of GMOTION, MOVMO, MOVPH and TVMODE changed its value 0: None of GMOTION, MOVMO, MOVPH and TVMODE changed its value
D0	NMSTATUS	Status bit for noise measurement parameter: 1: New value of NOISEME available 0: No new value of NOISEME available

Subaddress FF		
Bit	**Name**	**Function**
D7...D0		Store command for all subaddresses

7 Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit	Remark
Operating Temperature	T_A	0	70	°C	
Storage Temperature	T_{STG}	-65	125	°C	
Junction Temperature	T_J		125	°C	
Soldering Temperature	T_S		260	°C	
Soldering Time	ts		10	s	
Input Voltage	V_I	-0.3	V_{DD}+0.3	V	not valid for I²C bus pins
Output Voltage	V_O	-0.3	V_{DD}+0.3	V	not valid for I²C bus pins
Input Voltage	V_I	-0.3	5.5	V	I²C bus pins only
Output Voltage	V_O	-0.3	5.5	V	I²C bus pins only
Supply Voltages	V_{DD}	-0.3	3.8	V	
Total Power Dissipation	THD		1	W	
ESD Protection	ESD	-2,0	2,0	kV	MIL STD 883C method 3015.6, 100pF, 1500Ω (HBM)
ESD Protection	ESD	-1,5	1,5	kV	EOS/ESD Assn. Standard DS 5.3-1993 (CDM)
Latch-Up Protection		-100	100	mA	all inputs/outputs

All voltages listed are referenced to ground (0V, V_{SS}) except where noted.

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions or at any other condition beyond those indicated in the operational sections of this specification is not implied.

8 Recommended operating conditions

Parameter	Symbol	Min	Nom	Max	Unit	Remark
Supply Voltages	V_{DD}	3.15	3.3	3.45	V	
Ambient Temperature	T_A	0	25	70	°C	
All TTL Inputs						
High-Level Input Voltage	V_{IH}	2.0		V_{DD} +0.2	V	
Low-Level Input Voltage	V_{IL}	-0.2		0.8	V	
Input Current	I_{IN}			+/- 5	µA	
All TTL Outputs						
High-Level Output Voltage	V_{OH}	2.4			V	I_{OH} = -2.0 mA
Low-Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 2.0 mA
INPUT/OUTPUT: SDA						
Low-Level Output Voltage	V_{OL}			0.5	V	at I_{OL} = max
Clock TTL Input CLK1						
Clock frequency	$1/T$		27		MHz	see diagr. 11.3
Low time	t_{WL}	10			ns	
High time	t_{WH}	10			ns	
Rise time	t_{TLH}			10	ns	
Fall time	t_{THL}			10	ns	
Input SYNCEN						
Low time	t_{WL2}	22			ns	see diagr. 11.3
High time	t_{WH2}	22			ns	
Rise time	t_{TLH2}			10	ns	
Fall time	t_{THL2}			10	ns	
Clock TTL Input X1/CLK2						
Clock frequency	$1/T$			40.5	MHz	see diagr. 11.3
Low time	t_{WL}	9			ns	
High time	t_{WH}	9			ns	
Rise time	t_{TLH}			3	ns	
Fall time	t_{THL}			3	ns	
I²C bus (All Values Are Referred To min(V_{IH}) And max(V_{IL})), f_{SCL} = 400 KHz						
High-Level Input Voltage	V_{IH}	3		5.25	V	see diagr. 11.1
Low-Level Input Voltage	V_{IL}	0		1.5	V	see diagr. 11.2
SCL Clock Frequency	f_{SCL}	0		400	kHz	
Inactive Time Before Start Of Transmission	t_{BUF}	1.3			µs	
Set-Up Time Start Condition	$t_{SU;STA}$	0.6			µs	

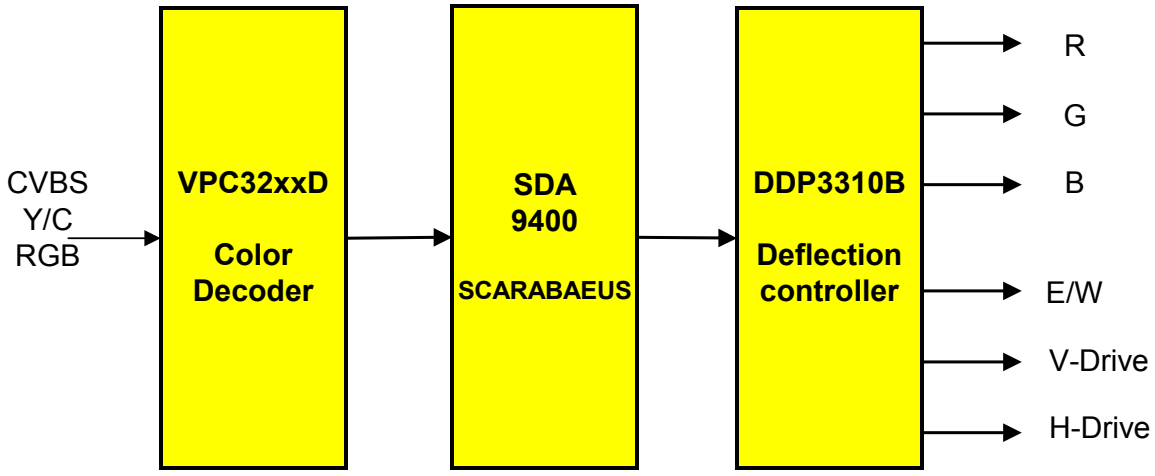
Parameter	Symbol	Min	Nom	Max	Unit	Remark
Hold Time Start Condition	$t_{HD;STA}$	0.6			µs	
SCL Low Time	t_{LOW}	1.3			µs	
SCL High Time	t_{HIGH}	0.6			µs	
Set-Up Time DATA	$t_{SU;DAT}$	100			ns	
Hold Time DATA	$t_{HD;DAT}$	0			µs	
SDA/SCL Rise Times	t_R			300	ns	
SDA/SCL Fall Times	t_F			300	ns	
Set-Up Time Stop Condition	$t_{SU;STO}$	0.6			µs	
Output valid from clock	t_{AA}			900	ns	
Input filter spike suppression (SDA and SCL pins)	t_{SP}			50	ns	
Low-Level Output Current	I_{QL}			3	mA	
Inputs crystal connections X1/CLK2, X2						see diagr. 11.4
Crystal frequency	xtal		27.0		MHz	fundamental crystal
Equivalent parallel Capacitance	Cin			27	pF	
Equivalent parallel Capacitance	Cout			27	pF	

9 Characteristics (Assuming Recommended Operating Conditions)

Parameter	Symbol	Min	Max	Unit	Remark
Average Supply Current		t.b.d.	t.b.d.	mA	All V_{DD} pins, typ. t.b.d.mA
All Digital Inputs (Including I/O Inputs)					
Input Capacitance			10	pF	
Input Leakage Current		-5	5	µA	
TTL Inputs: YIN, UVIN, HIN, VIN (Referenced To CLK1)					
Set-Up Time	t_{SU}	7		ns	see diagr. 11.3
Input Hold Time	t_{IH}	6		ns	
TTL Inputs: HEXT, VEXT (Referenced To X1/CLK2)					
Set-Up Time	t_{SU}	7		ns	see diagr. 11.3
Input Hold Time	t_{IH}	6		ns	
TTL Outputs: YOUT, UVOUT, HREF, INTERLACED (Referenced To CLKOUT*)					
Hold time	t_{OH}	6		ns	see diagr. 11.3
Delay time	t_{OD}		25	ns	C_L = 30 pF, 27 MHz
TTL Outputs: HOUT, VOUT (Referenced To CLKOUT)					
Hold time	t_{OH}	6		ns	see diagr. 11.3
Delay time	t_{OD}		25	ns	C_L = 50 pF, 27 MHz
TTL Outputs: YOUT, UVOUT, HREF, INTERLACED (Referenced To CLKOUT)					
Hold time	t_{OH}	3		ns	see diagr. 11.3
Delay time	t_{OD}		15	ns	C_L = 30 pF, 40,5 MHz
TTL Outputs: HOUT, VOUT (Referenced To CLKOUT)					
Hold time	t_{OH}	3		ns	see diagr. 11.3
Delay time	t_{OD}		15	ns	C_L = 50 pF, 40,5 MHz
TTL Inputs: SYNCEN (Referenced To CLK1)					
Set-Up Time	t_{SU2}	25		ns	see diagr. 11.3
Input Hold Time	t_{IH2}	0		ns	

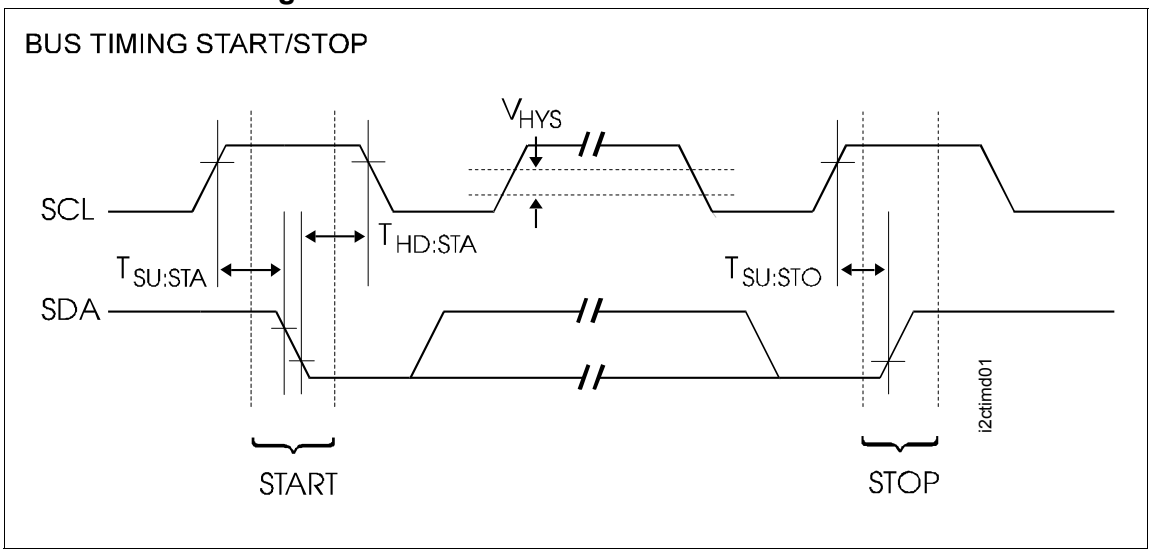
*: see also *Clock concept* on page 37

10 Application information

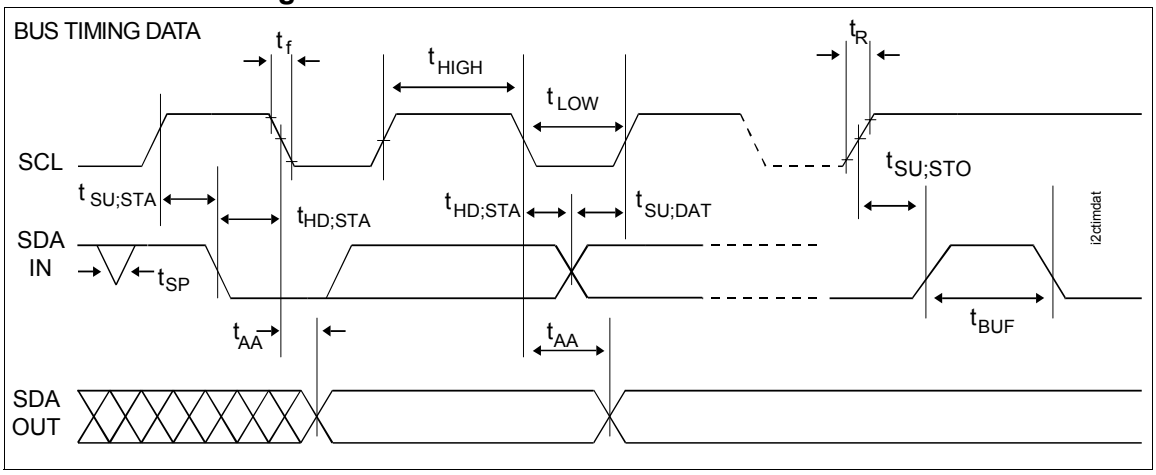


11 Waveforms

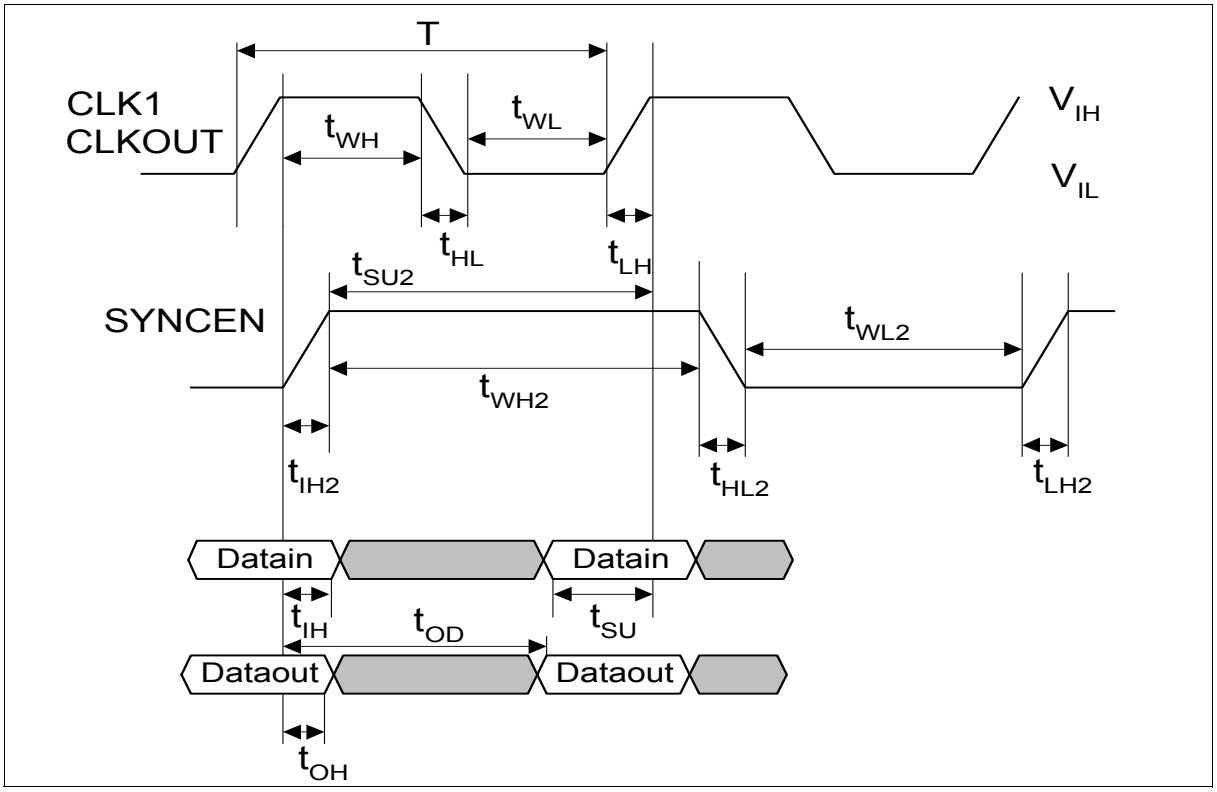
11.1 I²C-bus timing START/STOP



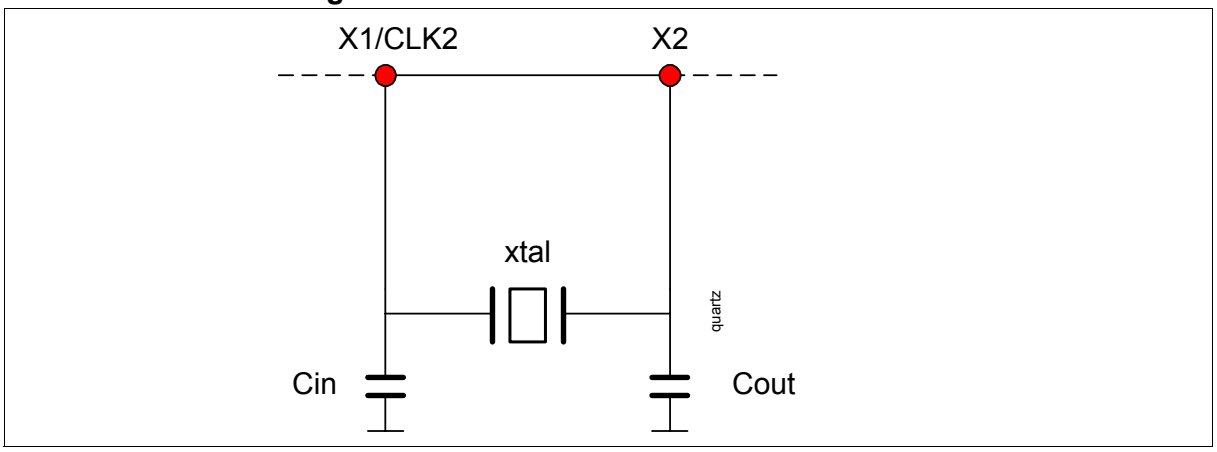
11.2 I²C-bus timing DATA



11.3 Timing diagram clock

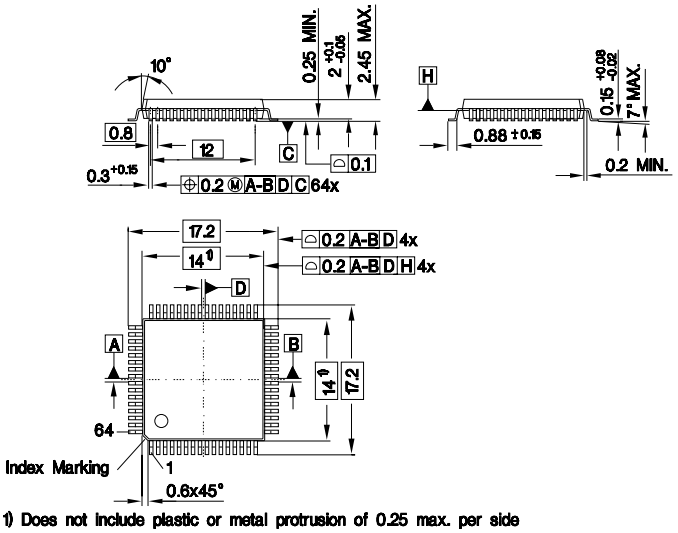


11.4 Clock circuit diagram



12 Package Outlines

P-MQFP-64



[All dimensions in mm]

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