

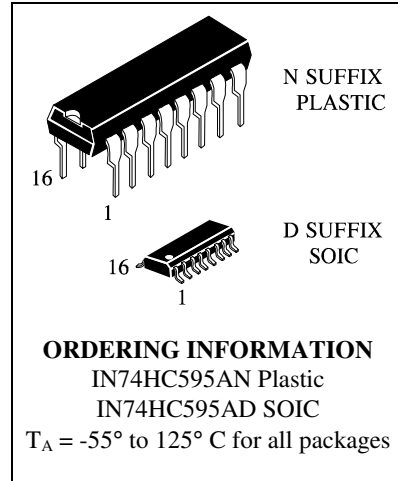
IN74HC595A

8-Bit Serial-Input/Serial or Parallel-Output Shift Register with Latched 3-State Outputs
High-Performance Silicon-Gate CMOS

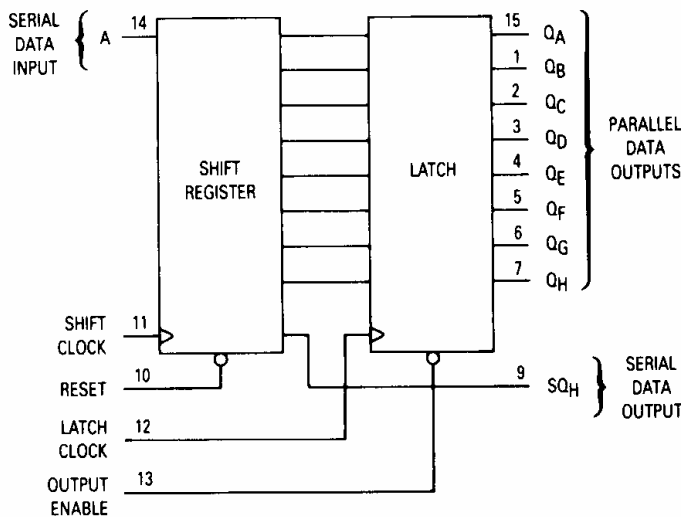
The IN74HC595A is identical in pinout to the LS/ALS595. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

The IN74HC595A consists of an 8-bit shift register and an 8-bit D-type latch with three-state parallel outputs. The shift register accepts serial data and provides a serial output. The shift register also provides parallel data to the 8-bit latch. The shift register and latch have independent clock inputs. This device also has an asynchronous reset for the shift register.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices

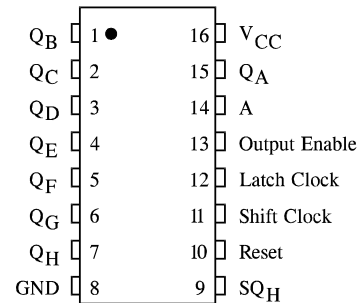


LOGIC DIAGRAM



PIN 16 = V_{CC}
 PIN 8 = GND

PIN ASSIGNMENT



MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|------------------|--|------------------------------|------|
| V _{CC} | DC Supply Voltage (Referenced to GND) | -0.5 to +7.0 | V |
| V _{IN} | DC Input Voltage (Referenced to GND) | -1.5 to V _{CC} +1.5 | V |
| V _{OUT} | DC Output Voltage (Referenced to GND) | -0.5 to V _{CC} +0.5 | V |
| I _{IN} | DC Input Current, per Pin | ±20 | mA |
| I _{OUT} | DC Output Current, per Pin | ±35 | mA |
| I _{CC} | DC Supply Current, V _{CC} and GND Pins | ±75 | mA |
| P _D | Power Dissipation in Still Air, Plastic DIP+ SOIC Package+ | 750 500 | mW |
| T _{stg} | Storage Temperature | -65 to +150 | °C |
| T _L | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) | 260 | °C |

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
 +Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
 SOIC Package: - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|------------------------------------|--|-----|-----------------|------|
| V _{CC} | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V |
| V _{IN} , V _{OUT} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V _{CC} | V |
| T _A | Operating Temperature, All Package Types | -55 | +125 | °C |
| t _r , t _f | Input Rise and Fall Time (Figure 1) | | | |
| | V _{CC} =2.0 V | 0 | 1000 | ns |
| | V _{CC} =4.5 V | 0 | 500 | |
| | V _{CC} =6.0 V | 0 | 400 | |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limit | | | Unit |
|-----------------|---|---|----------------------|----------------------|-----------|------------|------|
| | | | | 25 °C to -55°C | ≤85 °C | ≤125 °C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA | 2.0 | 1.5 | 1.5 | 1.5 | V |
| | | | 4.5 | 3.15 | 3.15 | 3.15 | |
| | | | 6.0 | 4.2 | 4.2 | 4.2 | |
| V _{IL} | Maximum Low - Level Input Voltage | V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA | 2.0 | 0.5 | 0.5 | 0.5 | V |
| | | | 4.5 | 1.35 | 1.35 | 1.35 | |
| | | | 6.0 | 1.8 | 1.8 | 1.8 | |
| V _{OH} | Minimum High-Level Output Voltage, Q _A -Q _H | V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | | 6.0 | 5.9 | 5.9 | 5.9 | |
| | | V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 6.0 mA I _{OUT} ≤ 7.8 mA | 4.5 | 3.98 | 3.84 | 3.7 | |
| | | | 6.0 | 5.48 | 5.34 | 5.2 | |
| | | | | | | | |
| V _{OL} | Maximum Low-Level Output Voltage, Q _A -Q _H | V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA | 2.0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5 | 0.1 | 0.1 | 0.1 | |
| | | | 6.0 | 0.1 | 0.1 | 0.1 | |
| | | V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 6.0 mA I _{OUT} ≤ 7.8 mA | 4.5 | 0.26 | 0.33 | 0.4 | |
| | | | 6.0 | 0.26 | 0.33 | 0.4 | |
| | | | | | | | |
| V _{OH} | Minimum High-Level Output Voltage, S _{Q_H} | V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | | 6.0 | 5.9 | 5.9 | 5.9 | |
| | | V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA | 4.5 | 3.98 | 3.84 | 3.7 | |
| | | | 6.0 | 5.48 | 5.34 | 5.2 | |
| | | | | | | | |
| V _{OL} | Maximum Low-Level Output Voltage, S _{Q_H} | V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA | 2.0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5 | 0.1 | 0.1 | 0.1 | |
| | | | 6.0 | 0.1 | 0.1 | 0.1 | |
| | | V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA | 4.5 | 0.26 | 0.33 | 0.4 | |
| | | | 6.0 | 0.26 | 0.33 | 0.4 | |
| | | | | | | | |
| I _{IN} | Maximum Input Leakage Current | V _{IN} =V _{CC} or GND | 6.0 | ±0.1 | ±1.0 | ±1.0 | μA |
| I _{OZ} | Maximum Three-State Leakage Current, Q _A -Q _H | Output in High-Impedance State V _{IN} = V _{IL} or V _{IH} V _{IN} =V _{CC} or GND | 6.0 | ±0.5 | ±5.0 | ±10 | μA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{IN} =V _{CC} or GND I _{OUT} =0μA | 6.0 | 4.0 | 40 | 160 | μA |

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6.0 ns)

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|-------------------------------------|---|---------------------------------------|----------------------|-----------|------------|------|
| | | | 25 °C to -55°C | ≤85 °C | ≤125 °C | |
| f _{max} | Minimum Clock Frequency (50% Duty Cycle) (Figures 1 and 7) | 2.0 | 6.0 | 4.8 | 4.0 | MHz |
| | | 4.5 | 30 | 24 | 20 | |
| | | 6.0 | 35 | 28 | 24 | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Shift Clock to SQ _H (Figures 1 and 7) | 2.0 | 140 | 175 | 210 | ns |
| | | 4.5 | 28 | 35 | 42 | |
| | | 6.0 | 24 | 30 | 36 | |
| t _{PHL} | Maximum Propagation Delay, Reset to SQ _H (Figures 2 and 7) | 2.0 | 145 | 180 | 220 | ns |
| | | 4.5 | 29 | 36 | 44 | |
| | | 6.0 | 25 | 31 | 38 | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Latch Clock to Q _A -Q _H (Figures 3 and 7) | 2.0 | 140 | 175 | 210 | ns |
| | | 4.5 | 28 | 35 | 42 | |
| | | 6.0 | 24 | 30 | 36 | |
| t _{PLZ} , t _{PHZ} | Maximum Propagation Delay, Output Enable to Q _A -Q _H (Figures 4 and 8) | 2.0 | 150 | 190 | 225 | ns |
| | | 4.5 | 30 | 38 | 45 | |
| | | 6.0 | 26 | 33 | 38 | |
| t _{PZL} , t _{PZH} | Maximum Propagation Delay, Output Enable to Q _A -Q _H (Figures 4 and 8) | 2.0 | 135 | 170 | 205 | ns |
| | | 4.5 | 27 | 34 | 41 | |
| | | 6.0 | 23 | 29 | 35 | |
| t _{TLH} , t _{THL} | Maximum Output Transition Time, Q _A -Q _H (Figures 3 and 7) | 2.0 | 60 | 75 | 90 | ns |
| | | 4.5 | 12 | 15 | 18 | |
| | | 6.0 | 10 | 13 | 15 | |
| t _{TLH} , t _{THL} | Maximum Output Transition Time, SQ _H (Figures 1 and 7) | 2.0 | 75 | 95 | 110 | ns |
| | | 4.5 | 15 | 19 | 22 | |
| | | 6.0 | 13 | 16 | 19 | |
| C _{IN} | Maximum Input Capacitance | - | 10 | 10 | 10 | pF |
| C _{OUT} | Maximum Three-State Output Capacitance (Output in High-Impedance State), Q _A -Q _H | - | 15 | 15 | 15 | pF |
| C _{PD} | Power Dissipation Capacitance (Per Package) | Typical @25°C, V _{CC} =5.0 V | | | | pF |
| | Used to determine the no-load dynamic power consumption: P _D =C _{PD} V _{CC} ² f+I _{CC} V _{CC} | 300 | | | | |

TIMING REQUIREMENTS ($C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|---------------------------------|---|----------------------|-------------------|-------|--------|------|
| | | | 25 °C to -55°C | ≤85°C | ≤125°C | |
| t _{su} | Minimum Setup Time, Serial Data Input A to Shift Clock (Figure 5) | 2.0 | 50 | 65 | 75 | ns |
| | | 4.5 | 10 | 13 | 15 | |
| | | 6.0 | 9 | 11 | 13 | |
| t _{su} | Minimum Setup Time, Shift Clock to Latch Clock (Figure 6) | 2.0 | 75 | 95 | 110 | ns |
| | | 4.5 | 15 | 19 | 22 | |
| | | 6.0 | 13 | 16 | 19 | |
| t _h | Minimum Hold Time, Shift Clock to Serial Data Input A (Figure 5) | 2.0 | 5 | 5 | 5 | ns |
| | | 4.5 | 5 | 5 | 5 | |
| | | 6.0 | 5 | 5 | 5 | |
| t _{rec} | Minimum Recovery Time, Reset Inactive to Shift Clock (Figure 2) | 2.0 | 50 | 65 | 75 | ns |
| | | 4.5 | 10 | 13 | 15 | |
| | | 6.0 | 9 | 11 | 13 | |
| t _w | Minimum Pulse Width, Reset (Figure 2) | 2.0 | 60 | 75 | 90 | ns |
| | | 4.5 | 12 | 15 | 18 | |
| | | 6.0 | 10 | 13 | 15 | |
| t _w | Minimum Pulse Width, Shift Clock (Figure 1) | 2.0 | 50 | 65 | 75 | ns |
| | | 4.5 | 10 | 13 | 15 | |
| | | 6.0 | 9 | 11 | 13 | |
| t _w | Minimum Pulse Width, Latch Clock (Figure 6) | 2.0 | 50 | 65 | 75 | ns |
| | | 4.5 | 10 | 13 | 15 | |
| | | 6.0 | 9 | 11 | 13 | |
| t _r , t _f | Maximum Input Rise and Fall Times (Figure 1) | 2.0 | 1000 | 1000 | 1000 | ns |
| | | 4.5 | 500 | 500 | 500 | |
| | | 6.0 | 400 | 400 | 400 | |

FUNCTION TABLE

| Operation | Inputs | | | | | Resulting Function | | | |
|--|--------|----------------|-------------|-------------|---------------|--|-----------------------------------|-----------------------------------|---|
| | Reset | Serial Input A | Shift Clock | Latch Clock | Output Enable | Shift Register Contents | Latch Register Contents | Serial Output SQ _H | Parallel Outputs Q _A -Q _H |
| Reset shift register | L | X | X | L,H, | L | L | U | L | U |
| Shift data into shift register | H | D | | L,H, | L | D → SR _A SR _N → SR _{N+1} | U | SR _G → SR _H | U |
| Shift register remains unchanged | H | X | L,H, | L,H, | L | U | U | U | U |
| Transfer shift register contents to latch register | H | X | L,H, | | L | U | SR _N → LR _N | U | SR _N |
| Latch register remains unchanged | X | X | X | L,H, | L | * | U | * | U |
| Enable parallel outputs | X | X | X | X | L | * | ** | * | Enabled |
| Force outputs into high-impedance state | X | X | X | X | H | * | ** | * | Z |

SR = shift register contents
 LR = latch register contents
 D = data (L,H) logic level
 U = remains unchanged

X = don't care
 Z = high impedance
 * = depends on Reset and Shift Clock inputs
 ** = depends on Latch Clock input

PIN DESCRIPTIONS

INPUTS:

A - Serial Data Input. The data on this pin is shifted into the 8-bit serial shift register.

CONTROL INPUTS:

Shift Clock - Shift Register Clock Input. A low-to-high transition on this input causes the data at the Serial Input pin to be shifted into the 8-bit shift register.

Reset - Active-low, Asynchronous, Shift Register Reset Input. A low on this pin resets the shift register portion of this device only. The 8-bit latch is not affected.

Latch Clock - Storage Latch Clock Input. A low-to-high transition on this input latches the shift register data.

Output Enable - Active-Low Output Enable. A low on this input allows the data from the latches to be presented at the outputs. A high on this input forces the outputs (Q_A-Q_H) into the high-impedance state. The serial output is not affected by this control unit.

OUTPUTS:

Q_A-Q_H - Noninverted, 3-state, latch outputs.

SQ_H - Noninverted, Serial Data Output. This is the output of the eighth stage of the 8-bit shift register. This output does not have three-state capability.

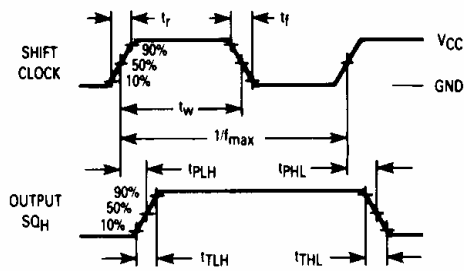


Figure 1. Switching Waveforms

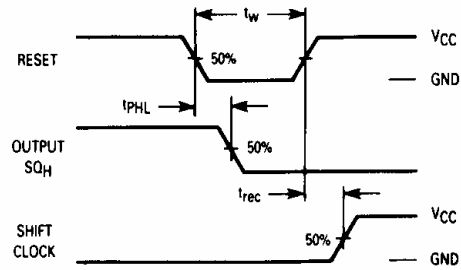


Figure 2. Switching Waveforms

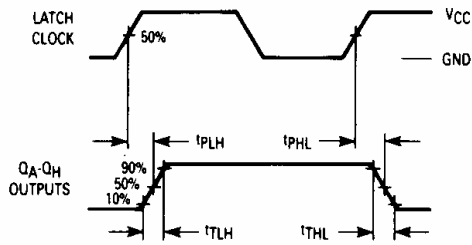


Figure 3. Switching Waveforms

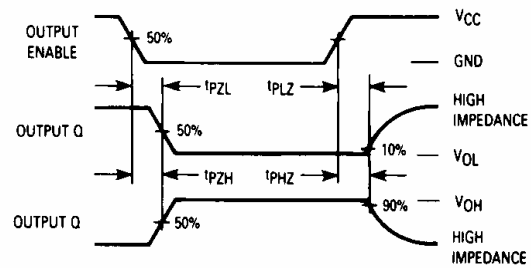


Figure 4. Switching Waveforms

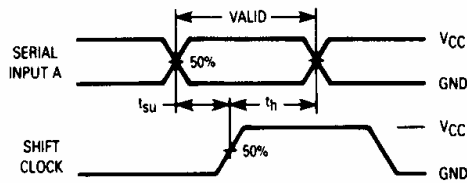


Figure 5. Switching Waveforms

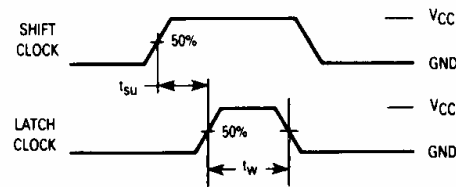
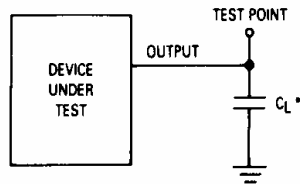
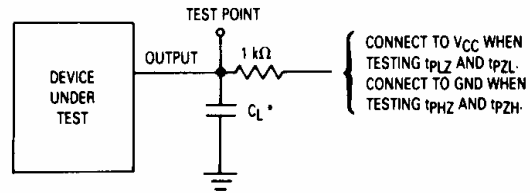


Figure 6. Switching Waveforms



*Includes all probe and jig capacitance.

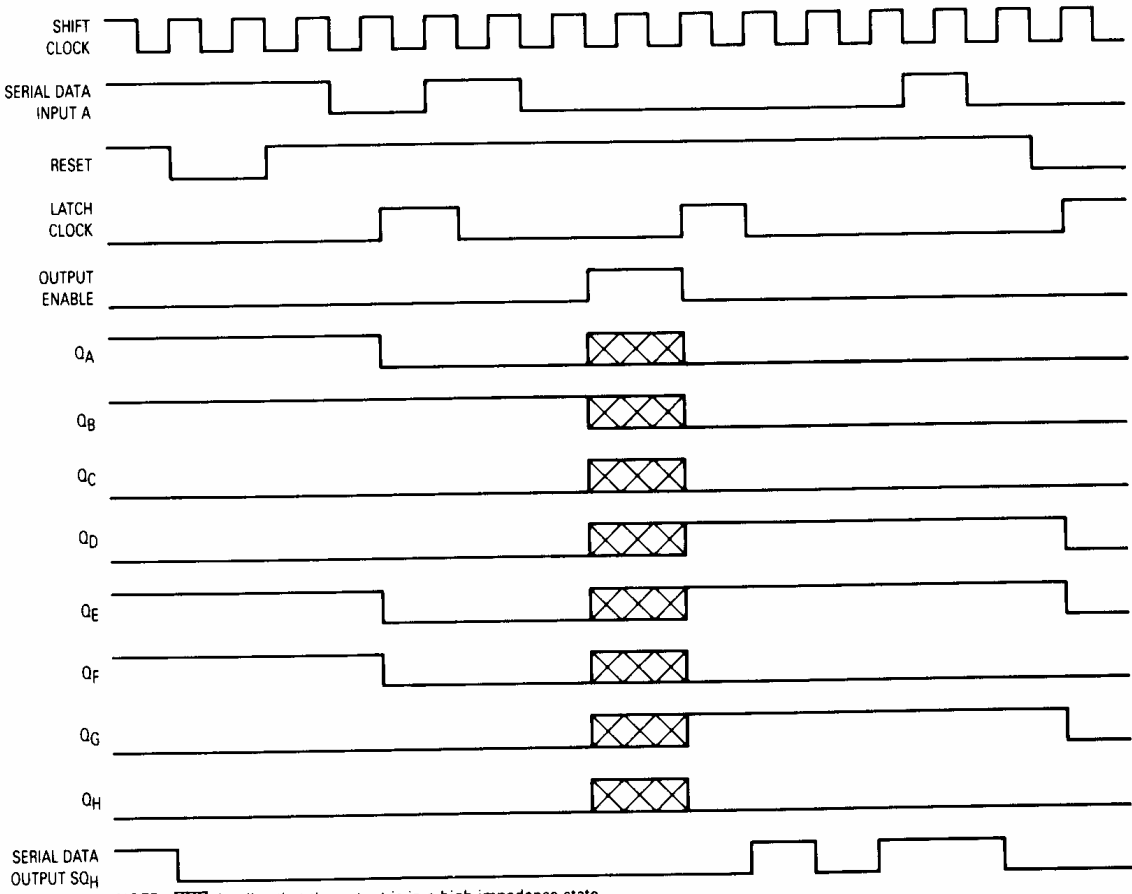
Figure 7. Test Circuit



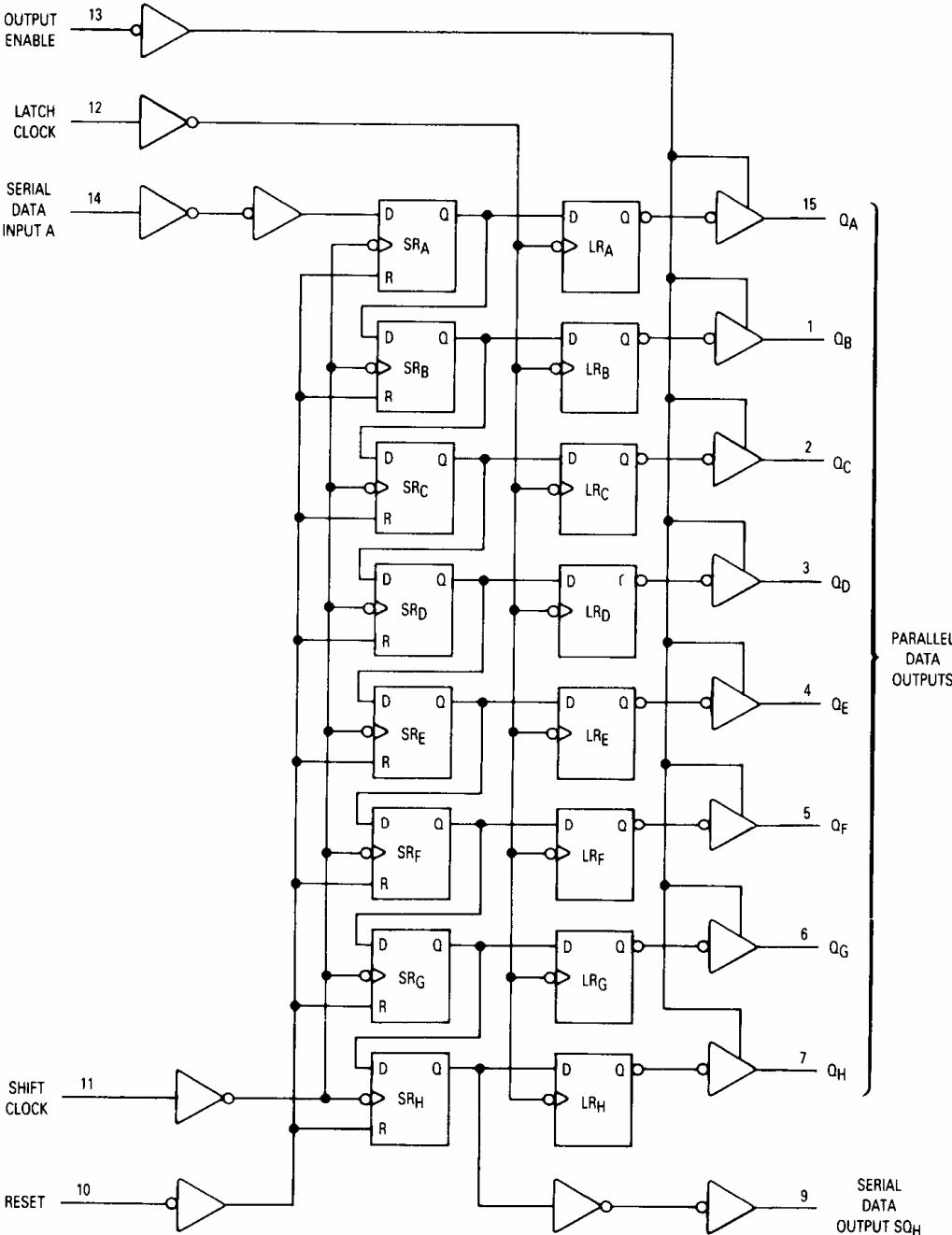
*Includes all probe and jig capacitance.

Figure 8. Test Circuit

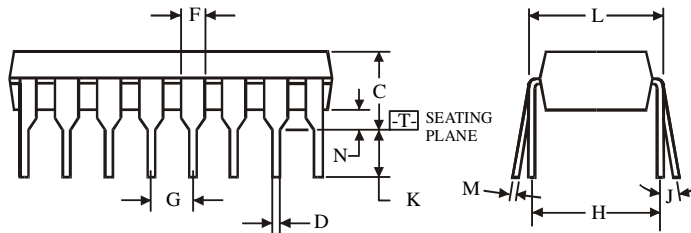
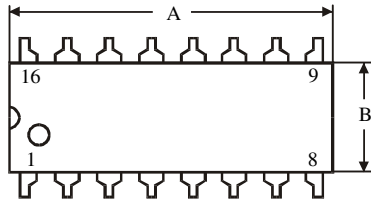
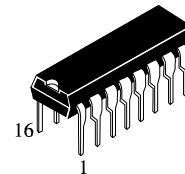
TIMING DIAGRAM



EXPANDED LOGIC DIAGRAM



N SUFFIX PLASTIC DIP
(MS - 001BB)



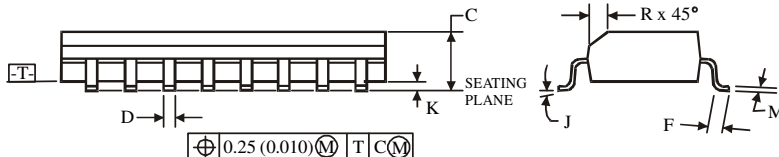
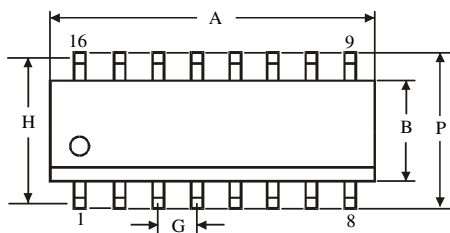
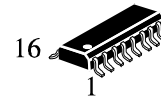
$\oplus 0.25 (0.010) \text{ (M) T}$

NOTES:

- Dimensions "A", "B" do not include mold flash or protrusions.
Maximum mold flash or protrusions 0.25 mm (0.010) per side.

| Symbol | Dimension, mm | |
|--------|---------------|-------|
| | MIN | MAX |
| A | 18.67 | 19.69 |
| B | 6.1 | 7.11 |
| C | | 5.33 |
| D | 0.36 | 0.56 |
| F | 1.14 | 1.78 |
| G | 2.54 | |
| H | 7.62 | |
| J | 0° | 10° |
| K | 2.92 | 3.81 |
| L | 7.62 | 8.26 |
| M | 0.2 | 0.36 |
| N | 0.38 | |

D SUFFIX SOIC
(MS - 012AC)



$\oplus 0.25 (0.010) \text{ (M) T C (M)}$

NOTES:

- Dimensions A and B do not include mold flash or protrusion.
- Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B - 0.25 mm (0.010) per side.

| Symbol | Dimension, mm | |
|--------|---------------|------|
| | MIN | MAX |
| A | 9.8 | 10 |
| B | 3.8 | 4 |
| C | 1.35 | 1.75 |
| D | 0.33 | 0.51 |
| F | 0.4 | 1.27 |
| G | 1.27 | |
| H | 5.72 | |
| J | 0° | 8° |
| K | 0.1 | 0.25 |
| M | 0.19 | 0.25 |
| P | 5.8 | 6.2 |
| R | 0.25 | 0.5 |