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CY7C343B

64-Macrocell MAX® EPLD

Features

- **64 MAX macrocells in 4 LABs**
- **8 dedicated inputs, 24 bidirectional I/O pins**
- **Programmable interconnect array**
- **Advanced 0.65-micron CMOS technology to increase performance**
- **Available in 44-pin HLCC, PLCC**
- **Lowest power MAX device**

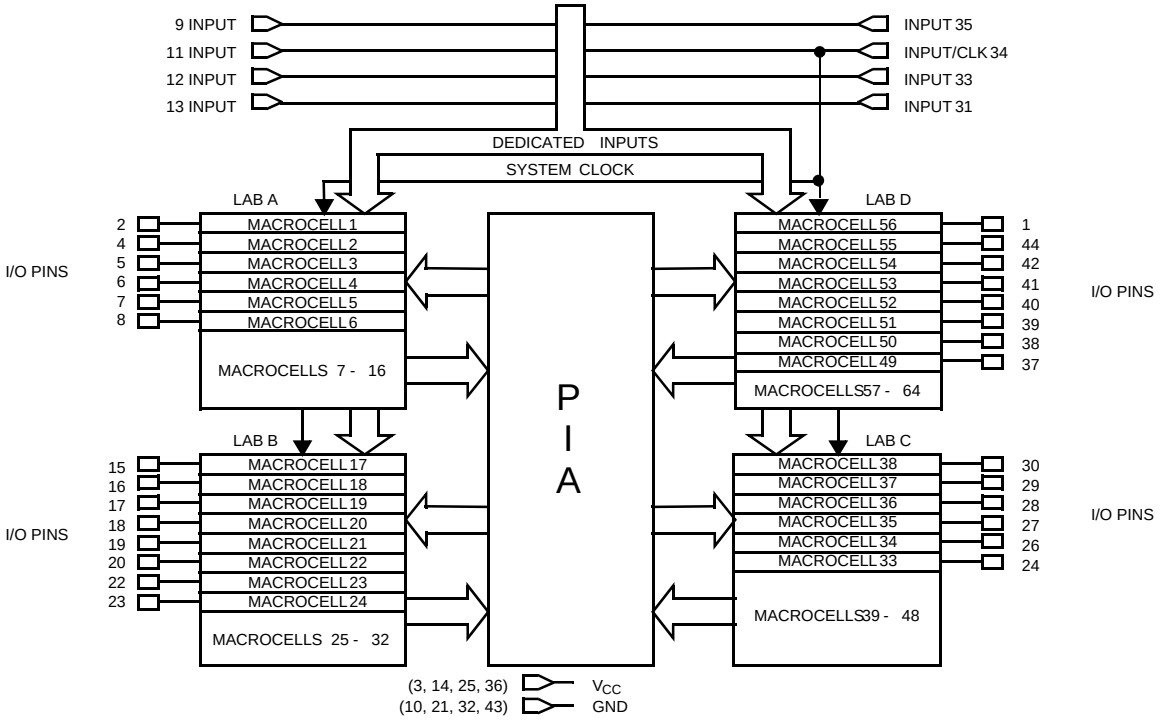
Functional Description

The CY7C343B is a high-performance, high-density erasable programmable logic device, available in 44-pin PLCC and HLCC packages.

The CY7C343B contains 64 highly flexible macrocells and 128 expander product terms. These resources are divided into four Logic Array Blocks (LABs) connected through the Programmable Inter-connect Array (PIA). There are 8 input pins, one that doubles as a clock pin when needed. The CY7C343B also has 28 I/O pins, each connected to a macrocell (6 for LABs A and C, and 8 for LABs B and D). The remaining 36 macrocells are used for embedded logic.

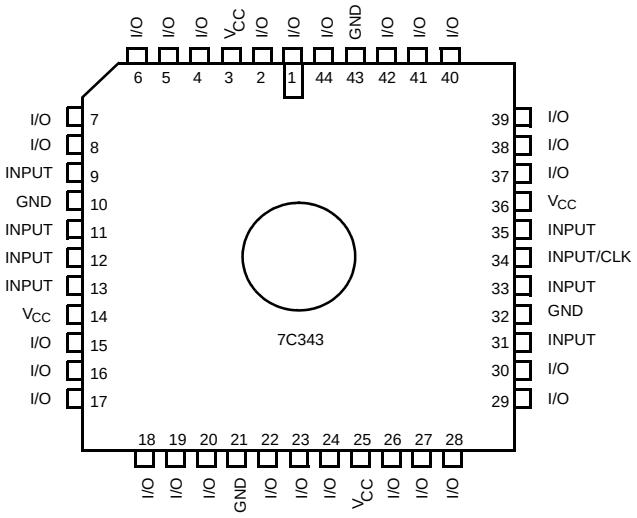
The CY7C343B is excellent for a wide range of both synchronous and asynchronous applications.

Logic Block Diagram



Pin Configuration

HLCC, PLCC
Top View



Selection Guide

	7C343B-25	7C343B-30	7C343B-35
Maximum Access Time (ns)	25	30	35

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +135°C

Ambient Temperature with Power Applied.....–65°C to +135°C

Maximum Junction Temperature (Under Bias).....150°C

Supply Voltage to Ground Potential[1].....–2.0V to +7.0V

DC Output Current, per Pin[1].....–25 mA to +25 mA

DC Input Voltage[1].....–2.0V to +7.0V

Operating Range[2]

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ±5%
Industrial	–40°C to +85°C	5V ±10%
Military	–55°C to +125°C (Case)	5V ±10%

Note:
1. Minimum DC input is –0.3V. During transactions, the inputs may undershoot to –2.0V or overshoot to 7.0V for input currents less then 100 mA and periods shorter than 20 ns.
2. The Voltage on any input or I/O pin cannot exceed the power pin during power-up.

Electrical Characteristics Over the Operating Range

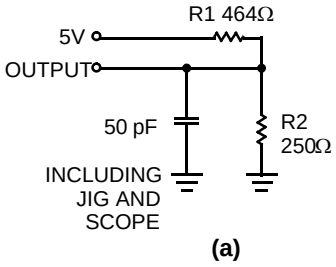
Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage	Maximum V_{CC} rise time is 10 ms	4.75(4.5)	5.25(5.5)	V
V_{OH}	Output HIGH Voltage	I_{OH} = –4.0 mA DC[3]	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA DC[3]		0.45	V
V_{IH}	Input HIGH Level		2.0	V_{CC}+0.3	V
V_{IL}	Input LOW Level		–0.3	0.8	V
I_{IX}	Input Current	V_I = V_{CC} or ground	–10	+10	µA
I_{OZ}	Output Leakage Current	V_O = V_{CC} or ground	–40	+40	µA
t_R	Recommended Input Rise Time			100	ns
t_F	Recommended Input Fall Time			100	ns

Capacitance

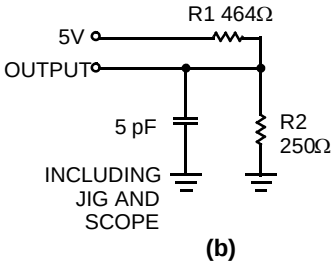
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V, f = 1.0 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, f = 1.0 MHz	20	pF

Note:
3. The I_{OH} parameter refers to high-level TTL output current; the I_{OL} parameter refers to low-level TTL output current.

AC Test Loads and Waveforms



(a)



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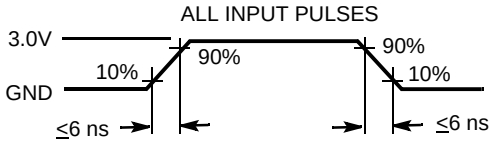
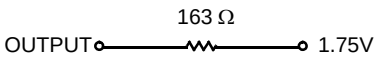


Equivalent to: THÉVENIN EQUIVALENT (commercial/military)



Programmable Interconnect Array

The Programmable Interconnect Array (PIA) solves interconnect limitations by routing only the signals needed by each logic array block. The inputs to the PIA are the outputs of every macrocell within the device and the I/O pin feedback of every pin on the device.

Unlike masked or programmable gate arrays, which induce variable delay dependent on routing, the PIA has a fixed delay. This eliminates undesired skews among logic signals, which may cause glitches in internal or external logic. The fixed delay, regardless of programmable interconnect array configuration, simplifies design by ensuring that internal signal skews or races are avoided. The result is simpler design implementation, often in a single pass, without the multiple internal logic placement and routing iterations required for a programmable gate array to achieve design timing objectives.

Design Recommendations

Operation of the devices described herein with conditions above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect device reliability. The CY7C343B contains circuitry to protect device pins from high static voltages or electric fields; however, normal precautions should be taken to avoid applying any voltage higher than maximum rated voltages.

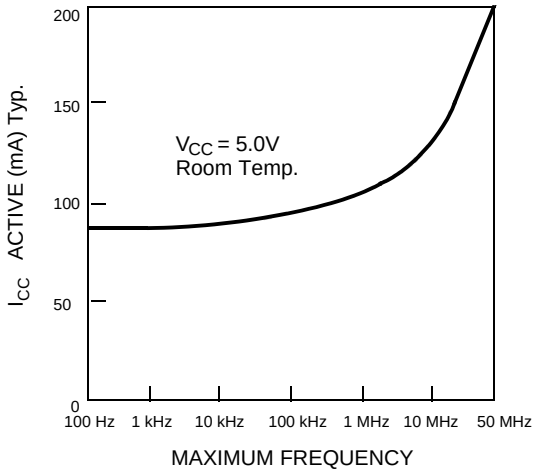
For proper operation, input and output pins must be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic level (either V_{CC} or GND). Each set of V_{CC} and GND pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2 µF must be connected between V_{CC} and GND. For the most effective decoupling, each V_{CC} pin should be separately decoupled to GND, directly at the device. Decoupling capacitors should have good frequency response, such as monolithic ceramic types.

Timing Considerations

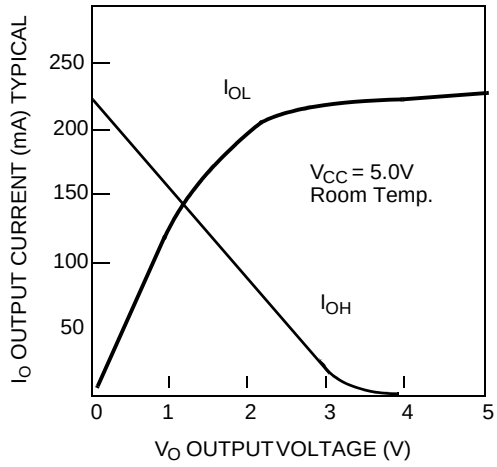
Unless otherwise stated, propagation delays do not include expanders. When using expanders, add the maximum expander delay t_{EXP} to the overall delay. Similarly, there is an additional t_{PIA} delay for an input from an I/O pin when compared to a signal from a straight input pin.

When calculating synchronous frequencies, use t_{S1} if all inputs are on the input pins. When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{S1}. Determine which of $1/(t_{WH} + t_{WL})$, $1/t_{CO1}$, or $1/(t_{EXP} + t_{S1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the synchronous configuration.

Typical I_{CC} vs. f_{MAX}



Output Drive Current



When calculating external asynchronous frequencies, use t_{AS1} if all inputs are on dedicated input pins.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{AS1}. Determine which of $1/(t_{AWH} + t_{AWL})$, $1/t_{ACO1}$, or $1/(t_{EXP} + t_{AS1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the asynchronous configuration.

The parameter t_{OH} indicates the system compatibility of this device when driving other synchronous logic with positive input hold times, which is controlled by the same synchronous clock. If t_{OH} is greater than the minimum required input hold time of the subsequent synchronous logic, then the devices are guaranteed to function properly with a common synchronous clock under worst-case environmental and supply voltage conditions.

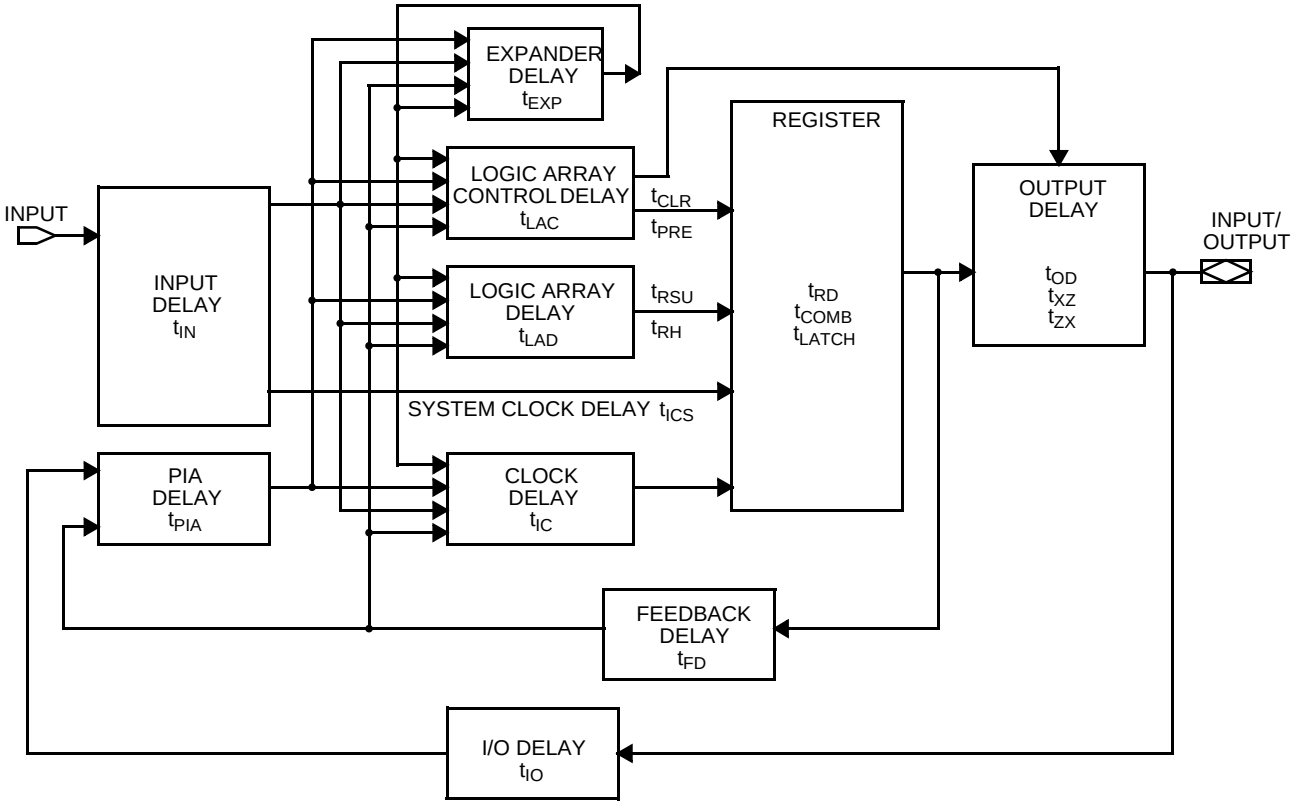


Figure 1. CY7C343B Internal Timing Model

External Synchronous Switching Characteristics Over Operating Range

Parameter	Description		7C343B-25		7C343B-30		7C343B-35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[4]	Com'l/Ind		25		30		35	ns
t_{PD2}	I/O Input to Combinatorial Output Delay[4]	Com'l/Ind		40		45		55	ns
t_{SU}	Global clock setup time	Com'l/ Ind	15		20		25		ns
t_{CO1}	Synchronous Clock Input to Output Delay[3]	Com'l/Ind		14		16		20	ns
t_{H}	Input Hold Time from Synchronous Clock Input	Com'l/Ind	0		0		0		ns
t_{WH}	Synchronous Clock Input HIGH Time	Com'l/Ind	8		10		12.5		ns
t_{WL}	Synchronous Clock Input LOW Time	Com'l/Ind	8		10		12.5		ns
f_{MAX}	Maximum Register Toggle Frequency[5]	Com'l/Ind	62.5		50		40		MHz
t_{CNT}	Minimum Global Clock Period	Com'l/Ind		20		25		30	ns
t_{ODH}	Output Data Hold Time After Clock	Com'l/Ind	2		2		2		ns
f_{CNT}	Maximum Internal Global Clock Frequency[6]	Com'l/Ind	50		40		33.3		MHz

Notes:
4. C1 = 35 pF.
5. The f_{MAX} values represent the highest frequency for pipeline data.
6. This parameter is measured with a 16-bit counter programmed into each LAB.

External Asynchronous Switching Characteristics Over Operating Range

Parameter	Description		7C343B-25		7C343B-30		7C343B-35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACO1}	Asynchronous Clock Input to Output Delay[4]	Com'l/Ind		25		30		35	ns
t_{AS1}	Dedicated Input or Feedback Set-Up Time to Asynchronous Clock Input	Com'l/Ind	5		6		8		ns
t_{AH}	Input Hold Time from Asynchronous Clock Input	Com'l/Ind	6		8		10		ns
t_{AWH}	Asynchronous Clock Input HIGH Time[7]	Com'l/Ind	11		14		16		ns
t_{AWL}	Asynchronous Clock Input LOW Time[7]	Com'l/Ind	9		11		14		ns
t_{ACNT}	Minimum Internal Array Clock Frequency	Com'l/Ind		20		25		30	ns
f_{ACNT}	Maximum Internal Array Clock Frequency[6]	Com'l/Ind	50		40		33.3		MHz

Internal Switching Characteristics Over Operating Range

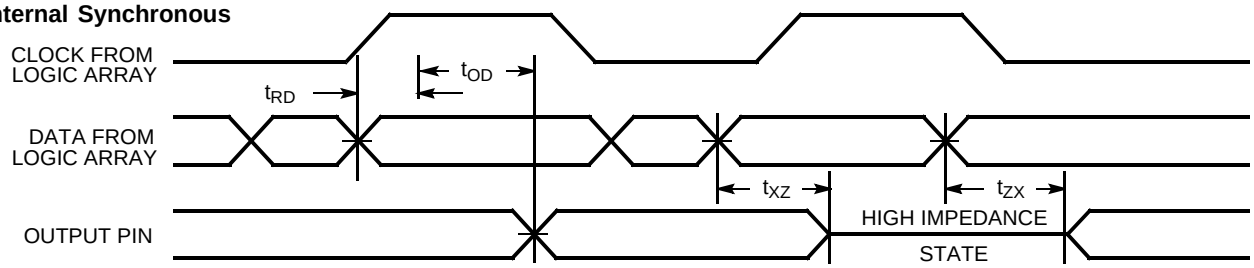
Parameter	Description		7C343B-25		7C343B-30		7C343B-35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay	Com'l/Ind		5		7		11	ns
t_{IO}	I/O Input Pad and Buffer Delay	Com'l/Ind		6		6		11	ns
t_{EXP}	Expander Array Delay	Com'l/Ind		12		14		20	ns
t_{LAD}	Logic Array Data Delay	Com'l/Ind		12		14		14	ns
t_{LAC}	Logic Array Control Delay	Com'l/Ind		10		12		13	ns
t_{OD}	Output Buffer and Pad Delay[4]	Com'l/Ind		5		5		6	ns
t_{ZX}	Output Buffer Enable Delay[4]	Com'l/Ind		10		11		13	ns
t_{XZ}	Output Buffer Disable Delay[8]	Com'l/Ind		10		11		13	ns
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	Com'l/Ind	6		8		12		ns
t_{RH}	Register Hold Time Relative to Clock Signal at Register	Com'l/Ind	4		6		8		ns
t_{LATCH}	Flow-Through Latch Delay	Com'l/Ind		3		4		4	ns
t_{RD}	Register Delay	Com'l/Ind		1		2		2	ns
t_{COMB}	Transparent Mode Delay	Com'l/Ind		3		4		4	ns
t_{IC}	Asynchronous Clock Logic Delay	Com'l/Ind		14		16		18	ns
t_{ICS}	Synchronous Clock Delay	Com'l/Ind		3		2		1	ns
t_{FD}	Feedback Delay	Com'l/Ind		1		1		2	ns
t_{PRE}	Asynchronous Register Preset Time	Com'l/Ind		5		6		7	ns
t_{CLR}	Asynchronous Register Clear Time	Com'l/Ind		5		6		7	ns
t_{PIA}	Programmable Interconnect Array Delay Time	Com'l/Ind		14		16		20	ns

Notes:

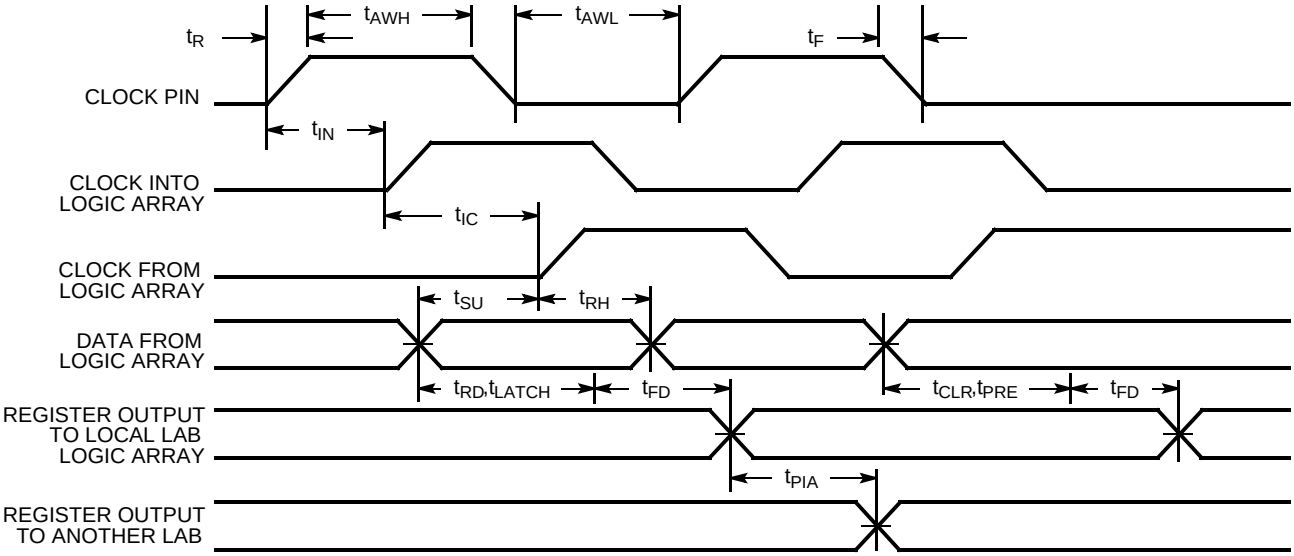
7. This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameter must be swapped.
8. C1 = 5 pF.

Switching Waveforms

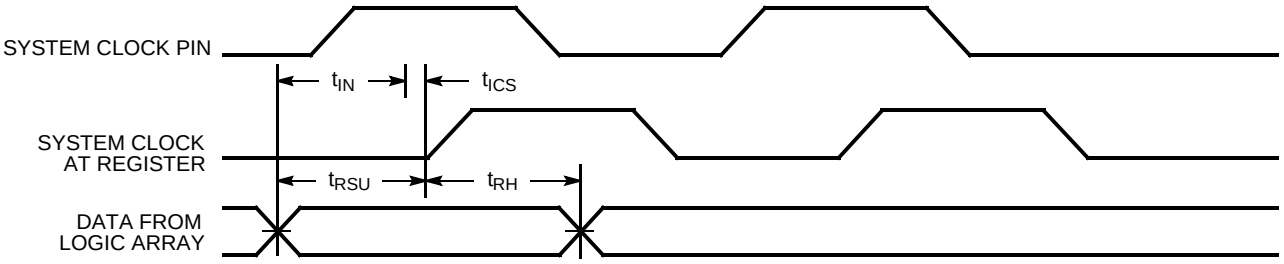
Internal Synchronous



Internal Asynchronous

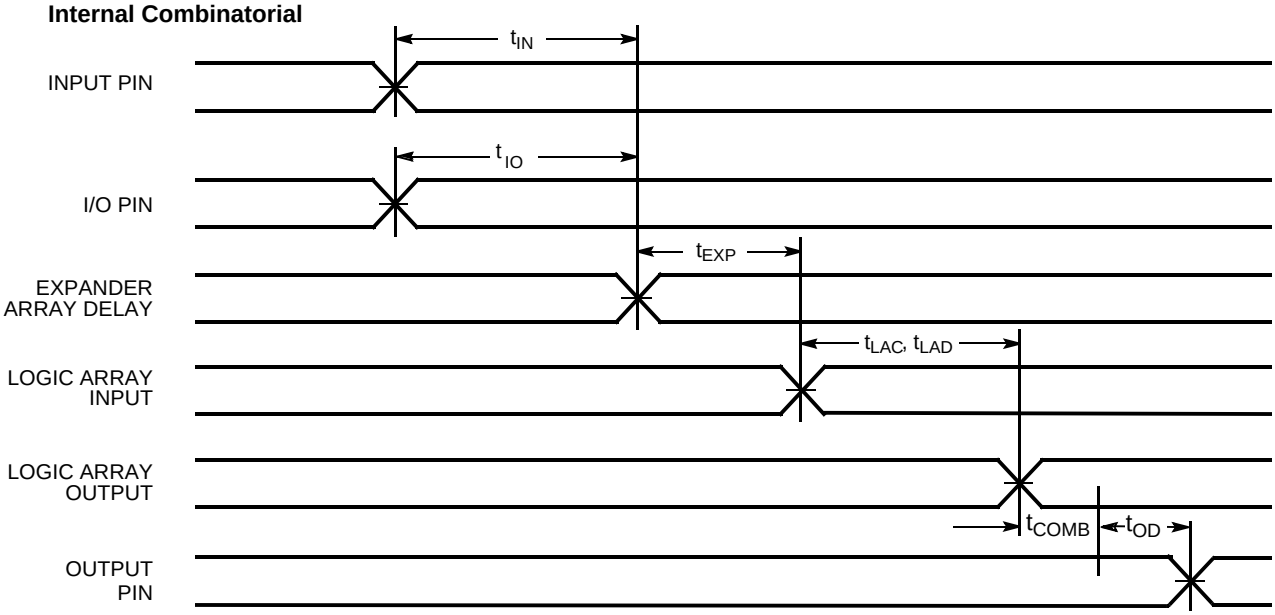


Internal Synchronous

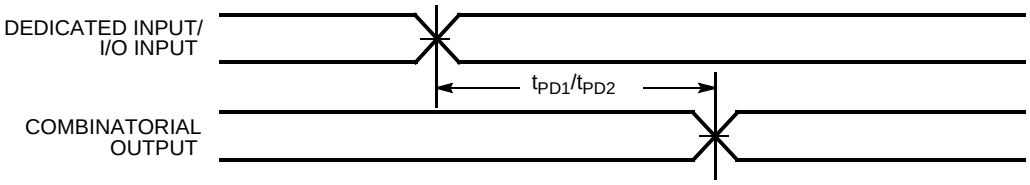


Switching Waveforms (continued)

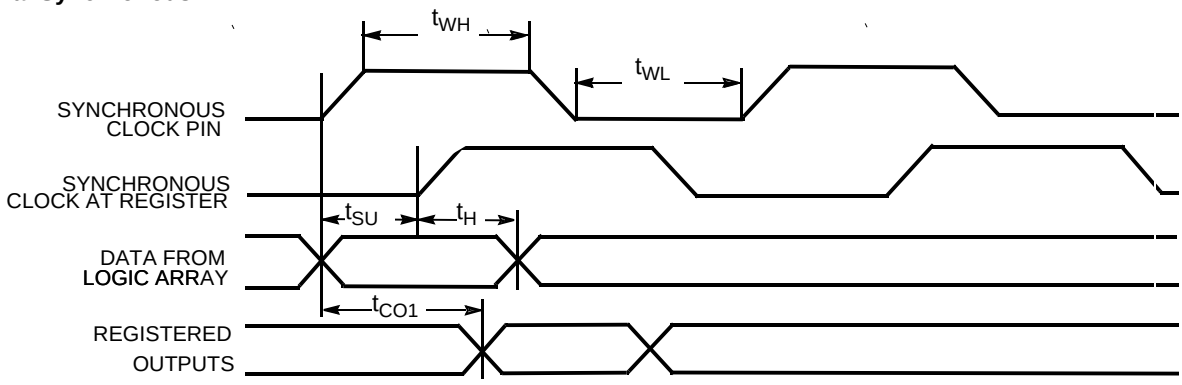
Internal Combinatorial



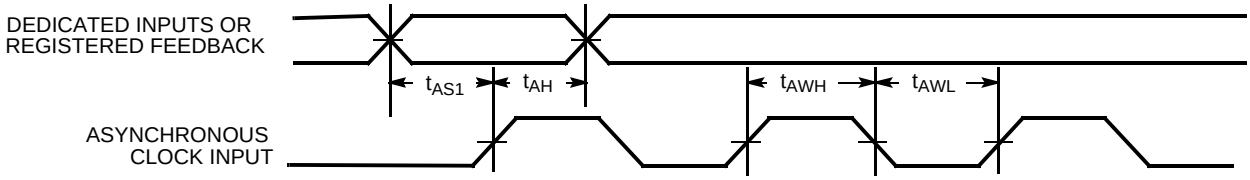
External Combinatorial



External Synchronous



External Asynchronous

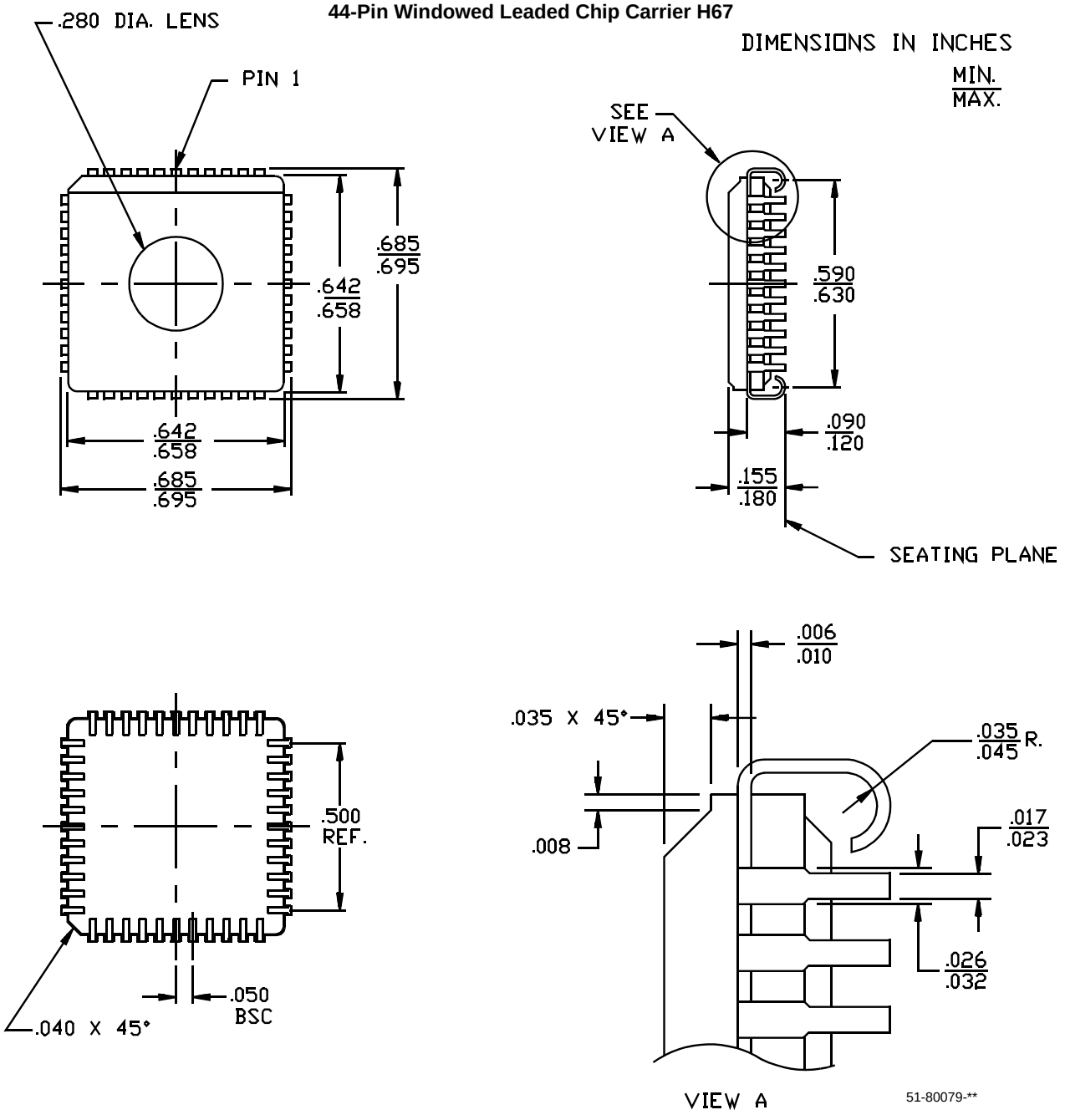


Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C343B-25HC/HI	H67	44-Pin Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C343B-25JC/JI	J67	44-Lead Plastic Leaded Chip Carrier	
30	CY7C343B-30JC/JI	J67	44-Lead Plastic Leaded Chip Carrier	Commercial/Industrial
35	CY7C343B-35HC/HI	H67	44-Pin Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C343B-35JC/JI	J67	44-Lead Plastic Leaded Chip Carrier	

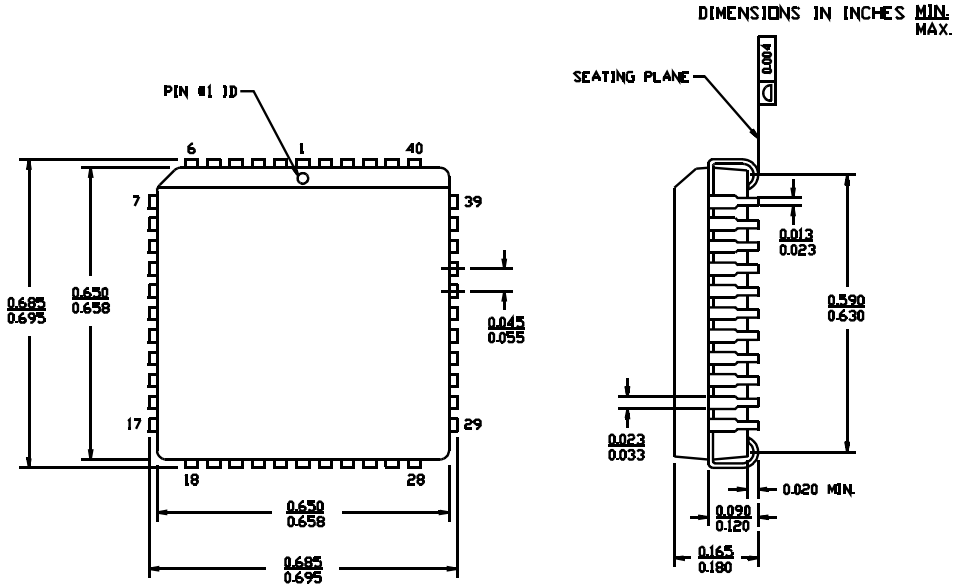
Package Diagrams

44-Pin Windowed Leaded Chip Carrier H67



Package Diagrams (continued)

44-Lead Plastic Leaded Chip Carrier J67



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Document History Page

Document Title: CY7C343B 64-Macrocell Max ® EPLD Document Number: 38-03038				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106461	07/11/01	SZV	Change from Spec Number: 38-00862 to 38-03038
*A	122237	12/28/02	RBI	Power up requirements added to Operating Range Information
*B	213375	See ECN	FSG	Added note to title page: “Use Ultra37000 For All New Designs”