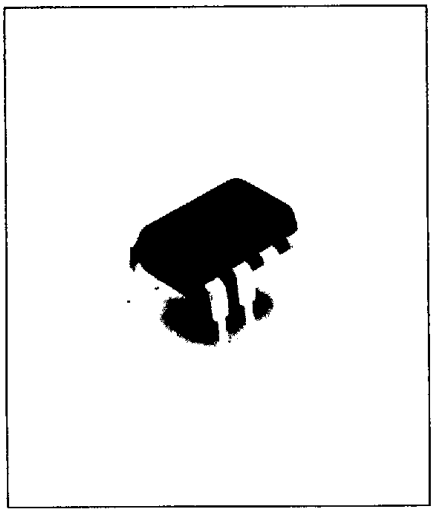
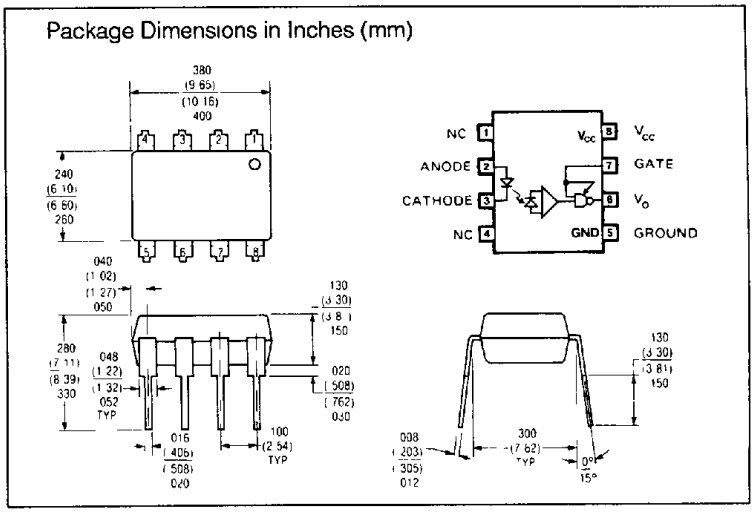
SIEMENS

IL101B

HIGH SPEED THREE STATE OPTOCOUPLER





FEATURES

- **High Speed**
- **Faraday Shielded Photodetector Improves Common Mode Rejection**
- **DTL/TTL Compatible, 5 V Supply**
- **Three State Output Logic for Multiplexing**
- **Built-In Schmitt Trigger Avoids Oscillation**
- **UL Approval #E52744**

DESCRIPTION

IL101B is an optically coupled pair with a Gallium Arsenide Phosphide LED and a silicon monolithic integrated circuit including a photodetector. High speed digital information can be transmitted while maintaining a high degree of electrical isolation between input and output. The IL101B can be used to replace pulse transformers in many digital interface applications. A built-in Schmitt Trigger provides hysteresis reducing oscillation possibility.

Maximum Ratings

Input Diode

Forward DC Current	25 mA
Reverse Voltage	5 V

Output IC

Supply Voltage (V_{CC})	7 V
Enable Input Voltage (V_E) (not to exceed V_{CC} by more than 500 mV)	5.5 V
Output Collector Current (I_C)	100 mA
Output Collector Power Dissipation	100 mW
Output Collector Voltage (V_{OUT})	7 V
Isolation Voltage (Input-Output), DC	6000 V

Package

Storage Temperature	-55°C to +125°C
Operating Temperature	0°C to +70°C
Lead Solder Temperature	260°C for 10 sec

Electrical Characteristics (T_{amb}=0°C to 70°C)

Parameter	Min.	Typ.	Max.	Unit	Test Condition
I_{in} (1) – Logic (1) Input Current for Logic (0) Output (Figure 1)	12			mA	
I_{in} (0) – Logic (0) Input Current for Logic (1) Output (Figure 1)			250	mA	
V_G (1) – Logic (1) Gate Voltage	2.0			V	
V_G (0) – Logic (0) Gate Voltage			8	V	
V_{OUT} (0) – Logic (0) Output Voltage		35	6	V	V_{CC}=5.5 V, V_G=2.4 V, I_{in}=12 mA, I_{out} (sinking) =16 mA
I_{CC}		18	22	mA	V_{CC}= 5.5 V, V_G=0.5 V, I_{in}=0.10 mA

Switching Characteristics (T_{amb}=25°C, V_{CC}=5 V)

Parameter	Min.	Typ.	Max.	Unit	Test Condition
t_{pd} (1) – Propagation Delay Time to Logic Level (1) (Fig 1, Note 1)		175	300	ns	R_L=350 Ω, C_L=15 pF, I_{in}=12 mA
t_{pd} (0) – Propagation Delay Time to Logic Level (0) (Fig. 1, Note 2)		70	300	ns	R_L = 350 Ω, C_L=15 pF, I_{in}=12 mA
t_R - t_F(0) – Output Rise-Fall Time (10-90%)		15		ns	R_L=350 Ω, C_L=15 pF, I_{in}=12 mA

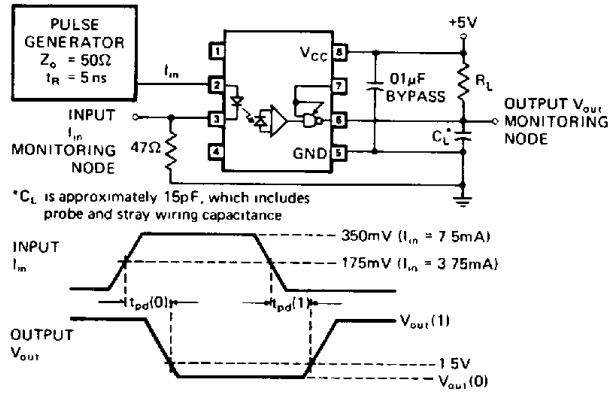
Electrical Characteristics (T_{amb}=25°C) – Input to Output

Parameter	Min.	Typ.	Max.	Unit	Test Condition
Insulation Voltage Input-Output (BV_{10}) (Note 3)	6000	7500		VDC	t = 1 sec.
Resistance, Input-Output (R_{1-0}) (Note 3)	10^{12}			Ω	V_{1-0}= 500 V
Capacitance Input-Output (C_{1-0}) (Note 3)	0.5	0.8		pF	f = 1 MHz

Electrical Characteristics (T_{amb}=25°C) – Input Diode

Parameter	Min.	Typ.	Max.	Unit	Test Condition
Forward Voltage (V_F)		1 5	1 75	V	I_{in}=10 mA
Reverse Breakdown Voltage (V_{BR})	5			V	I_R=10 mA
Capacitance (I_{in})		10		pF	V = 0, f = 1MHz

FIGURE 1. TEST CIRCUIT FOR t_{pd} (0) AND t_{pd} (1)



Notes:
1. The t_{pd}(1) propagation delay is measured from the 3 75 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse
2. The t_{pd}(0) propagation delay is measured from the 3 75 mA point on the input pulse to the 1.5 V point on the leading edge of the output pulse
3. Pins 2 and 3 are shorted together, and pins 5, 6, 7, and 8 shorted together.
4. At 10 mA V_F decreases with increasing temperature at the rate of 1.6 mV/°C.

OPERATING PROCEDURES AND DEFINITIONS

Logic Convention: The IL101B is defined in terms of positive logic.

Bypassing: A ceramic capacitor (.01mF min.) should be connected from pin 8 to pin 5 to stabilize the switching amplifier operation. Switching properties may be impaired by not providing for bypassing.

Polarities: All voltages are referenced to network ground (pin 5). Current flowing toward a terminal is considered positive.

Gate input: No external pull-up required for a logic (1).

TRUTH TABLE (Positive Logic)

Input*	Enable	Output
1	1	0
0	1	1
1	0	off
0	0	off

*See definition of terms for logic state.