PRELIMINARY

CY7B9514V

3.3V Quad SONET Transceiver

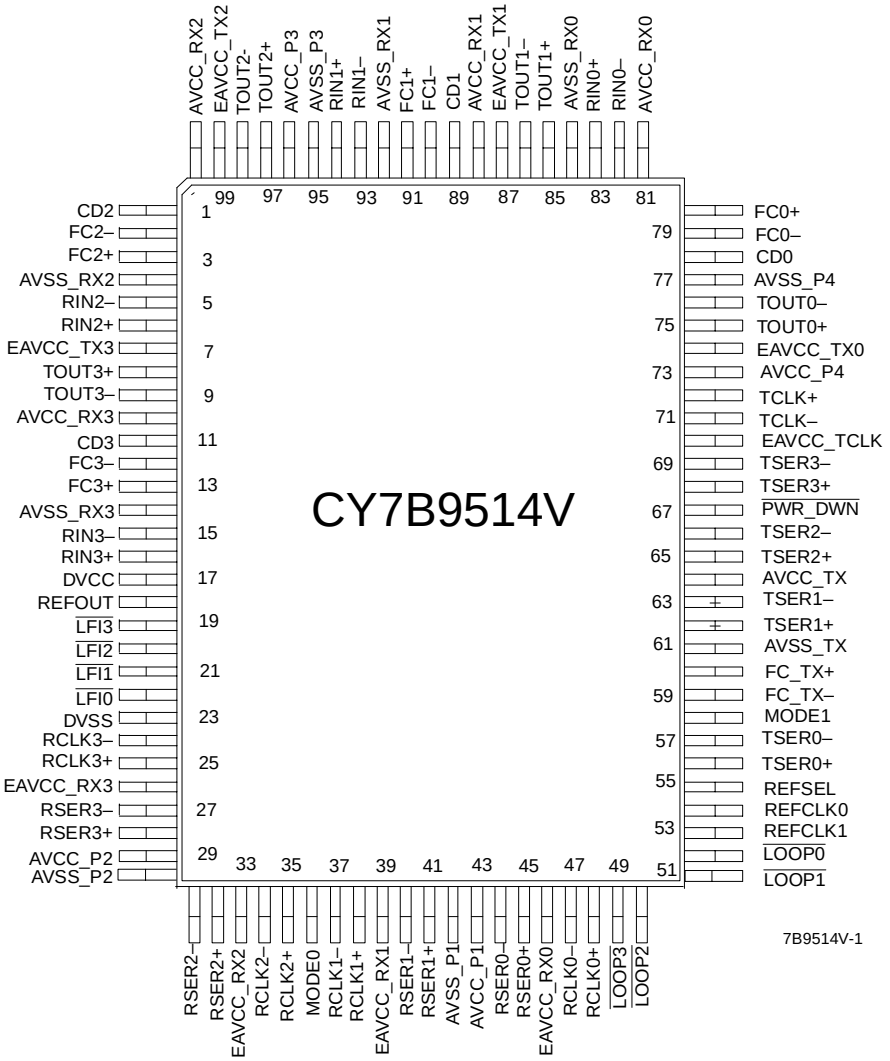
Features

- SONET/SDH and ATM Compatible
- Clock and data recovery from 51.84- or 155.52-MHz datastream
- 155.52-MHz clock multiplication from 19.44-MHz source
- 51.84-MHz clock multiplication from 6.48-MHz source
- ±1% frequency agility
- Line Receiver Inputs: No external buffering required
- Differential output buffering
- 100K PECL compatible I/O
- No output clock “drift” without data transitions
- Link Status Indication
- Loop-back testing
- Dual reference clock inputs and reference clock output
- Transition between REFCLKs is slowed to prevent data recovery errors
- Single +3.3V ±10% supply
- 100-pin TQFP
- Compatible with fiber-optic modules, coaxial cable, and twisted pair media
- Power-down options to minimize power or crosstalk
- Low operating current: <400 mA
- 0.8µ BiCMOS

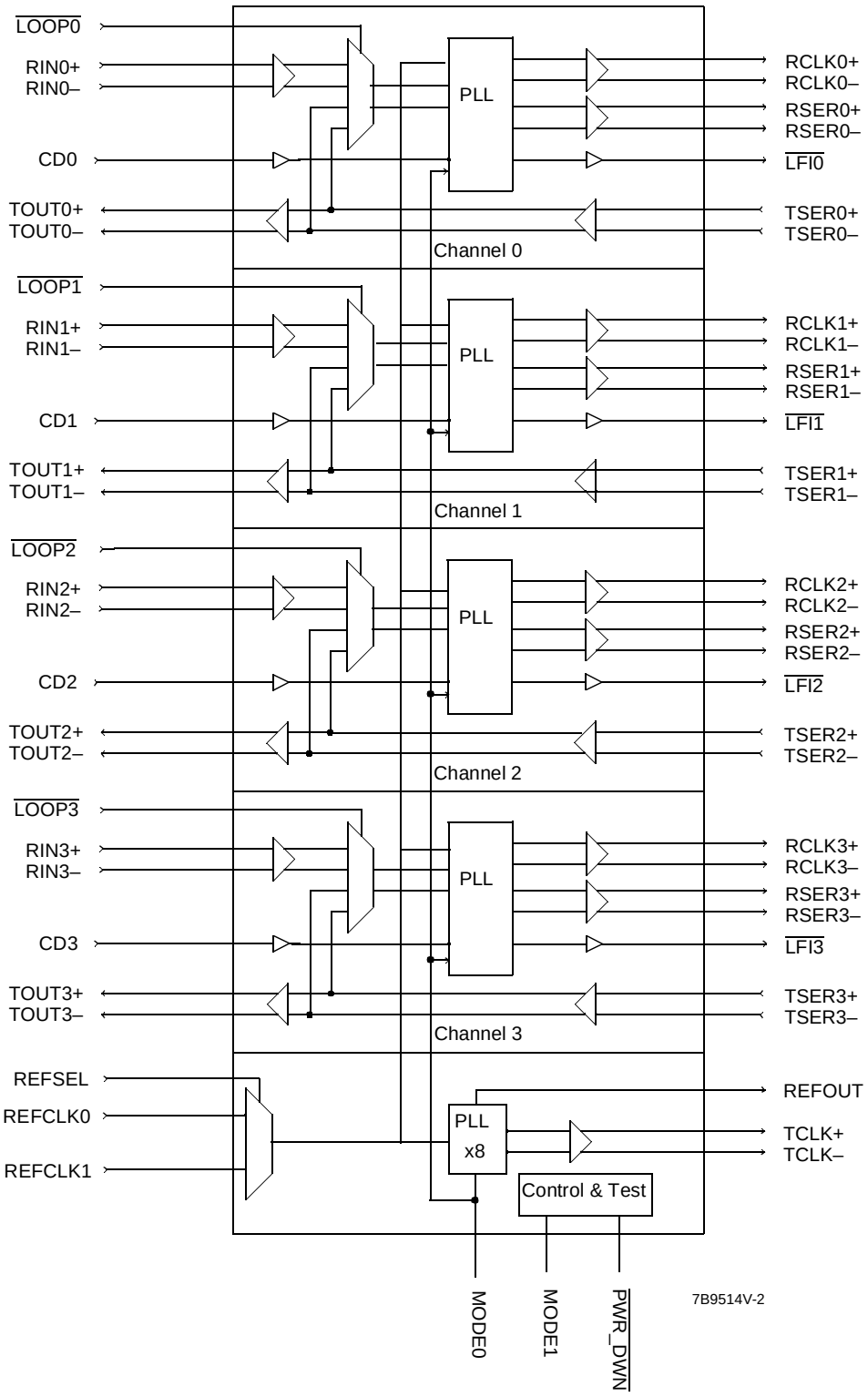
Functional Description

The Quad PMD ATM Transceiver is used in SONET/SDH and ATM applications to recover clock and data information from a 155.52-MHz or 51.84-MHz NRZ or NRZI serial data stream and to provide differential data buffering for the Transmit side of the system.

Pin Configuration



Logic Block Diagram



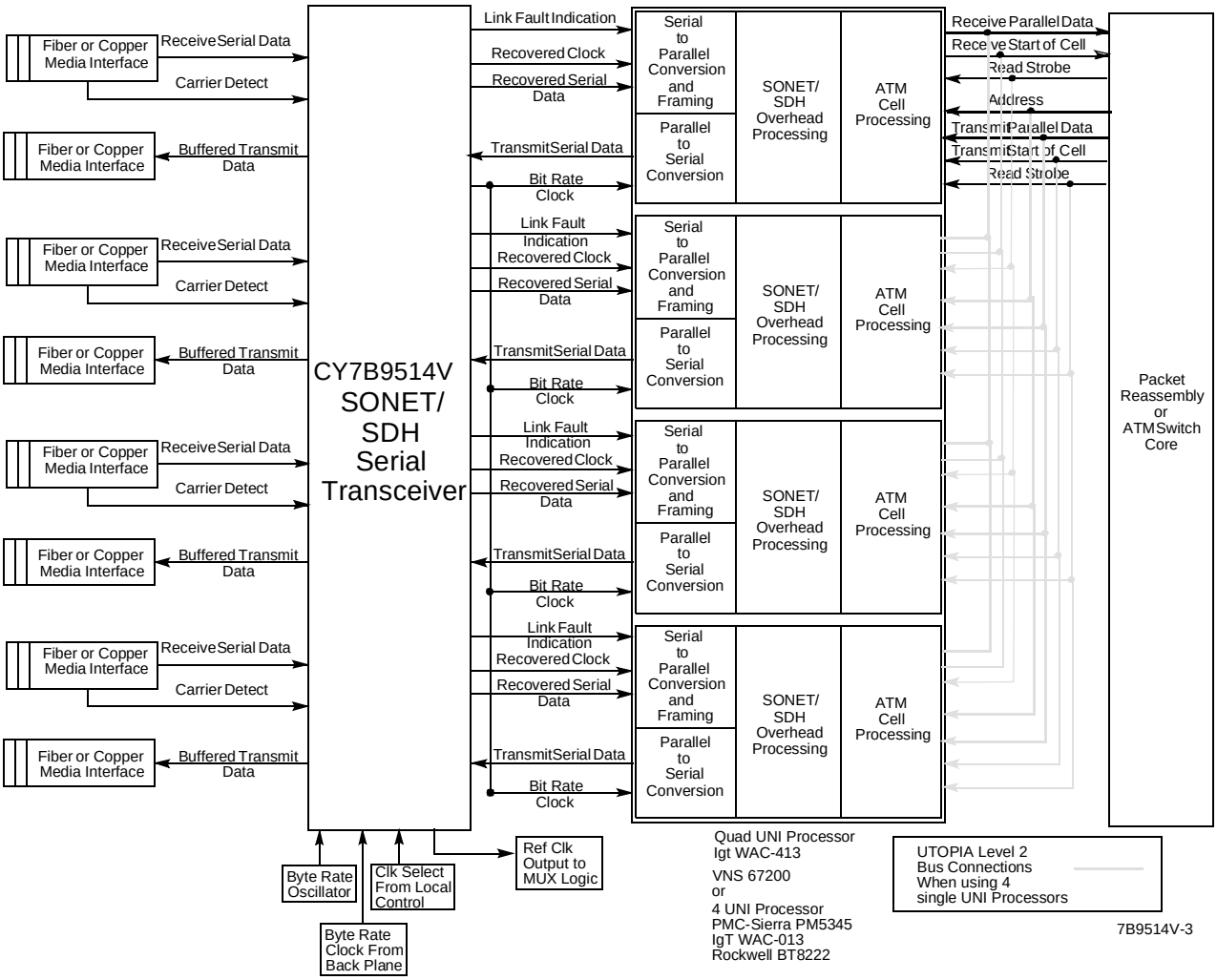


Figure 1. SONET/SDH and ATM Interface

Pin Descriptions

Name	I/O	Description
RIN0± RIN1± RIN2± RIN3±	Differential In	Receive Input. This line receiver port connects the receive differential serial input data stream to the internal Receive PLL. This PLL will recover the embedded clock (RCLK±) and data (RSER±) information for one of two data rates depending on the state of the MODE pin. These inputs can receive very low amplitude signals and are compatible with all PECL signaling levels. If the RIN± inputs are not being used, connect RIN+ to V_{CC} and RIN– to V_{SS}.
RSER0± RSER1± RSER2± RSER3±	PECL Out Differential	Recovered Serial Data. These PECL 100K outputs (+3.3V referenced) are the recovered data from the input data stream (RIN±). This recovered data is aligned with the recovered clock (RCLK±) with a set-up and hold window compatible with most data processing devices. All PECL outputs can be powered down by connecting both outputs to V_{CC} or by leaving them both unconnected.
RCLK0± RCLK1± RCLK2± RCLK3±	PECL Out Differential	Recovered Clock. These PECL 100K outputs (+3.3V referenced) are the recovered clock from the input data stream (RIN±). This recovered clock is used to sample the recovered data (RSER±) and is timing compatible with most data processing devices. If both the RSER± and the RCLK± are tied to V_{CC} or left unconnected, the entire Receive PLL will be powered down.
CD0 CD1 CD2 CD3	PECL In Single Ended	Carrier Detect. These inputs control the recovery function of the Receive PLLs and can be driven by the carrier detect outputs from optical modules or from external transition detection circuitry. When this input is at a PECL HIGH, the input data stream (RIN±) is recovered normally by the Receive PLL. When this input is at a PECL LOW, the Receive PLL no longer aligns to RIN±, but instead aligns with the REFCLK×8 frequency. Also, the Link Fault Indicator ($\overline{LFI}$) will transition LOW, and the recovered data outputs (RSER) will remain LOW regardless of the signal level on the Receive data-stream inputs (RIN). Each CD input has an internal pull-down resistor.
$\overline{LFI0}$ $\overline{LFI1}$ $\overline{LFI2}$ $\overline{LFI3}$	LVTTL Out	Link Fault Indicator. These outputs indicate the status of the input data stream (RIN±). It is controlled by three functions; the Carrier Detect (CD) input, the internal Transition Detector, and the Out of Lock (OOL) detector. The Transition Detector determines if RIN± contains enough transitions to be accurately recovered by the Receive PLL. The Out-of-Lock detector determines if RIN± is within the frequency range of the Receive PLL. When CD is HIGH and RIN± has sufficient transitions and is within the frequency range of the Receive PLL, the $\overline{LFI}$ output will be HIGH. If CD is at a PECL LOW or RIN± does not contain sufficient transitions or RIN± is outside the frequency range of the Receive PLL then the $\overline{LFI}$ output will be LOW (see MODE1).
TSER0± TSER1± TSER2± TSER3±	Differential In	Transmit Serial Data. This line receiver port connects the transmit differential serial input data stream to the TOUT transmit buffers. Depending on the state of the $\overline{LOOP}$ pin, this input port can also be set up to supply the serial input data stream to the Receive PLL. These inputs can receive very low amplitude signals and are compatible with all PECL signaling levels. If the TSER± inputs are not being used, connect TSER+ to V_{CC} and TSER– to V_{SS}.
TOUT0± TOUT1± TOUT2± TOUT3±	PECL Out Differential	Transmit Output. These PECL 100K outputs (+3.3V referenced) are the buffered version of the Transmit data stream (TSER±). This Transmit path is used to take weak input signals and rebuffer them to drive low-impedance copper media or fiber-optic modules. All PECL outputs can be powered down by connecting both outputs to V_{CC} or by leaving them both unconnected.
REFCLK0 REFCLK1	LVTTL In	Reference Clocks. One of these inputs is selected by the REFSEL pin as the clock frequency reference for the clock and data recovery Receive PLL. REFCLK is multiplied internally by eight and sets the approximate center frequency for the internal Receive PLL to track the incoming bit stream. This input is also multiplied by eight by the frequency multiplier Transmit PLL to produce the bit rate Transmit Clock (TCLK±). REFCLK can be connected to a TTL frequency source.
TCLK±	PECL Out Differential	Transmit Clock. These PECL 100K outputs (+3.3V referenced) provide the bit rate frequency source for external Transmit data processing devices. This output is synthesized by the Transmit PLL and is derived by multiplying the REFCLK frequency by eight. When this output is turned off, the entire Transmit PLL is powered down. All PECL outputs can be powered down by connecting both outputs to V_{CC} or by leaving them both unconnected.
$\overline{LOOP0}$ $\overline{LOOP1}$ $\overline{LOOP2}$ $\overline{LOOP3}$	LVTTL In	Loop Back Select. This input is used to select the input data stream source that the Receive PLL uses for clock and data recovery. When the $\overline{LOOP}$ input is HIGH, the Receive input data stream (RIN±) is used for clock and data recovery. When LOOP is LOW, the Transmit input data stream (TSER±) is used by the Receive PLL for clock and data recovery.

Pin Descriptions (continued)

Name	I/O	Description
MODE0	3-Level In	Frequency Mode Select. This three-level input selects the frequency range for the clock and data recovery Receive PLL and the frequency multiplier Transmit PLL. When this input is held HIGH (V_{CC}) the PLLs operate at the SONET (SDH) STS-3 (STM-1) line rate of 155.52 MHz. When this input is held LOW (V_{SS}) the PLLs operate at the SONET STS-1 line rate of 51.84 MHz. The REFCLK frequency in both operating modes is 1/8 the PLL operating frequency. When the MODE0 input is left floating or held at $V_{CC}/2$, the TSER± inputs substitute for the internal PLL VCO for use in factory testing.
MODE1	3-Level In	MODE1 enables the transition detector when it is held HIGH (V_{CC}). The transition detector is disabled when MODE1 is held LOW (V_{SS}). When the MODE1 input is left floating or held at $V_{CC}/2$, the factory test mode is enabled.
FC0± FC1± FC2± FC3±	External 1-µF caps	These external capacitors are used only to reduce the PLL bandwidth and peaking, when desired. The PLL lock time will also be increased.
FC_TXP FC_TXN	External 1-µF caps	These external capacitors are used only when the slew rate between the two REFCLKs needs to be reduced.
REFOUT	LVTTL Out	Reference Output. This output is a buffered version of the selected reference clock. Depending on the state of the REFSEL pin this output can be a buffered version of REFCLK1 and REFCLK2. When there is a change of state at the REFSEL, this output will change over from one reference clock to another reference clock smoothly without glitch, except if TCLK outputs are held HIGH or left floating.
REFSEL	LVTTL In	Reference Select. This pin selects one of the external reference clock (REFCLK 0/1) to be used as the internal reference clock for the Transmit and Receive PLLs. When this input is at a TTL HIGH, REFCLK1 is selected. When this input is at a TTL LOW, REFCLK0 is selected.
$\overline{\text{PWR\_DWN}}$	LVTTL In	Power Down. This pin will power down all the PLLs and logic components of the device. When this pin is held LOW, the Transmit PLL, transition detection logic, and Receive PLLs will power down. When this pin is held HIGH, the Transmit PLL, transition detection logic, and Receive PLLs will resume normal operation.
EAVCC_TX0 EAVCC_TX1 EAVCC_TX2 EAVCC_TX3	Power	Analog Power. Power pins for the PECL drivers for the TOUT± outputs. These pins must be connected to a well decoupled 3.3V DC supply.
AVCC_P1 AVCC_P2 AVCC_P3 AVCC_P4 AVCC_RX0 AVCC_RX1 AVCC_RX2 AVCC_RX3 AVCC_TX	Power	Analog Power. Power pins for the analog portion of the Receive and Transmit PLLs.
AVSS_P1 AVSS_P2 AVSS_P3 AVSS_P4 AVSS_RX0 AVSS_RX1 AVSS_RX2 AVSS_RX3 AVSS_TX	Gnd	Analog Ground. Ground pins for the analog portion of the Receive and Transmit PLLs.
EAVCC_RX0 EAVCC_RX1 EAVCC_RX2 EAVCC_RX3	Power	Analog Power. Power for the PECL RSER and RCLK outputs.These pins must be connected to a well decoupled +3.3V DC supply.

Pin Descriptions (continued)

Name	I/O	Description
EAVCC_TCLK	Power	Analog Power. Power pin for the TCLK PECL drivers. This pin must be connected to a well decoupled +3.3V DC supply.
DVCC	Power	Digital Power. Power pin for the digital logic of the device. This pin must be connected to a well decoupled 3.3V DC supply.
DVSS	Gnd	Digital Ground. Ground pin for the digital logic of the device.

Description

The CY7B9514V Quad Local Area Network ATM Transceiver can be used in both SONET/SDH and ATM applications to recover clock and data information from four 155.52-MHz or 51.84-MHz NRZ (Non Return to Zero) or NRZI (Non Return to Zero Invert on ones) serial data streams. A byte-rate reference clock is provided by buffering one of the two reference clock sources.This device also provides a bit-rate Transmit clock, by multiplying the buffered byte-rate reference clock through the use of a frequency multiplier PLL and four channels of differential data buffering for the Transmit side of the system (see *Figure 1*).

Operating Frequency

The CY7B9514V operates at either of two frequency ranges. The MODE0 input selects which of the two frequency ranges the Transmit frequency multiplier PLL and the Receive clock and data recovery PLLs in all four channels will operate at. The MODE0 input has three different functional selections. When MODE0 is connected to V_{CC}, the highest operating range of the device is selected. The device has two reference clock inputs, REFCLK0 and REFCLK1. REFSEL is used to select which clock input is used to serve as a reference source for the Transmit frequency multiplier PLL and the Receive clock and data recovery PLLs. A 19.44-MHz ±1% source must drive the selected REFCLK input and the five PLLs will multiply this rate by 8 to provide output clocks that operate at 155.52 MHz ±1%. When the MODE0 input is connected to ground (GND), the lowest operating range of the device is selected. A 6.48-MHz ±1% source must drive the selected REFCLK input and the five PLLs will multiply this rate by 8 to provide output clocks that operate at 51.84 MHz ±1%. When the MODE0 input is left unconnected or forced to approximately $V_{CC}/2$, the device enters a factory test mode.

Transmit Functions

The transmit section of the CY7B9514V contains a PLL that takes the selected REFCLK input and multiplies it by 8 (REFCLK×8) to produce a PECL (Pseudo ECL) differential output clock (TCLK±). The transmitter has two operating ranges that are selectable with the three-level MODE0 pin as explained above. The CY7B9514V Transmit frequency multiplier PLL allows low-cost byte rate clock sources to be used to time the upstream serial data transmitter as shown in *Figure 1*.

Both of the REFCLK inputs are LVTTL-level inputs, allowing them to be driven by low-cost TTL crystal oscillators, or any TTL-level clock source.

The four Transmit PECL differential input pairs (TSER±) are buffered by the CY7B9514V yielding the differential data outputs (TOUT±). These outputs can be used to directly drive transmission media such as Printed Circuit Board (PCB) traces, optical drivers, twisted pair, or coaxial cable.

Receive Functions

The CY7B9514V has four receiver channels. The primary function of the receivers is to recover clock (RCLK±) and data (RSER±) from the four different incoming differential PECL data streams (RIN±) without the need for external buffering. These built-in line receiver inputs, as well as the TSER± inputs mentioned above, have a wide common-mode range (1.25V) and the ability to receive signals with as little as 50 mV differential voltage. They are compatible with all PECL signals and any copper media.

The clock recovery function is performed using embedded PLLs. The recovered clock is not only passed to the RCLK± outputs, but also used internally to sample the input serial data stream in order to recover the data pattern. The Receive PLL uses the selected REFCLK input as a byte-rate reference. This input is multiplied by 8 (REFCLK×8) and is used to improve PLL lock time and to provide a center frequency for operation in the absence of input data stream transitions. The receiver can recover clock and data in two different frequency ranges depending on the state of the three-level MODE0 pin as explained earlier. To insure accurate data and clock recovery, REFCLK×8 must be within 250 ppm of the transmit bit rate. The standards, however, specify that the REFCLK×8 frequency accuracy be within 20–100 ppm.

Carrier Detect (CD) and Link Fault Indicator ($\overline{\text{LFI}}$) Functions

The Link Fault Indicator ($\overline{\text{LFI}}$) outputs are LVTTL-level outputs that indicate the status of each of the four receivers. These outputs can be used by an external controller for Loss of Signal (LOS), Loss of Frame (LOF), or Out of Frame (OOF) indications. Each $\overline{\text{LFI}}$ output is controlled by the respective Carrier Detect (CD) input, the internal Transitions Detector, and the PLL Out of Lock (OOL) circuitry.

Each CD input may be driven by external circuitry that is monitoring the respective incoming data stream. Optical modules have CD outputs that indicate the presence of light on the optical fiber and some copper based systems use external threshold detection circuitry to monitor the incoming data stream. The CD input is a 100K PECL compatible signal that should be held HIGH when the incoming data stream is valid. When CD is pulled to a 3.3V PECL LOW ($\leq$1.475V Max.), the $\overline{\text{LFI}}$ output will transition LOW and the Receiver PLL will align itself with the REFCLK×8 frequency and the recovered data outputs (RSER) will remain LOW regardless of the signal level on the Receive data-stream inputs (RIN).

In addition, the CY7B9514V has four built-in transition detectors for each channel that also check the quality of the incoming data stream. The absence of data transitions can be caused by a broken transmission media, a broken transmitter, or a problem with the transmit or receive media coupling. The CY7B9514V will detect a quiet link by counting the number of

bit times that have passed without a data transition. A bit time is defined as the period of RCLK±. When 512 bit times have passed without a data transition on RIN±, LFI will transition LOW. The receiver will assume that the serial data stream is invalid, and, instead of allowing the RCLK± frequency to wander in the absence of data, the PLL will lock to the REFCLK*8 frequency. This will insure that RCLK± is as close to the correct link operating frequency as the REFCLK accuracy. LFI will be driven HIGH, and the receiver will recover clock and data from the incoming data stream when the transition detection circuitry determines that at least 64 transitions have been detected within 256 bit-times. The transition detector is disabled when MODE1 is held LOW (V_{SS}).

Loop Back Testing

The LVTTL level LOOP pins are used to perform loop-back testing. When LOOP is asserted (held LOW) the Transmit serial input (TSER±) is used by the respective Receiver PLL for clock and data recovery. This allows in-system testing to be performed on each clock and data recovery PLL and transition detection logic. When a channel is in loop-back mode the state of the CD pin is ignored. For example, an ATM controller can present ATM cells to the input of the ATM cell processor and check to see that these same cells are received from each of the four channels. When the LOOP input is deasserted (held HIGH) the Receive PLL is once again connected to the Receiver serial inputs (RIN±).

The LOOP feature can also be used in applications where clock and data recovery are to be performed from either of two data streams from each channel. In these systems the LOOP pin is used to select whether the TSER± or the RIN± inputs are used by the Receive PLL for clock and data recovery.

Power-Down Modes

There are several power-down features on the CY7B9514V. Any of the differential output drivers can be powered down by either tying both outputs to V_{CC} or by simply leaving them unconnected where internal pull-up resistors will force these outputs to V_{CC}. This will save approximately 4 mA per output pair in addition to the associated output load current. If the TOUT± outputs are tied to V_{CC} or left unconnected, the Transmit buffer path will be turned off. If the TCLK± outputs are tied to V_{CC} or left unconnected, the entire Transmit PLL will be powered down.

For each receive channel, by leaving both the RCLK± and RSER± outputs unconnected or tied to V_{CC}, the corresponding Receive PLL is turned off.

Besides the option of turning off drivers and PLLs selectively, the PWR_DWN pin can also be used to power down the entire device. When PWR_DWN pin is at TTL LOW, the Transmit PLL, transition detection logic and all four Receive PLLs will be powered down (see application section concerning PECL output loading when PWR_DWN is asserted). When the PWR_DWN pin is at TTL HIGH, the Transmit PLL, transition detection logic, and all four Receive PLLs will be enabled.

Applications

The CY7B9514V can be used in Local Area Network ATM applications. The operating frequency of the CY7B9514V is centered around the SONET/SDH STS-1 rate of 51.84 MHz and the SONET/SDH STS-3/STM-1 rate of 155.52 MHz. This device can also be used in data mover and Local Area Network (LAN) applications that operate at these frequencies.

The CY7B9514V can provide clock and data recovery as well as output buffering for physical layer protocol engines such as the SONET/SDH and ATM processing application shown in *Figure 1.*

Figure 1 shows the CY7B9514V in an ATM system that uses the IgT WAC-413 device. The CY7B9514V will recover clock and data from the input serial data streams and pass them to the WAC-413. The WAC-413 device will perform serial to parallel conversion on each channel, SONET/SDH overhead processing, and ATM cell processing and then pass ATM cells to an ATM packet reassembly engine. On the Transmit side, a segmentation engine will divide long packets of data such as Ethernet packets into 53 byte cells and pass them to each of the channels of the WAC-413. The WAC-413 device will then perform ATM cell processing, such as header generation, SONET/SDH overhead processing, and parallel to serial conversion on each channel. These serial data streams will then be passed to the CY7B9514V, which will buffer these data streams and pass them along to the transmission media.

The CY7B9514V provides the necessary clock and data recovery function to the WAC-413. These differential PECL clock and data signals interface directly with the RS_SER_DATA± and RS_SER_CLK± inputs of the WAC-413 device as shown in *Figure 1*. In addition, the CY7B9514V provides transmit data output buffering for direct drive of cable transmission media. The CY7B9514V has two local reference clock inputs. An internal mux controls which input clock is used as the reference. Changing from one input to the other will happen smoothly without glitch on REFOUT. Therefore, a low-cost crystal oscillator can drive one input, and a clock from another external clock source, e.g., a distributed clock from a central clock board, can drive the other clock input. Another application of the two clock inputs is feeding a 19.44-MHz clock to one input and a 6.48-MHz to the other clock input, so now the CY7B9514V can operate at both STS-1/OC-1 rate as well as STS-3/OC-3/STM-1 rate by configuring the MODE0 pin and REFSEL pin to the appropriate state. Lastly, the CY7B9514V provides a bit rate reference clock to the WAC-413 transmitter by multiplying one of the two local reference clocks by eight.

Utilized PECL outputs must be terminated by external resistors at the end of the connected transmission line. *Figure 2* shows an example of terminating a 50Ω transmission line connected to a pair of PECL outputs.

CY7B9514V offers a Power-Down feature. When the PWR_DWN input is asserted (to a TTL LOW), the Transmit PLL, transition detection logic, and Receive PLLs will power down. When this power-down feature is used, a power-down control circuit shall be implemented at each PECL output termination as shown in *Figure 3*. Each power-down control block will connect the terminating resistors to ground in normal operating mode. The pass gate, shown in *Figure 3*, must be able to sink at least 25 mA when turned on. It also provides a low resistance path to ground. In power-down mode, the power-down control circuit will allow the terminating resistors to pull both outputs to V_{CC}.

The power-down control logic should consume minimal power when in power-down mode (i.e., PWR_DWN asserted). A CMOS device is suitable to implement the power down control logic. CYBUS3384 is a good candidate for this application.

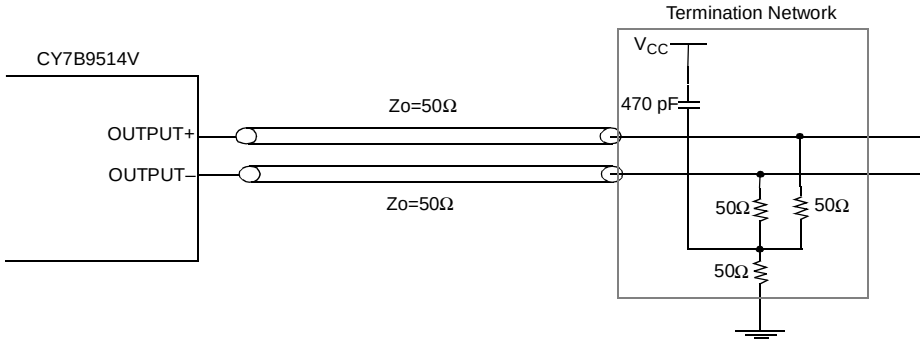


Figure 2. Termination Network Design

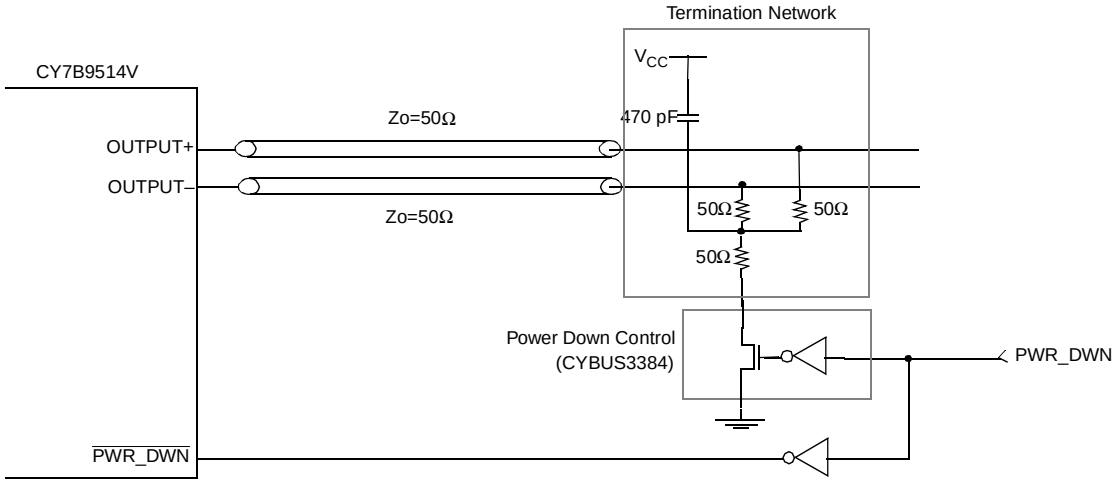


Figure 3. Power Down Control System Block (one terminated output)

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential..... –0.5V to +5.0V

DC Input Voltage ..... –0.5V to + (V_{CC} + 0.5)V

Output Current into TTL Outputs (LOW)..... 30 mA

Output Current into ECL Outputs (HIGH)..... –50 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 10%
Industrial	–40°C to +85°C	3.3V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description		Test Condition	Min.	Max.	Unit
TTL Compatible Input Pins (LOOP, REFCLK, REFSEL, PWR_DWN)						
V_{IHT}	Input HIGH Voltage			2.0	V_{CC}	V
V_{ILT}	Input LOW Voltage			–0.5	0.8	V
I_{IHT}	Input HIGH Current		$V_{IN}=V_{CC}$	–50	+50	µA
I_{ILT}	Input LOW Current		$V_{IN}=0.0V$	–50	+50	µA
TTL Compatible Output Pins ($\overline{LFI}$, REFOUT)						
V_{OHT}	Output HIGH Voltage		I_{OH}=–2 mA	2.4		V
V_{OLT}	Output LOW Voltage		I_{OL}=4 mA		0.45	V
PECL Compatible Input Pins (CD, TSER±, RIN±)						
I_{IHE}	PECL Input HIGH Current	CD	$V_{IN}=V_{IHE(MAX)}$	+0.5	+300	µA
		TSER/RIN	$V_{IN}=V_{IHE(MAX)}$	–250	+250	µA
I_{ILE}[1]	PECL Input LOW Current	CD	V_{IN}=1.3V	+0.5	+300	µA
		TSER/RIN	$V_{IN}=V_{ILE(MIN)}$	–250	+250	µA
V_{IHE}	Input High Voltage	CD		V_{CC} – 1.145	V_{CC}	V
		TSER/RIN			V_{CC}	V
V_{ILE}	Input LOW Voltage	CD		0	V_{CC} – 1.475	V
		TSER/RIN		1.3		V
V_{IDIFF}	Input Differential Voltage	TSER/RIN		100	1200	mV
PECL Compatible Output Pins (RCLK±, RSER±, TOUT±, TCLK±)						
V_{OHE}	PECL Output HIGH Voltage	Test Load=50Ω to V_{CC} – 2V			V_{CC} – 0.83	V
V_{OLE}	PECL Output LOW Voltage		T > 0°C	V_{CC} – 1.96		V
V_{ODIFF}	Output Differential Voltage			0.6		V
Three-Level Input Pins (MODE0 MODE1)						
V_{IHH}	Three-Level Input HIGH			V_{CC} – 0.6	V_{CC}	V
V_{IMM}	Three-Level Input MID[2]			$V_{CC}/2$ – 0.3	$V_{CC}/2$ + 0.3	V
V_{ILL}	Three-Level Input LOW			0.0	0.6	V
Operating Current[3]						
I_{CCM}	Total Operating Current. Excluding output currents[3]				400	mA
I_{STBY}	Standby Current	$\overline{PWR\_DWN}$ = LOW	PECLOUT pins are forced to V_{OH}		20	mA

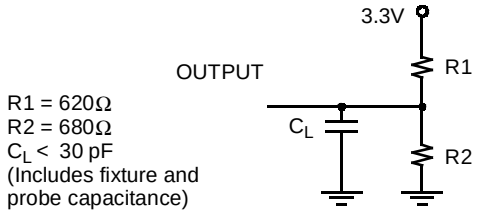
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f_0 = 1 MHz, V_{CC} = 3.3V	10	pF

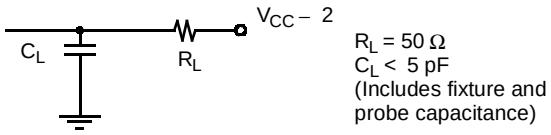
Notes:

1. Input currents are always positive at all voltages above $V_{CC}/2$.
2. No more than ±5 µA leakage when held at MID level.
3. For each active received channel not active (i.e., RSERx & RCLKx tied to V_{CC} or left floating) the I_{CCM} is reduced by 65 mA. For each transmit channel with the outputs tied to V_{CC} or left floating, I_{CCM} is reduced by 7 mA. If TCLK outputs are tied to V_{CC} or left floating, reduce I_{CCM} by 37mA.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

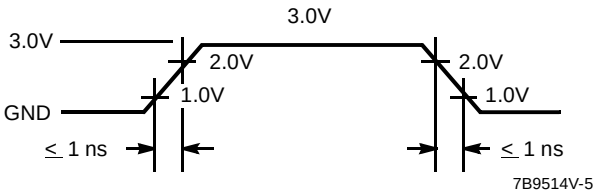


(a) TTL AC Test Load[5]

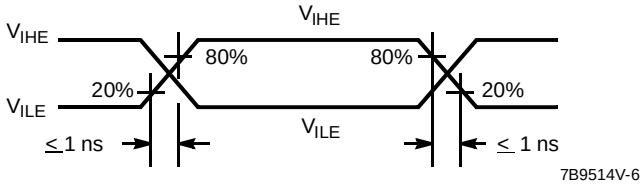


(b) PECL AC Test Load[5]

7B9514V-7



(c) TTL Input Test Waveform



(d) PECL Input Test Waveform

Note:

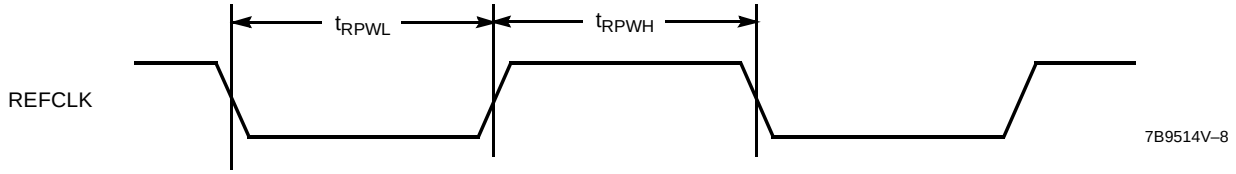
5. Cypress uses constant current (ATE) load configurations and forcing functions. This figure is for reference only.

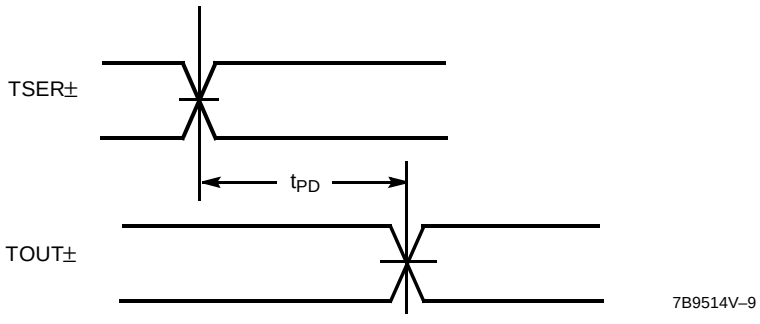
Switching Characteristics Over the Operating Range

Parameter	Description		Min.	Max.	Unit
f_{REF}	Reference Frequency	MODE0=LOW	6.41	6.55	MHz
		MODE0=HIGH	19.24	19.64	MHz
t_B	Bit Time[6]	MODE0=LOW	19.50	19.10	ns
		MODE0=HIGH	6.50	6.40	ns
t_{PE}	Receiver Static Phase Error[4]	MODE0=LOW		200	ps
		MODE0=HIGH		200	ps
t_{ODC}	Output Duty Cycle (TCLK±, RCLK±)[4]		45	55	%
t_{RF}	Output Rise/Fall Time[4]		0.4	1.2	ns
t_{LOCK}	PLL Lock Time (RIN transition density 25%)[7]	MODE0=LOW		3000	µs
		MODE0=HIGH		1000	µs
t_{RPWH}	REFCLK Pulse Width HIGH		10		ns
t_{RPWL}	REFCLK Pulse Width LOW		10		ns
t_{DV}	Data Valid		3		ns
t_{DH}	Data Hold		1		ns
t_{PD}	Propagation Delay (TSER to TOUT)[8]			10	ns
t_{RL}	No Transition Run Length, 25% data field			75	f_B

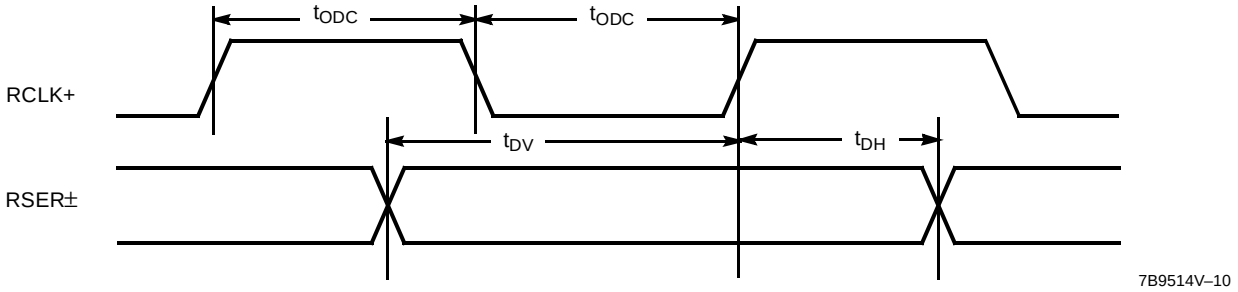
Notes:
6. t_B is calculated as $1/(f_{REF}X8)$.
7. t_{LOCK} is the time needed for transitioning from lock to REFCLK X8 to lock to data.
8. The PECL switching threshold is the differential zero crossing (i.e., the place where + and – signals cross).

Switching Waveforms

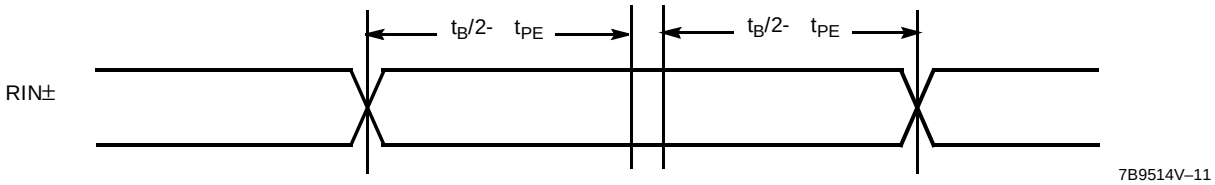




Switching Waveforms (continued)



7B9514V–10



7B9514V–11

Ordering Information

Ordering Code	Package Name	Package Type	OperatingRange
CY7B9514V-AC	A101	100-Lead (14 X 20 mm) Molded TQFP	Commercial

Document #: 38-00648-D

Package Diagram

100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101