Delta39K™ ISR™ CPLD Family

CPLDs at FPGA Densities™

Features

- High density
  - 30K to 200K usable gates
  - 512 to 3072 macrocells
  - 136 to 428 maximum I/O pins
  - Twelve dedicated inputs including four clock pins, four global I/O control signal pins and four JTAG interface pins for boundary scan and reconfigurability
- Embedded memory
  - 80K to 480K bits embedded SRAM
    - 16K to 96K bits of (dual-port) channel memory
- High speed – 233-MHz in-system operation
- AnyVolt™ interface
  - 3.3V, 2.5V,1.8V, and 1.5V I/O capability
- Low-power operation
  - 0.18-mm six-layer metal SRAM-based logic process
  - Full-CMOS implementation of product term array
  - Standby current as low as 5mA
- Simple timing model
  - No penalty for using full 16 product terms/macrocell
  - No delay for single product term steering or sharing
- Flexible clocking
  - Spread Aware™ PLL drives all four clock networks
    - Allows 0.6% spread spectrum input clocks
    - Several multiply, divide and phase shift options
  - Four synchronous clock networks per device
  - Locally generated product term clock
  - Clock polarity control at each register
- Carry-chain logic for fast and efficient arithmetic operations
- Multiple I/O standards supported
  - LVCMOS (3.3/3.0/2.5/1.8V), LVTTL, 3.3V PCI, SSTL2 (I-II), SSTL3 (I-II), HSTL (I-IV), and GTL+
- Compatible with NOBL™, ZBT™, and QDR™ SRAMs
- Programmable slew rate control on each I/O pin
- User-programmable Bus Hold capability on each I/O pin
- Fully 3.3V PCI-compliant (to 66-MHz 64-bit PCI spec, rev. 2.2)
- CompactPCI hot swap ready
- Multiple package/pinout offering across all densities
  - 208 to 676 pins in PQFP, BGA, and FBGA packages
  - Simplifies design migration across density
  - Self-Boot™ solution in BGA and FBGA packages
  - Lead (Pb)-free packages available.
- In-System Reprogrammable™ (ISR™)
  - JTAG-compliant on-board programming
  - Design changes do not cause pinout changes
- IEEE1149.1 JTAG boundary scan

Development Software

- *Warp*®
  - IEEE 1076/1164 VHDL or IEEE 1364 Verilog context sensitive editing
  - Active-HDL FSM graphical finite state machine editor
  - Active-HDL SIM post-synthesis timing simulator
  - Architecture Explorer for detailed design analysis
  - Static Timing Analyzer for critical path analysis
  - Available on Windows® 95/98/2000/XP™ and Windows NT™ for $99
  - Supports all Cypress programmable logic products

Delta39K™ ISR CPLD Family Members

Device	Typical Gates[1]	Macrocells	Cluster memory (Kbits)	Channel memory (Kbits)	Maximum I/O Pins	f_{MAX2} (MHz)	Speed-t_{PD} Pin-to-Pin (ns)	Standby I_{CC}[2] T_A = 25°C
								3.3/2.5V
39K30	16K – 48K	512	64	16	174	233	7.2	5 mA
39K50	23K – 72K	768	96	24	218	233	7.2	5 mA
39K100	46K – 144K	1536	192	48	302	222	7.5	10 mA
39K200	92K – 288K	3072	384	96	428	181	8.5	20 mA

Notes:
1. Upper limit of typical gates is calculated by assuming only 10% of the channel memory is used.
2. Standby I_{CC} values are with PLL not utilized, no output load and stable inputs.

Delta39K Speed Bins[3]

Device	V_{CC}	233	200	181	125	83
39K30	3.3/2.5V	X			X	X
39K50	3.3/2.5V	X			X	X
39K100	3.3/2.5V		X		X	X
39K200	3.3/2.5V			X	X	X

Device Package Offering and I/O Count Including Dedicated Clock and Control Inputs

Device	208 EQFP 28 × 28 mm 0.5-mm pitch	256 FBGA 17 × 17 mm 1.0-mm pitch	484-FBGA 23 × 23 mm 1.0-mm pitch	Self-Boot Solution[4] 256-FBGA 17 × 17 mm 1.0-mm pitch	388-BGA 35 × 35 mm 1.27-mm pitch	484-FBGA 23 × 23 mm 1.0-mm pitch	676-FBGA 27 × 27 mm 1.0-mm pitch
39K30	136	174		174			
39K50	136	180			218	218	
39K100	136	180	302		294		302
39K200	136		368		294		428

Notes:
3. Speed bins shown here are for commercial operating range. Please refer to Delta39K ordering information on industrial-range speed bins on page 37.
4. Self-boot solution integrates the boot PROM (flash memory) with Delta39K die inside the same package. This flash memory can endure at least 10,000 programming/erase cycles and can retain data for at least 100 years.

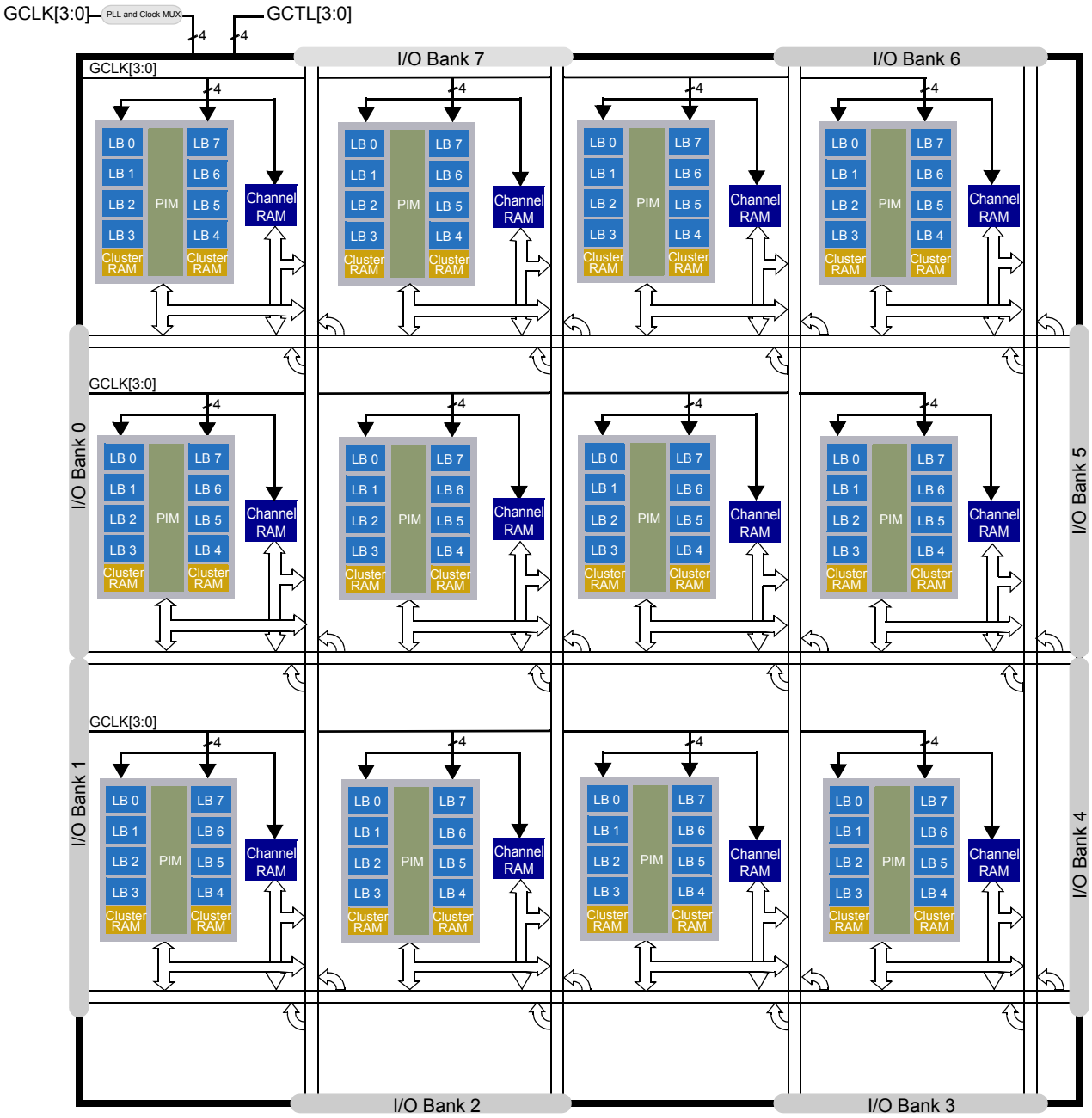


Figure 1. Delta39K100 Block Diagram (Three Rows × Four Columns) with I/O Bank Structure

General Description

The Delta39K family, based on a 0.18-mm, six-layer metal CMOS logic process, offers a wide range of high-density solutions at unparalleled system performance. The Delta39K family is designed to combine the high speed, predictable timing, and ease of use of CPLDs with the high densities and low power of FPGAs. With devices ranging from 30,000 to 200,000 usable gates, the family features devices ten times the size of previously available CPLDs. Even at these large densities, the Delta39K family is fast enough to implement a fully synthesizable 64-bit, 66-MHz PCI core.

The architecture is based on Logic Block Clusters (LBC) that are connected by Horizontal and Vertical (H and V) routing channels. Each LBC features eight individual Logic Blocks (LB) and two cluster memory blocks. Adjacent to each LBC is a channel memory block, which can be accessed directly from the I/O pins. Both types of memory blocks are highly configurable and can be cascaded in width and depth. See *Figure 1* for a block diagram of the Delta39K architecture.

All the members of the Delta39K family have Cypress's highly regarded In-System Reprogrammability (ISR) feature, which simplifies both design and manufacturing flows, thereby reducing costs. The ISR feature provides the ability to recon-

figure the devices without having design changes cause pinout or timing changes in most cases. The Cypress ISR function is implemented through a JTAG-compliant serial interface. Data is shifted in and out through the TDI and TDO pins respectively. Superior routability, simple timing, and the ISR allows users to change existing logic designs while simultaneously fixing pinout assignments and maintaining system performance.

The entire family features JTAG for ISR and boundary scan, and is compatible with the PCI Local Bus specification, meeting the electrical and timing requirements. The Delta39K family also features user programmable bus-hold and slew rate control capabilities on each I/O pin.

AnyVolt Interface

All Delta39KV devices feature an on-chip regulator, which accepts 3.3V or 2.5V on the V_{CC} supply pins and steps it down to 1.8V internally, the voltage level at which the core operates.

With Delta39K's AnyVolt technology, the I/O pins can be connected to either 1.8V, 2.5V, or 3.3V. All Delta39K devices are 3.3V-tolerant regardless of V_{CCIO} or V_{CC} settings.

Table 1.

Device	V_{CC}	V_{CCIO}
39KV	3.3V or 2.5V	3.3V or 2.5V or 1.8V or 1.5V[5]

Global Routing Description

The routing architecture of the Delta39K is made up of horizontal and vertical (H and V) routing channels. These routing channels allow signals from each of the Delta39K architectural components to communicate with one another. In addition to the horizontal and vertical routing channels that interconnect the I/O banks, channel memory blocks, and logic block clusters, each LBC contains a Programmable Interconnect Matrix™ (PIM™), which is used to route signals among the logic blocks and the cluster memory blocks.

Figure 2 is a block diagram of the routing channels that interface within the Delta39K architecture. The LBC is exactly the same for every member of the Delta39K CPLD family.

Logic Block Cluster (LBC)

The Delta39K architecture consists of several logic block clusters, each of which have eight Logic Blocks (LB) and two cluster memory blocks connected via a Programmable Interconnect Matrix (PIM) as shown in *Figure 3*. Each cluster memory block consists of 8-Kbit single-port RAM, which is configurable as synchronous or asynchronous. The cluster memory blocks can be cascaded with other cluster memory blocks within the same LBC as well as other LBCs to implement larger memory functions. If a cluster memory block is not specifically utilized by the designer, Cypress's *Warp* software can automatically use it to implement large blocks of logic.

All LBCs interface with each other via horizontal and vertical routing channels.

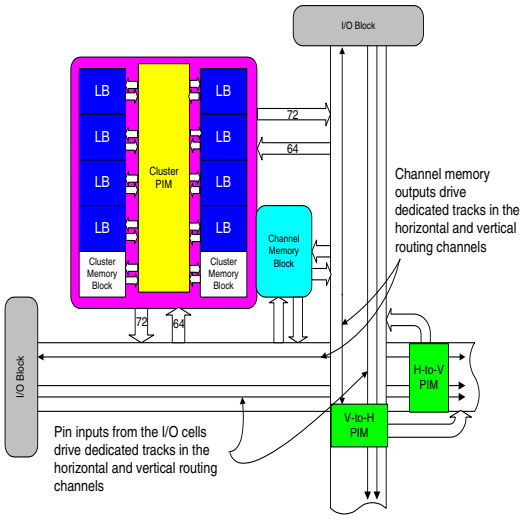


Figure 2. Delta39K Routing Interface

Note:
5. For HSTL only.

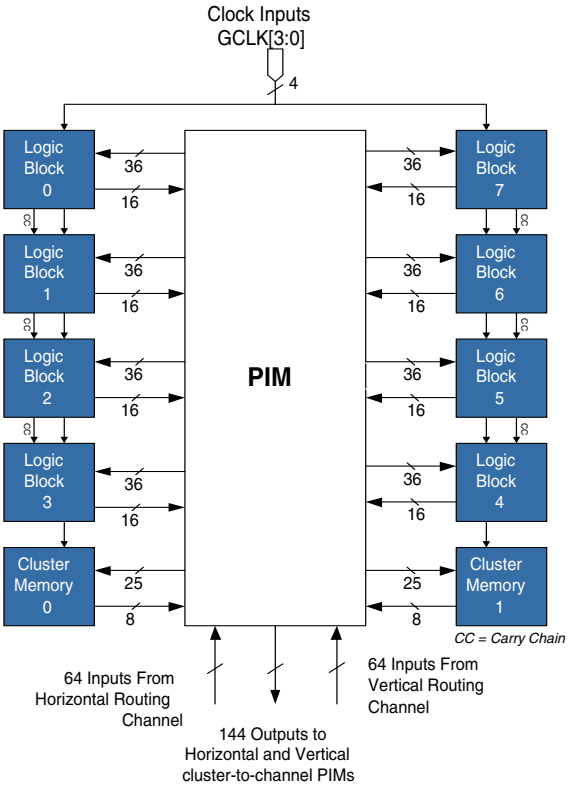


Figure 3. Delta39K Logic Block Cluster Diagram

Logic Block

The LB is the basic building block of the Delta39K architecture. It consists of a product term array, an intelligent product-term allocator, and 16 macrocells.

Product Term Array

Each logic block features a 72 x 83 programmable product term array. This array accepts 36 inputs from the PIM. These inputs originate from device pins and macrocell feedbacks as well as cluster memory and channel memory feedbacks. Active LOW and active HIGH versions of each of these inputs are generated to create the full 72-input field. The 83 product terms in the array can be created from any of the 72 inputs.

Of the 83 product terms, 80 are for general-purpose use for the 16 macrocells in the logic block. Two of the remaining three product terms in the logic block are used as asynchronous set and asynchronous reset product terms. The final product term is the Product Term clock (PTCLK) and is shared by all 16 macrocells within a logic block.

Product Term Allocator

Through the product term allocator, *Warp* software automatically distributes the 80 product terms as needed among the 16 macrocells in the logic block. The product term allocator provides two important capabilities without affecting performance: product term steering and product term sharing.

Product Term Steering

Product term steering is the process of assigning product terms to macrocells as needed. For example, if one macrocell requires ten product terms while another needs just three, the product term allocator will “steer” ten product terms to one macrocell and three to the other. On Delta39K devices, product terms are steered on an individual basis. Any number between 1 and 16 product terms can be steered to any macrocell.

Product Term Sharing

Product term sharing is the process of using the same product term among multiple macrocells. For example, if more than one function has one or more product terms in its equation that are common to other functions, those product terms are only programmed once. The Delta39K product term allocator allows sharing across groups of four macrocells in a variable fashion. The software automatically takes advantage of this capability so that the user does not have to intervene.

Note that neither product term sharing nor product term steering have any effect on the speed of the product. All steering and sharing configurations have been incorporated in the timing specifications for the Delta39K devices.

Macrocell

Within each logic block there are 16 macrocells. Each macrocell accepts a sum of up to 16 product terms from the product term array. The sum of these 16 product terms can be output in either registered or combinatorial mode. *Figure 4* displays the block diagram of the macrocell. The register can be asynchronously preset or asynchronously reset at the macrocell level with the separate preset and reset product terms. Each of these product terms features programmable polarity. This allows the registers to be preset or reset based on an AND expression or an OR expression.

An XOR gate in the Delta39K macrocell allows for many different types of equations to be realized. It can be used as a polarity mux to implement the true or complement form of an equation in the product term array or as a toggle to turn the D flip-flop into a T flip-flop. The carry-chain input mux allows additional flexibility for the implementation of different types of logic. The macrocell can utilize the carry chain logic to implement adders, subtractors, magnitude comparators, parity tree, or even generic XOR logic. The output of the macrocell is either registered or combinatorial.

Carry Chain Logic

The Delta39K macrocell features carry chain logic which is used for fast and efficient implementation of arithmetic operations. The carry logic connects macrocells in up to four logic blocks for a total of 64 macrocells. Effective data path operations are implemented through the use of carry-in arithmetic, which drives through the circuit quickly. *Figure 4* shows that the carry chain logic within the macrocell consists of two product terms (CPT0 and CPT1) from the PTA and an input carry-in for carry logic. The inputs to the carry chain mux are connected directly to the product terms in the PTA. The output of the carry chain mux generates the carry-out for the next macrocell in the logic block as well as the local carry input that is connected to an input of the XOR input mux. Carry-in and a configuration bit are inputs to an AND gate. This AND gate provides a method of segmenting the carry chain in any macrocell in the logic block.

Macrocell Clocks

Clocking of the register is highly flexible. Four global synchronous clocks (GCLK[3:0]) and a PTCLK are available at each macrocell register. Furthermore, a clock polarity mux within each macrocell allows the register to be clocked on the rising or the falling edge (see macrocell diagram in *Figure 4*).

PRESET/RESET Configurations

The macrocell register can be asynchronously preset and reset using the PRESET and RESET mux. Both signals are active high and can be controlled by either of two Preset/Reset product terms (PRC[1:0] in *Figure 4*) or GND. In situations where the PRESET and RESET are active at the same time, RESET takes priority over PRESET.

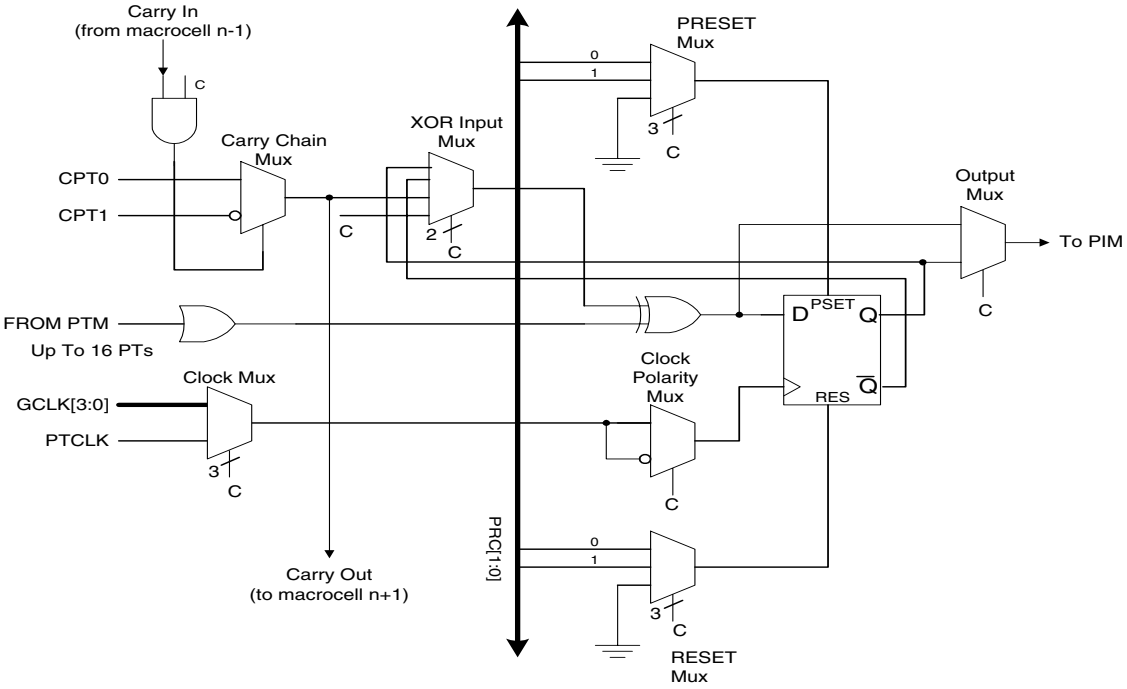


Figure 4. Delta39K Macrocell

Embedded Memory

Each member of the Delta39K family contains two types of embedded memory blocks. The channel memory block is placed at the intersection of horizontal and vertical routing channels. Each channel memory block is 4096 bits in size and can be configured as asynchronous or synchronous Dual-Port RAM, Single-Port RAM, Read-Only memory (ROM), or synchronous FIFO memory. The memory organization is configurable as 4K × 1, 2K × 2, 1K × 4 and 512K × 8. The second type of memory block is located within each LBC and is referred to as a cluster memory block. Each LBC contains two cluster memory blocks that are 8192 bits in size. Similar to the channel memory blocks, the cluster memory blocks can be configured as 8K × 1, 4K × 2, 2K × 4 and 1K × 8 asynchronous or synchronous Single-Port RAM or ROM.

Cluster Memory

Each logic block cluster of the Delta39K contains two 8192-bit cluster memory blocks. *Figure 5* is a block diagram of the cluster memory block and the interface of the cluster memory block to the cluster PIM.

The output of the cluster memory block can be optionally registered to perform synchronous pipelining or to register asynchronous Read and Write operations. The output registers contain an asynchronous RESET which can be used in any type of sequential logic circuits (e.g., state machines).

There are four global clocks (GCLK[3:0]) and one local clock available for the input and the output registers. The local clock for the input registers is independent of the one used for the output registers. The local clock is generated in the user design in a macrocell or comes from an I/O pin.

Cluster Memory Initialization

The cluster memory powers up in an undefined state, but is set to a user-defined known state during configuration. To facilitate the use of look-up-table (LUT) logic and ROM applications, the cluster memory blocks can be initialized with a given set of data when the device is configured at power up. For LUT and ROM applications, the user cannot write to memory blocks.

Channel Memory

The Delta39K architecture includes an embedded memory block at each crossing point of horizontal and vertical routing channels. The channel memory is a 4096-bit embedded memory block that can be configured as asynchronous or synchronous single-port RAM, dual-port RAM, ROM, or synchronous FIFO memory.

Data, address, and control inputs to the channel memory are driven from horizontal and vertical routing channels. All data and FIFO logic outputs drive dedicated tracks in the horizontal and vertical routing channels. The clocks for the channel memory block are selected from four global clocks and pin inputs from the horizontal and vertical channels. The clock muxes also include a polarity mux for each clock so that the user can choose an inverted clock.

Dual-Port (Channel Memory) Configuration

Each port has distinct address inputs, as well as separate data and control inputs that can be accessed simultaneously. The inputs to the Dual-Port memory are driven from the horizontal and vertical routing channels. The data outputs drive dedicated tracks in the routing channels. The interface to the routing is such that Port A of the Dual-Port interfaces primarily with the horizontal routing channel and Port B interfaces primarily with the vertical routing channel.

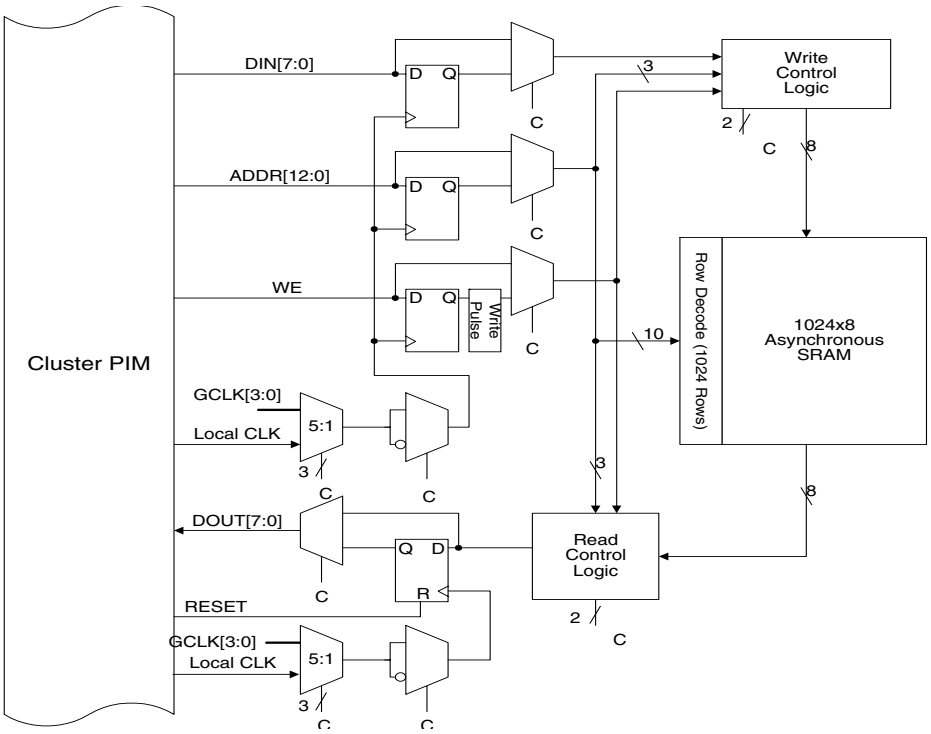


Figure 5. Block Diagram of Cluster Memory Block

The clocks for each port of the Dual-Port configuration are selected from four global clocks and two local clocks. One local clock is sourced from the horizontal channel and the other from the vertical channel. The data outputs of the dual-port memory can also be registered. Clocks for the output registers are also selected from four global clocks and two local clocks. One clock polarity mux per port allows the use of true or complement polarity for input and output clocking purposes.

Arbitration

The Dual-Port configuration of the Channel Memory Block provides arbitration when both ports access the same address at the same time. Depending on the memory operation being attempted, one port always gets priority. See *Table 2* for details on which port gets priority for Read and Write operations. An active-LOW “Address Match” signal is generated when an address collision occurs.

Table 2. Arbitration Result: Address Match Signal Becomes Active

Port A	Port B	Result of Arbitration	Comment
Read	Read	No arbitration required	Both ports read at the same time
Write	Read	Port A gets priority	If Port B requests first then it will read the current data. The output will then change to the newly written data by Port A
Read	Write	Port B gets priority	If Port A requests first then it will read the current data. The output will then change to the newly written data by Port B
Write	Write	Port A gets priority	Port B is blocked until Port A is finished writing

FIFO (Channel Memory) Configuration

The channel memory blocks are also configurable as synchronous FIFO RAM. In the FIFO mode of operation, the channel memory block supports all normal FIFO operations without the use of any general-purpose logic resources in the device.

The FIFO block contains all of the necessary FIFO flag logic, including the Read and Write address pointers. The FIFO flags include an empty/full flag ($\overline{EF}$), half-full flag (HF), and programmable almost-empty/full ($\overline{PAEF}$) flag output. The FIFO configuration has the ability to perform simultaneous Read and Write operations using two separate clocks. These clocks may be tied together for a single operation or may run independently for asynchronous Read/Write (with regard to each other) applications. The data and control inputs to the FIFO block are driven from the horizontal or vertical routing channels. The data and flag outputs are driven onto dedicated routing tracks in both the horizontal and vertical routing channels. This allows the FIFO blocks to be expanded by using multiple FIFO blocks on the same horizontal or vertical routing channel without any speed penalty.

In FIFO mode, the Write and Read ports are controlled by separate clock and enable signals. The clocks for each port are selected from four global clocks and two local clocks.

One local clock is sourced from the horizontal channel and the other from the vertical channel. The data outputs from the Read port of the FIFO can also be registered. One clock polarity mux per port allows using true or complement polarity for Read and Write operations. The Write operation is controlled by the clock and the Write enable pin. The Read operation is controlled by the clock and the Read enable pin. The enable pins can be sourced from horizontal or vertical channels.

Channel Memory Initialization

The channel memory powers up in an undefined state, but is set to a user-defined known state during configuration. To facilitate the use of look-up-table (LUT) logic and ROM applications, the channel memory blocks can be initialized with a given set of data when the device is configured at power up. For LUT and ROM applications, the user cannot write to memory blocks.

Channel Memory Routing Interface

Similar to LBC outputs, the channel memory blocks feature dedicated tracks in the horizontal and vertical routing channels for the data outputs and the flag outputs, as shown in *Figure 6*. This allows the channel memory blocks to be expanded easily. These dedicated lines can be routed to I/O pins as chip outputs or to other logic block clusters to be used in logic equations.

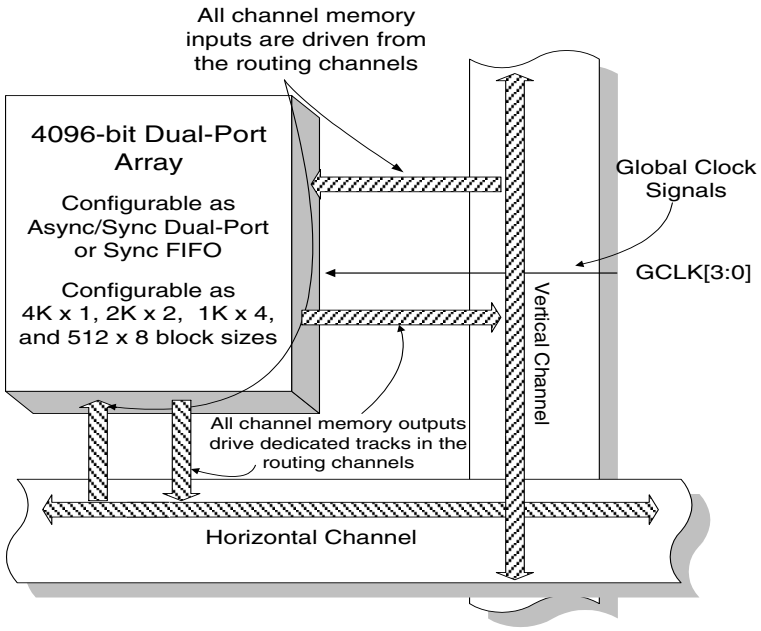


Figure 6. Block Diagram of Channel Memory Block

I/O Banks

The Delta39K interfaces the horizontal and vertical routing channels to the pins through I/O banks. There are eight I/O banks per device as shown in *Figure 7*, and all I/Os from an I/O bank are located in the same section of a package for PCB layout convenience.

Delta39K devices support True Vertical Migration™ (i.e., for each package type, Delta39K devices of different densities keep given pins in the same I/O banks). This allows for easy and simple implementation of multiple I/O standards during the design and prototyping phase, before a final density has been determined. Please refer to the application note titled *"Family, Package and Density Migration in Delta 39K and Quantum38K CPLDs."*

Each I/O bank contains several I/O cells, and each I/O cell contains an input/output register, an output enable register, programmable slew rate control and programmable bus hold control logic. Each I/O cell drives a pin output of the device; the cell also supplies an input to the device that connects to a dedicated track in the associated routing channel.

Each I/O bank can use any supported I/O standard by supplying appropriate V_{REF} and V_{CCIO} voltages and configuring the I/O through the Warp software. All the V_{REF} and V_{CCIO} pins in an I/O bank must be connected to the same V_{REF} and V_{CCIO} voltage respectively. This requirement restricts the number of I/O standards supported by an I/O bank at any given time.

The number of I/Os which can be used in each I/O bank depend on the type of I/O standards and the number of V_{CCIO} and GND pins being used. This restriction is derived from the electromigration limit of the V_{CCIO} and GND bussing on the chip. Please refer to the note on page 17 and the application note titled *"Delta39K Family Device I/O Standards and Configurations"* for details.

I/O Cell

Figure 8 is a block diagram of the Delta39K I/O cell. The I/O cell contains a three-state input buffer, an output buffer, and a register that can be configured as an input or output register. The output buffer has a slew rate control option that can be used to configure the output for a slower slew rate. The input of the device and the pin output can each be configured as registered or combinatorial; however, only one path can be configured as registered in a given design.

The output enable in an I/O cell can be selected from one of the four global control signals or from one of two Output Control Channel (OCC) signals. The output enable can be configured as always enabled or always disabled or it can be controlled by one of the remaining inputs to the mux. The selection is done via a mux that includes V_{CC} and GND as inputs.

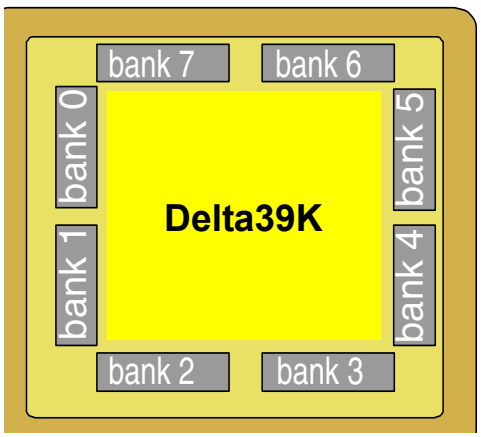


Figure 7. Delta39K I/O Bank Block Diagram

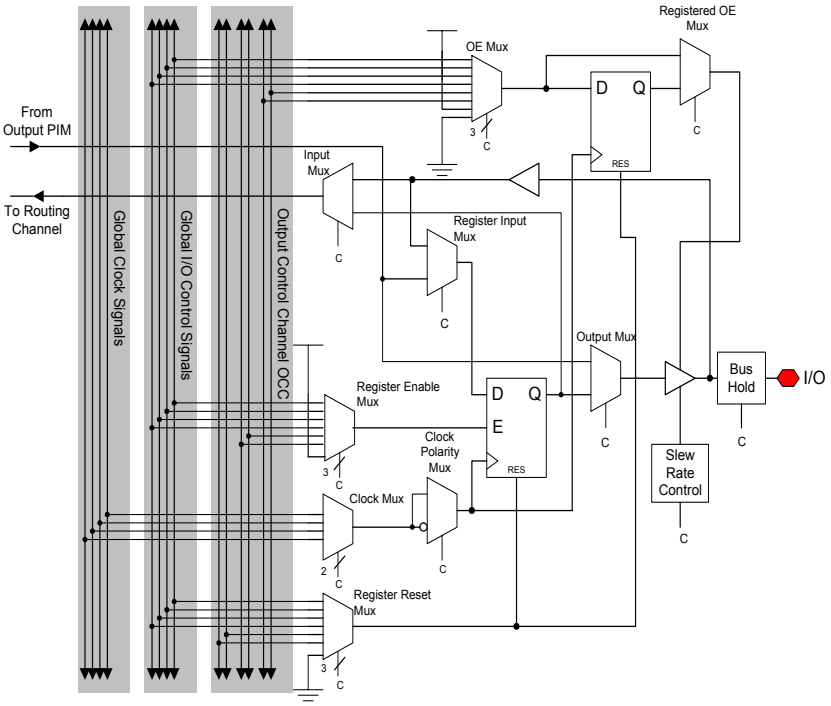


Figure 8. Block Diagram of I/O Cell

I/O Signals

There are four dedicated inputs (GCTL[3:0]) that are used as Global I/O Control Signals available to every I/O cell. These global I/O control signals may be used as output enables, register resets and register clock enables as shown in *Figure 8*. These global control signals, driven from four dedicated pins, can only be used as active-high signals and are available only to the I/O cells thereby implementing fast resets, register and output enables.

In addition, there are six OCC signals available to each I/O cell. These control signals may be used as output enables, register resets and register clock enables as shown in *Figure 8*. Unlike global control signals, these OCC signal can be driven from internal logic or and I/O pin.

One of the four global clocks can be selected as the clock for the I/O cell register. The clock mux output is an input to a clock polarity mux that allows the input/output register to be clocked on either edge of the clock

Slew Rate Control

The output buffer has a slew rate control option. This allows the output buffer to slew at a fast rate (3 V/ns) or a slow rate (1 V/ns). All I/Os default to fast slew rate. For designs concerned with meeting FCC emissions standards the slow edge provides for lower system noise. For designs requiring very high performance the fast edge rate provides maximum system performance.

Table 3.

I/O Standards

I/O Standard	V_{REF} (V)		V_{CCIO}	Termination Voltage (V_{TT})
	Min.	Max.		
LVTTL	N/A		3.3V	N/A
LVCMOS			3.3V	N/A
LVCMOS3			3.0V	N/A
LVCMOS2			2.5V	N/A
LVCMOS18			1.8V	N/A
3.3V PCI			3.3V	N/A
GTL+	0.9	1.1	N/A	1.5
SSTL3 I	1.3	1.7	3.3V	1.5
SSTL3 II	1.3	1.7	3.3V	1.5
SSTL2 I	1.15	1.35	2.5V	1.25
SSTL2 II	1.15	1.35	2.5V	1.25
HSTL I	0.68	0.9	1.5V	0.75
HSTL II	0.68	0.9	1.5V	0.75
HSTL III	0.68	0.9	1.5V	1.5
HSTL IV	0.68	0.9	1.5V	1.5

Programmable Bus Hold

On each I/O pin, user-programmable-bus-hold is included. Bus-hold, which is an improved version of the popular internal pull-up resistor, is a weak latch connected to the pin that does not degrade the device's performance. As a latch, bus-hold maintains the last state of a pin when the pin is placed in a high-impedance state, thus reducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototyping as designers can route new signals to the device without cutting trace connections to V_{CC} or GND. For more information, see the application note titled *"Understanding Bus-Hold–A Feature of Cypress CPLDs."*

Clocks

Delta39K has four dedicated clock input pins (GCLK[3:0]) to accept system clocks. One of these clocks (GCLK[0]) may be selected to drive an on-chip phase-locked loop (PLL) for frequency modulation (see *Figure 9* for details).

The global clock tree for a Delta39K device can be driven by a combination of the dedicated clock pins and/or the PLL-derived clocks. The global clock tree consists of four global clocks that go to every macrocell, memory block, and I/O cell.

Clock Tree Distribution

The global clock tree performs two primary functions. First, the clock tree generates the four global clocks by multiplexing four dedicated clocks from the package pins and four PLL driven clocks. Second, the clock tree distributes the four global clocks to every cluster, channel memory, and I/O block on the die. The global clock tree is designed such that the clock skew is minimized while maintaining an acceptable clock delay.

Spread Aware PLL

Each device in the Delta39K family features an on-chip PLL designed using Spread Aware technology for low EMI applications. In general, PLLs are used to implement time-division-multiplex circuits to achieve higher performance with fewer device resources.

For example, a system that operates on a 32-bit data path that runs at 40 MHz can be implemented with 16-bit circuitry that runs internally at 80 MHz. PLLs can also be used to take advantage of the positioning of the internally generated clock edges to shift performance towards improved setup, hold or clock-to-out times.

There are several frequency multiply (X1, X2, X3, X4, X5, X6, X8, X16) and divide (/1, /2, /3, /4, /5, /6, /8, /16) options available to create a wide range of clock frequencies from a single clock input (GCLK[0]). For increased flexibility, there are seven phase shifting options which allow clock skew/deskew by 45°, 90°, 135°, 180°, 225°, 270°, or 315°.

The Spread Aware feature refers to the ability of the PLL to track a spread-spectrum input clock such that its spread is seen on the output clock with the PLL staying locked. The total amount of spread on the input clock should be limited to 0.6% of the fundamental frequency. Spread Aware feature is supported only with X1, X2, and X4 multiply options.

The Voltage Controlled Oscillator (VCO), the core of the Delta39K PLL is designed to operate within the frequency range of 100 MHz to 266 MHz. Hence, the multiply option combined with input (GCLK[0]) frequency should be selected such that this VCO operating frequency requirement is met. This is demonstrated in *Table 4* (columns 1, 2, and 3).

Another feature of this PLL is the ability to drive the output clock (INTCLK) off the Delta39K chip to clock other devices on the board, as shown in *Figure 9* above. This off-chip clock is half the frequency of the output clock as it has to go through a register (I/O register or a macrocell register).

This PLL can also be used for board de-skewing purpose by driving a PLL output clock off-chip, routing it to the other devices on the board and feeding it back to the PLL's external feedback input (GCLK[1]). When this feature is used, only limited multiply, divide and phase shift options can be used. *Table 4* describes the valid multiply and divide options that can be used without external feedback. *Table 5* describes the valid multiply and divide options that can be used with an external feedback.

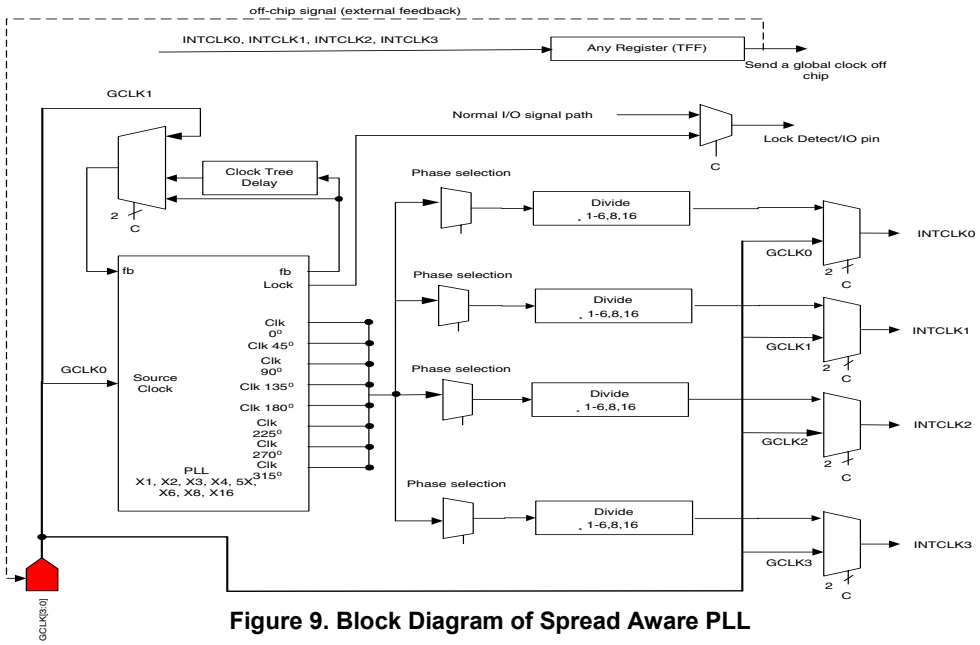


Figure 9. Block Diagram of Spread Aware PLL

Table 6 describes the valid phase shift options that can be used with or without an external feedback.

Table 7 is an example of the effect of all the available divide and phase shift options on a VCO output of 250 MHz. It also shows the effect of division on the duty cycle of the resultant clock. Note that the duty cycle is 50-50 when a VCO output is divided by an even number. Also note that the phase shift applies to the VCO output and not to the divided output.

For more details on the architecture and operation of this PLL please refer to the application note entitled *"Delta39K PLL and Clock Tree"*.

Table 4. Valid PLL Multiply and Divide Options—without External Feedback

Input Frequency (GCLK[0]) f_{PLLI} (MHz)	Valid Multiply Options		Valid Divide Options		
	Value	VCO Output Frequency (MHz)	Value	Output Frequency (INTCLK[3:0]) f_{PLLO} (MHz)	Off-chip Clock Frequency
DC–12.5	N/A	N/A	N/A	DC–12.5	DC–6.25
100–133	1	100–133	**1–6, 8, 16**	6.25–133	3.125–66
50–133	2	100–266	**1–6, 8, 16**	6.25–266	3.125–133
33.3–88.7	3	100–266	**1–6, 8, 16**	6.25–266	3.1–266
25–66	4	100–266	**1–6, 8, 16**	6.25–266	3.125–133
20–53.2	5	100–266	**1–6, 8, 16**	6.25–266	3.1–133
16.6–44.3	6	100–266	**1–6, 8, 16**	6.25–266	3.1–133
12.5–33	8	100–266	**1–6, 8, 16**	6.25–266	3.125–133
12.5–16.625	16	200–266	**1–6, 8, 16**	6.25–266	3.125–133

Table 5. Valid PLL Multiply and Divide Options—With External Feedback

Input (GCLK) Frequency f_{PLLI} (MHz)	Valid Multiply Options		Valid Divide Options		
	Value	VCO Output Frequency (MHz)	Value	Output (INTCLK) Frequency f_{PLLO} (MHz)	Off-chip Clock Frequency
50–133	**1**	100–266	**1**	100–266	50–133
25–66.5	**1**	100–266	**2**	50–133	25–66.5
16.67–44.33	**1**	100–266	**3**	33.33–88.66	16.67–44.33
12.5–33.25	**1**	100–266	**4**	25–66.5	12.5–33.25
12.5–26.6	**1**	125–266	**5**	25–53.2	12.5–26.6
12.5–22.17	**1**	150–266	**6**	25–44.34	12.5–22.17
12.5–16.63	**1**	200–266	**8**	25–33.25	12.5–16.63

Table 6. Recommended PLL Phase Shift Options

Without External Feedback	With External Feedback
0°,45°, 90°, 135°, 180°, 225°, 270°, 315°	0°

Table 7. Timing of Clock Phases for all Divide Options for a V_{CO} Output Frequency of 250 MHz

Divide Factor	Period (ns)	Duty Cycle%	0° (ns)	45° (ns)	90° (ns)	135° (ns)	180° (ns)	225° (ns)	270° (ns)	315° (ns)
1	4	40–60	0	0.5	1.0	1.5	2.0	2.5	3.0	3.5
2	8	50	0	0.5	1.0	1.5	2.0	2.5	3.0	3.5
3	12	33–67	0	0.5	1.0	1.5	2.0	2.5	3.0	3.5
4	16	50	0	0.5	1.0	1.5	2.0	2.5	3.0	3.5
5	20	40–60	0	0.5	1.0	1.5	2.0	2.5	3.0	3.5
6	24	50	0	0.5	1.0	1.5	2.0	2.5	3.0	3.5
8	32	50	0	0.5	1.0	1.5	2.0	2.5	3.0	3.5
16	64	50	0	0.5	1.0	1.5	2.0	2.5	3.0	3.5

CompactPCI Hot Swap

The CompactPCI Hot Swap specification allows the removal and insertion of cards into CompactPCI sockets without switching-off the bus. Delta39K CPLDs can be used as a CompactPCI host or target on these cards.

This feature is useful in telecommunication and networking applications as it allows implementation of high availability systems, where repairs and upgrades can be done without downtime.

Delta39K CPLDs are CompactPCI Hot Swap Ready per CompactPCI Hot Swap specification R2.0, with the following exception:

- The I/O cells do not provide bias voltage support. External resistors can be used to achieve this, per section 3.1.3.1 of the CompactPCI Hot Swap specification R2.0. A simple board level solution is provided in the application note titled *"Hot-Swapping Delta39K and Quantum38K CPLDs."*

Timing Model

One important feature of the Delta39K family is the simplicity of its timing. All combinatorial and registered/synchronous delays are worst case and system performance is static (as shown in the AC specs section) as long as data is routed through the same horizontal and vertical channels. *Figure 10* illustrates the true timing model for the 200-MHz devices. For synchronous clocking of macrocells, a delay is incurred from macrocell clock to macrocell clock of separate Logic Blocks within the same cluster, as well as separate Logic Blocks within different clusters. This is respectively shown as t_{SCS} and t_{SCS2} in *Figure 10.* For combinatorial paths, any input to any output (from corner to corner on the device), incurs a worst-case delay in the 39K100 regardless of the amount of logic or which horizontal and vertical channels are used. This is the t_{PD} shown in *Figure 10.* For synchronous systems, the input set-up time to the output macrocell register and the clock to output time are shown as the parameters t_{MCS} and t_{MCCO} shown in the *Figure 10.* These measurements are for any output and synchronous clock, regardless of the logic placement.

The Delta39K features:

- no dedicated vs. I/O pin delays
- no penalty for using 0 – 16 product terms
- no added delay for steering product terms
- no added delay for sharing product terms
- no output bypass delays.

The simple timing model of the Delta39K family eliminates unexpected performance penalties.

Family, Package, and Density Migration in Delta39K CPLDs

The Delta39K CPLDs combine dense logic, embedded memory and configurable I/O standards. Further design flexibility is added by the easy migration options available between different packages and densities of Delta39K CPLD offerings.

This migration flexibility makes changes or additions to designs simple even after PCB layout. It also provides the ability for experimental designs to be used on production PCBs. Please refer to the application note titled *"Family, Package, and Density Migration in Delta39K CPLDs."*

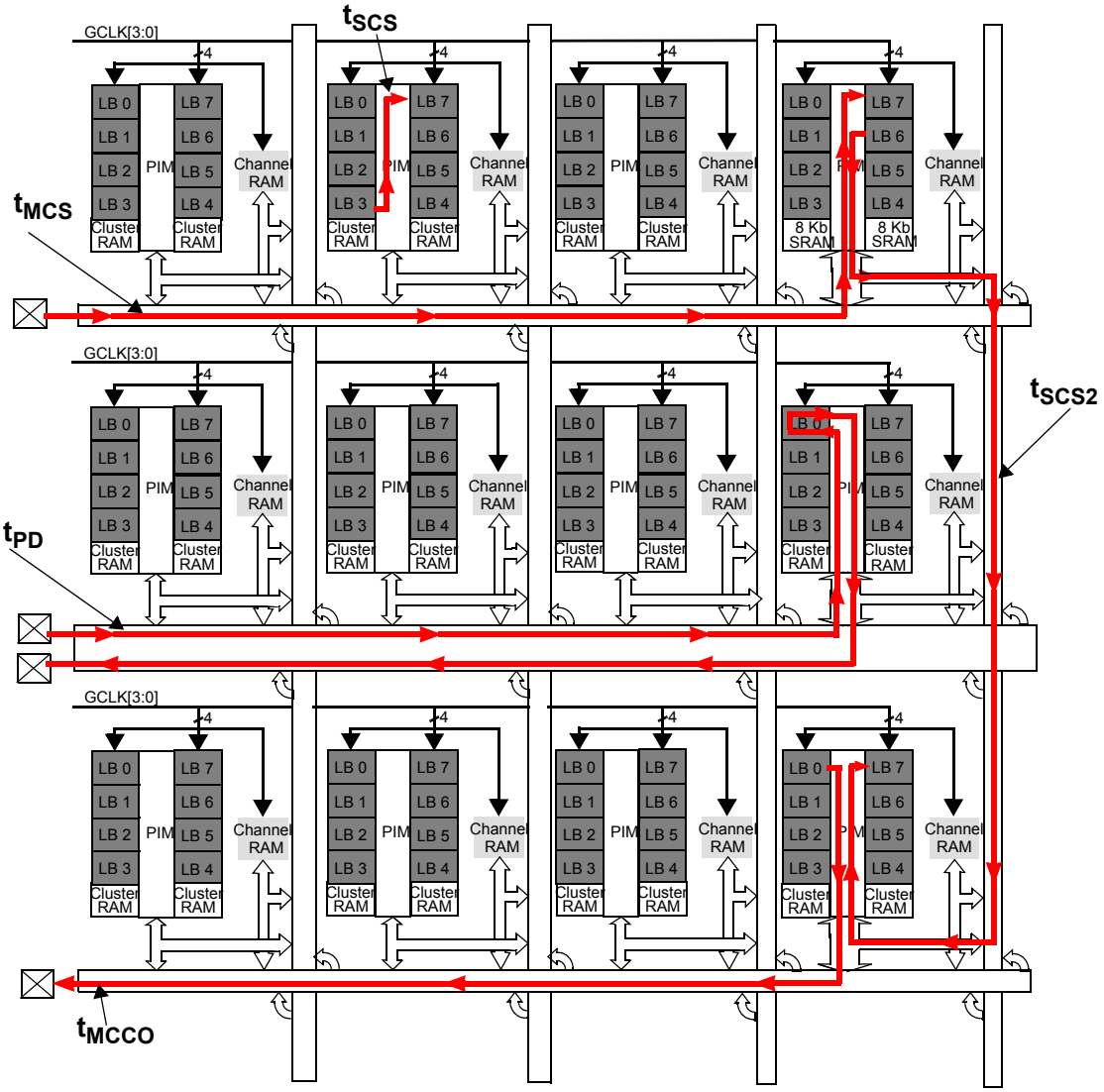


Figure 10. Timing Model for 39K100 Device

IEEE 1149.1-compliant JTAG Operation

The Delta39K family has an IEEE 1149.1 JTAG interface for both Boundary Scan and ISR operations.

Four dedicated pins are reserved on each device for use by the Test Access Port (TAP).

Boundary Scan

The Delta39K family supports Bypass, Sample/Preload, Extest, Intest, Idcode and Usercode boundary scan instructions. The JTAG interface is shown in *Figure 11*.

In-System Reprogramming (ISR)

In-System Reprogramming is the combination of the capability to program or reprogram a device on-board, and the ability to support design changes without changing the system timing or device pinout. This combination means design changes during debug or field upgrades do not cause board respins.

The Delta39K family implements ISR by providing a JTAG compliant interface for on-board programming, robust routing resources for pinout flexibility, and a simple timing model for consistent system performance.

Configuration

Each device of the Delta39K family is available in a volatile and a Self-Boot package. Cypress's CPLD boot EEPROM is used to store configuration data for the volatile solution and an embedded on-chip FLASH memory device is used for the Self-Boot solution.

For volatile Delta39K packages, programming is defined as the loading of a user's design into the external CPLD boot EEPROM. For Self-Boot Delta39K packages, programming is defined as the loading of a user's design into the on-chip FLASH internal to the Delta39K package. Configuration is defined as the loading of a user's design into the Delta39K die.

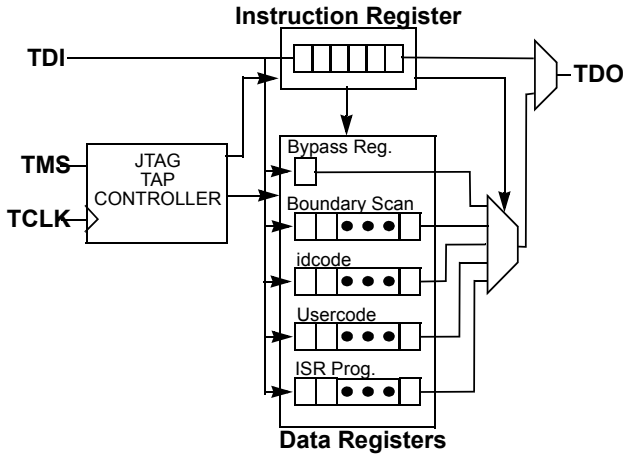


Figure 11. JTAG Interface

Configuration can begin in two ways. It can be initiated by toggling the *Reconfig* pin from LOW to HIGH, or by issuing the appropriate IEEE STD 1149.1 JTAG instruction to the Delta39K device via the JTAG interface. There are two IEEE STD 1149.1 JTAG instructions that initiate configuration of the Delta39K. The *Self Config* instruction causes the Delta39K to (re)configure with data stored in the serial boot PROM or the embedded FLASH memory. The *Load Config* instruction causes the Delta39K to (re)configure according to data provided by other sources such as a PC, automatic test equipment (ATE), or an embedded micro-controller/processor via the JTAG interface. For more information on configuring Delta39K devices, refer to the application note titled *"Configuring Delta39K/Quantum38K"* at http://www.cypress.com.

There are two configuration options available for issuing the IEEE STD 1149.1 JTAG instructions to the Delta39K. The first method is to use a PC with the C3ISR programming cable and software. With this method, the ISR pins of the Delta39K devices in the system are routed to a connector at the edge of the printed circuit board. The C3ISR programming cable is then connected between the PC and this connector. A simple configuration file instructs the ISR software of the programming operations to be performed on the Delta39K devices in the system. The ISR software then automatically completes all of the necessary data manipulations required to accomplish configuration, reading, verifying, and other ISR functions. For more information on the Cypress ISR interface, see the ISR Programming Kit data sheet (CY3900i).

The second configuration option for the Delta39K is to utilize the embedded controller or processor that already exists in the system. The Delta39K ISR software assists in this method by converting the device HEX file into the ISR serial stream that contains the ISR instruction information and the addresses and data of locations to be configured. The embedded controller then simply directs this ISR stream to the chain of Delta39K devices to complete the desired reconfiguration or diagnostic operations. Contact your local sales office for information on the availability of this option.

Programming

The on-chip FLASH device of the Delta39K Self-Boot package is programmed by issuing the appropriate IEEE STD 1149.1 JTAG instruction to the internal FLASH memory via the JTAG interface. This can be done automatically using ISR/STAPL software. The configuration bits are sent from a PC through the JTAG port into the Delta39K via the C3ISR programming cable. The data is then internally passed from Delta39K to the on-chip FLASH. For more information on how to program the Delta39K through ISR/STAPL, please refer to the ISR/STAPL User Guide.

The external CPLD boot EEPROM used to store configuration data for the Delta39K volatile package is programmed through Cypress's CYDH2200E CPLD Boot PROM Programming Kit via a two-wire interface. For more information on how to program the CPLD boot EEPROM, please refer to the data sheet titled "*CYDH2200E CPLD Boot PROM Programming Kit*." For more information on the architecture and timing specification of the boot EEPROM, refer to the data sheet titled "*512K/1Mb CPLD Boot EEPROM*" or "*2-Mbit CPLD Boot EEPROM.*"

Third-Party Programmers

Cypress support is available on a wide variety of third-party programmers. All major programmers (including BP Micro, System General, Hi-Lo) support the Delta39K family.

Development Software Support

Warp

Warp is a state-of-the-art design environment for designing with Cypress programmable logic. *Warp* utilizes a subset of IEEE 1076/1164 VHDL and IEEE 1364 as the Hardware Description Language (HDL) for design entry. *Warp* accepts VHDL or Verilog input, synthesizes and optimizes the entered design, and outputs a configuration bitstream for the desired Delta39K device. For simulation, *Warp* provides a graphical waveform simulator as well as VHDL and Verilog Timing Models.

VHDL and Verilog are open, powerful, non-proprietary Hardware Description Languages (HDLs) that are standards for behavioral design entry and simulation. HDL allows designers to learn a single language that is useful for all facets of the design process.

Third-Party Software

Cypress products are supported in a number of third-party design entry and simulation tools. Refer to the third-party software data sheet or contact your local sales office for a list of currently supported third party vendors.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature (39K200, 208 EQFP) ..... –45°C to +125°C

Storage Temperature (all other densities and packages) ..... –65°C to +150°C

Soldering Temperature ..... 220°C

Ambient Temperature with Power Applied ..... –40°C to +85°C

Junction Temperature ..... 135°C

V_{CC} to Ground Potential ..... –0.5V to 4.6V

V_{CCIO} to Ground Potential ..... –0.5V to 4.6V

DC Voltage Applied to Outputs in High-Z state ..... –0.5V to 4.5V

DC Input voltage ..... –0.5V to 4.5V

DC Current into Outputs ..... ± 20 mA[6]

Static Discharge Voltage (per JEDEC EIA./JESD22–A114A) ..... >2001V

Latch-up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	Junction Temperature	Output Condition	V_{CCIO}	V_{CC}	V_{CCJTAG}/ V_{CCCNFG}	V_{CCPLL}	V_{CCPRG}
Commercial	0°C to +70°C	0°C to +85°C	3.3V	3.3V ± 0.3V	3.3V ± 0.3V or 2.5V ± 0.2V (39KV)	Same as V_{CCIO}	Same as V_{CC}	3.3V ± 0.3V
			2.5V	2.5V ± 0.2V				
			1.8V	1.8V ± 0.15V				
			1.5V	1.5V ± 0.1V[5]				
Industrial	–40°C to +85°C	–40°C to +100°C	3.3V	3.3V ± 0.3V				
			2.5V	2.5V ± 0.2V				
			1.8V	1.8V ± 0.15V				
			1.5V	1.5V ± 0.1V[5]				

DC Characteristics

Parameter	Description	Test Conditions	V_{CCIO} = 3.3V		V_{CCIO} = 2.5V		V_{CCIO} = 1.8V		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{DRINT}	Data Retention V_{CC} Voltage (config data may be lost below this)		1.5		1.5		1.5		V
V_{DRIO}	Data Retention V_{CCIO} Voltage (config data may be lost below this)		1.2		1.2		1.2		V
I_{IX}[7]	Input Leakage Current	$GND \le V_I \le 3.6V$	–10	10	–10	10	–10	10	µA
I_{OZ}	Output Leakage Current	$GND \le V_O \le V_{CCIO}$	–10	10	–10	10	–10	10	µA
I_{OS}[8]	Output Short Circuit Current	V_{CCIO} = Max. V_{OUT} = 0.5V		–160		–160		–160	µA
I_{BHL}	Input Bus Hold LOW Sustaining Current	V_{CC} = Min. $V_{PIN} = V_{IL}$	+40		+30		+25		µA
I_{BHH}	Input Bus Hold HIGH Sustaining Current	V_{CC} = Min. $V_{PIN} = V_{IH}$	–40		–30		–25		µA
I_{BHLO}	Input Bus Hold LOW Overdrive Current	V_{CC} = Max.		+250		+200		+150	µA
I_{BHHO}	Input Bus Hold HIGH Overdrive Current	V_{CC} = Max.		–250		–200		–150	µA
I_{CC0}	Standby Current	39K30 39K50 39K100 39K200		*All bins* 20 20 30 60		*All bins* 20 20 30 60		*–125 bin* / *–83 bin* 3 / 12 3 / 12 5 / 20 10 / 40	µA

Notes:

6. DC current into outputs is 36 mA with HSTL III, 48 mA with HSTL IV, and 36 mA with GTL+ (with 25W pull-up resistor and V_{TT} = 1.5).
7. Input Leakage current is ±10µA for all the pins on all the Delta39K package except the following pins in Delta39K100 packages: The input leakage current spec for these pins in ±200µA

Delta39K100	
Package	**Pins**
388-BGA	B4, C2
484-FBGA	B8, G9
676-FBGA	F11, J11

8. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester-ground degradation. Tested initially and after any design or process changes that may affect these parameters.

Capacitance

Parameter	Description	Test Conditions	Min.	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	$V_{in} = V_{CCIO}$ @ f = 1 MHz 25°C		10	pF
C_{CLK}	Clock Signal Capacitance	$V_{in} = V_{CCIO}$ @ f = 1 MHz 25°C	5	12	pF
C_{PCI}	PCI-compliant[9] Capacitance	$V_{in} = V_{CCIO}$ @ f = 1 MHz 25°C		8	pF

DC Characteristics (I/O)[10]

I/O Standards	V_{REF} (V)	V_{CCIO} (V)	V_{OH} (V)		V_{OL} (V)		V_{IH} (V)		V_{IL} (V)	
			@ I_{OH} =	V_{OH} (min.)	@ I_{OL} =	V_{OL} (max.)	Min.	Max.	Min.	Max.
LVTTL –2 mA	N/A	3.3	–2 mA	2.4	2 mA	0.4	2.0V	V_{CCIO} + 0.3	–0.3V	0.8V
LVTTL –4 mA		3.3	–4 mA	2.4	4 mA	0.4	2.0V	V_{CCIO} + 0.3	–0.3V	0.8V
LVTTL –6 mA		3.3	–6 mA	2.4	6 mA	0.4	2.0V	V_{CCIO} + 0.3	–0.3V	0.8V
LVTTL –8 mA		3.3	–8 mA	2.4	8 mA	0.4	2.0V	V_{CCIO} + 0.3	–0.3V	0.8V
LVTTL –12 mA		3.3	–12 mA	2.4	12 mA	0.4	2.0V	V_{CCIO} + 0.3	–0.3V	0.8V
LVTTL –16 mA		3.3	–16 mA	2.4	16 mA	0.4	2.0V	V_{CCIO} + 0.3	–0.3V	0.8V
LVTTL –24 mA		3.3	–24 mA	2.4	24 mA	0.4	2.0V	V_{CCIO} + 0.3	–0.3V	0.8V
LVCMOS		3.3	–0.1 mA	V_{CCIO} – 0.2V	0.1 mA	0.2	2.0V	V_{CCIO} + 0.3	–0.3V	0.8V
LVCMOS3		3.0	–0.1 mA	V_{CCIO} – 0.2V	0.1 mA	0.2	2.0V	V_{CCIO} + 0.3	–0.3V	0.8V
LVCMOS2		2.5	–0.1 mA	2.1	0.1 mA	0.2	1.7V	V_{CCIO} + 0.3	–0.3V	0.7V
			–1.0 mA	2.0	1.0 mA	0.4				
			–2.0 mA	1.7	2.0 mA	0.7				
LVCMOS18		1.8	–2 mA	V_{CCIO} – 0.45V	2.0 mA	0.45	0.65V_{CCIO}	V_{CCIO} + 0.3	–0.3V	0.35V_{CCIO}
3.3V PCI		3.3	–0.5 mA	0.9V_{CCIO}	1.5 mA	0.1V_{CCIO}	0.5V_{CCIO}	V_{CCIO} + 0.5	–0.5V	0.3V_{CCIO}
GTL+	1.0	[11]			36 mA[12]	0.6	V_{REF} + 0.2			V_{REF} – 0.2
SSTL3 I	1.5	3.3	–8 mA	V_{CCIO} – 1.1V	8 mA	0.7	V_{REF} + 0.2	V_{CCIO} + 0.3	–0.3V	V_{REF} – 0.2
SSTL3 II	1.5	3.3	–16 mA	V_{CCIO} – 0.9V	16 mA	0.5	V_{REF} + 0.2	V_{CCIO} + 0.3	–0.3V	V_{REF} – 0.2
SSTL2 I	1.25	2.5	–7.6 mA	V_{CCIO} – 0.62V	7.6 mA	0.54	V_{REF} + 0.18	V_{CCIO} + 0.3	–0.3V	V_{REF} – 0.18
SSTL2 II	1.25	2.5	–15.2 mA	V_{CCIO} – 0.43V	15.2 mA	0.35	V_{REF} + 0.18	V_{CCIO} + 0.3	–0.3V	V_{REF} – 0.18
HSTL I	0.75	1.5	–8 mA	V_{CCIO} – 0.4V	8 mA	0.4	V_{REF} + 0.1	V_{CCIO} + 0.3	–0.3V	V_{REF} – 0.1
HSTL II	0.75	1.5	–16 mA	V_{CCIO} – 0.4V	16 mA	0.4	V_{REF} + 0.1	V_{CCIO} + 0.3	–0.3V	V_{REF} – 0.1
HSTL III	0.9	1.5	–8 mA	V_{CCIO} – 0.4V	24 mA	0.4	V_{REF} + 0.1	V_{CCIO} + 0.3	–0.3V	V_{REF} – 0.1
HSTL IV	0.9	1.5	–8 mA	V_{CCIO} – 0.4V	48 mA	0.4	V_{REF} + 0.1	V_{CCIO} + 0.3	–0.3V	V_{REF} – 0.1

Configuration Parameters

Parameter	Description	Min.	Unit
$t_{RECONFIG}$	*Reconfig* pin LOW time before it goes HIGH	200	ns

Power-up Sequence Requirements

- Upon power-up, all the outputs remain three-stated until all the V_{CC} pins have powered-up to the nominal voltage and the part has completed configuration.
- The part will not start configuration until V_{CC}, V_{CCIO}, V_{CCJTAG}, V_{CCCNFG}, V_{CCPLL} and V_{CCPRG} have reached nominal voltage.
- V_{CC} pins can be powered up in any order. This includes V_{CC}, V_{CCIO}, V_{CCJTAG}, V_{CCCNFG}, V_{CCPLL} and V_{CCPRG}.
- All V_{CCIO}s on a bank should be tied to the same potential and powered up together.
- All V_{CCIO}s (even the unused banks) need to be powered up to at least 1.5V before configuration has completed.
- Maximum ramp time for all V_{CC}s should be 0V to nominal voltage in 100 ms.

Notes:

9. PCI spec (rev 2.2) requires the IDSEL pin to have capacitance less than or equal to 8 pF. Delta39K Pin Tables starting from page 44, identify all the I/O pins in a given package, which can be used as IDSEL in a PCI design. All other I/O pins meet the PCI requirement of capacitance less than or equal to 10 pF.
10. The number of I/Os which can be used in each I/O bank depends on the type of I/O standards and the number of V_{CCIO} and GND pins being used. Please refer to the application note titled *"Delta39K and Quantum38K I/O Standards and Configurations"* for details.
    - The source current limit per I/O bank per V_{CCIO} pin is 165 mA.
    - The sink current limit per I/O bank per GND pin is 230 mA.
11. See "Power-up Sequence Requirements" below for V_{CCIO} requirement.
12. 25Ω resistor terminated to termination voltage of 1.5V.

Switching Characteristics — Parameter Descriptions Over the Operating Range[13]

Parameter	Description
Combinatorial Mode Parameters	
t_{PD}	Delay from any pin input, through any cluster on the channel associated with that pin input, to any pin output on the horizontal or vertical channel associated with that cluster
t_{EA}	Global control to output enable
t_{ER}	Global control to output disable
t_{PRR}	Asynchronous macrocell RESET or PRESET recovery time from any pin input on the horizontal or vertical channel associated with the cluster the macrocell is in
t_{PRO}	Asynchronous macrocell RESET or PRESET from any pin input on the horizontal or vertical channel associated with the cluster that the macrocell is in to any pin output on those same channels
t_{PRW}	Asynchronous macrocell RESET or PRESET minimum pulse width, from any pin input to a macrocell in the farthest cluster on the horizontal or vertical channel the pin is associated with
Synchronous Clocking Parameters	
t_{MCS}	Set-up time of any input pin to a macrocell in any cluster on the channel associated with that input pin, relative to a global clock
t_{MCH}	Hold time of any input pin to a macrocell in any cluster on the channel associated with that input pin, relative to a global clock
t_{MCCO}	Global clock to output of any macrocell to any output pin on the horizontal or vertical channel associated with the cluster that macrocell is in
t_{IOS}	Set-up time of any input pin to the I/O cell register associated with that pin, relative to a global clock
t_{IOH}	Hold time of any input pin to the I/O cell register associated with that pin, relative to a global clock
t_{IOCO}	Clock to output of an I/O cell register to the output pin associated with that register
t_{SCS}	Macrocell clock to macrocell clock through array logic within the same cluster
t_{SCS2}	Macrocell clock to macrocell clock through array logic in different clusters on the same channel
t_{ICS}	I/O register clock to any macrocell clock in a cluster on the channel the I/O register is associated with
t_{OCS}	Macrocell clock to any I/O register clock on the horizontal or vertical channel associated with the cluster that the macrocell is in
t_{CHZ}	Clock to output disable (high-impedance)
t_{CLZ}	Clock to output enable (low-impedance)
f_{MAX}	Maximum frequency with internal feedback—within the same cluster
f_{MAX2}	Maximum frequency with internal feedback—within different clusters at the opposite ends of a horizontal or vertical channel
Product Term Clock	
t_{MCSPT}	Set-up time for macrocell used as input register, from input to product term clock
t_{MCHPT}	Hold time of macrocell used as an input register
t_{MCCOPT}	Product term clock to output delay from input pin
t_{SCS2PT}	Register to register delay through array logic in different clusters on the same channel using a product term clock
Channel Interconnect Parameters	
t_{CHSW}	Adder for a signal to switch from a horizontal to vertical channel and vice-versa
t_{CL2CL}	Cluster-to-cluster delay adder (through channels and channel PIM)
Miscellaneous Delays	
t_{CPLD}	Delay from the input of a cluster PIM, through a macrocell in the cluster, back to a cluster PIM input. This parameter can be added to the t_{PD} and t_{SCS} parameters for each extra pass through the AND/OR array required by a given signal path
t_{MCCD}	Adder for carry chain logic per macrocell
t_{IOD}	Delay from the input of the output buffer to the I/O pin
t_{IOIN}	Delay from the I/O pin to the input of the channel buffer

Note:
13. Add t_{CHSW} to signals making a horizontal to vertical channel switch or vice-versa.

Switching Characteristics — Parameter Descriptions Over the Operating Range[13] (continued)

Parameter	Description
t_{CKIN}	Delay from the clock pin to the input of the clock driver
$t_{IOREGPIN}$	Delay from the I/O pin to the input of the I/O register
PLL Parameters	
t_{MCCJ}	Maximum cycle to cycle jitter time
t_{DWSA}	PLL zero phase delay with clock tree deskewed
t_{DWOSA}	PLL zero phase delay without clock tree deskewed
t_{LOCK}	Lock time for the PLL
t_{INDUTY}	Input duty cycle
f_{PLLI}	Input frequency of the PLL
f_{PLLO}	Output frequency of the PLL
f_{PLLVCO}	PLL VCO frequency of operation
P_{SAPLLI}	Percentage modulation allowed (spread awareness) on the PLL input clock
f_{MPLLI}	Frequency of modulation allowed on PLL input clock. This specifies how fast the f_{PLLI} sweeps between f_{PLLI}* (1–P_{SAPLLI}/100) and f_{PLLI}* (1+ P_{SAPLLI}/100)
JTAG Parameters	
t_{JCKH}	TCLK HIGH time
t_{JCKL}	TCLK LOW time
t_{JCP}	TCLK clock period
t_{JSU}	JTAG port set-up time (TDI/TMS inputs)
t_{JH}	JTAG port hold time (TDI/TMS inputs)
t_{JCO}	JTAG port clock to output time (TDO)
t_{JXZ}	JTAG port valid output to high impedance (TDO)
t_{JZX}	JTAG port high impedance to valid output (TDO)

Cluster Memory Timing Parameter Descriptions Over the Operating Range

Parameter	Description
Asynchronous Mode Parameters	
t_{CLMAA}	Cluster memory access time. Delay from address change to Read data out
t_{CLMPWE}	Write Enable pulse width
t_{CLMSA}	Address set-up to the beginning of Write Enable with both signals from the same I/O block
t_{CLMHA}	Address hold after the end of Write Enable with both signals from the same I/O block
t_{CLMSD}	Data set-up to the end of Write Enable
t_{CLMHD}	Data hold after the end of Write Enable
Synchronous Mode Parameters	
$t_{CLMCYC1}$	Clock cycle time for flow through Read and Write operations (from macrocell register through cluster memory back to a macrocell register in the same cluster)
$t_{CLMCYC2}$	Clock cycle time for pipelined Read and Write operations (from cluster memory input register through the memory to cluster memory output register)
t_{CLMS}	Address, data, and WE set-up time of pin inputs, relative to a global clock
t_{CLMH}	Address, data, and WE hold time of pin inputs, relative to a global clock
t_{CLMDV1}	Global clock to data valid on output pins for flow through data
t_{CLMDV2}	Global clock to data valid on output pins for pipelined data
$t_{CLMMACS1}$	Cluster memory input clock to macrocell clock in the same cluster
$t_{CLMMACS2}$	Cluster memory output clock to macrocell clock in the same cluster
$t_{MACCLMS1}$	Macrocell clock to cluster memory input clock in the same cluster

Cluster Memory Timing Parameter Descriptions Over the Operating Range (continued)

Parameter	Description
$t_{MACCLMS2}$	Macrocell clock to cluster memory output clock in the same cluster
Internal Parameters	
$t_{CLMCLAA}$	Asynchronous cluster memory access time from input of cluster memory to output of cluster memory

Channel Memory Timing Parameter Descriptions Over the Operating Range

Parameter	Description
Dual Port Asynchronous Mode Parameters	
t_{CHMAA}	Channel memory access time. Delay from address change to Read data out
t_{CHMPWE}	Write enable pulse width
t_{CHMSA}	Address set-up to the beginning of Write enable with both signals from the same I/O block
t_{CHMHA}	Address hold after the end of Write enable with both signals from the same I/O block
t_{CHMSD}	Data set-up to the end of Write enable
t_{CHMHD}	Data hold after the end of Write enable
t_{CHMBA}	Channel memory asynchronous dual port address match (busy access time)
Dual Port Synchronous Mode Parameters	
$t_{CHMCYC1}$	Clock cycle time for flow through Read and Write operations (from macrocell register through channel memory back to a macrocell register in the same cluster)
$t_{CHMCYC2}$	Clock cycle time for pipelined Read and Write operations (from channel memory input register through the memory to channel memory output register)
t_{CHMS}	Address, data, and WE set-up time of pin inputs, relative to a global clock
t_{CHMH}	Address, data, and WE hold time of pin inputs, relative to a global clock
t_{CHMDV1}	Global clock to data valid on output pins for flow through data
t_{CHMDV2}	Global clock to data valid on output pins for pipelined data.
t_{CHMBDV}	Channel memory synchronous dual-port address match (busy, clock to data valid)
$t_{CHMMACS1}$	Channel memory input clock to macrocell clock in the same cluster
$t_{CHMMACS2}$	Channel memory output clock to macrocell clock in the same cluster
$t_{MACCHMS1}$	Macrocell clock to channel memory input clock in the same cluster
$t_{MACCHMS2}$	Macrocell clock to channel memory output clock in the same cluster
Synchronous FIFO Data Parameters	
t_{CHMCLK}	Read and Write minimum clock cycle time
t_{CHMFS}	Data, Read enable, and Write enable set-up time relative to pin inputs
t_{CHMFH}	Data, Read enable, and Write enable hold time relative to pin inputs
$t_{CHMFRDV}$	Data access time to output pins from rising edge of Read clock (Read clock to data valid)
$t_{CHMMACS}$	Channel memory FIFO Read clock to macrocell clock for Read data
$t_{MACCHMS}$	Macrocell clock to channel memory FIFO Write clock for Write data
Synchronous FIFO Flag Parameters	
t_{CHMFO}	Read or Write clock to respective flag output at output pins
$t_{CHMMACF}$	Read or Write clock to macrocell clock with FIFO flag
t_{CHMFRS}	Master Reset Pulse Width
$t_{CHMFRSR}$	Master Reset Recovery Time
$t_{CHMFRSF}$	Master Reset to Flag and Data Output Time
$t_{CHMSKEW1}$	Read/Write Clock Skew Time for Full Flag
$t_{CHMSKEW2}$	Read/Write Clock Skew Time for Empty Flag
$t_{CHMSKEW3}$	Read/Write Clock Skew Time for Boundary Flags

Channel Memory Timing Parameter Descriptions Over the Operating Range (continued)

Parameter	Description
Internal Parameters	
$t_{CHMCHAA}$	Asynchronous channel memory access time from input of channel memory to output of channel memory

Switching Characteristics—Parameter Values Over the Operating Range

Parameter	233		200		181		125		83		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters											
t_{PD}		7.2		7.5		8.5		10		15	ns
t_{EA}		4.5		5.0		5.6		9.0		10	ns
t_{ER}		4.5		5.0		5.3		9.0		10	ns
t_{PRR}	6.0		6.0		6.0		8.0		10		ns
t_{PRO}	9.5		10		10.5		13		15		ns
t_{PRW}	3.3		3.6		4.0		6.0		7.0		ns
Synchronous Clocking Parameters											
t_{MCS}	2.7		3.0		3.5		5.0		6.7		ns
t_{MCH}	0		0		0		0		0		ns
t_{MCCO}		5.8		6.0		7.0		10		12	ns
t_{IOS}	1.0		1.0		1.2		2.0		2.5		ns
t_{IOH}	0.9		1.0		1.2		2.0		2.5		ns
t_{IOCO}		3.8		4.0		4.5		7.0		8.0	ns
t_{SCS}	3.4		3.5		3.6		6.4		9.6		ns
t_{SCS2}	4.3		4.5		5.5		8.0		12		ns
t_{ICS}	4.5		5.0		5.5		8.0		12		ns
t_{OCS}	4.5		5.0		5.5		8.0		12		ns
t_{CHZ}		3.5		3.5		3.8		6.0		7.0	ns
t_{CLZ}	1.5		1.5		1.5		1.5		1.5		ns
f_{MAX}		294		286		278		156		104	MHz
f_{MAX2}		233		222		181		125		83	MHz
Product Term Clocking Parameters											
t_{MCSPT}	2.7		3.0		3.3		5.0		6.0		ns
t_{MCHPT}	0.9		1.0		1.4		2.0		2.5		ns
t_{MCCOPT}		7.5		8.0		8.8		11.0		15.0	ns
t_{SCS2PT}	6.0		6.5		7.2		10.0		15.0		ns
Channel Interconnect Parameters											
t_{CHSW}		0.9		1.0		1.2		1.7		2.0	ns
t_{CL2CL}		1.8		2.0		2.3		2.8		3.0	ns
Miscellaneous Parameters											
t_{CPLD}		2.8		3.0		3.3		4.0		5.0	ns
t_{MCCD}		0.22		0.25		0.28		0.35		0.38	ns
PLL Parameters											
t_{MCCJ}	–150	150	–150	150	–150	150	–180	180	–200	200	ps
t_{DWSA}	–1.35	–0.85	–1.35	–0.85	–1.35	–0.85	–2.0	–1.5	–2.9	–2.4	ns
t_{DWOSA}	–150	150	–150	150	–150	150	–180	180	–200	200	ps
t_{LOCK}		250		250		250		250		250	ms

Switching Characteristics—Parameter Values Over the Operating Range (continued)

Parameter	233		200		181		125		83		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{INDUTY}	40	60	40	60	40	60	40	60	40	60	%
f_{PLLO}[14]	6.2	266	6.2	266	6.2	266	6.2	200	6.2	200	MHz
f_{PLLI}[14]	12.5	133	12.5	133	12.5	133	12.5	100	12.5	100	MHz
f_{PLLVCO}	100	266	100	266	100	266	100	266	100	266	MHz
P_{SAPLLI}	–0.3	+0.3	–0.3	+0.3	–0.3	+0.3	–0.3	+0.3	–0.3	+0.3	%
f_{MPLLI}		50		50		50		50		50	KHz
JTAG Parameters											
t_{JCKH}	25		25		25		25		25		ns
t_{JCKL}	25		25		25		25		25		ns
t_{JCP}	50		50		50		50		50		ns
t_{JSU}	10		10		10		10		10		ns
t_{JH}	10		10		10		10		10		ns
t_{JCO}		20		20		20		20		20	ns
t_{JXZ}		20		20		20		20		20	ns
t_{JZX}		20		20		20		20		20	ns

Input and Output Standard Timing Delay Adjustments

All the timing specifications in this data sheet are specified based on LVCMOS compliant inputs and outputs (fast slew rates).[15] Apply following adjustments if the inputs and outputs are configured to operate at other standards.

I/O Standard	Output Delay Adjustments						Input Delay Adjustments		
	Fast Slew Rate			Slow Slew Rate (additional delay to fast slew rate)					
	t_{IOD}	t_{EA}	t_{ER}	$t_{IODSLOW}$	t_{EASLOW}	t_{ERSLOW}	t_{IOIN}	t_{CKIN}	$t_{IOREGPIN}$
LVTTL – 2 mA	2.75	0	0	2.6	2.0	2.0	0	0	0
LVTTL – 4 mA	1.8	0	0	2.5	2.0	2.0	0	0	0
LVTTL – 6 mA	1.8	0	0	2.5	2.0	2.0	0	0	0
LVTTL – 8 mA	1.2	0	0	2.4	2.0	2.0	0	0	0
LVTTL – 12 mA	0.6	0	0	2.3	2.0	2.0	0	0	0
LVTTL – 16 mA	0.16	0	0	2.0	2.0	2.0	0	0	0
LVTTL – 24 mA	0	0	0	1.6	2.0	2.0	0	0	0
LVCMOS	0	0	0	2.0	2.0	2.0	0	0	0
LVCMOS3	0.14	0.05	0	2.0	2.0	2.0	0.1	0.1	0.2
LVCMOS2	0.41	0.1	0	2.0	2.0	2.0	0.2	0.2	0.4
LVCMOS18	1.6	0.7	0.1	2.1	2.0	2.0	0.5	0.4	0.3
3.3V PCI	–0.14	0	0	2.0	2.0	2.0	0	0	0
GTL+	0.02[16]	0.6[16]	0.9[16]	2.0	2.0	2.0	0.5	0.4	0.2
SSTL3 I	–0.15	0.3	0.1	2.0	2.0	2.0	0.5	0.3	0.3
SSTL3 II	–0.4	0.2	0	2.0	2.0	2.0	0.5	0.3	0.3

Notes:

14. Refer to page 11 and the application note titled *"Delta39K PLL and Clock Tree"* for details on the PLL operation.
15. For "slow slew rate" output delay adjustments, refer to *Warp* software's static timing analyzer results.
16. These delays are based on falling edge output. The rising edge delay depends on the size of pull-up resistor and termination voltage.

I/O Standard	Output Delay Adjustments						Input Delay Adjustments		
	Fast Slew Rate			Slow Slew Rate (additional delay to fast slew rate)					
	t_{IOD}	t_{EA}	t_{ER}	$t_{IODSLOW}$	t_{EASLOW}	t_{ERSLOW}	t_{IOIN}	t_{CKIN}	$t_{IOREGPIN}$
SSTL2 I	–0.02	0.4	0	2.0	2.0	2.0	0.9	0.5	0.6
SSTL2 II	–0.22	0.2	0	2.0	2.0	2.0	0.9	0.5	0.6
HSTL I	0.94	0.9	0.5	2.0	2.0	2.0	0.5	0.5	0.3
HSTL II	0.79	0.8	0.5	2.0	2.0	2.0	0.5	0.5	0.3
HSTL III	0.77	0.5	0.1	2.0	2.0	2.0	0.5	0.5	0.3
HSTL IV	0.44	0.6	0	2.0	2.0	2.0	0.5	0.5	0.3

Cluster Memory Timing Parameter Values Over the Operating Range

Parameter	233		200		181		125		83		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Asynchronous Mode Parameters											
t_{CLMAA}		10.2		11		12		17		20	ns
t_{CLMPWE}	5.5		6		6.5		10		12		ns
t_{CLMSA}	1.8		2.0		2.2		3.2		4.0		ns
t_{CLMHA}	0.9		1.0		1.1		1.8		2.0		ns
t_{CLMSD}	5.5		6.0		6.5		10		12		ns
t_{CLMHD}	0.4		0.5		0.6		0.9		1.0		ns
Synchronous Mode Parameters											
$t_{CLMCYC1}$	9.5		10		10.5		15		20		ns
$t_{CLMCYC2}$	5.0		5.0		5.5		8.0		10.0		ns
t_{CLMS}	2.8		3.0		3.8		4.0		5.0		ns
t_{CLMH}	0		0		0		0		0		ns
t_{CLMDV1}		10		11		12		17		20	ns
t_{CLMDV2}		7.0		7.5		8.0		10		15	ns
$t_{CLMMACS1}$	7.7		8.0		8.5		12		15		ns
$t_{CLMMACS2}$	4.5		5.0		5.5		8.0		10		ns
$t_{MACCLMS1}$	3.6		4.0		4.4		6.6		8.0		ns
$t_{MACCLMS2}$	6.0		6.5		7.0		10		12		ns
Internal Parameters											
$t_{CLMCLAA}$	6		6		6.5		10		12		ns

Channel Memory Timing Parameter Values Over the Operating Range

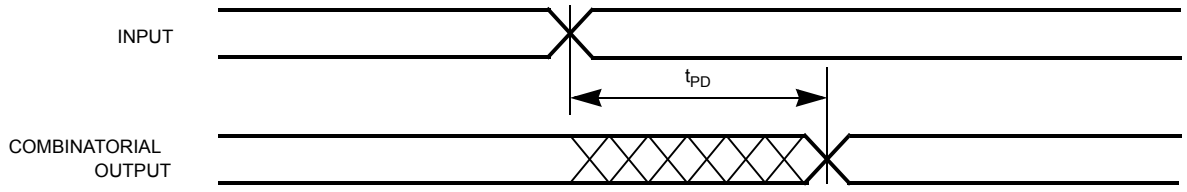
Parameter	233		200		181		125		83		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dual-Port Asynchronous Mode Parameters											
t_{CHMAA}		10		11		12		17		20	ns
t_{CHMPWE}	5.5		6.0		6.5		10		12		ns
t_{CHMSA}	1.8		2.0		2.2		3.2		4.0		ns
t_{CHMHA}	0.9		1.0		1.1		1.8		2.0		ns
t_{CHMSD}	5.5		6.0		6.5		10		12		ns
t_{CHMHD}	0.4		0.5		0.6		0.9		1.0		ns
t_{CHMBA}		8.5		9.0		10.0		14.0		16.0	ns

Channel Memory Timing Parameter Values Over the Operating Range (continued)

Dual-Port Synchronous Mode Parameters											
$t_{CHMCYC1}$	9.5		10		10		15		20		ns
$t_{CHMCYC2}$	5.0		5.3		5.4		7.4		10.6		ns
t_{CHMS}	3.0		3.3		3.9		5.0		6.0		ns
t_{CHMH}	0		0		0		0		0		ns
t_{CHMDV1}		10		11		12		17		20	ns
t_{CHMDV2}		7.0		7.5		8.0		10		15	ns
t_{CHMBDV}		8.5		9.0		10.0		14.0		16.0	ns
$t_{CHMMACS1}$	8.5		9.0		10.0		14.0		16.0		ns
$t_{CHMMACS2}$	4.8		5.0		5.5		8.0		10		ns
$t_{MACCHMS1}$	4.6		5.0		5.4		7.6		9.0		ns
$t_{MACCHMS2}$	7.3		7.3		7.7		10.0		13.0		ns
Synchronous FIFO Data Parameters											
t_{CHMCLK}	4.8		5.0		5.4		7.4		10.6		ns
t_{CHMFS}	3.7		4.0		4.3		6.0		7.0		ns
t_{CHMFH}	0		0		0		0		0		ns
$t_{CHMFRDV}$		6.5		7.0		7.5		10.0		13.0	
$t_{CHMMACS}$	4.6		5.0		5.4		7.4		10.6		ns
$t_{MACCHMS}$	4.7		5.0		5.4		7.4		10.6		ns
Synchronous FIFO Flag Parameters											
t_{CHMFO}		10.5		11		11.5		15		20	ns
$t_{CHMMACF}$	8.5		9		9.5		13		17		ns
t_{CHMFRS}	4.5		5.0		5.5		8.0		10		ns
$t_{CHMFRSR}$		3.6		4.0		4.4		6.6		8.0	ns
$t_{CHMFRSF}$		9.5		10.0		11.0		15.0		18.0	ns
$t_{CHMSKEW1}$		1.8		2.0		2.2		3.2		4.0	ns
$t_{CHMSKEW2}$		1.8		2.0		2.2		3.2		4.0	ns
$t_{CHMSKEW3}$		4.6		5.0		5.4		7.4		10.6	ns
Internal Parameters											
$t_{CHMCHAA}$	6.5		7.0		7.5		10.0		13.0		ns

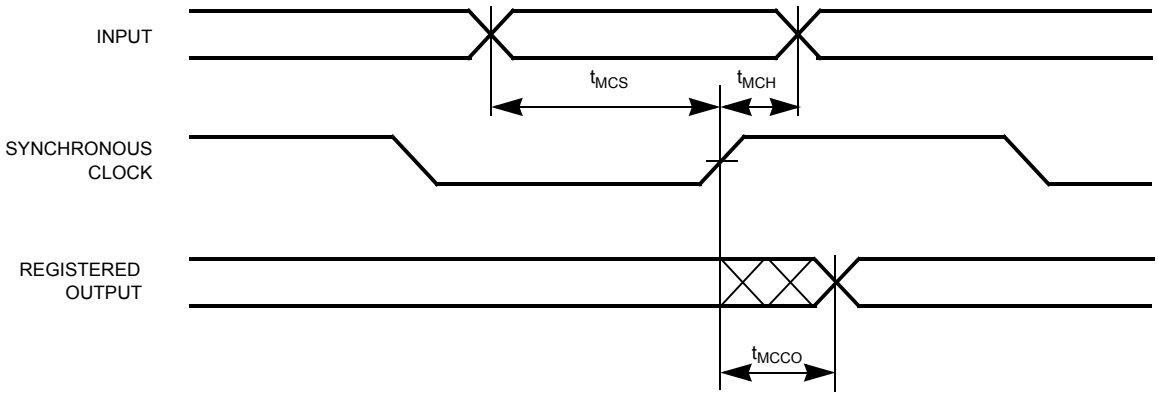
Switching Waveforms

Combinatorial Output

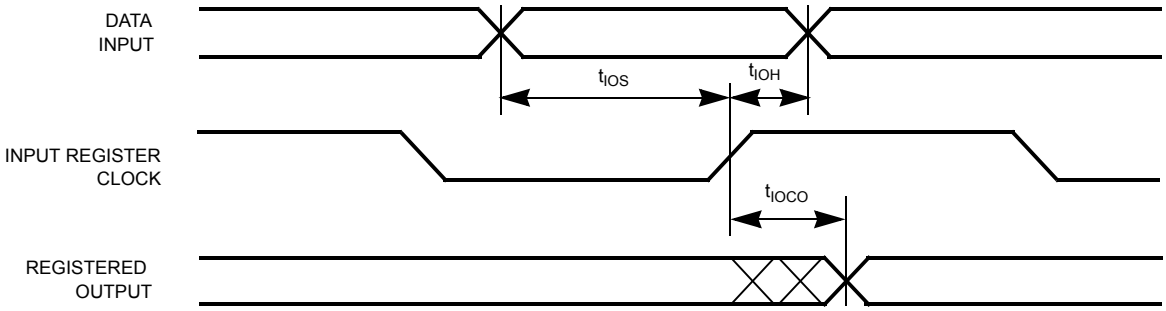


Switching Waveforms (continued)

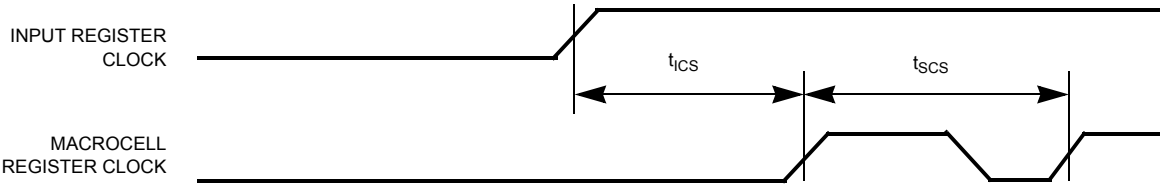
Registered Output with Synchronous Clocking (Macrocell)



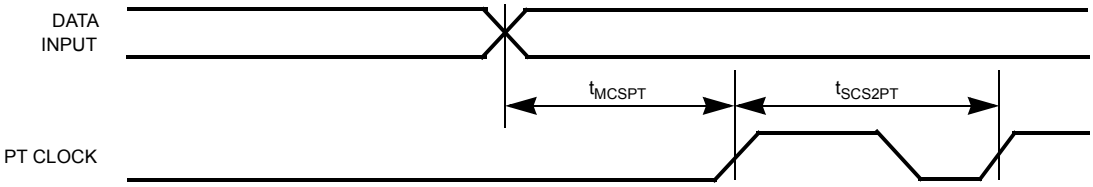
Registered Input in I/O Cell



Clock to Clock

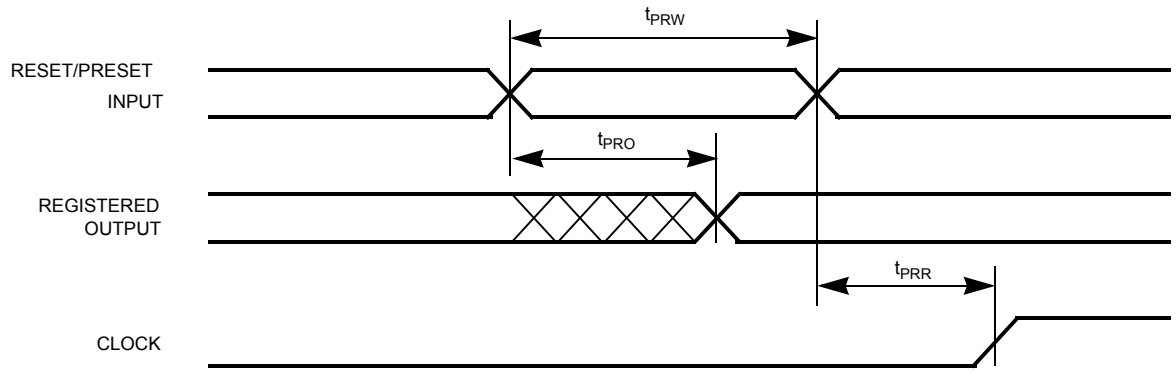


PT Clock to PT Clock

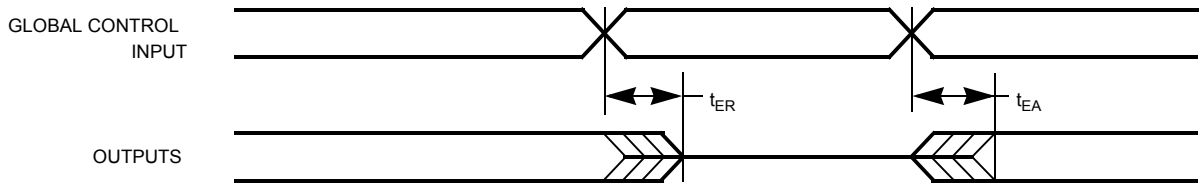


Switching Waveforms (continued)

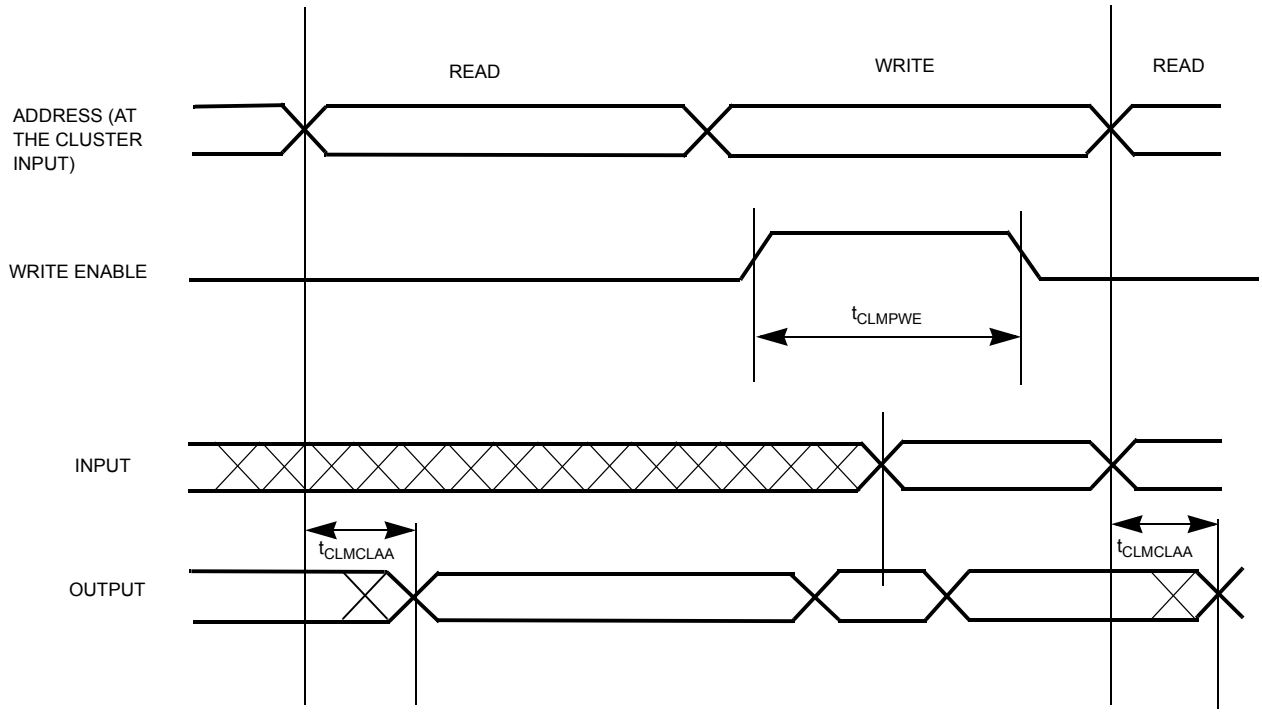
Asynchronous Reset/Preset



Output Enable/Disable

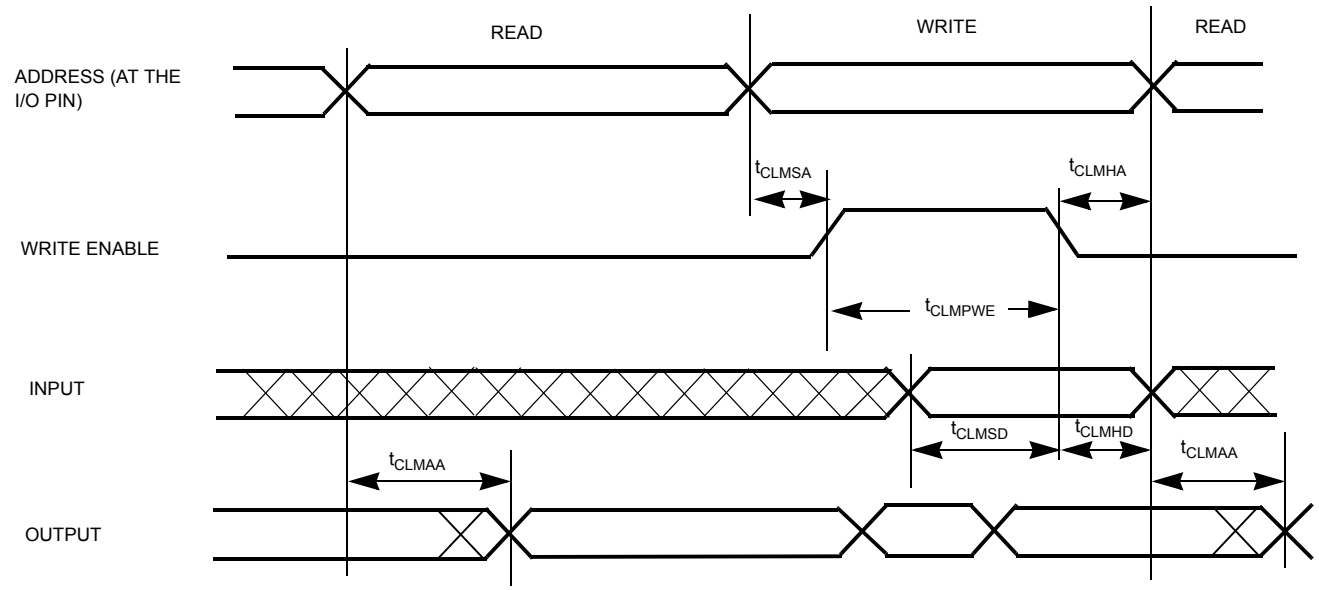


Cluster Memory Asynchronous Timing

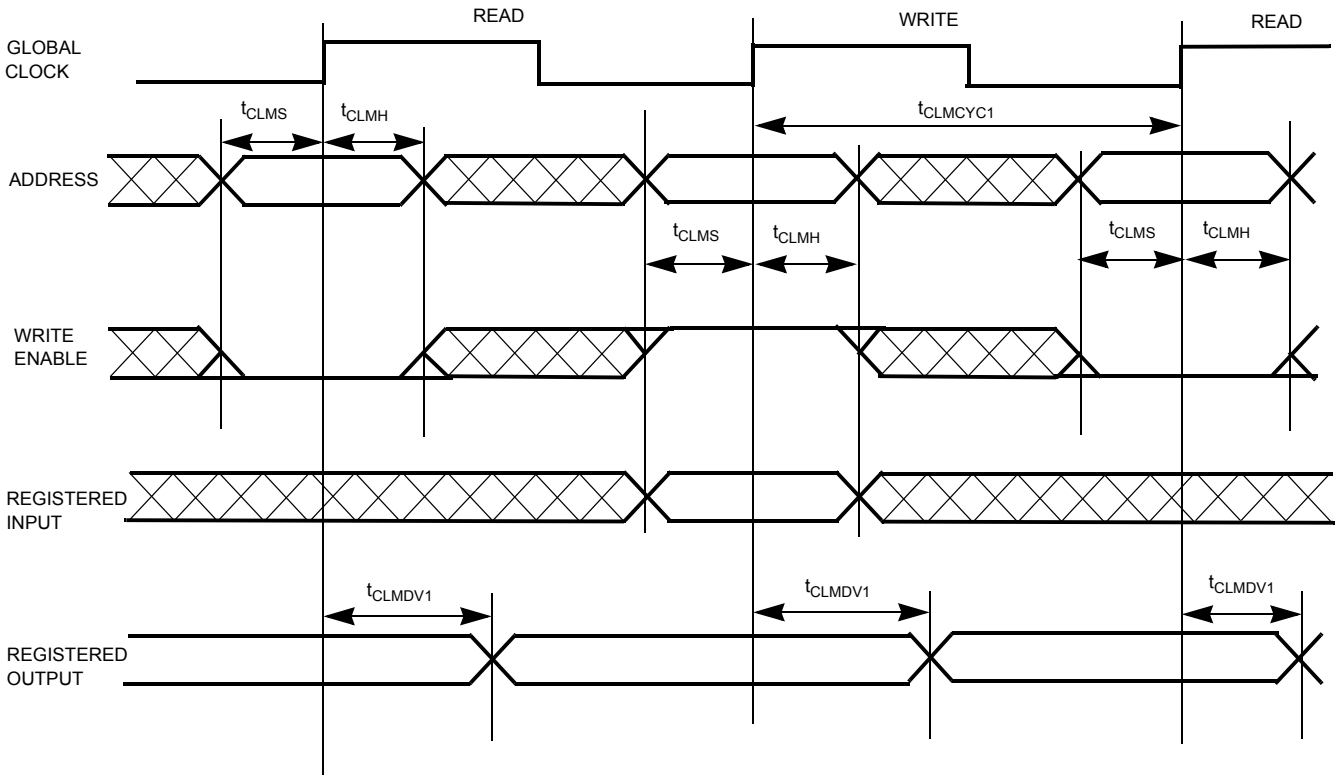


Switching Waveforms (continued)

Cluster Memory Asynchronous Timing 2

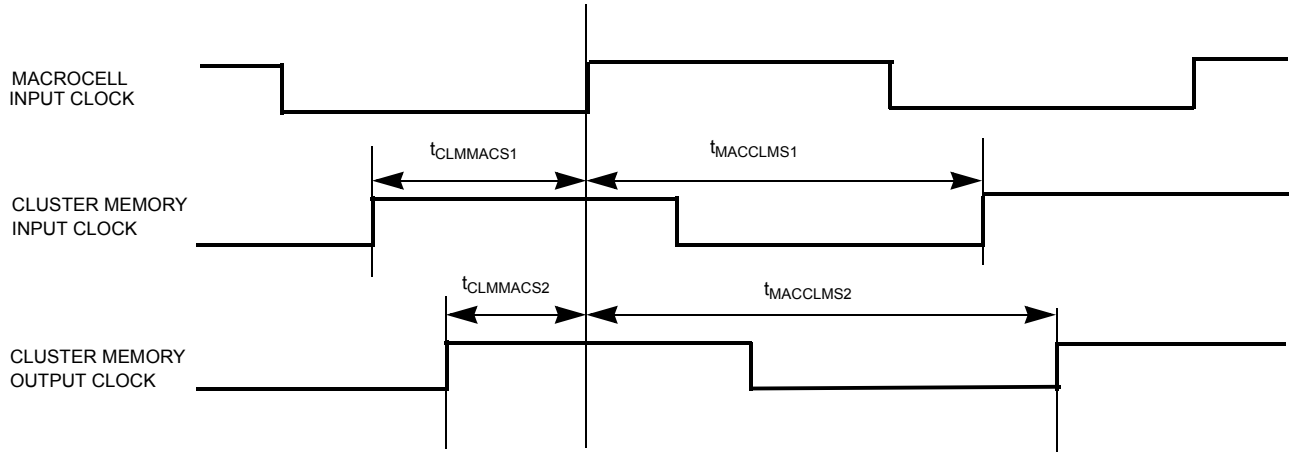


Cluster Memory Synchronous Flow-Through Timing

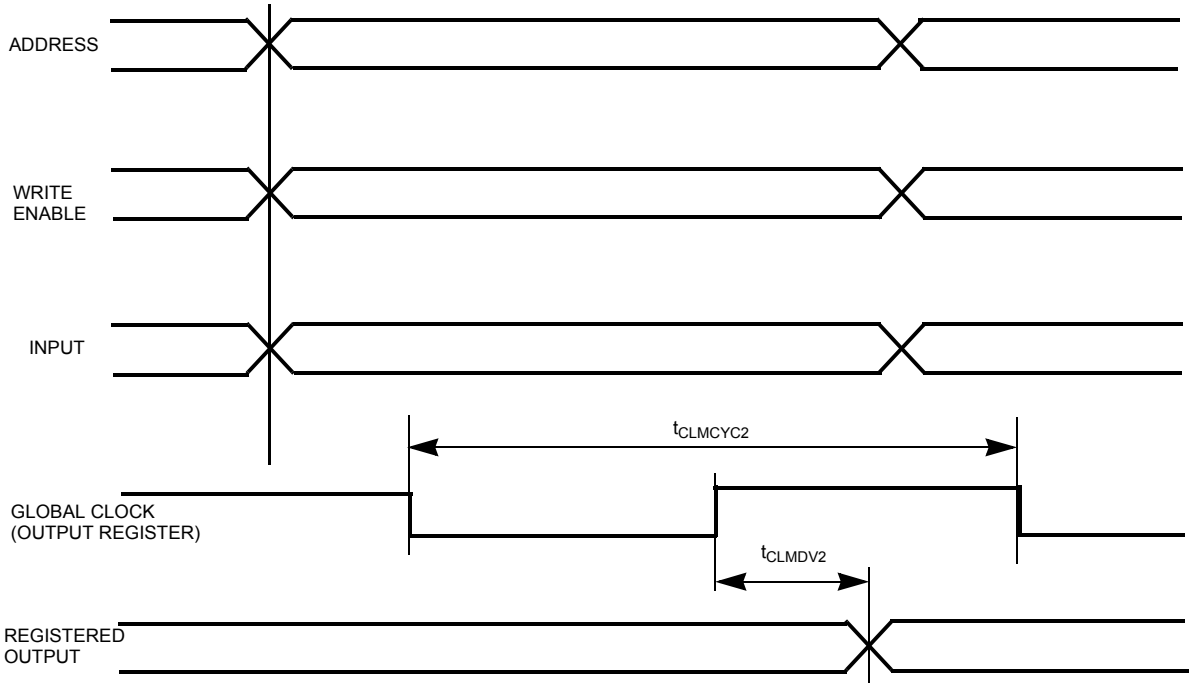


Switching Waveforms (continued)

Cluster Memory Internal Clocking

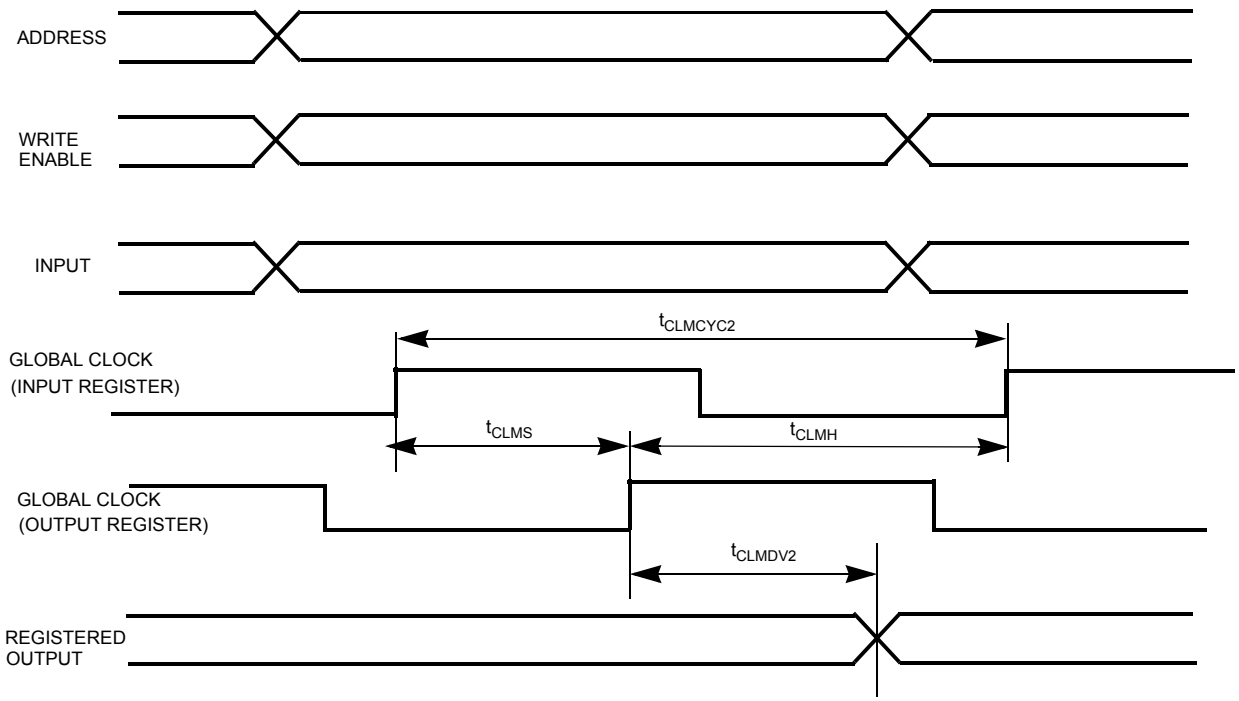


Cluster Memory Output Register Timing (Asynchronous Inputs)

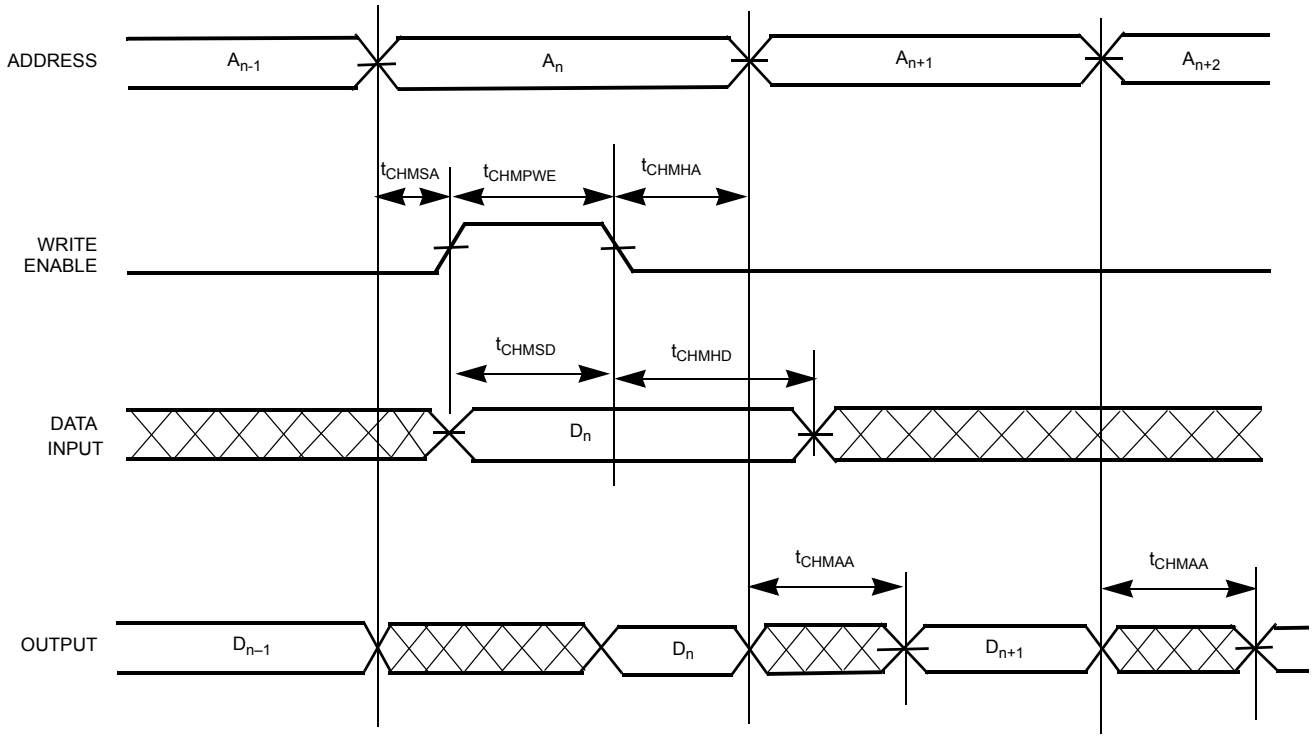


Switching Waveforms (continued)

Cluster Memory Output Register Timing (Synchronous Inputs)

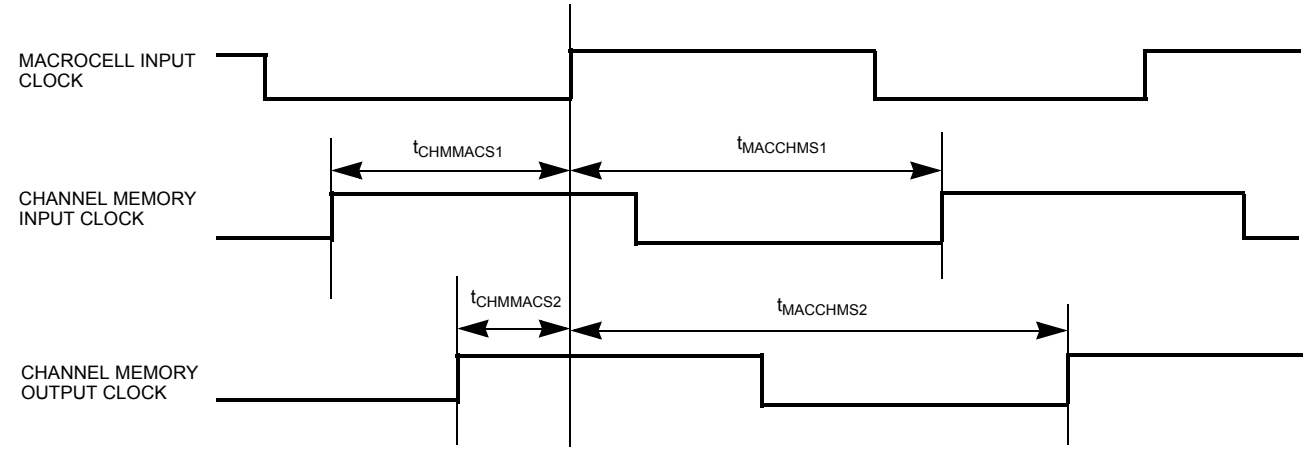


Channel Memory DP Asynchronous Timing

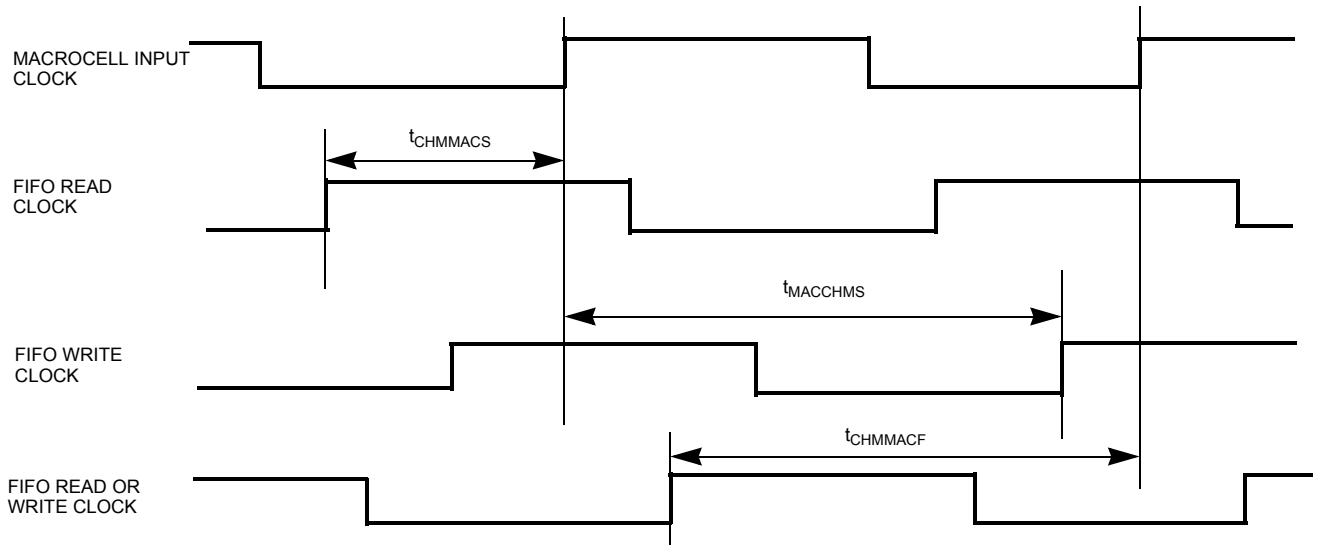


Switching Waveforms (continued)

Channel Memory Internal Clocking

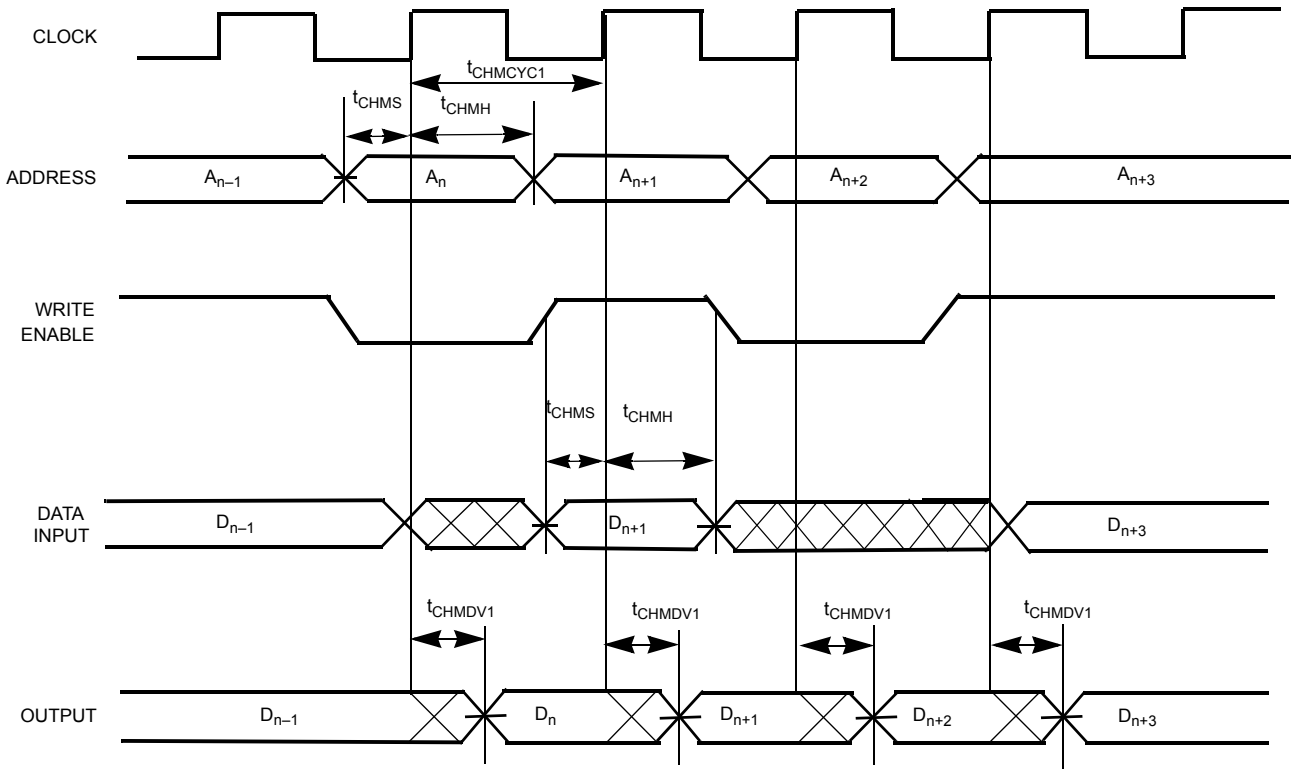


Channel Memory Internal Clocking 2

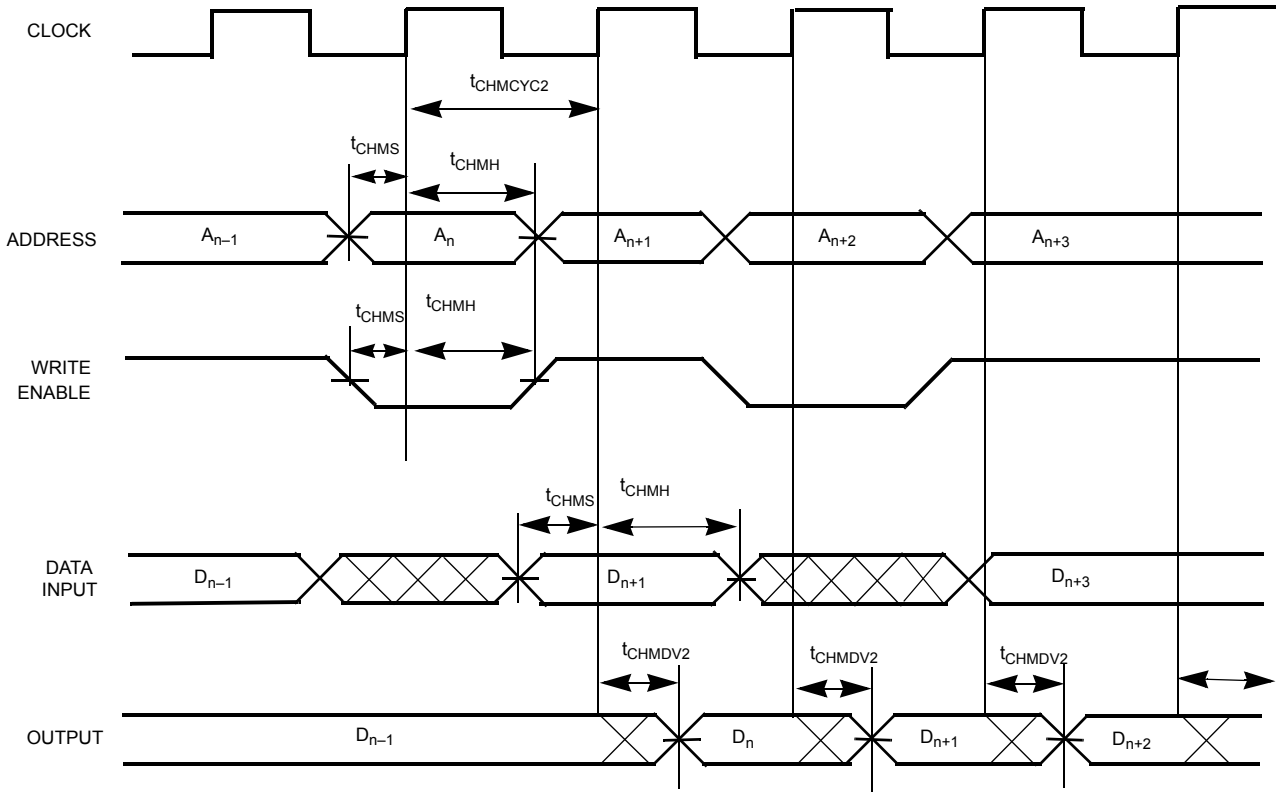


Switching Waveforms (continued)

Channel Memory DP SRAM Flow-Through R/W Timing

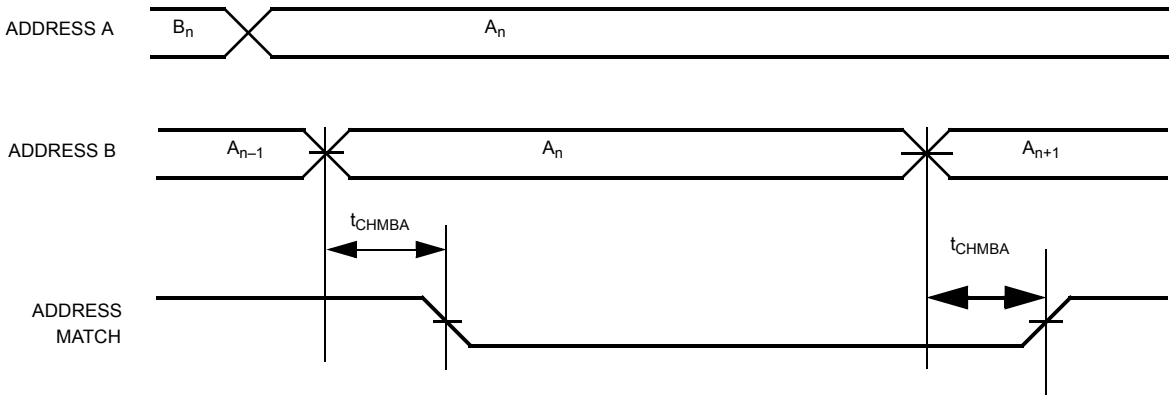


Channel Memory DP SRAM Pipeline R/W Timing

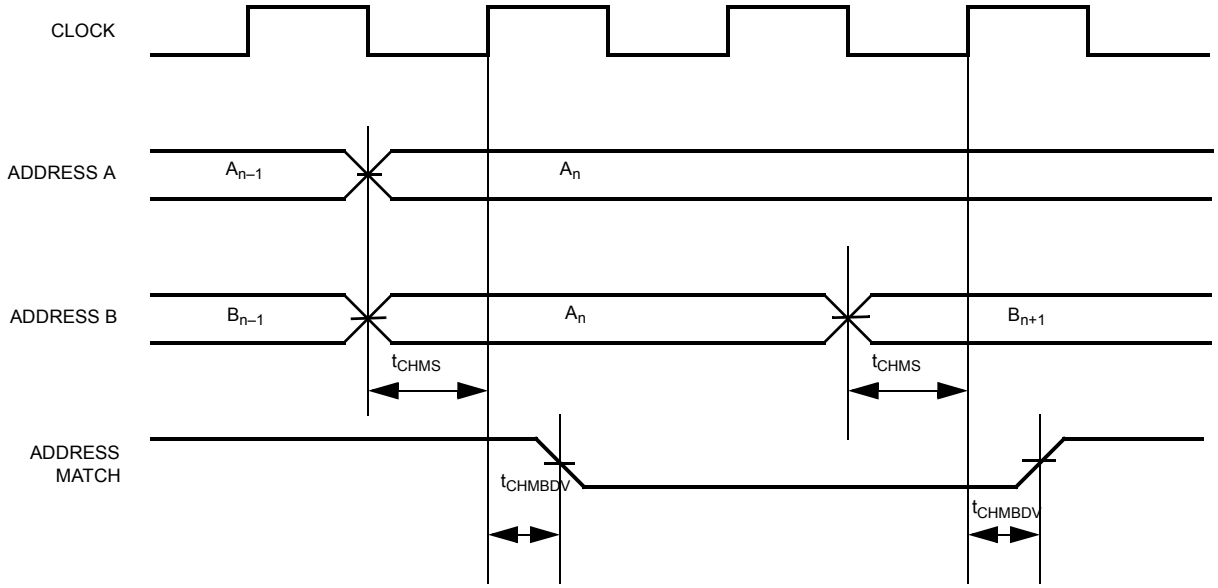


Switching Waveforms (continued)

Dual-Port Asynchronous Address Match Busy Signal

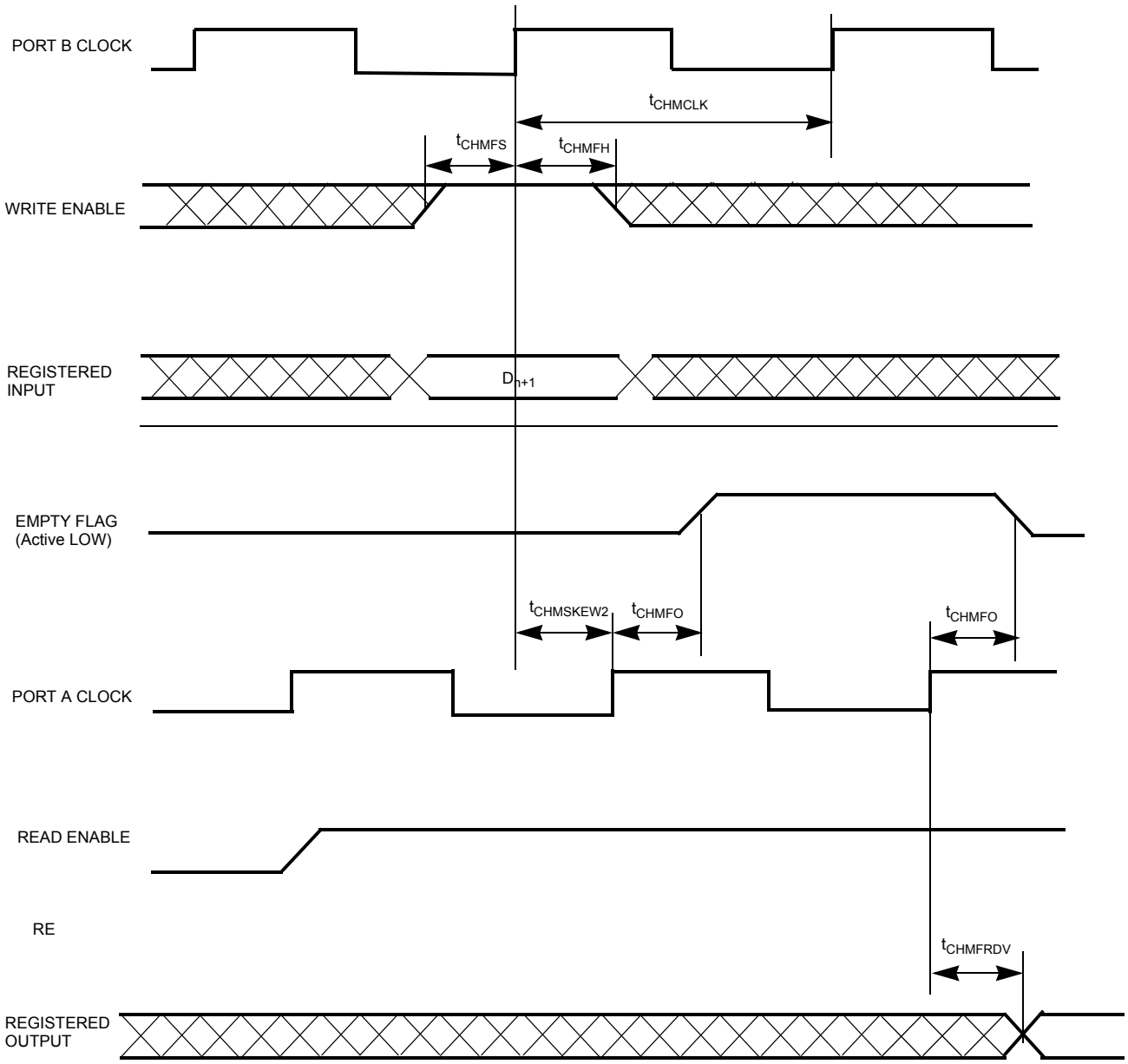


Dual-Port Synchronous Address Match Busy Signal



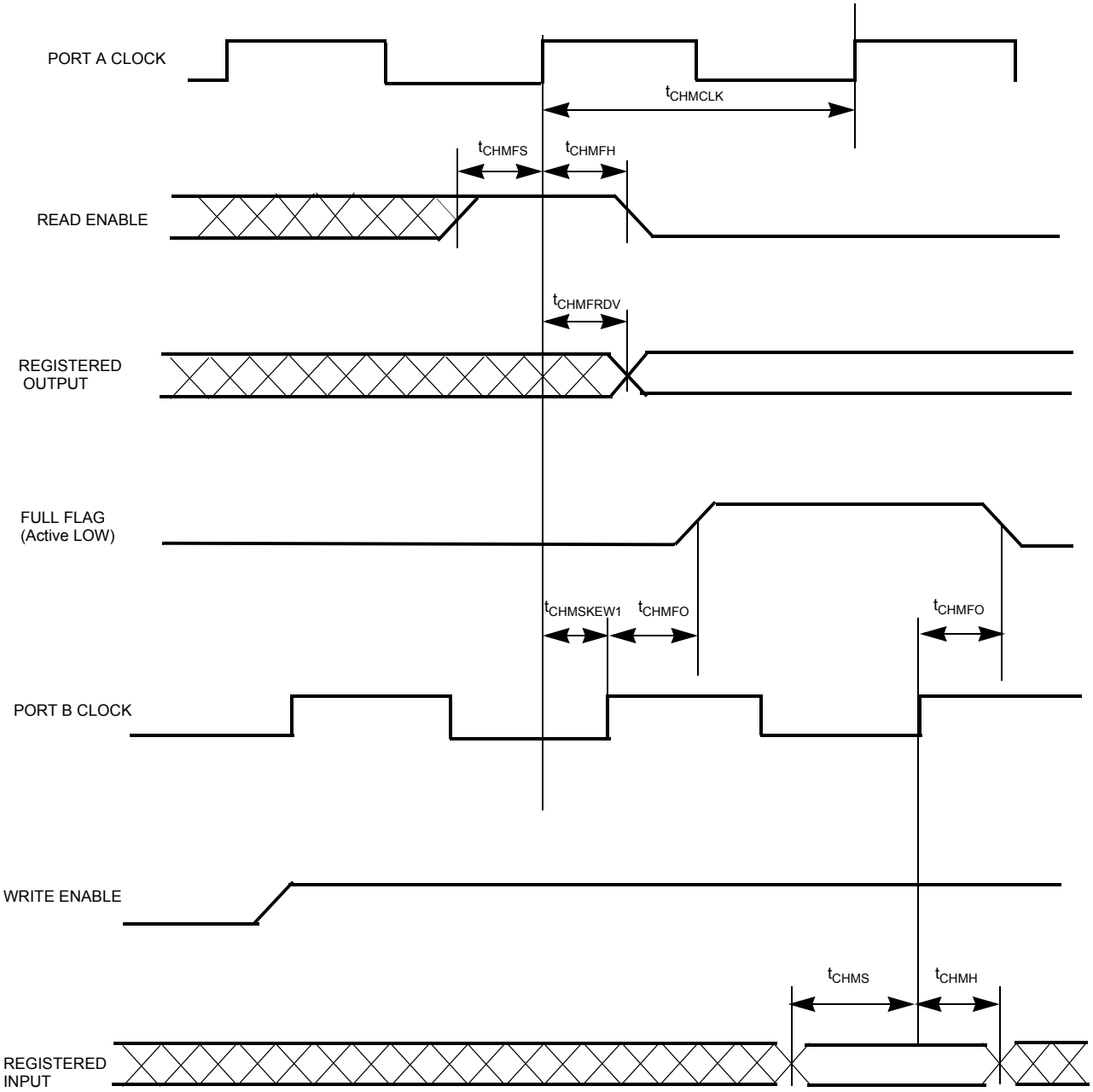
Switching Waveforms (continued)

Channel Memory Synchronous FIFO Empty/Write Timing



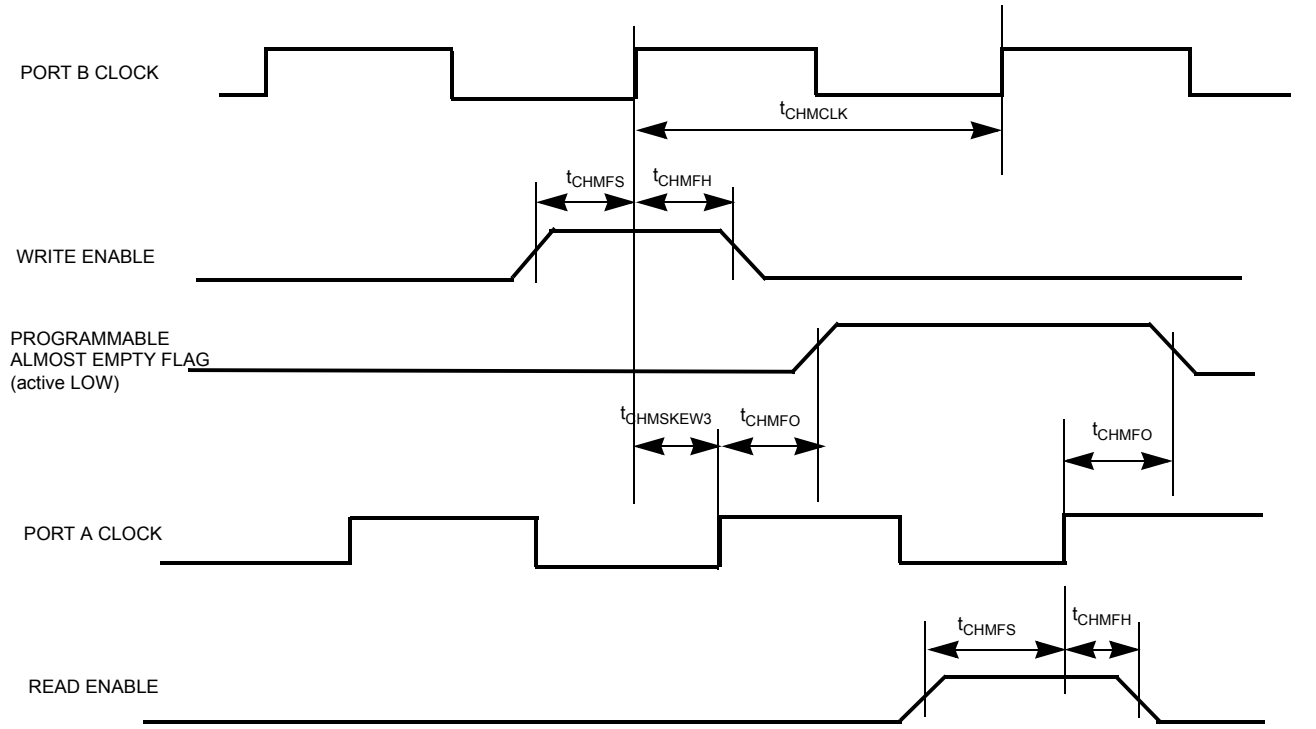
Switching Waveforms (continued)

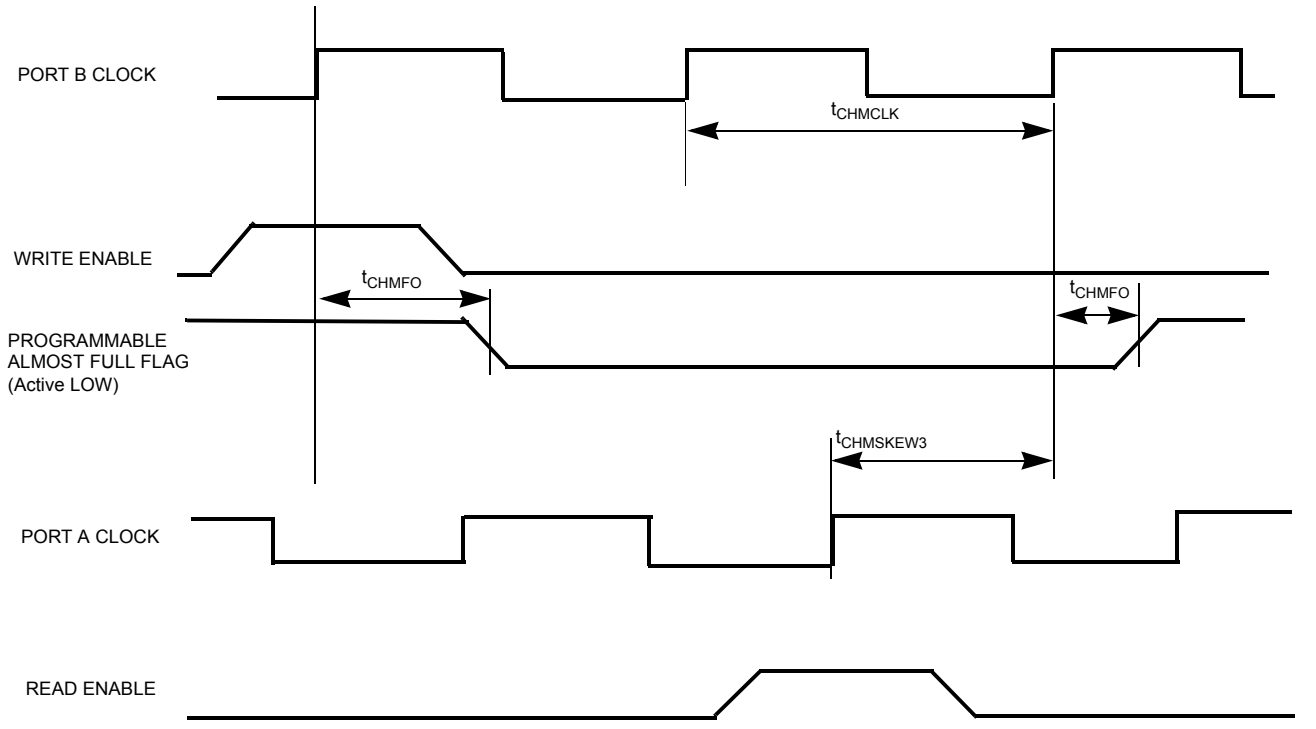
Channel Memory Synchronous FIFO Full/Read Timing



Switching Waveforms (continued)

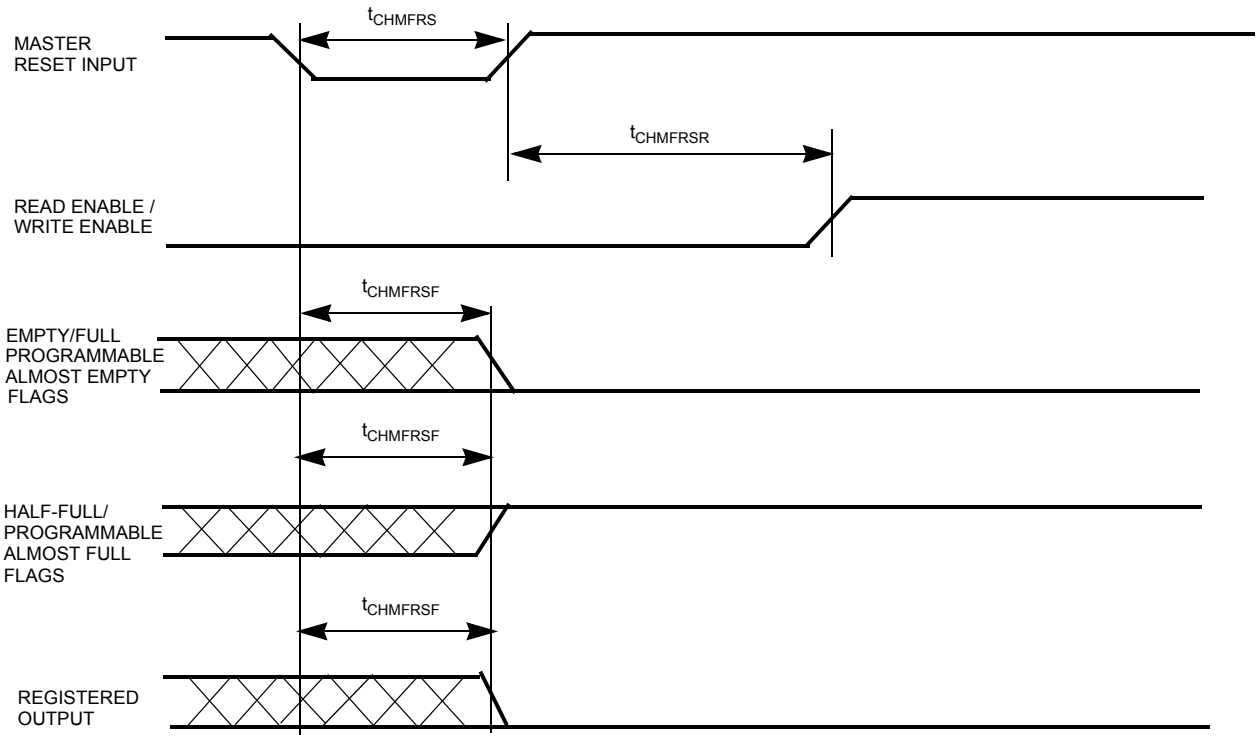
Channel Memory Synchronous FIFO Programmable Flag Timing





Switching Waveforms (continued)

Channel Memory Synchronous FIFO Master Reset Timing



CY 39 050 V 208 - 125 NT X C

Cypress Semiconductor ID

Family Type
39 = Delta39K Family

Gate Density
30=30k Usable Gates 100=100k Usable Gates
50=50k Usable Gates 200=200k Usable Gates

Operating Reference Voltage
V = 3.3V or 2.5V Supply Voltage
Z = 1.8V Supply Voltage

Pin Count
208 = 208 Leads 484 = 484 Balls
256 = 256 Balls 676 = 676 Balls
388 = 388 Balls

Opearting Conditions
Commercial 0 ° C to +70 ° C
Industrial -40 ° C to +85 ° C

Lead Free
X Lead (Pb) Free

Package Type
A = Thin Quad Flat Pack (TQFP)
U = Ceramic Quad Flat Pack (CQFP)
N = Plastic Quad Flat Pack (PQFP)
NT = Thermally Enhanced Plastic Quad Flat Pack (EQFP)
J = Plastic Leaded Chip Carrier (PLCC)
Y = Ceramic Leaded Chip Carier (CLCC)
BG = Plastic Ball Grid Array (PBGA)
BA = Fine-Pitch Ball Grid Array (FBGA) 0.8mm Lead Pitch
BB = Fine-Pitch Ball Grid Array (FBGA) 1.0mm Lead Pitch

Speed
66 = 66MHz 143 = 143MHz
83 = 83MHz 154 = 154 MHz
100 = 100MHz 167 = 167MHz

Delta39K Part Numbers (Ordering Information)

Device	Speed (MHz)	Ordering Code	Package Name	Package Type	Self-Boot Solution	Operating Range
39K30	233	CY39030V208-233NTC	NT208	208-Lead Enhanced Quad Flat Pack		Commercial
		CY39030V208-233NTXC	NT208	208-Lead Lead-Free Enhanced Quad Flat Pack		
		CY39030V256-233BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39030V256-233MBC	MB256	256-Lead Fine Pitch Ball Grid Array	√	
	125	CY39030V208-125NTC	NT208	208-Lead Enhanced Quad Flat Pack		
		CY39030V208-125NTXC	NT208	208-Lead Lead-Free Enhanced Quad Flat Pack		
		CY39030V256-125BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39030V256-125MBC	MB256	256-Lead Fine Pitch Ball Grid Array	√	
		CY39030V208-125NTI	NT208	208-Lead Enhanced Quad Flat Pack		Industrial
		CY39030V208-125NTXI	NT208	208-Lead Lead-Free Enhanced Quad Flat PaCK		
		CY39030V256-125BBI	BB256	256-Lead Fine Pitch Ball Grid Array		
	83	CY39030V208-83NTC	NT208	208-Lead Enhanced Quad Flat Pack		Commercial
		CY39030V208-83NTXC	NT208	208-Lead Lead-Free Enhanced Quad Flat Pack		
		CY39030V256-83BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39030V256-83MBC	MB256	256-Lead Fine Pitch Ball Grid Array	√	
		CY39030V208-83NTI	NT208	208-Lead Enhanced Quad Flat Pack		Industrial
		CY39030V208-83NTXI	NT208	208-Lead Lead-Free Enhanced Quad Flat Pack		
		CY39030V256-83BBI	BB256	256-Lead Fine Pitch Ball Grid Array		
39K50	233	CY39050V208-233NTC	NT208	208-Lead Enhanced Quad Flat Pack		Commercial
		CY39050V208-233NTXC	NT208	208-Lead Lead-Free Enhanced Quad Flat Pack		
		CY39050V256-233BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39050V388-233MGC	MG388	388-Lead Ball Grid Array	√	
		CY39050V484-233MBC	MB484	484-Lead Fine Pitch Ball Grid Array	√	
	125	CY39050V208-125NTC	NT208	208-Lead Enhanced Quad Flat Pack		
		CY39050V208-125NTXC	NT208	208-Lead Lead-Free Enhanced Quad Flat Pack		
		CY39050V256-125BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39050V388-125MGC	MG388	388-Lead Pitch Ball Grid Array	√	
		CY39050V484-125MBC	MB484	484-Lead Fine Pitch Ball Grid Array	√	

Delta39K Part Numbers (Ordering Information) (continued)

Device	Speed (MHz)	Ordering Code	Package Name	Package Type	Self-Boot Solution	Operating Range
39K50	125	CY39050V208-125NTI	NT208	208-Lead Enhanced Quad Flat Pack		Industrial
		CY39050V208-125NTXI	NT208	208-Lead Lead-Free Enhanced Quad Flat Pack		
		CY39050V256-125BBI	BB256	256-Lead Fine Pitch Ball Grid Array		
	83	CY39050V208-83NTC	NT208	208-Lead Enhanced Quad Flat Pack		Commercial
		CY39050V208-83NTXC	NT208	208-Lead Lead-Free Enhanced Quad Flat Pack		
		CY39050V256-83BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39050V388-83MGC	MG388	388-Lead Ball Grid Array	√	
		CY39050V484-83MBC	MB484	484-Lead Fine Pitch Ball Grid Array	√	
		CY39050V208-83NTI	NT208	208-Lead Enhanced Quad Flat Pack		Industrial
		CY39050V208-83NTXI	NT208	208-Lead Lead-Free Enhanced Quad Flat Pack		
		CY39050V256-83BBI	BB256	256-Lead Fine Pitch Ball Grid Array		
39K100	200	CY39100V208B-200NTC	NT208	208-Lead Enhanced Quad Flat Pack		Commercial
		CY39100V208B-200NTXC	NT208	208-Lead Lead-Free Enhanced Quad Flat Pack		
		CY39100V256B-200BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39100V484B-200BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39100V388B-200MGC	MG388	388-Lead Ball Grid Array	√	
		CY39100V676B-200MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
39K100	125	CY39100V208B-125NTC	NT208	208-Lead Enhanced Quad Flat Pack		Commercial
		CY39100V208B-125NTXC	NT208	208-Lead Lead-Free Enhanced Quad Flat Pack		
		CY39100V256B-125BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39100V484B-125BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39100V388B-125MGC	MG388	388-Lead Ball Grid Array	√	
		CY39100V676B-125MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39100V208B-125NTI	NT208	208-Lead Enhanced Quad Flat Pack		Industrial
		CY39100V256B-125BBI	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39100V484B-125BBI	BB484	484-Lead Fine Pitch Ball Grid Array		
	83	CY39100V208B-83NTC	NT208	208-Lead Enhanced Quad Flat Pack		Commercial
		CY39100V208B-83NTXC	NT208	208-Lead Lead-Free Enhanced Quad Flat Pack		
		CY39100V256B-83BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39100V484B-83BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39100V388B-83MGC	MG388	388-Lead Ball Grid Array	√	
		CY39100V676B-83MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39100V208B-83NTI	NT208	208-Lead Enhanced Quad Flat Pack		Industrial
		CY39100V256B-83BBI	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39100V484B-83BBI	BB484	484-Lead Fine Pitch Ball Grid Array		

Delta39K Part Numbers (Ordering Information) (continued)

Device	Speed (MHz)	Ordering Code	Package Name	Package Type	Self-Boot Solution	Operating Range
39K200	181	CY39200V208-181NTC	NT208	208-Lead Enhanced Quad Flat Pack		Commercial
		CY39200V208-181NTXC	NT208	208-Lead Lead-Free Enhanced Quad Flat Pack		
		CY39200V484-181BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39200V388-181MGC	MG388	388-Lead Ball Grid Array	√	
		CY39200V676-181MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
	125	CY39200V208-125NTC	NT208	208-Lead Enhanced Quad Flat Pack		Commercial
		CY39200V208-125NTXC	NT208	208-Lead Lead-Free Enhanced Quad Flat Pack		
		CY39200V484-125BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39200V388-125MGC	MG388	388-Lead Ball Grid Array	√	
		CY39200V676-125MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39200V208-125NTI	NT208	208-Lead Enhanced Quad Flat Pack		Industrial
		CY39200V484-125BBI	BB484	484-Lead Fine Pitch Ball Grid Array		
	83	CY39200V208-83NTC	NT208	208-Lead Enhanced Quad Flat Pack		Commercial
		CY39200V208-83NTXC	NT208	208-Lead Lead-Free Enhanced Quad Flat Pack		
		CY39200V484-83BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39200V388-83MGC	MG388	388-Lead Ball Grid Array	√	
		CY39200V676-83MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39200V208-83NTI	NT208	208-Lead Enhanced Quad Flat Pack		Industrial
		CY39200V484-83BBI	BB484	484-Lead Fine Pitch Ball Grid Array		

CPLD Boot EEPROM[17] Part Numbers (Ordering Information)

Device	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
2 Mbit	15	AT17LV002-10JC	20J	20-Lead Plastic Leaded Chip Carrier	Commercial
	10	AT17LV002-10JC	20J	20-Lead Plastic Leaded Chip Carrier	Industrial
1 Mbit	15	AT17LV010-10JC	20J	20-Lead Plastic Leaded Chip Carrier	Commercial
	10	AT17LV010-10JI	20J	20-Lead Plastic Leaded Chip Carrier	Industrial
512 Kbit	15	AT17LV512-10JC	20J	20-Lead Plastic Leaded Chip Carrier	Commercial
	10	AT17LV512-10JI	20J	20-Lead Plastic Leaded Chip Carrier	Industrial

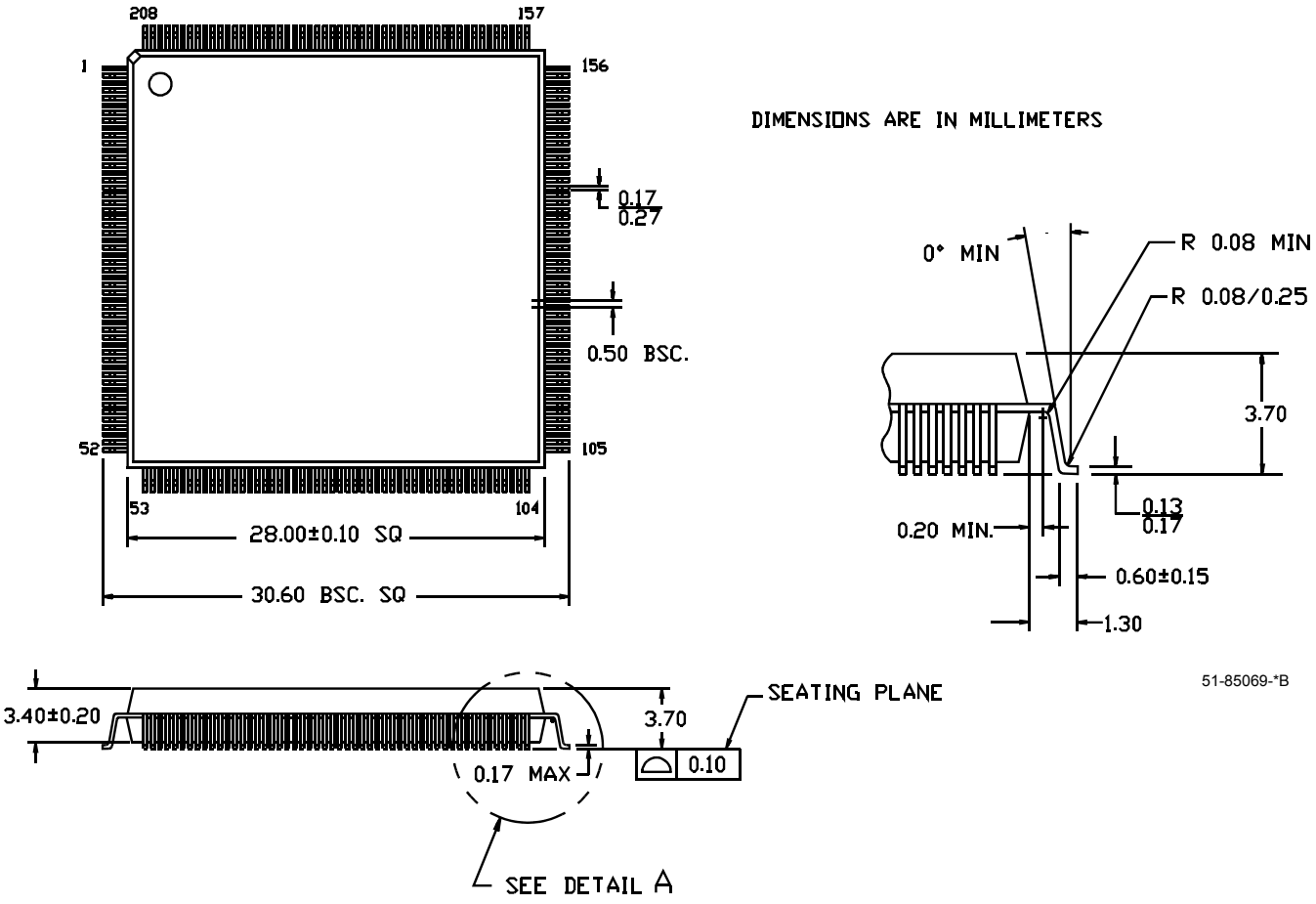
Recommended ATMEL CPLD Boot EEPROM for corresponding Delta39K CPLDs

CPLD Device	Recommended boot EEPROM
39K30	AT17LV512
39K50	AT17LV512
39K100	AT17LV010
39K200	AT17LV002

Note:
17. Refer to the data sheets at www.atmel.com for detailed architectural and timing information.

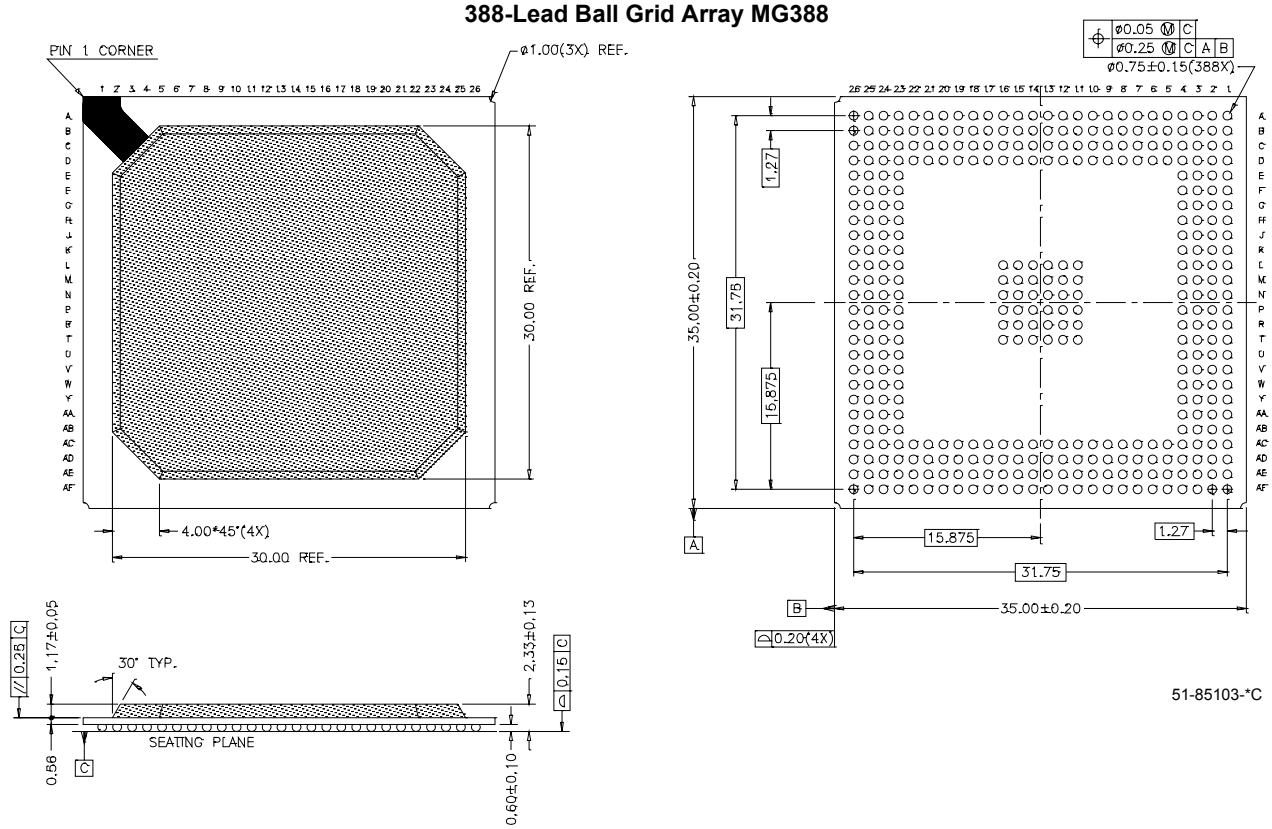
Package Diagrams

208-Lead Enhanced Quad Flat Pack (EQFP) NT208
208-Lead Lead-Free Enhanced Quad Flat Pack (EQFP) NT208



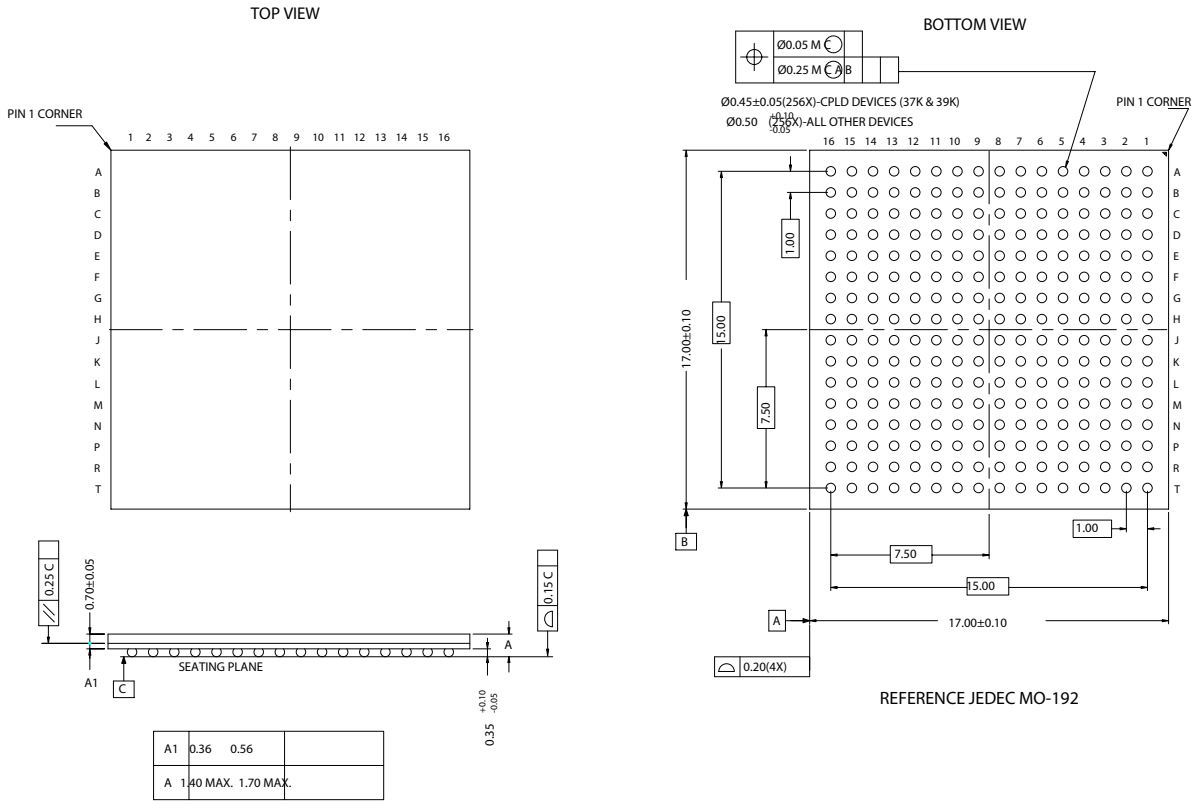
Package Diagrams (continued)

388-Lead Ball Grid Array MG388



Package Diagrams (continued)

256-Ball FBGA (17 x 17 mm) BB256

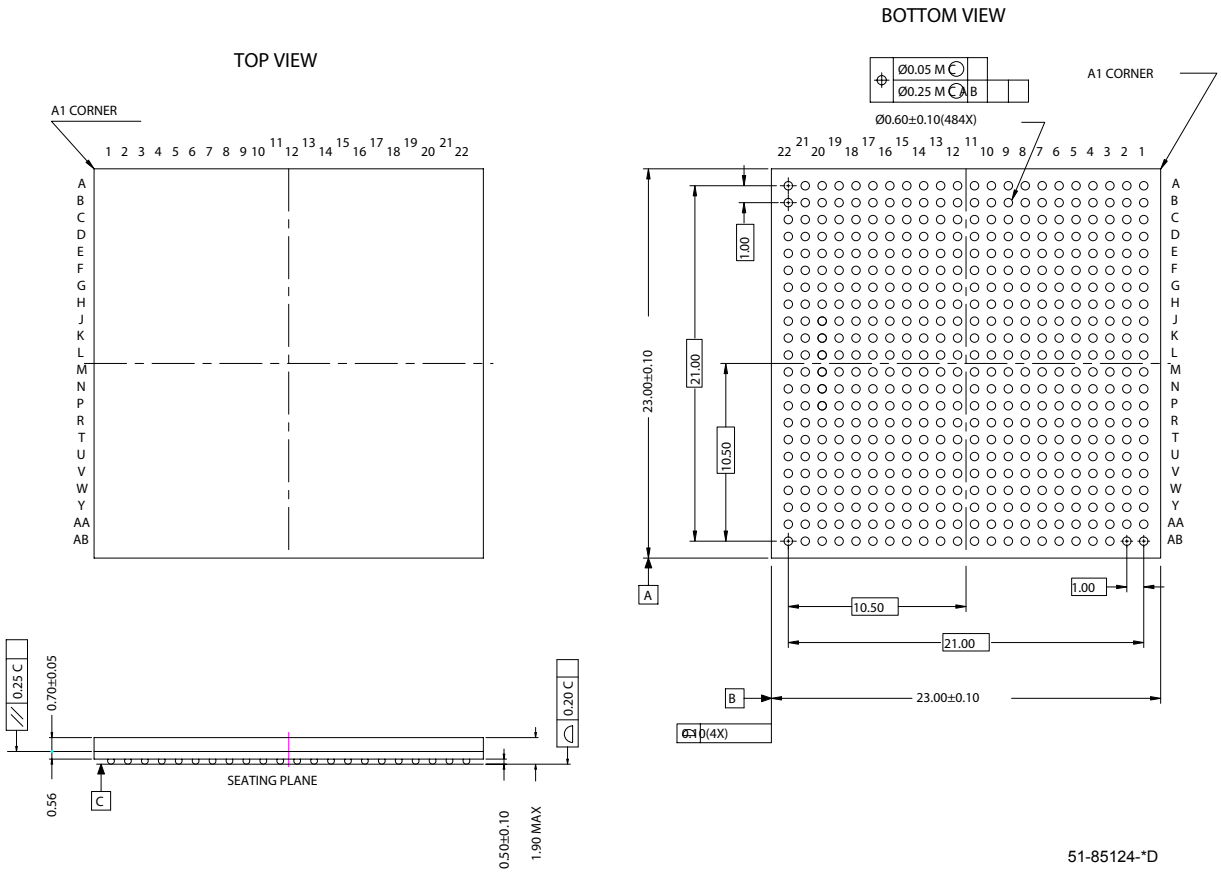


A1	0.36	0.56	
A	1.40 MAX.	1.70 MAX.	

51-85108-*F

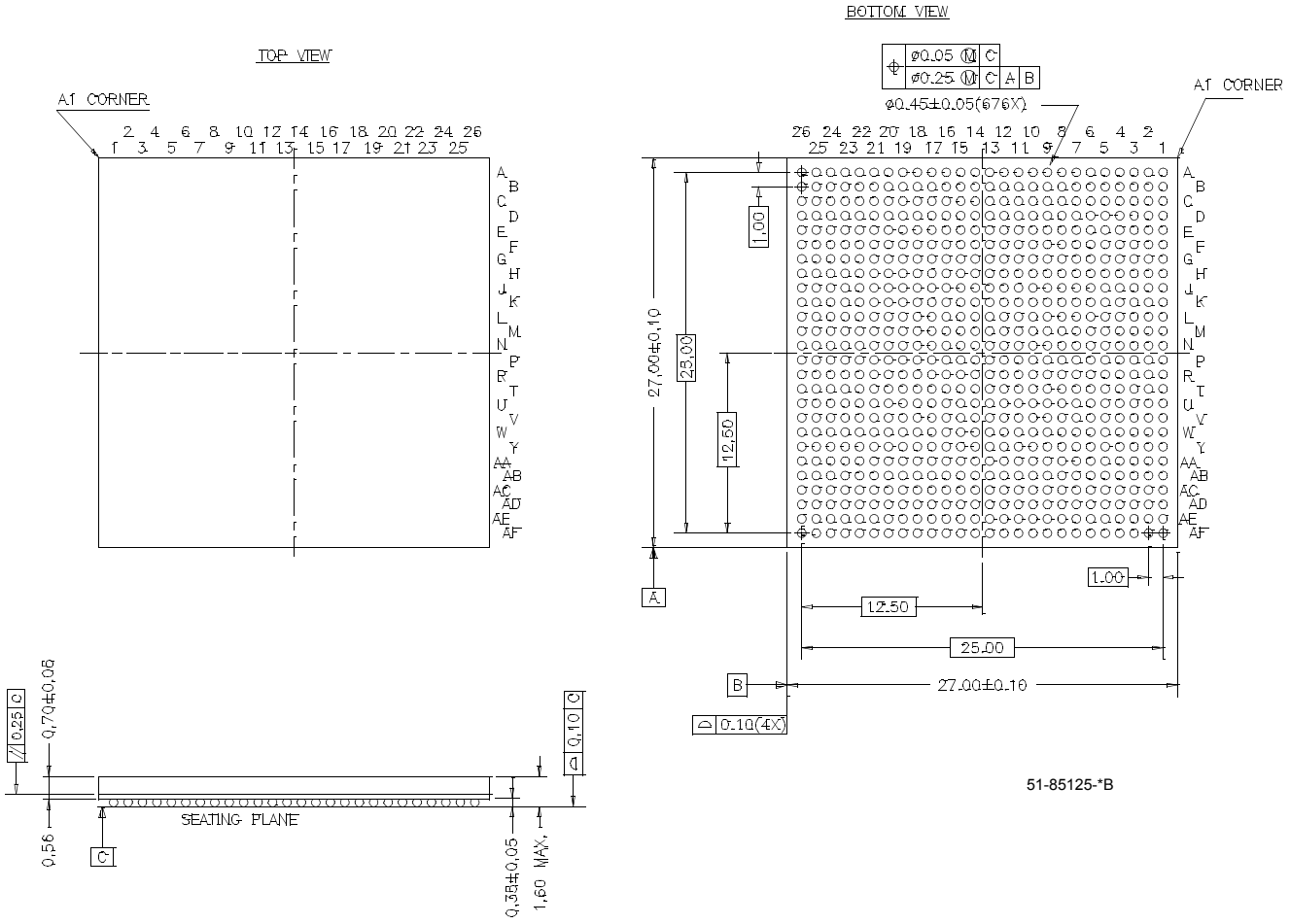
Package Diagrams (continued)

484-ball FBGA (23 mm x 23 mm x 1.6 mm) BB484



Package Diagrams (continued)

676-Ball FBGA (27 x 27 x 1.6 mm) BB676/MB676



Pin Tables

Table 8. Pin Definition Table

Pin Name	Function	Description
GCLK0-3	Input	Global Clock signals 0 through 3
GCTL0-3	Input	Global Control signals 0 through 3
GND	Ground	Ground
IO/V_{REF0}	Input/Output	Dual function pin: IO or Reference Voltage for Bank 0
IO/V_{REF1}	Input/Output	Dual function pin: IO or Reference Voltage for Bank 1
IO/V_{REF2}	Input/Output	Dual function pin: IO or Reference Voltage for Bank 2
IO/V_{REF3}	Input/Output	Dual function pin: IO or Reference Voltage for Bank 3
IO/V_{REF4}	Input/Output	Dual function pin: IO or Reference Voltage for Bank 4
IO/V_{REF5}	Input/Output	Dual function pin: IO or Reference Voltage for Bank 5
IO/V_{REF6}	Input/Output	Dual function pin: IO or Reference Voltage for Bank 6
IO/V_{REF7}	Input/Output	Dual function pin: IO or Reference Voltage for Bank 7
IO	Input/Output	Input or Output pin
IO6/Lock	Input/Output	Dual function pin: IO in Bank 6 or PLL lock output signal
MSEL	Input	Mode Select Pin (see *Table 9*)

Table 8. Pin Definition Table

Pin Name	Function	Description
Reconfig	Input	Pin to start configuration of Delta39K
TCLK	Input	JTAG Test Clock
TDI	Input	JTAG Test Data In
TDO	Output	JTAG Test Data Out
TMS	Input	JTAG Test Mode Select
V_{CC}	Power	Operating Voltage
V_{CCIO0}	Power	V_{CC} for I/O bank 0
V_{CCIO1}	Power	V_{CC} for I/O bank 1
V_{CCIO2}	Power	V_{CC} for I/O bank 2
V_{CCIO3}	Power	V_{CC} for I/O bank 3
V_{CCIO4}	Power	V_{CC} for I/O bank 4
V_{CCIO5}	Power	V_{CC} for I/O bank 5
V_{CCIO6}	Power	V_{CC} for I/O bank 6
V_{CCIO7}	Power	V_{CC} for I/O bank 7
V_{CCJTAG}	Power	V_{CC} for JTAG pins
V_{CCCNFG}	Power	V_{CC} for Configuration port
V_{CCPLL}[18]	Power	V_{CC} for PLL
V_{CCPRG}	Power	V_{CC} for programming the Self-Boot™ solution embedded boot PROM
Config_Done	Output	Flag indicating that configuration is complete
CCLK	Output	Configuration Clock for serial interface with the external boot PROM
CCE	Output	Chip select for the external boot PROM (active low)
Data	Input	Pin to receive configuration data from the external boot PROM
Reset	Output	Reset signal to interface with the external boot PROM

Table 9. Mode Select (MSEL) Pin Connectivity Table

GND	Delta39K - Self-Boot™ Solution
V_{CCCNFG}	Delta39K - with external boot PROM

Table 10. I/O Banks for Global Clock and Global Control Pins (in all densities and packages)

	GCLK[0] GCTL[0]	GCLK[1] GCTL[1]	GCLK[2] GCTL[2]	GCLK[3] GCTL[3]
Bank Number	0	5	6	7

Table 11. 208 EQFP/PQFP Pin Table

Pin	CY39030	CY39050	CY39100	CY39200
1	GCTL0	GCTL0	GCTL0	GCTL0
2	GND	GND	GND	GND
3	GCLK0	GCLK0	GCLK0	GCLK0
4	GND	GND	GND	GND
5	IO0	IO0	IO0	IO0
6	IO0	IO0	IO0	IO0
7	IO0	IO0	IO0	IO0
8	IO/V_{REF0}	IO/V_{REF0}	IO/V_{REF0}	IO/V_{REF0}
9	IO0	IO0	IO0	IO0
10	IO0	IO0	IO0	IO0
11	V_{CCIO0}	V_{CCIO0}	V_{CCIO0}	V_{CCIO0}

Note:
18. The PLL is available in Delta39K 'V' devices (2.5V/3.3V) and not in Delta39K 'Z' devices (1.8V). In Delta39K 'Z' devices, connect V_{CCPLL} to V_{CC}.

Table 11. 208 EQFP/PQFP Pin Table (continued)

Pin	CY39030	CY39050	CY39100	CY39200
12	IO0	IO0	IO0	IO0
13	IO0	IO0	IO0	IO0
14	IO0	IO0	IO0	IO0
15	IO0	IO0	IO0	IO0
16	IO/V_{REF0}	IO/V_{REF0}	IO/V_{REF0}	IO/V_{REF0}
17	IO0	IO0	IO0	IO0
18	IO0	IO0	IO0	IO0
19	IO0	IO0	IO0	IO0
20	V_{CCIO0}	V_{CCIO0}	V_{CCIO0}	V_{CCIO0}
21[19]	IO0	IO0	IO0	IO0
22[19]	IO0	IO0	IO0	IO0
23	V_{CC}	V_{CC}	V_{CC}	V_{CC}
24	GND	GND	GND	GND
25	NC	NC	V_{CC}	V_{CC}
26	NC	NC	GND	GND
27[19]	IO/V_{REF0}	IO/V_{REF0}	IO/V_{REF0}	IO/V_{REF0}
28	V_{CCIO0}	V_{CCIO0}	V_{CCIO0}	V_{CCIO0}
29	V_{CCIO1}	V_{CCIO1}	V_{CCIO1}	V_{CCIO1}
30[19]	IO/V_{REF1}	IO/V_{REF1}	IO/V_{REF1}	IO/V_{REF1}
31[19]	IO1	IO1	IO1	IO1
32[19]	IO1	IO1	IO1	IO1
33	IO1	IO1	IO1	IO1
34	IO1	IO1	IO1	IO1
35	V_{CCIO1}	V_{CCIO1}	V_{CCIO1}	V_{CCIO1}
36	GND	GND	GND	GND
37	IO1	IO1	IO1	IO1
38	IO1	IO1	IO1	IO1
39	IO1	IO1	IO1	IO1
40	IO/V_{REF1}	IO/V_{REF1}	IO/V_{REF1}	IO/V_{REF1}
41	IO1	IO1	IO1	IO1
42	IO1	IO1	IO1	IO1
43	IO1	IO1	IO1	IO1
44	IO1	IO1	IO1	IO1
45	V_{CCPRG}	V_{CCPRG}	V_{CCPRG}	V_{CCPRG}
46	V_{CCIO1}	V_{CCIO1}	V_{CCIO1}	V_{CCIO1}
47	GND	GND	GND	GND
48	IO1	IO1	IO1	IO1
49	IO/V_{REF1}	IO/V_{REF1}	IO/V_{REF1}	IO/V_{REF1}
50	IO1	IO1	IO1	IO1
51	IO1	IO1	IO1	IO1
52	V_{CCCNFG}	V_{CCCNFG}	V_{CCCNFG}	V_{CCCNFG}
53	Data	Data	Data	Data
54	Config_Done	Config_Done	Config_Done	Config_Done
55	Reset	Reset	Reset	Reset

Table 11. 208 EQFP/PQFP Pin Table (continued)

Pin	CY39030	CY39050	CY39100	CY39200
56	Reconfig	Reconfig	Reconfig	Reconfig
57	CCE	CCE	CCE	CCE
58	CCLK	CCLK	CCLK	CCLK
59	V_{CCCNFG}	V_{CCCNFG}	V_{CCCNFG}	V_{CCCNFG}
60	MSEL	MSEL	MSEL	MSEL
61	IO2	IO2	IO2	IO2
62	IO2	IO2	IO2	IO2
63	IO2	IO2	IO2	IO2
64	IO/V_{REF2}	IO/V_{REF2}	IO/V_{REF2}	IO/V_{REF2}
65	IO2	IO2	IO2	IO2
66	V_{CCIO2}	V_{CCIO2}	V_{CCIO2}	V_{CCIO2}
67	GND	GND	GND	GND
68	IO2	IO2	IO2	IO2
69	IO2	IO2	IO2	IO2
70	IO2	IO2	IO2	IO2
71	IO2	IO2	IO2	IO2
72	IO/V_{REF2}	IO/V_{REF2}	IO/V_{REF2}	IO/V_{REF2}
73	GND	GND	GND	GND
74	V_{CCIO2}	V_{CCIO2}	V_{CCIO2}	V_{CCIO2}
75	V_{CC}	V_{CC}	V_{CC}	V_{CC}
76	GND	GND	GND	GND
77	NC	NC	V_{CC}	V_{CC}
78	NC	NC	GND	GND
79	IO2	IO2	IO2	IO2
80	IO/V_{REF2}	IO/V_{REF2}	IO/V_{REF2}	IO/V_{REF2}
81[19]	IO2	IO2	IO2	IO2
82[19]	IO2	IO2	IO2	IO2
83[19]	IO2	IO2	IO2	IO2
84	V_{CCIO2}	V_{CCIO2}	V_{CCIO2}	V_{CCIO2}
85	V_{CCIO3}	V_{CCIO3}	V_{CCIO3}	V_{CCIO3}
86[19]	IO3	IO3	IO3	IO3
87[19]	IO3	IO3	IO3	IO3
88[19]	IO/V_{REF3}	IO/V_{REF3}	IO/V_{REF3}	IO/V_{REF3}
89	V_{CCIO3}	V_{CCIO3}	V_{CCIO3}	V_{CCIO3}
90	GND	GND	GND	GND
91	IO3	IO3	IO3	IO3
92	IO3	IO3	IO3	IO3
93	IO3	IO3	IO3	IO3
94	IO3	IO3	IO3	IO3
95	IO3	IO3	IO3	IO3
96	IO/V_{REF3}	IO/V_{REF3}	IO/V_{REF3}	IO/V_{REF3}
97	IO3	IO3	IO3	IO3
98	V_{CCIO3}	V_{CCIO3}	V_{CCIO3}	V_{CCIO3}
99	IO3	IO3	IO3	IO3

Table 11. 208 EQFP/PQFP Pin Table (continued)

Pin	CY39030	CY39050	CY39100	CY39200
100	GND	GND	GND	GND
101	IO3	IO3	IO3	IO3
102	IO3	IO3	IO3	IO3
103	IO3	IO3	IO3	IO3
104	IO/V_{REF3}	IO/V_{REF3}	IO/V_{REF3}	IO/V_{REF3}
105	IO4	IO4	IO4	IO4
106	IO4	IO4	IO4	IO4
107	IO4	IO4	IO4	IO4
108	IO/V_{REF4}	IO/V_{REF4}	IO/V_{REF4}	IO/V_{REF4}
109	IO4	IO4	IO4	IO4
110	IO4	IO4	IO4	IO4
111	V_{CCIO4}	V_{CCIO4}	V_{CCIO4}	V_{CCIO4}
112	GND	GND	GND	GND
113	IO4	IO4	IO4	IO4
114	V_{CCPRG}	V_{CCPRG}	V_{CCPRG}	V_{CCPRG}
115	IO4	IO4	IO4	IO4
116	IO/V_{REF4}	IO/V_{REF4}	IO/V_{REF4}	IO/V_{REF4}
117	IO4	IO4	IO4	IO4
118	IO4	IO4	IO4	IO4
119	IO4	IO4	IO4	IO4
120	IO4	IO4	IO4	IO4
121	IO4	IO4	IO4	IO4
122[19]	IO/V_{REF4}	IO/V_{REF4}	IO/V_{REF4}	IO/V_{REF4}
123[19]	IO4	IO4	IO4	IO4
124	V_{CCIO4}	V_{CCIO4}	V_{CCIO4}	V_{CCIO4}
125	GND	GND	GND	GND
126[19]	IO4	IO4	IO4	IO4
127	V_{CC}	V_{CC}	V_{CC}	V_{CC}
128	GND	GND	GND	GND
129	NC	NC	V_{CC}	V_{CC}
130	NC	NC	GND	GND
131	V_{CCIO4}	V_{CCIO4}	V_{CCIO4}	V_{CCIO4}
132	V_{CCIO5}	V_{CCIO5}	V_{CCIO5}	V_{CCIO5}
133[19]	IO5	IO5	IO5	IO5
134[19]	IO5	IO5	IO5	IO5
135[19]	IO/V_{REF5}	IO/V_{REF5}	IO/V_{REF5}	IO/V_{REF5}
136	IO5	IO5	IO5	IO5
137	IO5	IO5	IO5	IO5
138	V_{CCIO5}	V_{CCIO5}	V_{CCIO5}	V_{CCIO5}
139	IO5	IO5	IO5	IO5
140	IO5	IO5	IO5	IO5
141	IO5	IO5	IO5	IO5
142	IO/V_{REF5}	IO/V_{REF5}	IO/V_{REF5}	IO/V_{REF5}
143	IO5	IO5	IO5	IO5

Table 11. 208 EQFP/PQFP Pin Table (continued)

Pin	CY39030	CY39050	CY39100	CY39200
144	IO5	IO5	IO5	IO5
145	IO5	IO5	IO5	IO5
146	IO5	IO5	IO5	IO5
147	IO5	IO5	IO5	IO5
148	V_{CCIO5}	V_{CCIO5}	V_{CCIO5}	V_{CCIO5}
149	IO/V_{REF5}	IO/V_{REF5}	IO/V_{REF5}	IO/V_{REF5}
150	IO5	IO5	IO5	IO5
151	IO5	IO5	IO5	IO5
152	GND	GND	GND	GND
153	GCLK1	GCLK1	GCLK1	GCLK1
154	GND	GND	GND	GND
155	GCTL1	GCTL1	GCTL1	GCTL1
156	TDO	TDO	TDO	TDO
157	TCLK	TCLK	TCLK	TCLK
158	TDI	TDI	TDI	TDI
159	V_{CCJTAG}	V_{CCJTAG}	V_{CCJTAG}	V_{CCJTAG}
160	GCLK2	GCLK2	GCLK2	GCLK2
161	GND	GND	GND	GND
162	TMS	TMS	TMS	TMS
163	GCTL2	GCTL2	GCTL2	GCTL2
164	IO6	IO6	IO6	IO6
165	IO6	IO6	IO6	IO6
166	IO6	IO6	IO6	IO6
167	IO/V_{REF6}	IO/V_{REF6}	IO/V_{REF6}	IO/V_{REF6}
168	IO6	IO6	IO6	IO6
169	V_{CCIO6}	V_{CCIO6}	V_{CCIO6}	V_{CCIO6}
170	IO6	IO6	IO6	IO6
171	IO6	IO6	IO6	IO6
172	IO6	IO6	IO6	IO6
173	IO/V_{REF6}	IO/V_{REF6}	IO/V_{REF6}	IO/V_{REF6}
174	IO6	IO6	IO6	IO6
175	IO6	IO6	IO6	IO6
176	IO6	IO6	IO6	IO6
177	GND	GND	GND	GND
178	V_{CCIO6}	V_{CCIO6}	V_{CCIO6}	V_{CCIO6}
179	V_{CCPLL}	V_{CCPLL}	V_{CCPLL}	V_{CCPLL}
180	GND	GND	GND	GND
181	V_{CC}	V_{CC}	V_{CC}	V_{CC}
182	GND	GND	GND	GND
183[19]	IO/V_{REF6}	IO/V_{REF6}	IO/V_{REF6}	IO/V_{REF6}
184[19]	IO6	IO6	IO6	IO6
185[19]	IO6/Lock	IO6/Lock	IO6/Lock	IO6/Lock
186	V_{CCIO6}	V_{CCIO6}	V_{CCIO6}	V_{CCIO6}
187	V_{CCIO7}	V_{CCIO7}	V_{CCIO7}	V_{CCIO7}

Table 11. 208 EQFP/PQFP Pin Table (continued)

Pin	CY39030	CY39050	CY39100	CY39200
188[19]	IO7	IO7	IO7	IO7
189[19]	IO7	IO7	IO7	IO7
190[19]	IO/V_{REF7}	IO/V_{REF7}	IO/V_{REF7}	IO/V_{REF7}
191	V_{CCIO7}	V_{CCIO7}	V_{CCIO7}	V_{CCIO7}
192	IO7	IO7	IO7	IO7
193	IO7	IO7	IO7	IO7
194	IO7	IO7	IO7	IO7
195	IO7	IO7	IO7	IO7
196	IO/V_{REF7}	IO/V_{REF7}	IO/V_{REF7}	IO/V_{REF7}
197	IO7	IO7	IO7	IO7
198	IO7	IO7	IO7	IO7
199	V_{CCIO7}	V_{CCIO7}	V_{CCIO7}	V_{CCIO7}
200	IO7	IO7	IO7	IO7
201	IO/V_{REF7}	IO/V_{REF7}	IO/V_{REF7}	IO/V_{REF7}
202	IO7	IO7	IO7	IO7
203	IO7	IO7	IO7	IO7
204	IO7	IO7	IO7	IO7
205	GND	GND	GND	GND
206	GCLK3	GCLK3	GCLK3	GCLK3
207	GND	GND	GND	GND
208	GCTL3	GCTL3	GCTL3	GCTL3

Table 12. 388 BGA Pin Table

Pin	CY39050	CY39100	CY39200
A1	GND	GND	GND
A2	NC	IO7	IO7
A3	IO7	IO7	IO7
A4	IO7	IO7	IO7
A5	IO7	IO7	IO7
A6	IO7	IO7	IO7
A7	IO7	IO7	IO7
A8	NC	IO/VREF7	IO/VREF7
A9	IO7	IO7	IO7
A10	IO7	IO7	IO7
A11	IO/V_{REF7}	IO/V_{REF7}	IO/V_{REF7}
A12	IO7	IO7	IO7
A13[19]	IO7	IO7	IO7
A14[19]	IO6	IO6	IO6
A15	IO6	IO6	IO6
A16	GND	GND	GND
A17	IO6	IO6	IO6
A18	IO6	IO6	IO6

Note:
19. Capacitance on these I/O pins meets the PCI spec (rev. 2.2), which requires IDSEL pin in a PCI design to have capacitance less than or equal to 8 F. In the document titled “Delta39K CPLD Family data sheet”, this spec is defined as C_{PCI}. All other I/O pins have a capacitance less than or equal to 10 pF.

Table 12. 388 BGA Pin Table (continued)

Pin	CY39050	CY39100	CY39200
A19	NC	IO6	IO6
A20	NC	IO6	IO6
A21	IO6	IO6	IO6
A22	IO/V_{REF6}	IO/V_{REF6}	IO/V_{REF6}
A23	IO6	IO6	IO6
A24	IO6	IO6	IO6
A25	IO6	IO6	IO6
A26	GND	GND	GND
B1	IO7	IO7	IO7
B2	NC	IO7	IO7
B3	NC	IO7	IO7
B4	NC	IO/V_{REF7}	IO/V_{REF7}
B5	IO7	IO7	IO7
B6	IO/V_{REF7}	IO/V_{REF7}	IO/V_{REF7}
B7	IO7	IO7	IO7
B8	IO7	IO7	IO7
B9	IO7	IO7	IO7
B10	IO/V_{REF7}	IO/V_{REF7}	IO/V_{REF7}
B11	IO7	IO7	IO7
B12	IO7	IO7	IO7
B13[19]	IO7	IO7	IO7
B14[19]	IO6	IO6	IO6
B15	IO6	IO6	IO6
B16	IO6	IO6	IO6
B17	IO6/Lock	IO6/Lock	IO6/Lock
B18	IO6	IO6	IO6
B19	IO6	IO6	IO6
B20	IO/VREF6	IO/VREF6	IO/VREF6
B21	IO6	IO6	IO6
B22	NC	IO6	IO6
B23	NC	IO6	IO6
B24	IO6	IO6	IO6
B25	IO6	IO6	IO6
B26	IO6	IO6	IO6
C1	IO0	IO0	IO0
C2	IO/V_{REF7}	IO/V_{REF7}	IO/V_{REF7}
C3	NC	IO7	IO7
C4	IO7	IO7	IO7
C5	IO7	IO7	IO7
C6	NC	IO7	IO7
C7	IO7	IO7	IO7
C8	IO7	IO7	IO7
C9	IO7	IO7	IO7
C10	IO7	IO7	IO7

Table 12. 388 BGA Pin Table (continued)

Pin	CY39050	CY39100	CY39200
C11	IO7	IO7	IO7
C12	IO7	IO7	IO7
C13[19]	IO7	IO7	IO7
C14[19]	IO6	IO6	IO6
C15	IO/V_{REF6}	IO/V_{REF6}	IO/V_{REF6}
C16	IO6	IO6	IO6
C17	NC	IO/V_{REF6}	IO/V_{REF6}
C18	IO6	IO6	IO6
C19	IO6	IO6	IO6
C20	IO6	IO6	IO6
C21	IO6	IO6	IO6
C22	NC	IO6	IO6
C23	NC	IO6	IO6
C24	IO6	IO6	IO6
C25	IO/V_{REF6}	IO/V_{REF6}	IO/V_{REF6}
C26	IO6	IO6	IO6
D1	IO0	IO0	IO0
D2	IO0	IO0	IO0
D3	IO/V_{REF0}	IO/V_{REF0}	IO/V_{REF0}
D4	IO7	IO7	IO7
D5	GCTL3	GCTL3	GCTL3
D6	NC	IO7	IO7
D7	GCLK3	GCLK3	GCLK3
D8	V_{CCIO7}	V_{CCIO7}	V_{CCIO7}
D9	V_{CCIO7}	V_{CCIO7}	V_{CCIO7}
D10	V_{CCIO7}	V_{CCIO7}	V_{CCIO7}
D11	IO7	IO7	IO7
D12	V_{CCIO7}	V_{CCIO7}	V_{CCIO7}
D13	V_{CC}	V_{CC}	V_{CC}
D14	V_{CCIO6}	V_{CCIO6}	V_{CCIO6}
D15	V_{CCIO6}	V_{CCIO6}	V_{CCIO6}
D16	IO6	IO6	IO6
D17	V_{CCPLL}	V_{CCPLL}	V_{CCPLL}
D18	V_{CCIO6}	V_{CCIO6}	V_{CCIO6}
D19	V_{CCIO6}	V_{CCIO6}	V_{CCIO6}
D20	GCLK2	GCLK2	GCLK2
D21	NC	IO/V_{REF6}	IO/V_{REF6}
D22	GCTL2	GCTL2	GCTL2
D23	NC	IO6	IO6
D24	IO5	IO5	IO5
D25	TMS	TMS	TMS
D26	TCLK	TCLK	TCLK
E1	IO0	IO0	IO0
E2	IO0	IO0	IO0

Table 12. 388 BGA Pin Table (continued)

Pin	CY39050	CY39100	CY39200
E3	IO0	IO0	IO0
E4	GCTL0	GCTL0	GCTL0
E23	GCLK1	GCLK1	GCLK1
E24	IO5	IO5	IO5
E25	TDI	TDI	TDI
E26	TDO	TDO	TDO
F1	NC	IO0	IO0
F2	NC	IO0	IO0
F3	NC	IO0	IO0
F4	IO0	IO0	IO0
F23	NC	IO5	IO5
F24	IO5	IO5	IO5
F25	IO5	IO5	IO5
F26	IO5	IO5	IO5
G1	IO0	IO0	IO0
G2	IO0	IO0	IO0
G3	IO/V_{REF0}	IO/V_{REF0}	IO/V_{REF0}
G4	GCLK0	GCLK0	GCLK0
G23	GCTL1	GCTL1	GCTL1
G24	IO/V_{REF5}	IO/V_{REF5}	IO/V_{REF5}
G25	IO5	IO5	IO5
G26	IO5	IO5	IO5
H1	IO0	IO0	IO0
H2	NC	IO0	IO0
H3	NC	IO0	IO0
H4	V_{CCIO0}	V_{CCIO0}	V_{CCIO0}
H23	V_{CCJTAG}	V_{CCJTAG}	V_{CCJTAG}
H24	IO5	IO5	IO5
H25	IO5	IO5	IO5
H26	IO5	IO5	IO5
J1	NC	IO0	IO0
J2	NC	IO/V_{REF0}	IO/V_{REF0}
J3	NC	IO0	IO0
J4	V_{CCIO0}	V_{CCIO0}	V_{CCIO0}
J23	V_{CCIO5}	V_{CCIO5}	V_{CCIO5}
J24	NC	IO/V_{REF5}	IO/V_{REF5}
J25	IO5	IO5	IO5
J26	IO5	IO5	IO5
K1	NC	IO0	IO0
K2	NC	IO0	IO0
K3	NC	IO0	IO0
K4	V_{CC}	V_{CC}	V_{CC}
K23	V_{CCIO5}	V_{CCIO5}	V_{CCIO5}
K24	IO5	IO5	IO5

Table 12. 388 BGA Pin Table (continued)

Pin	CY39050	CY39100	CY39200
K25	NC	IO5	IO5
K26	NC	IO5	IO5
L1	IO0	IO0	IO0
L2	IO0	IO0	IO0
L3	IO0	IO0	IO0
L4	IO0	IO0	IO0
L11	GND	GND	GND
L12	GND	GND	GND
L13	GND	GND	GND
L14	GND	GND	GND
L15	GND	GND	GND
L16	GND	GND	GND
L23	NC	IO5	IO5
L24	IO/V_{REF5}	IO/V_{REF5}	IO/V_{REF5}
L25	NC	IO5	IO5
L26	NC	IO5	IO5
M1	IO0	IO0	IO0
M2[19]	IO0	IO0	IO0
M3[19]	IO0	IO0	IO0
M4	V_{CCIO0}	V_{CCIO0}	V_{CCIO0}
M11	GND	GND	GND
M12	GND	GND	GND
M13	GND	GND	GND
M14	GND	GND	GND
M15	GND	GND	GND
M16	GND	GND	GND
M23	V_{CCIO5}	V_{CCIO5}	V_{CCIO5}
M24	NC	IO5	IO5
M25	NC	IO5	IO5
M26	NC	IO5	IO5
N1	NC	VCC	VCC
N2	IO/V_{REF0}	IO/V_{REF0}	IO/V_{REF0}
N3[19]	IO0	IO0	IO0
N4[19]	IO1	IO1	IO1
N11	GND	GND	GND
N12	GND	GND	GND
N13	GND	GND	GND
N14	GND	GND	GND
N15	GND	GND	GND
N16	GND	GND	GND
N23[19]	IO5	IO5	IO5
N24	IO5	IO5	IO5
N25	IO5	IO5	IO5
N26	IO/V_{REF5}	IO/V_{REF5}	IO/V_{REF5}

Table 12. 388 BGA Pin Table (continued)

Pin	CY39050	CY39100	CY39200
P1	IO1	IO1	IO1
P2	IO/V_{REF1}	IO/V_{REF1}	IO/V_{REF1}
P3[19]	IO1	IO1	IO1
P4[19]	IO1	IO1	IO1
P11	GND	GND	GND
P12	GND	GND	GND
P13	GND	GND	GND
P14	GND	GND	GND
P15	GND	GND	GND
P16	GND	GND	GND
P23	V_{CC}	V_{CC}	V_{CC}
P24[19]	IO5	IO5	IO5
P25[19]	IO5	IO5	IO5
P26	NC	V_{CC}	V_{CC}
R1	IO1	IO1	IO1
R2	IO1	IO1	IO1
R3	NC	IO1	IO1
R4	V_{CCIO1}	V_{CCIO1}	V_{CCIO1}
R11	GND	GND	GND
R12	GND	GND	GND
R13	GND	GND	GND
R14	GND	GND	GND
R15	GND	GND	GND
R16	GND	GND	GND
R23	V_{CCIO4}	V_{CCIO4}	V_{CCIO4}
R24[19]	IO4	IO4	IO4
R25[19]	IO4	IO4	IO4
R26	NC	IO5	IO5
T1	NC	IO1	IO1
T2	NC	IO1	IO1
T3	NC	IO/V_{REF1}	IO/V_{REF1}
T4	NC	IO1	IO1
T11	GND	GND	GND
T12	GND	GND	GND
T13	GND	GND	GND
T14	GND	GND	GND
T15	GND	GND	GND
T16	GND	GND	GND
T23[19]	IO4	IO4	IO4
T24	IO4	IO4	IO4
T25	IO/V_{REF4}	IO/V_{REF4}	IO/V_{REF4}
T26	IO4	IO4	IO4
U1	NC	IO1	IO1
U2	NC	IO1	IO1

Table 12. 388 BGA Pin Table (continued)

Pin	CY39050	CY39100	CY39200
U3	NC	IO1	IO1
U4	V_{CCPRG}	V_{CCPRG}	V_{CCPRG}
U23	V_{CCPRG}	V_{CCPRG}	V_{CCPRG}
U24	IO4	IO4	IO4
U25	IO4	IO4	IO4
U26	NC	IO4	IO4
V1	NC	IO1	IO1
V2	NC	IO1	IO1
V3	IO1	IO1	IO1
V4	V_{CCIO1}	V_{CCIO1}	V_{CCIO1}
V23	V_{CCIO4}	V_{CCIO4}	V_{CCIO4}
V24	NC	IO4	IO4
V25	NC	IO4	IO4
V26	NC	IO4	IO4
W1	IO1	IO1	IO1
W2	IO1	IO1	IO1
W3	IO/V_{REF1}	IO/V_{REF1}	IO/V_{REF1}
W4	V_{CCIO1}	V_{CCIO1}	V_{CCIO1}
W23	V_{CCIO4}	V_{CCIO4}	V_{CCIO4}
W24	NC	IO4	IO4
W25	NC	IO/V_{REF4}	IO/V_{REF4}
W26	NC	IO4	IO4
Y1	IO1	IO1	IO1
Y2	IO1	IO1	IO1
Y3	IO1	IO1	IO1
Y4	IO1	IO1	IO1
Y23	NC	IO4	IO4
Y24	NC	IO4	IO4
Y25	NC	IO4	IO4
Y26	IO4	IO4	IO4
AA1	IO1	IO1	IO1
AA2	IO1	IO1	IO1
AA3	IO/V_{REF1}	IO/V_{REF1}	IO/V_{REF1}
AA4	IO1	IO1	IO1
AA23	IO4	IO4	IO4
AA24	IO4	IO4	IO4
AA25	IO/V_{REF4}	IO/V_{REF4}	IO/V_{REF4}
AA26	IO4	IO4	IO4
AB1	V_{CCCNFG}	V_{CCCNFG}	V_{CCCNFG}
AB2	Config_Done	Config_Done	Config_Done
AB3	IO1	IO1	IO1
AB4	IO1	IO1	IO1
AB23	IO4	IO4	IO4
AB24	IO4	IO4	IO4

Table 12. 388 BGA Pin Table (continued)

Pin	CY39050	CY39100	CY39200
AB25	IO4	IO4	IO4
AB26	IO4	IO4	IO4
AC1	Data	Data	Data
AC2	Reconfig	Reconfig	Reconfig
AC3	IO2	IO2	IO2
AC4	IO2	IO2	IO2
AC5	IO2	IO2	IO2
AC6	IO2	IO2	IO2
AC7	NC	IO2	IO2
AC8	V_{CCIO2}	V_{CCIO2}	V_{CCIO2}
AC9	V_{CCIO2}	V_{CCIO2}	V_{CCIO2}
AC10	V_{CCCNFG}	V_{CCCNFG}	V_{CCCNFG}
AC11	IO2	IO2	IO2
AC12	V_{CCIO2}	V_{CCIO2}	V_{CCIO2}
AC13	V_{CCIO2}	V_{CCIO2}	V_{CCIO2}
AC14	V_{CCIO3}	V_{CCIO3}	V_{CCIO3}
AC15	V_{CCIO3}	V_{CCIO3}	V_{CCIO3}
AC16	IO3	IO3	IO3
AC17	NC	V_{CC}	V_{CC}
AC18	V_{CCIO3}	V_{CCIO3}	V_{CCIO3}
AC19	V_{CCIO3}	V_{CCIO3}	V_{CCIO3}
AC20	IO3	IO3	IO3
AC21	IO3	IO3	IO3
AC22	IO3	IO3	IO3
AC23	IO/V_{REF4}	IO/V_{REF4}	IO/V_{REF4}
AC24	IO4	IO4	IO4
AC25	IO4	IO4	IO4
AC26	IO4	IO4	IO4
AD1	Reset	Reset	Reset
AD2	CCLK	CCLK	CCLK
AD3	IO/V_{REF2}	IO/V_{REF2}	IO/V_{REF2}
AD4	IO2	IO2	IO2
AD5	IO/V_{REF2}	IO/V_{REF2}	IO/V_{REF2}
AD6	IO2	IO2	IO2
AD7	NC	IO2	IO2
AD8	NC	IO/V_{REF2}	IO/V_{REF2}
AD9	IO2	IO2	IO2
AD10	IO/V_{REF2}	IO/V_{REF2}	IO/V_{REF2}
AD11	IO2	IO2	IO2
AD12	IO2	IO2	IO2
AD13	IO/V_{REF2}	IO/V_{REF2}	IO/V_{REF2}
AD14[19]	IO2	IO2	IO2
AD15[19]	IO3	IO3	IO3
AD16	IO3	IO3	IO3

Table 12. 388 BGA Pin Table (continued)

Pin	CY39050	CY39100	CY39200
AD17	IO3	IO3	IO3
AD18	IO/V_{REF3}	IO/V_{REF3}	IO/V_{REF3}
AD19	IO3	IO3	IO3
AD20	IO3	IO3	IO3
AD21	IO3	IO3	IO3
AD22	IO3	IO3	IO3
AD23	IO3	IO3	IO3
AD24	NC	IO3	IO3
AD25	IO/V_{REF3}	IO/V_{REF3}	IO/V_{REF3}
AD26	IO3	IO3	IO3
AE1	CCE	CCE	CCE
AE2	MSEL	MSEL	MSEL
AE3	IO2	IO2	IO2
AE4	IO2	IO2	IO2
AE5	IO2	IO2	IO2
AE6	NC	IO2	IO2
AE7	NC	IO/V_{REF2}	IO/V_{REF2}
AE8	IO2	IO2	IO2
AE9	IO2	IO2	IO2
AE10	IO2	IO2	IO2
AE11	IO2	IO2	IO2
AE12	IO2	IO2	IO2
AE13[19]	IO2	IO2	IO2
AE14[19]	IO2	IO2	IO2
AE15	IO/V_{REF3}	IO/V_{REF3}	IO/V_{REF3}
AE16	IO3	IO3	IO3
AE17	IO3	IO3	IO3
AE18	IO3	IO3	IO3
AE19	IO3	IO3	IO3
AE20	IO/V_{REF3}	IO/V_{REF3}	IO/V_{REF3}
AE21	NC	IO3	IO3
AE22	IO3	IO3	IO3
AE23	NC	IO/V_{REF3}	IO/V_{REF3}
AE24	NC	IO3	IO3
AE25	IO3	IO3	IO3
AE26	IO3	IO3	IO3
AF1	GND	GND	GND
AF2	IO2	IO2	IO2
AF3	IO2	IO2	IO2
AF4	IO2	IO2	IO2
AF5	IO2	IO2	IO2
AF6	NC	IO2	IO2
AF7	NC	IO2	IO2
AF8	NC	IO2	IO2

Table 12. 388 BGA Pin Table (continued)

Pin	CY39050	CY39100	CY39200
AF9	NC	IO2	IO2
AF10	IO2	IO2	IO2
AF11	GND	GND	GND
AF12	IO2	IO2	IO2
AF13	V_{CC}	V_{CC}	V_{CC}
AF14[19]	IO3	IO3	IO3
AF15[19]	IO3	IO3	IO3
AF16	IO3	IO3	IO3
AF17	IO3	IO3	IO3
AF18	IO3	IO3	IO3
AF19	IO3	IO3	IO3
AF20	IO3	IO3	IO3
AF21	NC	IO3	IO3
AF22	NC	IO/V_{REF3}	IO/V_{REF3}
AF23	IO3	IO3	IO3
AF24	NC	IO3	IO3
AF25	NC	IO3	IO3
AF26	GND	GND	GND

Table 13. 256 FBGA Pin Table

Pin	CY39030	CY39050	CY39100
A1	GND	GND	GND
A2	IO7	IO7	IO7
A3	IO7	IO7	IO7
A4	IO7	IO7	IO7
A5	IO7	IO7	IO7
A6	IO/V_{REF7}	IO/V_{REF7}	IO/V_{REF7}
A7	NC	IO/V_{REF7}	IO/V_{REF7}
A8	IO6/Lock	IO6/Lock	IO6/Lock
A9	IO6	IO6	IO6
A10	IO/V_{REF6}	IO/V_{REF6}	IO/V_{REF6}
A11	IO/V_{REF6}	IO/V_{REF6}	IO/V_{REF6}
A12	IO6	IO6	IO6
A13	IO6	IO6	IO6
A14	IO6	IO6	IO6
A15	IO6	IO6	IO6
A16	GND	GND	GND
B1	IO0	IO0	IO0
B2	GND	GND	GND
B3	IO7	IO7	IO7
B4	IO7	IO7	IO7
B5	IO7	IO7	IO7
B6	V_{CCIO7}	V_{CCIO7}	V_{CCIO7}
B7	V_{CC}	V_{CC}	V_{CC}

Table 13. 256 FBGA Pin Table (continued)

Pin	CY39030	CY39050	CY39100
B8	IO/V_{REF7}	IO/V_{REF7}	IO/V_{REF7}
B9	NC	IO/VR_{EF6}	IO/V_{REF6}
B10	V_{CCPLL}	V_{CCPLL}	V_{CCPLL}
B11	V_{CCIO6}	V_{CCIO6}	V_{CCIO6}
B12	IO6	IO6	IO6
B13	IO6	IO6	IO6
B14	IO6	IO6	IO6
B15	GND	GND	GND
B16	TDO	TDO	TDO
C1	IO0	IO0	IO0
C2	IO0	IO0	IO0
C3	GND	GND	GND
C4	IO7	IO7	IO7
C5	IO7	IO7	IO7
C6	V_{CCIO7}	V_{CCIO7}	V_{CCIO7}
C7	V_{CCIO7}	V_{CCIO7}	V_{CCIO7}
C8[19]	NC	IO7	IO7
C9[19]	IO6	IO6	IO6
C10	V_{CCIO6}	V_{CCIO6}	V_{CCIO6}
C11	V_{CCIO6}	V_{CCIO6}	V_{CCIO6}
C12	IO6	IO6	IO6
C13	IO6	IO6	IO6
C14	GND	GND	GND
C15	TDI	TDI	TDI
C16	IO5	IO5	IO5
D1	IO0	IO0	IO0
D2	IO0	IO0	IO0
D3	IO0	IO0	IO0
D4	GND	GND	GND
D5	IO7	IO7	IO7
D6	IO/V_{REF7}	IO/V_{REF7}	IO/V_{REF7}
D7	IO7	IO7	IO7
D8[19]	IO7	IO7	IO7
D9[19]	NC	IO6	IO6
D10	IO6	IO6	IO6
D11	IO/V_{REF6}	IO/V_{REF6}	IO/V_{REF6}
D12	IO6	IO6	IO6
D13	GND	GND	GND
D14	TCLK	TCLK	TCLK
D15	IO5	IO5	IO5
D16	IO5	IO5	IO5
E1	IO0	IO0	IO0
E2	IO0	IO0	IO0
E3	IO0	IO0	IO0

Table 13. 256 FBGA Pin Table (continued)

Pin	CY39030	CY39050	CY39100
E4	IO0	IO0	IO0
E5	IO7	IO7	IO7
E6	IO7	IO7	IO7
E7	IO7	IO7	IO7
E8[19]	IO7	IO7	IO7
E9[19]	IO6	IO6	IO6
E10	IO6	IO6	IO6
E11	IO6	IO6	IO6
E12	TMS	TMS	TMS
E13	IO5	IO5	IO5
E14	IO5	IO5	IO5
E15	IO5	IO5	IO5
E16	IO5	IO5	IO5
F1	IO0	IO0	IO0
F2	V_{CC}	V_{CC}	V_{CC}
F3	V_{CCIO0}	V_{CCIO0}	V_{CCIO0}
F4	IO/V_{REF0}	IO/V_{REF0}	IO/V_{REF0}
F5	IO0	IO0	IO0
F6	IO7	IO7	IO7
F7	GCTL3	GCTL3	GCTL3
F8	GCLK3	GCLK3	GCLK3
F9	GCTL2	GCTL2	GCTL2
F10	GCLK2	GCLK2	GCLK2
F11	IO5	IO5	IO5
F12	IO5	IO5	IO5
F13	IO/V_{REF5}	IO/V_{REF5}	IO/V_{REF5}
F14	V_{CCIO5}	V_{CCIO5}	V_{CCIO5}
F15	V_{CCJTAG}	V_{CCJTAG}	V_{CCJTAG}
F16	IO5	IO5	IO5
G1	IO0	IO0	IO0
G2	NC	NC	V_{CC}
G3	V_{CCIO0}	V_{CCIO0}	V_{CCIO0}
G4	IO/V_{REF0}	IO/V_{REF0}	IO/V_{REF0}
G5	IO0	IO0	IO0
G6	GCTL0	GCTL0	GCTL0
G7	GND	GND	GND
G8	GND	GND	GND
G9	GND	GND	GND
G10	GND	GND	GND
G11	GCTL1	GCTL1	GCTL1
G12	IO5	IO5	IO5
G13	IO/V_{REF5}	IO/V_{REF5}	IO/V_{REF5}
G14	V_{CCIO5}	V_{CCIO5}	V_{CCIO5}
G15	NC	NC	VCC

Table 13. 256 FBGA Pin Table (continued)

Pin	CY39030	CY39050	CY39100
G16	IO5	IO5	IO5
H1[19]	IO0	IO0	IO0
H2[19]	IO0	IO0	IO0
H3[19]	IO0	IO0	IO0
H4	IO/V_{REF0}	IO/V_{REF0}	IO/V_{REF0}
H5	IO0	IO0	IO0
H6	GCLK0	GCLK0	GCLK0
H7	GND	GND	GND
H8	GND	GND	GND
H9	GND	GND	GND
H10	GND	GND	GND
H11	GCLK1	GCLK1	GCLK1
H12	IO5	IO5	IO5
H13	IO/V_{REF5}	IO/V_{REF5}	IO/V_{REF5}
H14[19]	IO5	IO5	IO5
H15[19]	IO5	IO5	IO5
H16[19]	IO5	IO5	IO5
J1	IO1	IO1	IO1
J2	IO1	IO1	IO1
J3[19]	IO1	IO1	IO1
J4[19]	IO1	IO1	IO1
J5[19]	IO1	IO1	IO1
J6	IO1	IO1	IO1
J7	GND	GND	GND
J8	GND	GND	GND
J9	GND	GND	GND
J10	GND	GND	GND
J11	IO4	IO4	IO4
J12[19]	IO4	IO4	IO4
J13[19]	IO4	IO4	IO4
J14[19]	IO4	IO4	IO4
J15	IO5	IO5	IO5
J16	IO5	IO5	IO5
K1	IO1	IO1	IO1
K2	V_{CCPRG}	V_{CCPRG}	V_{CCPRG}
K3	V_{CCIO1}	V_{CCIO1}	V_{CCIO1}
K4	IO/V_{REF1}	IO/V_{REF1}	IO/V_{REF1}
K5	IO1	IO1	IO1
K6	IO1	IO1	IO1
K7	GND	GND	GND
K8	GND	GND	GND
K9	GND	GND	GND
K10	GND	GND	GND
K11	IO4	IO4	IO4

Table 13. 256 FBGA Pin Table (continued)

Pin	CY39030	CY39050	CY39100
K12	IO4	IO4	IO4
K13	IO/V_{REF4}	IO/V_{REF4}	IO/V_{REF4}
K14	V_{CCIO4}	V_{CCIO4}	V_{CCIO4}
K15	V_{CCPRG}	V_{CCPRG}	V_{CCPRG}
K16	IO4	IO4	IO4
L1	IO1	IO1	IO1
L2	NC	NC	V_{CC}
L3	V_{CCIO1}	V_{CCIO1}	V_{CCIO1}
L4	IO/V_{REF1}	IO/V_{REF1}	IO/V_{REF1}
L5	V_{CCCNFG}	V_{CCCNFG}	V_{CCCNFG}
L6	Config_Done	Config_Done	Config_Done
L7	IO2	IO2	IO2
L8[19]	IO2	IO2	IO2
L9[19]	IO3	IO3	IO3
L10	IO3	IO3	IO3
L11	IO3	IO3	IO3
L12	IO4	IO4	IO4
L13	IO/V_{REF4}	IO/V_{REF4}	IO/V_{REF4}
L14	V_{CCIO4}	V_{CCIO4}	V_{CCIO4}
L15	V_{CC}	V_{CC}	V_{CC}
L16	IO4	IO4	IO4
M1	IO1	IO1	IO1
M2	IO1	IO1	IO1
M3	IO1	IO1	IO1
M4	Data	Data	Data
M5	Reconfig	Reconfig	Reconfig
M6	IO2	IO2	IO2
M7	IO2	IO2	IO2
M8[19]	IO2	IO2	IO2
M9[19]	IO3	IO3	IO3
M10	IO3	IO3	IO3
M11	IO3	IO3	IO3
M12	IO3	IO3	IO3
M13	IO4	IO4	IO4
M14	IO4	IO4	IO4
M15	IO4	IO4	IO4
M16	IO4	IO4	IO4
N1	IO/V_{REF1}	IO/V_{REF1}	IO/V_{REF1}
N2	IO1	IO1	IO1
N3	IO1	IO1	IO1
N4	GND	GND	GND
N5	MSEL	MSEL	MSEL
N6	IO/V_{REF2}	IO/V_{REF2}	IO/V_{REF2}
N7	IO/V_{REF2}	IO/V_{REF2}	IO/V_{REF2}

Table 13. 256 FBGA Pin Table (continued)

Pin	CY39030	CY39050	CY39100
N8[19]	IO2	IO2	IO2
N9[19]	IO3	IO3	IO3
N10	IO/V_{REF3}	IO/V_{REF3}	IO/V_{REF3}
N11	IO/V_{REF3}	IO/V_{REF3}	IO/V_{REF3}
N12	IO3	IO3	IO3
N13	GND	GND	GND
N14	IO4	IO4	IO4
N15	IO4	IO4	IO4
N16	IO/V_{REF4}	IO/V_{REF4}	IO/V_{REF4}
P1	IO1	IO1	IO1
P2	IO1	IO1	IO1
P3	GND	GND	GND
P4	CCE	CCE	CCE
P5	IO2	IO2	IO2
P6	V_{CCIO2}	V_{CCIO2}	V_{CCIO2}
P7	V_{CCIO2}	V_{CCIO2}	V_{CCIO2}
P8	IO2	IO2	IO2
P9	IO2	IO2	IO2
P10	V_{CCIO3}	V_{CCIO3}	V_{CCIO3}
P11	V_{CCIO3}	V_{CCIO3}	V_{CCIO3}
P12	IO3	IO3	IO3
P13	IO3	IO3	IO3
P14	GND	GND	GND
P15	IO4	IO4	IO4
P16	IO4	IO4	IO4
R1	IO1	IO1	IO1
R2	GND	GND	GND
R3	CCLK	CCLK	CCLK
R4	IO2	IO2	IO2
R5	IO2	IO2	IO2
R6	V_{CCCNFG}	V_{CCCNFG}	V_{CCCNFG}
R7	V_{CCIO2}	V_{CCIO2}	V_{CCIO2}
R8	IO2	IO2	IO2
R9	IO2	IO2	IO2
R10	V_{CC}	V_{CC}	V_{CC}
R11	V_{CCIO3}	V_{CCIO3}	V_{CCIO3}
R12	IO3	IO3	IO3
R13	IO3	IO3	IO3
R14	IO3	IO3	IO3
R15	GND	GND	GND
R16	IO4	IO4	IO4
T1	GND	GND	GND
T2	Reset	Reset	Reset
T3	IO2	IO2	IO2

Table 13. 256 FBGA Pin Table (continued)

Pin	CY39030	CY39050	CY39100
T4	IO2	IO2	IO2
T5	IO2	IO2	IO2
T6	IO/V_{REF2}	IO/V_{REF2}	IO/V_{REF2}
T7	NC	IO/V_{REF2}	IO/V_{REF2}
T8	IO2	IO2	IO2
T9	IO2	IO2	IO2
T10	NC	IO/V_{REF3}	IO/V_{REF3}
T11	IO/V_{REF3}	IO/V_{REF3}	IO/V_{REF3}
T12	IO3	IO3	IO3
T13	IO3	IO3	IO3
T14	IO3	IO3	IO3
T15	IO3	IO3	IO3
T16	GND	GND	GND

Table 14. 484 FBGA Pin Table

Pin	CY39050	CY39100	CY39200
A1	GND	GND	GND
A2	GND	GND	GND
A3	NC	NC	IO/V_{REF7}
A4	NC	NC	IO/V_{REF7}
A5	IO7	IO7	IO7
A6	IO7	IO7	IO7
A7	NC	IO7	IO7
A8	IO7	IO7	IO7
A9	IO7	IO7	IO7
A10	IO7	IO7	IO7
A11	GND	GND	GND
A12	GND	GND	GND
A13	IO6	IO6	IO6
A14	IO6	IO6	IO6
A15	IO6	IO6	IO6
A16	NC	IO6	IO6
A17	IO6	IO6	IO6
A18	IO6	IO6	IO6
A19	NC	NC	IO/V_{REF6}
A20	NC	NC	IO6
A21	GND	GND	GND
A22	GND	GND	GND
B1	GND	GND	GND
B2	GND	GND	GND
B3	NC	NC	IO7
B4	V_{CCIO7}	V_{CCIO7}	V_{CCIO7}
B5	NC	IO7	IO7
B6	IO7	IO7	IO7

Table 14. 484 FBGA Pin Table (continued)

Pin	CY39050	CY39100	CY39200
B7	NC	IO7	IO7
B8	IO/V_{REF7}	IO/V_{REF7}	IO/V_{REF7}
B9	NC	NC	V_{CCIO7}
B10	IO7	IO7	IO7
B11	IO7	IO7	IO7
B12	IO6	IO6	IO6
B13	IO6	IO6	IO6
B14	NC	NC	V_{CCIO6}
B15	IO/V_{REF6}	IO/V_{REF6}	IO/V_{REF6}
B16	NC	IO6	IO6
B17	IO6	IO6	IO6
B18	IO6	IO6	IO6
B19	V_{CCIO6}	V_{CCIO6}	V_{CCIO6}
B20	NC	NC	IO6
B21	GND	GND	GND
B22	GND	GND	GND
C1	NC	NC	IO7
C2	NC	NC	IO7
C3	NC	NC	IO7
C4	NC	IO7	IO7
C5	NC	IO7	IO7
C6	IO7	IO7	IO7
C7	NC	IO7	IO7
C8	IO7	IO7	IO7
C9	IO7	IO7	IO7
C10	IO/$_{VREF7}$	IO/$_{VREF7}$	IO/V_{REF7}
C11	IO7	IO7	IO7
C12	IO6	IO6	IO6
C13	NC	IO/V_{REF6}	IO/V_{REF6}
C14	IO6	IO6	IO6
C15	IO6	IO6	IO6
C16	NC	IO6	IO6
C17	IO6	IO6	IO6
C18	IO6	IO6	IO6
C19	IO6	IO6	IO6
C20	NC	NC	IO6
C21	NC	NC	IO6
C22	NC	NC	IO6
D1	NC	NC	IO/V_{REF0}
D2	V_{CCIO0}	V_{CCIO0}	V_{CCIO0}
D3	NC	NC	IO0
D4	GND	GND	GND
D5	NC	IO7	IO7
D6	NC	IO7	IO7

Table 14. 484 FBGA Pin Table (continued)

Pin	CY39050	CY39100	CY39200
D7	IO7	IO7	IO7
D8	IO7	IO7	IO7
D9	IO/V_{REF7}	IO/V_{REF7}	IO/V_{REF7}
D10	NC	IO/V_{REF7}	IO/V_{REF7}
D11	IO6/Lock	IO6/Lock	IO6/Lock
D12	IO6	IO6	IO6
D13	IO/V_{REF6}	IO/V_{REF6}	IO/V_{REF6}
D14	IO/V_{REF6}	IO/V_{REF6}	IO/V_{REF6}
D15	IO6	IO6	IO6
D16	NC	IO6	IO6
D17	NC	IO6	IO6
D18	IO6	IO6	IO6
D19	GND	GND	GND
D20	NC	NC	IO5
D21	V_{CCIO5}	V_{CCIO5}	V_{CCIO5}
D22	NC	NC	IO/V_{REF5}
E1	NC	NC	IO0
E2	NC	NC	IO0
E3	NC	NC	IO0
E4	IO0	IO0	IO0
E5	GND	GND	GND
E6	IO7	IO7	IO7
E7	IO7	IO7	IO7
E8	IO7	IO7	IO7
E9	V_{CCIO7}	V_{CCIO7}	V_{CCIO7}
E10	V_{CC}	V_{CC}	V_{CC}
E11	IO/V_{REF7}	IO/V_{REF7}	IO/V_{REF7}
E12	NC	IO/V_{REF6}	IO/V_{REF6}
E13	V_{CCPLL}	V_{CCPLL}	V_{CCPLL}
E14	V_{CCIO6}	V_{CCIO6}	V_{CCIO6}
E15	NC	IO6	IO6
E16	NC	IO6	IO6
E17	NC	IO6	IO6
E18	GND	GND	GND
E19	TDO	TDO	TDO
E20	NC	NC	IO5
E21	NC	NC	IO5
E22	NC	NC	IO5
F1	NC	NC	IO0
F2	NC	IO0	IO0
F3	IO0	IO0	IO0
F4	IO0	IO0	IO0
F5	IO0	IO0	IO0
F6	GND	GND	GND

Table 14. 484 FBGA Pin Table (continued)

Pin	CY39050	CY39100	CY39200
F7	IO7	IO7	IO7
F8	IO7	IO7	IO7
F9	V_{CCIO7}	V_{CCIO7}	V_{CCIO7}
F10	V_{CCIO7}	V_{CCIO7}	V_{CCIO7}
F11[19]	IO7	IO7	IO7
F12[19]	IO6	IO6	IO6
F13	V_{CCIO6}	V_{CCIO6}	V_{CCIO6}
F14	V_{CCIO6}	V_{CCIO6}	V_{CCIO6}
F15	IO6	IO6	IO6
F16	NC	IO6	IO6
F17	GND	GND	GND
F18	TDI	TDI	TDI
F19	IO5	IO5	IO5
F20	IO5	IO5	IO5
F21	NC	IO5	IO5
F22	NC	NC	IO5
G1	NC	NC	IO0
G2	IO0	IO0	IO0
G3	NC	IO0	IO0
G4	IO0	IO0	IO0
G5	IO0	IO0	IO0
G6	IO0	IO0	IO0
G7	GND	GND	GND
G8	IO7	IO7	IO7
G9	NC	IO/V_{REF7}	IO/V_{REF7}
G10	IO7	IO7	IO7
G11[19]	IO7	IO7	IO7
G12[19]	IO6	IO6	IO6
G13	IO6	IO6	IO6
G14	IO/V_{REF6}	IO/V_{REF6}	IO/V_{REF6}
G15	IO6	IO6	IO6
G16	GND	GND	GND
G17	TCLK	TCLK	TCLK
G18	IO5	IO5	IO5
G19	IO5	IO5	IO5
G20	IO5	IO5	IO5
G21	IO5	IO5	IO5
G22	NC	NC	IO5
H1	NC	NC	IO0
H2	IO0	IO0	IO0
H3	IO0	IO0	IO0
H4	IO0	IO0	IO0
H5	NC	IO0	IO0
H6	NC	IO0	IO0

Table 14. 484 FBGA Pin Table (continued)

Pin	CY39050	CY39100	CY39200
H7	NC	IO0	IO0
H8	IO7	IO7	IO7
H9	IO7	IO7	IO7
H10	IO7	IO7	IO7
H11[19]	IO7	IO7	IO7
H12[19]	IO6	IO6	IO6
H13	IO6	IO6	IO6
H14	IO6	IO6	IO6
H15	TMS	TMS	TMS
H16	IO5	IO5	IO5
H17	IO5	IO5	IO5
H18	IO5	IO5	IO5
H19	IO5	IO5	IO5
H20	IO5	IO5	IO5
H21	IO5	IO5	IO5
H22	NC	NC	IO5
J1	NC	NC	IO/V_{REF0}
J2	NC	NC	VCCIO0
J3	NC	IO/V_{REF0}	IO/V_{REF0}
J4	NC	IO0	IO0
J5	NC	V_{CC}	V_{CC}
J6	V_{CCIO0}	V_{CCIO0}	V_{CCIO0}
J7	IO/V_{REF0}	IO/V_{REF0}	IO/V_{REF0}
J8	NC	IO0	IO0
J9	IO7	IO7	IO7
J10	GCTL3	GCTL3	GCTL3
J11	GCLK3	GCLK3	GCLK3
J12	GCTL2	GCTL2	GCTL2
J13	GCLK2	GCLK2	GCLK2
J14	IO5	IO5	IO5
J15	IO5	IO5	IO5
J16	IO/V_{REF5}	IO/V_{REF5}	IO/V_{REF5}
J17	V_{CCIO5}	V_{CCIO5}	V_{CCIO5}
J18	V_{CCJTAG}	V_{CCJTAG}	V_{CCJTAG}
J19	NC	IO5	IO5
J20	NC	IO/V_{REF5}	IO/V_{REF5}
J21	NC	NC	V_{CCIO5}
J22	NC	NC	IO/V_{REF5}
K1	NC	NC	IO0
K2	IO0	IO0	IO0
K3	NC	IO0	IO0
K4	IO0	IO0	IO0
K5	V_{CC}	V_{CC}	V_{CC}
K6	V_{CCIO0}	V_{CCIO0}	V_{CCIO0}

Table 14. 484 FBGA Pin Table (continued)

Pin	CY39050	CY39100	CY39200
K7	IO/V_{REF0}	IO/V_{REF0}	IO/V_{REF0}
K8	NC	IO0	IO0
K9	GCTL0	GCTL0	GCTL0
K10	GND	GND	GND
K11	GND	GND	GND
K12	GND	GND	GND
K13	GND	GND	GND
K14	GCTL1	GCTL1	GCTL1
K15	NC	IO5	IO5
K16	IO/V_{REF5}	IO/V_{REF5}	IO/V_{REF5}
K17	V_{CCIO5}	V_{CCIO5}	V_{CCIO5}
K18	NC	V_{CC}	V_{CC}
K19	NC	IO5	IO5
K20	NC	IO5	IO5
K21	NC	IO5	IO5
K22	NC	NC	IO5
L1	GND	GND	GND
L2	IO0	IO0	IO0
L3	IO0	IO0	IO0
L4[19]	IO0	IO0	IO0
L5[19]	IO0	IO0	IO0
L6[19]	IO0	IO0	IO0
L7	IO/V_{REF0}	IO/V_{REF0}	IO/V_{REF0}
L8	NC	IO0	IO0
L9	GCLK0	GCLK0	GCLK0
L10	GND	GND	GND
L11	GND	GND	GND
L12	GND	GND	GND
L13	GND	GND	GND
L14	GCLK1	GCLK1	GCLK1
L15	NC	IO5	IO5
L16	IO/V_{REF5}	IO/V_{REF5}	IO/V_{REF5}
L17[19]	IO5	IO5	IO5
L18[19]	IO5	IO5	IO5
L19[19]	IO5	IO5	IO5
L20	IO5	IO5	IO5
L21	NC	IO5	IO5
L22	GND	GND	GND
M1	GND	GND	GND
M2	NC	IO1	IO1
M3	IO1	IO1	IO1
M4	IO1	IO1	IO1
M5	NC	IO1	IO1
M6[19]	IO1	IO1	IO1

Table 14. 484 FBGA Pin Table (continued)

Pin	CY39050	CY39100	CY39200
M7[19]	IO1	IO1	IO1
M8[19]	IO1	IO1	IO1
M9	IO1	IO1	IO1
M10	GND	GND	GND
M11	GND	GND	GND
M12	GND	GND	GND
M13	GND	GND	GND
M14	IO4	IO4	IO4
M15[19]	IO4	IO4	IO4
M16[19]	IO4	IO4	IO4
M17[19]	IO4	IO4	IO4
M18	NC	IO5	IO5
M19	NC	IO5	IO5
M20	IO4	IO4	IO4
M21	IO4	IO4	IO4
M22	GND	GND	GND
N1	NC	NC	IO1
N2	NC	IO1	IO1
N3	NC	IO1	IO1
N4	NC	IO1	IO1
N5	V_{CCPRG}	V_{CCPRG}	V_{CCPRG}
N6	V_{CCIO1}	V_{CCIO1}	V_{CCIO1}
N7	IO/V_{REF1}	IO/V_{REF1}	IO/V_{REF1}
N8	NC	IO1	IO1
N9	NC	IO1	IO1
N10	GND	GND	GND
N11	GND	GND	GND
N12	GND	GND	GND
N13	GND	GND	GND
N14	NC	IO4	IO4
N15	IO4	IO4	IO4
N16	IO/V_{REF4}	IO/V_{REF4}	IO/V_{REF4}
N17	V_{CCIO4}	V_{CCIO4}	V_{CCIO4}
N18	V_{CCPRG}	V_{CCPRG}	V_{CCPRG}
N19	NC	IO4	IO4
N20	NC	IO4	IO4
N21	NC	IO4	IO4
N22	NC	NC	IO4
P1	NC	NC	IO/V_{REF1}
P2	NC	NC	V_{CCIO1}
P3	IO/V_{REF1}	IO/V_{REF1}	IO/V_{REF1}
P4	NC	IO1	IO1
P5	V_{CC}	V_{CC}	V_{CC}
P6	V_{CCIO1}	V_{CCIO1}	V_{CCIO1}

Table 14. 484 FBGA Pin Table (continued)

Pin	CY39050	CY39100	CY39200
P7	NC	IO/V_{REF1}	IO/V_{REF1}
P8	V_{CCCNFG}	V_{CCCNFG}	V_{CCCNFG}
P9	Config_Done	Config_Done	Config_Done
P10	IO2	IO2	IO2
P11[19]	IO2	IO2	IO2
P12[19]	IO3	IO3	IO3
P13	IO3	IO3	IO3
P14	IO3	IO3	IO3
P15	NC	IO4	IO4
P16	IO/V_{REF4}	IO/V_{REF4}	IO/V_{REF4}
P17	V_{CCIO4}	V_{CCIO4}	V_{CCIO4}
P18	V_{CC}	V_{CC}	V_{CC}
P19	NC	IO4	IO4
P20	NC	IO/V_{REF4}	IO/V_{REF4}
P21	NC	NC	V_{CCIO4}
P22	NC	NC	IO/V_{REF4}
R1	NC	NC	IO1
R2	NC	IO1	IO1
R3	IO1	IO1	IO1
R4	IO1	IO1	IO1
R5	IO1	IO1	IO1
R6	IO1	IO1	IO1
R7	Data	Data	Data
R8	Reconfig	Reconfig	Reconfig
R9	IO2	IO2	IO2
R10	IO2	IO2	IO2
R11[19]	IO2	IO2	IO2
R12[19]	IO3	IO3	IO3
R13	IO3	IO3	IO3
R14	IO3	IO3	IO3
R15	NC	IO3	IO3
R16	NC	IO4	IO4
R17	NC	IO4	IO4
R18	NC	IO4	IO4
R19	IO4	IO4	IO4
R20	IO4	IO4	IO4
R21	IO4	IO4	IO4
R22	NC	NC	IO4
T1	NC	NC	IO1
T2	IO1	IO1	IO1
T3	IO1	IO1	IO1
T4	IO/V_{REF1}	IO/V_{REF1}	IO/V_{REF1}
T5	IO1	IO1	IO1
T6	IO1	IO1	IO1

Table 14. 484 FBGA Pin Table (continued)

Pin	CY39050	CY39100	CY39200
T7	GND	GND	GND
T8	MSEL	MSEL	MSEL
T9	IO/V_{REF2}	IO/V_{REF2}	IO/V_{REF2}
T10	IO/V_{REF2}	IO/V_{REF2}	IO/V_{REF2}
T11[19]	IO2	IO2	IO2
T12[19]	IO3	IO3	IO3
T13	IO/V_{REF3}	IO/V_{REF3}	IO/V_{REF3}
T14	IO/V_{REF3}	IO/V_{REF3}	IO/V_{REF3}
T15	IO3	IO3	IO3
T16	GND	GND	GND
T17	IO4	IO4	IO4
T18	IO4	IO4	IO4
T19	IO/V_{REF4}	IO/V_{REF4}	IO/V_{REF4}
T20	IO4	IO4	IO4
T21	IO4	IO4	IO4
T22	NC	NC	IO4
U1	NC	NC	IO1
U2	IO1	IO1	IO1
U3	IO1	IO1	IO1
U4	IO1	IO1	IO1
U5	IO1	IO1	IO1
U6	GND	GND	GND
U7	CCE	CCE	CCE
U8	IO2	IO2	IO2
U9	V_{CCIO2}	V_{CCIO2}	V_{CCIO2}
U10	V_{CCIO2}	V_{CCIO2}	V_{CCIO2}
U11	IO2	IO2	IO2
U12	IO2	IO2	IO2
U13	V_{CCIO3}	V_{CCIO3}	V_{CCIO3}
U14	V_{CCIO3}	V_{CCIO3}	V_{CCIO3}
U15	IO3	IO3	IO3
U16	IO3	IO3	IO3
U17	GND	GND	GND
U18	IO4	IO4	IO4
U19	IO4	IO4	IO4
U20	IO4	IO4	IO4
U21	IO4	IO4	IO4
U22	NC	NC	IO4
V1	NC	NC	IO1
V2	NC	NC	IO1
V3	NC	NC	IO1
V4	NC	NC	IO1
V5	GND	GND	GND
V6	CCLK	CCLK	CCLK

Table 14. 484 FBGA Pin Table (continued)

Pin	CY39050	CY39100	CY39200
V7	IO2	IO2	IO2
V8	NC	IO2	IO2
V9	V_{CCCNFG}	V_{CCCNFG}	V_{CCCNFG}
V10	V_{CCIO2}	V_{CCIO2}	V_{CCIO2}
V11	IO2	IO2	IO2
V12	IO2	IO2	IO2
V13	NC	V_{CC}	V_{CC}
V14	V_{CCIO3}	V_{CCIO3}	V_{CCIO3}
V15	IO3	IO3	IO3
V16	IO3	IO3	IO3
V17	IO3	IO3	IO3
V18	GND	GND	GND
V19	NC	NC	IO4
V20	NC	NC	IO4
V21	NC	NC	IO4
V22	NC	NC	IO4
W1	NC	NC	IO/V_{REF1}
W2	V_{CCIO1}	V_{CCIO1}	V_{CCIO1}
W3	NC	NC	IO1
W4	GND	GND	GND
W5	Reset	Reset	Reset
W6	IO2	IO2	IO2
W7	NC	IO2	IO2
W8	IO2	IO2	IO2
W9	NC	IO/V_{REF2}	IO/V_{REF2}
W10	NC	IO/V_{REF2}	IO/V_{REF2}
W11	IO2	IO2	IO2
W12	IO2	IO2	IO2
W13	NC	IO/V_{REF3}	IO/V_{REF3}
W14	NC	IO/V_{REF3}	IO/V_{REF3}
W15	IO3	IO3	IO3
W16	IO3	IO3	IO3
W17	IO3	IO3	IO3
W18	NC	IO3	IO3
W19	GND	GND	GND
W20	NC	NC	IO4
W21	V_{CCIO4}	V_{CCIO4}	V_{CCIO4}
W22	NC	NC	IO/V_{REF4}
Y1	NC	NC	IO2
Y2	NC	NC	IO2
Y3	NC	NC	IO2
Y4	IO2	IO2	IO2
Y5	IO2	IO2	IO2
Y6	IO2	IO2	IO2

Table 14. 484 FBGA Pin Table (continued)

Pin	CY39050	CY39100	CY39200
Y7	IO2	IO2	IO2
Y8	NC	IO2	IO2
Y9	NC	IO2	IO2
Y10	IO/V_{REF2}	IO/V_{REF2}	IO/V_{REF2}
Y11	IO2	IO2	IO2
Y12	IO3	IO3	IO3
Y13	IO/V_{REF3}	IO/V_{REF3}	IO/V_{REF3}
Y14	IO3	IO3	IO3
Y15	IO3	IO3	IO3
Y16	IO3	IO3	IO3
Y17	IO3	IO3	IO3
Y18	NC	IO3	IO3
Y19	NC	IO3	IO3
Y20	NC	NC	IO3
Y21	NC	NC	IO3
Y22	NC	NC	IO3
AA1	GND	GND	GND
AA2	GND	GND	GND
AA3	NC	NC	IO2
AA4	V_{CCIO2}	V_{CCIO2}	V_{CCIO2}
AA5	IO/V_{REF2}	IO/V_{REF2}	IO/V_{REF2}
AA6	IO2	IO2	IO2
AA7	NC	IO2	IO2
AA8	IO2	IO2	IO2
AA9	NC	NC	V_{CCIO2}
AA10	NC	IO2	IO2
AA11	IO2	IO2	IO2
AA12	IO3	IO3	IO3
AA13	IO3	IO3	IO3
AA14	NC	NC	V_{CCIO3}
AA15	IO3	IO3	IO3
AA16	NC	IO3	IO3
AA17	NC	IO3	IO3
AA18	IO/V_{REF3}	IO/V_{REF3}	IO/V_{REF3}
AA19	V_{CCIO3}	V_{CCIO3}	V_{CCIO3}
AA20	NC	NC	IO3
AA21	GND	GND	GND
AA22	GND	GND	GND
AB1	GND	GND	GND
AB2	GND	GND	GND
AB3	NC	NC	IO/V_{REF2}
AB4	NC	NC	IO/V_{REF2}
AB5	IO2	IO2	IO2
AB6	IO2	IO2	IO2

Table 14. 484 FBGA Pin Table (continued)

Pin	CY39050	CY39100	CY39200
AB7	IO2	IO2	IO2
AB8	NC	IO2	IO2
AB9	NC	IO2	IO2
AB10	NC	IO2	IO2
AB11	GND	GND	GND
AB12	GND	GND	GND
AB13	IO3	IO3	IO3
AB14	IO3	IO3	IO3
AB15	IO3	IO3	IO3
AB16	NC	IO3	IO3
AB17	IO3	IO3	IO3
AB18	NC	IO3	IO3
AB19	NC	NC	IO/V_{REF3}
AB20	NC	NC	IO3
AB21	GND	GND	GND
AB22	GND	GND	GND

Table 15. 676 FBGA Pin Table

Pin	CY39100	CY39200
A1	GND	GND
A2	NC	NC
A3	NC	IO7
A4	NC	IO7
A5	NC	IO7
A6	NC	V_{CCIO7}
A7	NC	IO7
A8	NC	IO7
A9	NC	IO7
A10	NC	NC
A11	NC	V_{CCIO7}
A12	NC	NC
A13	GND	GND
A14	GND	GND
A15	NC	NC
A16	NC	V_{CCIO6}
A17	NC	NC
A18	NC	IO6
A19	NC	IO6
A20	NC	IO6
A21	NC	V_{CCIO6}
A22	NC	IO6
A23	NC	IO6
A24	NC	IO6
A25	NC	NC

Table 15. 676 FBGA Pin Table (continued)

Pin	CY39100	CY39200
A26	GND	GND
B1	NC	NC
B2	GND	GND
B3	NC	IO7
B4	NC	IO7
B5	NC	IO7
B6	NC	NC
B7	NC	IO7
B8	NC	IO7
B9	NC	IO7
B10	NC	IO7
B11	NC	IO7
B12	NC	IO7
B13	GND	GND
B14	GND	GND
B15	NC	IO6
B16	NC	IO6
B17	NC	IO6
B18	NC	IO6
B19	NC	IO6
B20	NC	IO6
B21	NC	IO/V_{REF6}
B22	NC	IO6
B23	NC	IO6
B24	NC	NC
B25	GND	GND

Table 15. 676 FBGA Pin Table (continued)

Pin	CY39100	CY39200
B26	NC	NC
C1	NC	NC
C2	NC	NC
C3	GND	GND
C4	GND	GND
C5	NC	IO/V_{REF7}
C6	NC	IO/V_{REF7}
C7	IO7	IO7
C8	IO7	IO7
C9	IO7	IO7
C10	IO7	IO7
C11	IO7	IO7
C12	IO7	IO7
C13	GND	GND
C14	GND	GND
C15	IO6	IO6
C16	IO6	IO6
C17	IO6	IO6
C18	IO6	IO6
C19	IO6	IO6
C20	IO6	IO6
C21	NC	IO/V_{REF6}
C22	NC	IO6
C23	GND	GND
C24	GND	GND
C25	NC	NC
C26	NC	NC
D1	NC	NC
D2	NC	NC
D3	GND	GND
D4	GND	GND
D5	NC	IO7
D6	V_{CCIO7}	V_{CCIO7}
D7	IO7	IO7
D8	IO7	IO7
D9	IO7	IO7
D10	IO/V_{REF7}	IO/V_{REF7}
D11	NC	V_{CCIO7}
D12	IO7	IO7
D13	IO7	IO7
D14	IO6	IO6
D15	IO6	IO6
D16	NC	V_{CCIO6}
D17	IO/V_{REF6}	IO/V_{REF6}

Table 15. 676 FBGA Pin Table (continued)

Pin	CY39100	CY39200
D18	IO6	IO6
D19	IO6	IO6
D20	IO6	IO6
D21	V_{CCIO6}	V_{CCIO6}
D22	NC	IO6
D23	GND	GND
D24	GND	GND
D25	NC	NC
D26	NC	NC
E1	NC	NC
E2	NC	NC
E3	NC	IO7
E4	NC	IO7
E5	NC	IO7
E6	IO7	IO7
E7	IO7	IO7
E8	IO7	IO7
E9	IO7	IO7
E10	IO7	IO7
E11	IO7	IO7
E12	IO/V_{REF7}	IO/V_{REF7}
E13	IO7	IO7
E14	IO6	IO6
E15	IO/V_{REF6}	IO/V_{REF6}
E16	IO6	IO6
E17	IO6	IO6
E18	IO6	IO6
E19	IO6	IO6
E20	IO6	IO6
E21	IO6	IO6
E22	NC	IO6
E23	NC	IO6
E24	NC	IO6
E25	NC	NC
E26	NC	NC
F1	NC	NC
F2	NC	NC
F3	NC	IO/V_{REF0}
F4	V_{CCIO0}	V_{CCIO0}
F5	NC	IO0
F6	GND	GND
F7	IO7	IO7
F8	IO7	IO7
F9	IO7	IO7

Table 15. 676 FBGA Pin Table (continued)

Pin	CY39100	CY39200
F10	IO7	IO7
F11	IO/V_{REF7}	IO/V_{REF7}
F12	IO/V_{REF7}	IO/V_{REF7}
F13	IO6/Lock	IO6/Lock
F14	IO6	IO6
F15	IO/V_{REF6}	IO/V_{REF6}
F16	IO/V_{REF6}	IO/V_{REF6}
F17	IO6	IO6
F18	IO6	IO6
F19	IO6	IO6
F20	IO6	IO6
F21	GND	GND
F22	NC	IO5
F23	V_{CCIO5}	V_{CCIO5}
F24	NC	IO/V_{REF5}
F25	NC	NC
F26	NC	NC
G1	NC	NC
G2	NC	NC
G3	NC	IO0
G4	NC	IO0
G5	NC	IO0
G6	IO0	IO0
G7	GND	GND
G8	IO7	IO7
G9	IO7	IO7
G10	IO7	IO7
G11	V_{CCIO7}	V_{CCIO7}
G12	V_{CC}	V_{CC}
G13	IO/V_{REF7}	IO/V_{REF7}
G14	IO/V_{REF6}	IO/V_{REF6}
G15	V_{CCPLL}	V_{CCPLL}
G16	V_{CCIO6}	V_{CCIO6}
G17	IO6	IO6
G18	IO6	IO6
G19	IO6	IO6
G20	GND	GND
G21	TDO	TDO
G22	NC	IO5
G23	NC	IO5
G24	NC	IO5
G25	NC	NC
G26	NC	NC
H1	NC	NC

Table 15. 676 FBGA Pin Table (continued)

Pin	CY39100	CY39200
H2	NC	NC
H3	NC	IO0
H4	IO0	IO0
H5	IO0	IO0
H6	IO0	IO0
H7	IO0	IO0
H8	GND	GND
H9	IO7	IO7
H10	IO7	IO7
H11	V_{CCIO7}	V_{CCIO7}
H12	V_{CCIO7}	V_{CCIO7}
H13[19]	IO7	IO7
H14[19]	IO6	IO6
H15	V_{CCIO6}	V_{CCIO6}
H16	V_{CCIO6}	V_{CCIO6}
H17	IO6	IO6
H18	IO6	IO6
H19	GND	GND
H20	TDI	TDI
H21	IO5	IO5
H22	IO5	IO5
H23	IO5	IO5
H24	NC	IO5
H25	NC	NC
H26	NC	NC
J1	NC	NC
J2	NC	NC
J3	NC	IO0
J4	IO0	IO0
J5	IO0	IO0
J6	IO0	IO0
J7	IO0	IO0
J8	IO0	IO0
J9	GND	GND
J10	IO7	IO7
J11	IO/V_{REF7}	IO/V_{REF7}
J12	IO7	IO7
J13[19]	IO7	IO7
J14[19]	IO6	IO6
J15	IO6	IO6
J16	IO/V_{REF6}	IO/V_{REF6}
J17	IO6	IO6
J18	GND	GND
J19	TCLK	TCLK

Table 15. 676 FBGA Pin Table (continued)

Pin	CY39100	CY39200
J20	IO5	IO5
J21	IO5	IO5
J22	IO5	IO5
J23	IO5	IO5
J24	NC	IO5
J25	NC	NC
J26	NC	NC
K1	NC	NC
K2	NC	NC
K3	NC	IO0
K4	IO0	IO0
K5	IO0	IO0
K6	IO0	IO0
K7	IO0	IO0
K8	IO0	IO0
K9	IO0	IO0
K10	IO7	IO7
K11	IO7	IO7
K12	IO7	IO7
K13[19]	IO7	IO7
K14[19]	IO6	IO6
K15	IO6	IO6
K16	IO6	IO6
K17	TMS	TMS
K18	IO5	IO5
K19	IO5	IO5
K20	IO5	IO5
K21	IO5	IO5
K22	IO5	IO5
K23	IO5	IO5
K24	NC	IO5
K25	NC	NC
K26	NC	NC
L1	NC	NC
L2	NC	NC
L3	NC	IO/V_{REF0}
L4	NC	V_{CCIO0}
L5	IO/V_{REF0}	IO/V_{REF0}
L6	IO0	IO0
L7	V_{CC}	V_{CC}
L8	V_{CCIO0}	V_{CCIO0}
L9	IO/V_{REF0}	IO/V_{REF0}
L10	IO0	IO0
L11	IO7	IO7

Table 15. 676 FBGA Pin Table (continued)

Pin	CY39100	CY39200
L12	GCTL3	GCTL3
L13	GCLK3	GCLK3
L14	GCTL2	GCTL2
L15	GCLK2	GCLK2
L16	IO5	IO5
L17	IO5	IO5
L18	IO/V_{REF5}	IO/V_{REF5}
L19	V_{CCIO5}	V_{CCIO5}
L20	V_{CCJTAG}	V_{CCJTAG}
L21	IO5	IO5
L22	IO/V_{REF5}	IO/V_{REF5}
L23	NC	V_{CCIO5}
L24	NC	IO/V_{REF5}
L25	NC	NC
L26	NC	NC
M1	NC	NC
M2	NC	NC
M3	NC	IO0
M4	IO0	IO0
M5	IO0	IO0
M6	IO0	IO0
M7	V_{CC}	V_{CC}
M8	V_{CCIO0}	V_{CCIO0}
M9	IO/V_{REF0}	IO/V_{REF0}
M10	IO0	IO0
M11	GCTL0	GCTL0
M12	GND	GND
M13	GND	GND
M14	GND	GND
M15	GND	GND
M16	GCTL1	GCTL1
M17	IO5	IO5
M18	IO/V_{REF5}	IO/V_{REF5}
M19	V_{CCIO5}	V_{CCIO5}
M20	V_{CC}	V_{CC}
M21	IO5	IO5
M22	IO5	IO5
M23	IO5	IO5
M24	NC	IO5
M25	NC	NC
M26	NC	NC
N1	GND	GND
N2	GND	GND
N3	GND	GND

Table 15. 676 FBGA Pin Table (continued)

Pin	CY39100	CY39200
N4	IO0	IO0
N5	IO0	IO0
N6[19]	IO0	IO0
N7[19]	IO0	IO0
N8[19]	IO0	IO0
N9	IO/V_{REF0}	IO/V_{REF0}
N10	IO0	IO0
N11	GCLK0	GCLK0
N12	GND	GND
N13	GND	GND
N14	GND	GND
N15	GND	GND
N16	GCLK1	GCLK1
N17	IO5	IO5
N18	IO/V_{REF5}	IO/V_{REF5}
N19[19]	IO5	IO5
N20[19]	IO5	IO5
N21[19]	IO5	IO5
N22	IO5	IO5
N23	IO5	IO5
N24	GND	GND
N25	GND	GND
N26	GND	GND
P1	GND	GND
P2	GND	GND
P3	GND	GND
P4	IO1	IO1
P5	IO1	IO1
P6	IO1	IO1
P7	IO1	IO1
P8[19]	IO1	IO1
P9[19]	IO1	IO1
P10[19]	IO1	IO1
P11	IO1	IO1
P12	GND	GND
P13	GND	GND
P14	GND	GND
P15	GND	GND
P16	IO4	IO4
P17[19]	IO4	IO4
P18[19]	IO4	IO4
P19[19]	IO4	IO4
P20	IO5	IO5
P21	IO5	IO5

Table 15. 676 FBGA Pin Table (continued)

Pin	CY39100	CY39200
P22	IO4	IO4
P23	IO4	IO4
P24	GND	GND
P25	GND	GND
P26	GND	GND
R1	NC	NC
R2	NC	NC
R3	NC	IO1
R4	IO1	IO1
R5	IO1	IO1
R6	IO1	IO1
R7	V_{CCPRG}	V_{CCPRG}
R8	V_{CCIO1}	V_{CCIO1}
R9	IO/V_{REF1}	IO/V_{REF1}
R10	IO1	IO1
R11	IO1	IO1
R12	GND	GND
R13	GND	GND
R14	GND	GND
R15	GND	GND
R16	IO4	IO4
R17	IO4	IO4
R18	IO/V_{REF4}	IO/V_{REF4}
R19	V_{CCIO4}	V_{CCIO4}
R20	V_{CCPRG}	V_{CCPRG}
R21	IO4	IO4
R22	IO4	IO4
R23	IO4	IO4
R24	NC	IO4
R25	NC	NC
R26	NC	NC
T1	NC	NC
T2	NC	NC
T3	NC	IO/V_{REF1}
T4	NC	V_{CCIO1}
T5	IO/V_{REF1}	IO/V_{REF1}
T6	IO1	IO1
T7	V_{CC}	V_{CC}
T8	V_{CCIO1}	V_{CCIO1}
T9	IO/V_{REF1}	IO/V_{REF1}
T10	V_{CCCNFG}	V_{CCCNFG}
T11	Config_Done	Config_Done
T12	IO2	IO2
T13[19]	IO2	IO2

Table 15. 676 FBGA Pin Table (continued)

Pin	CY39100	CY39200
T14[19]	IO3	IO3
T15	IO3	IO3
T16	IO3	IO3
T17	IO4	IO4
T18	IO/V_{REF4}	IO/V_{REF4}
T19	V_{CCIO4}	V_{CCIO4}
T20	V_{CC}	V_{CC}
T21	IO4	IO4
T22	IO/V_{REF4}	IO/V_{REF4}
T23	NC	V_{CCIO4}
T24	NC	IO/V_{REF4}
T25	NC	NC
T26	NC	NC
U1	NC	NC
U2	NC	NC
U3	NC	IO1
U4	NC	IO1
U5	IO1	IO1
U6	IO1	IO1
U7	IO1	IO1
U8	IO1	IO1
U9	Data	Data
U10	Reconfig	Reconfig
U11	IO2	IO2
U12	IO2	IO2
U13[19]	IO2	IO2
U14[19]	IO3	IO3
U15	IO3	IO3
U16	IO3	IO3
U17	IO3	IO3
U18	IO4	IO4
U19	IO4	IO4
U20	IO4	IO4
U21	IO4	IO4
U22	IO4	IO4
U23	NC	IO4
U24	NC	IO4
U25	NC	NC
U26	NC	NC
V1	NC	NC
V2	NC	NC
V3	NC	IO1
V4	IO1	IO1
V5	IO1	IO1

Table 15. 676 FBGA Pin Table (continued)

Pin	CY39100	CY39200
V6	IO/V_{REF1}	IO/V_{REF1}
V7	IO1	IO1
V8	IO1	IO1
V9	GND	GND
V10	MSEL	MSEL
V11	IO/V_{REF2}	IO/V_{REF2}
V12	IO/V_{REF2}	IO/V_{REF2}
V13[19]	IO2	IO2
V14[19]	IO3	IO3
V15	IO/V_{REF3}	IO/V_{REF3}
V16	IO/V_{REF3}	IO/V_{REF3}
V17	IO3	IO3
V18	GND	GND
V19	IO4	IO4
V20	IO4	IO4
V21	IO/V_{REF4}	IO/V_{REF4}
V22	IO4	IO4
V23	IO4	IO4
V24	NC	IO4
V25	NC	NC
V26	NC	NC
W1	NC	NC
W2	NC	NC
W3	NC	IO1
W4	IO1	IO1
W5	IO1	IO1
W6	IO1	IO1
W7	IO1	IO1
W8	GND	GND
W9	CCE	CCE
W10	IO2	IO2
W11	V_{CCIO2}	V_{CCIO2}
W12	V_{CCIO2}	V_{CCIO2}
W13	IO2	IO2
W14	IO2	IO2
W15	V_{CCIO3}	V_{CCIO3}
W16	V_{CCIO3}	V_{CCIO3}
W17	IO3	IO3
W18	IO3	IO3
W19	GND	GND
W20	IO4	IO4
W21	IO4	IO4
W22	IO4	IO4
W23	IO4	IO4

Table 15. 676 FBGA Pin Table (continued)

Pin	CY39100	CY39200
W24	NC	IO4
W25	NC	NC
W26	NC	NC
Y1	NC	NC
Y2	NC	NC
Y3	NC	IO1
Y4	NC	IO1
Y5	NC	IO1
Y6	IO1	IO1
Y7	GND	GND
Y8	CCLK	CCLK
Y9	IO2	IO2
Y10	IO2	IO2
Y11	V_{CCCNFG}	V_{CCCNFG}
Y12	V_{CCIO2}	V_{CCIO2}
Y13	IO2	IO2
Y14	IO2	IO2
Y15	V_{CC}	V_{CC}
Y16	V_{CCIO3}	V_{CCIO3}
Y17	IO3	IO3
Y18	IO3	IO3
Y19	IO3	IO3
Y20	GND	GND
Y21	IO4	IO4
Y22	NC	IO4
Y23	NC	IO4
Y24	NC	IO4
Y25	NC	NC
Y26	NC	NC
AA1	NC	NC
AA2	NC	NC
AA3	NC	IO/V_{REF1}
AA4	V_{CCIO1}	V_{CCIO1}
AA5	NC	IO1
AA6	GND	GND
AA7	Reset	Reset
AA8	IO2	IO2
AA9	IO2	IO2
AA10	IO2	IO2
AA11	IO/V_{REF2}	IO/V_{REF2}
AA12	IO/V_{REF2}	IO/V_{REF2}
AA13	IO2	IO2
AA14	IO2	IO2
AA15	IO/V_{REF3}	IO/V_{REF3}

Table 15. 676 FBGA Pin Table (continued)

Pin	CY39100	CY39200
AA16	IO/V_{REF3}	IO/V_{REF3}
AA17	IO3	IO3
AA18	IO3	IO3
AA19	IO3	IO3
AA20	IO3	IO3
AA21	GND	GND
AA22	NC	IO4
AA23	V_{CCIO4}	V_{CCIO4}
AA24	NC	IO/V_{REF4}
AA25	NC	NC
AA26	NC	NC
AB1	NC	NC
AB2	NC	NC
AB3	NC	IO2
AB4	NC	IO2
AB5	NC	IO2
AB6	IO2	IO2
AB7	IO2	IO2
AB8	IO2	IO2
AB9	IO2	IO2
AB10	IO2	IO2
AB11	IO2	IO2
AB12	IO/V_{REF2}	IO/V_{REF2}
AB13	IO2	IO2
AB14	IO3	IO3
AB15	IO/V_{REF3}	IO/V_{REF3}
AB16	IO3	IO3
AB17	IO3	IO3
AB18	IO3	IO3
AB19	IO3	IO3
AB20	IO3	IO3
AB21	IO3	IO3
AB22	NC	IO3
AB23	NC	IO3
AB24	NC	IO3
AB25	NC	NC
AB26	NC	NC
AC1	NC	NC
AC2	NC	NC
AC3	GND	GND
AC4	GND	GND
AC5	NC	IO2
AC6	V_{CCIO2}	V_{CCIO2}
AC7	IO/V_{REF2}	IO/V_{REF2}

Table 15. 676 FBGA Pin Table (continued)

Pin	CY39100	CY39200
AC8	IO2	IO2
AC9	IO2	IO2
AC10	IO2	IO2
AC11	NC	V_{CCIO2}
AC12	IO2	IO2
AC13	IO2	IO2
AC14	IO3	IO3
AC15	IO3	IO3
AC16	NC	V_{CCIO3}
AC17	IO3	IO3
AC18	IO3	IO3
AC19	IO3	IO3
AC20	IO/V_{REF3}	IO/V_{REF3}
AC21	V_{CCIO3}	V_{CCIO3}
AC22	NC	IO3
AC23	GND	GND
AC24	GND	GND
AC25	NC	NC
AC26	NC	NC
AD1	NC	NC
AD2	NC	NC
AD3	GND	GND
AD4	GND	GND
AD5	NC	IO/V_{REF2}
AD6	NC	IO/V_{REF2}
AD7	IO2	IO2
AD8	IO2	IO2
AD9	IO2	IO2
AD10	IO2	IO2
AD11	IO2	IO2
AD12	IO2	IO2
AD13	GND	GND
AD14	GND	GND
AD15	IO3	IO3
AD16	IO3	IO3
AD17	IO3	IO3
AD18	IO3	IO3
AD19	IO3	IO3
AD20	IO3	IO3
AD21	NC	IO/V_{REF3}
AD22	NC	IO3
AD23	GND	GND
AD24	GND	GND
AD25	NC	NC

Table 15. 676 FBGA Pin Table (continued)

Pin	CY39100	CY39200
AD26	NC	NC
AE1	NC	NC
AE2	GND	GND
AE3	NC	IO2
AE4	NC	IO2
AE5	NC	IO2
AE6	NC	NC
AE7	NC	IO2
AE8	NC	IO2
AE9	NC	IO2
AE10	NC	IO2
AE11	NC	IO2
AE12	NC	IO2
AE13	GND	GND
AE14	GND	GND
AE15	NC	IO3
AE16	NC	IO3
AE17	NC	IO3
AE18	NC	IO3
AE19	NC	IO3
AE20	NC	IO3
AE21	NC	IO/V_{REF3}
AE22	NC	IO3
AE23	NC	IO3
AE24	NC	NC
AE25	GND	GND
AE26	NC	NC
AF1	GND	GND
AF2	NC	NC
AF3	NC	IO2
AF4	NC	IO2
AF5	NC	IO2
AF6	NC	V_{CCIO2}
AF7	NC	IO2
AF8	NC	IO2
AF9	NC	IO2
AF10	NC	NC
AF11	NC	V_{CCIO2}
AF12	NC	NC
AF13	GND	GND
AF14	GND	GND
AF15	NC	NC
AF16	NC	V_{CCIO3}

Table 15. 676 FBGA Pin Table (continued)

Pin	CY39100	CY39200
AF17	NC	NC
AF18	NC	IO3
AF19	NC	IO3
AF20	NC	IO3
AF21	NC	V_{CCIO3}
AF22	NC	IO3
AF23	NC	IO3
AF24	NC	IO3
AF25	NC	NC
AF26	GND	GND

Document History Page=

Document Title: Delta39K™ ISR™ CPLD Family CPLDs at FPGA Densities™ Document Number: 38-03039				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106503	05/30/01	SZV	Change from Spec #: 38-00830 to 38-03039
*A	107625	07/11/01	RN	Deleted 39K15 device and the associated -250-MHz bin specs Deleted 144FBGA package and associated part numbers Changed ESD spec from “MIL-STD-883” to “JEDEC EIA/JESD22-A114-A” Changed the Prime bin for 39K50 and 39K30 from “MHz” to “233 MHz” Changed the part ordering information accordingly Updated the -233-MHz timing specs to match modified timing specs achieved by design (main affected params: t_{PD}, t_{MCCO}, t_{IOS}, t_{SCS}, t_{SCS2}, f_{MAX2}, t_{CLMAA}, $t_{CLMCYC2}$, $t_{CHMCYC2}$, t_{CHMCLK}) Updated I/O standard Timing Delay Specs and changed the default I/O standard from 3.3V PCI to LVCMOS Added paragraph about Delta39K being CompactPCI hot swap Ready Added X8 mode in the PLL description Added Standby ICC spec Updated the recommended boot PROM for 39K165/200 to be CY3LV002 instead of CY3LV020
*B	109681	11/16/01	RN	Updated Delta39K family offering Modified PLL timing parameters t_{DWSA}, t_{DWOSA}, t_{MCCJ}, and t_{LOCK}. Added t_{INDUTY} parameter Deleted exception to CompactPCI Hot Swap compliance regarding “PCI buffers....” Added reference to app note “Hot Socketing Delta39K” Revised CompactPCI Hot Swap Specification R1.0 to be R2.0
*C	112376	12/21/01	RN	Combined with spec# 38-03040
*D	112946	04/04/02	RN	Updated pin tables for 39K30 (208PQFP, 256FBGA) Updated pin tables for 39K50 (208PQFP, 256/484FBGA, 388BGA) Added X3, X5, X6, X16 multiplication modes to Spread Aware PLL Added PLL parameters (f_{PLLVCO}, P_{SAPLLI}, f_{MPPLI}) Added and updated Storage Temperature for 39K200-208EQFP Changed the I_{cc0} spec for 39K165 and 39K200 Updated tCLZ, tCHMCYC2 parameter Values for -233 MHz bin Updated *Input and Output Standard Timing Delay Adjustment* table Removed Self Boot Industrial parts from the offering Removed Delta39K165Z (1.8V) from the offering Removed 144-FBGA package offering Added self-boot Flash Memory endurance and data retention data Added Family, Package, and Density Migration section Added note 20 to 484/676 FBGA pin table to identify slow 39K165 IOs
*E	117518	10/04/02	OOR	Changed data sheet status from Preliminary to Final Added note 7 to DC Characteristics
*F	121063	11/06/02	DSG	Updated spec 51-85103 (MG388 package drawing) to rev. *C
*G	122543	12/10/02	RN	Changed the definition of following pins on CY39030 -256FBGA package: Pin A10: From *IO/Vref7* to *IO/Vref6* Pin B7: From *IO/Vref6* to V_{CC} Added Table to identify Bank Location of Global Clock and Global Control Pins
*H	128684	08/04/03	OOR	Removed all “Z” parts (1.8V) Referenced EEPROM to ATMEL part number

Document Title: Delta39K™ ISR™ CPLD Family CPLDs at FPGA Densities™ Document Number: 38-03039				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
*I	328760	See ECN	PCX	Removed 39K165 family in part ordering information Removed 39K165 from 208-EQFP, 484-FBGA, 388-BGA, 676-FBGA pin tables. Removed old note 20 which identify slow 39K165 IOs Added Lead (Pb)-free logo on all pages, add note in Features section. Added Lead (Pb)-free package diagram labels. Added Lead (Pb)-free parts to Ordering Information: CY39030V208-233NTXC, CY39030V208-125NTXC, CY39030V208-125NTXI, CY39030V208-83NTXC, CY39030V208-83NTXI, CY39050V208-233NTXC, CY39050V208-125NTXC, CY39050V208-125NTXI, CY39050V208-83NTXC, CY39050V208-83NTXI, CY39100V208B-200NTXC, CY39100V208B-125NTXC, CY39100V208B-83NTXC, CY39200V208-181NTXC, CY39200V208-125NTXC, CY39200V208-83NTXC