Integrated Device Technology, Inc.

CMOS STATIC RAM 16K (4K x 4-BIT)

IDT6168SA
IDT6168LA

FEATURES:

- High-speed (equal access and cycle time)
  - — Military: 15/20/25/35/45ns (max.)
  - — Commercial: 15/20/25/35ns (max.)
- Low power consumption
- Battery backup operation—2V data retention voltage (IDT6168LA only)
- Available in high-density 20-pin ceramic or plastic DIP, 20-pin SOIC.
- Produced with advanced CMOS high-performance technology
- CMOS process virtually eliminates alpha particle soft-error rates
- Bidirectional data input and output
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

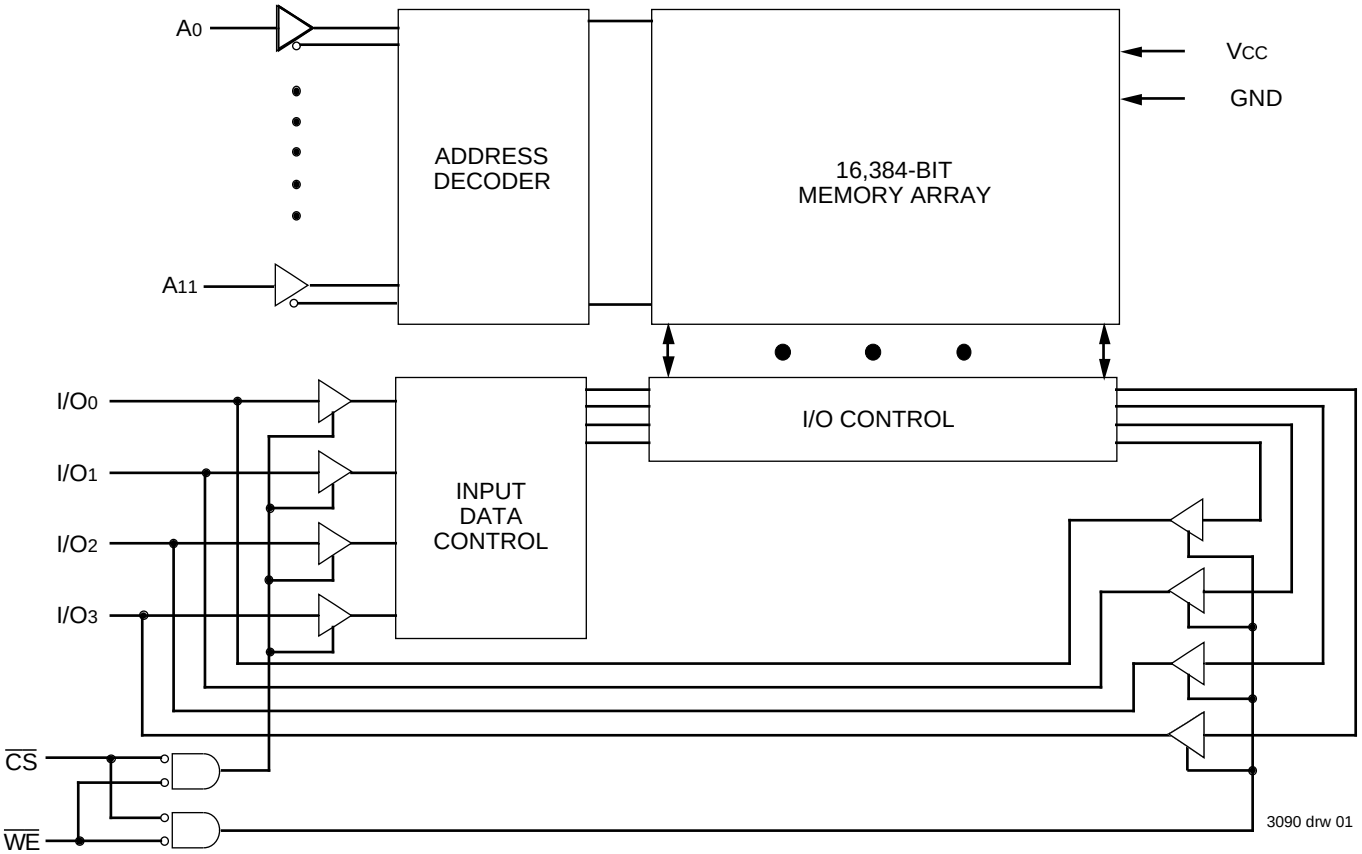
The IDT6168 is a 16,384-bit high-speed static RAM organized as 4K x 4. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective approach for high-speed memory applications.

Access times as fast 15ns are available. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes HIGH, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains HIGH. This capability provides significant system-level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1µW operating off a 2V battery. All inputs and outputs of the IDT6168 are TTL-compatible and operate from a single 5V supply.

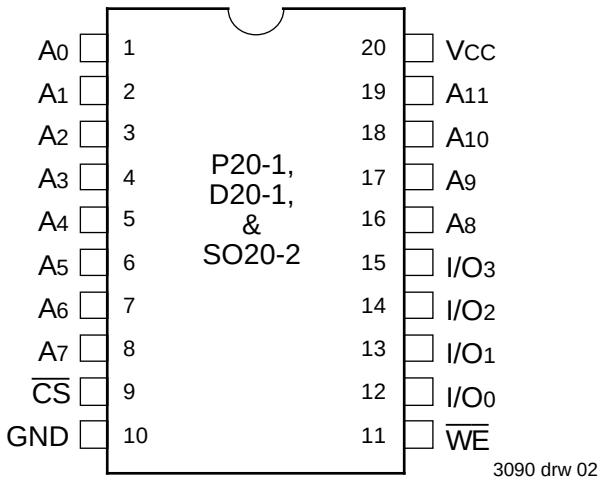
The IDT6168 is packaged in either a space saving 20-pin, 300-mil ceramic or plastic DIP, 20-pin SOIC providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



3090 drw 02

DIP/SOJ
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A_0–A_{11}	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
I/O_{0-3}	Data Input/Output
V_{CC}	Power
GND	Ground

3090 tbl 01

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	7	pF

NOTE: 3090 tbl 02
1. This parameter is determined by device characterization, but is not production tested.

TRUTH TABLE[1]

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High-Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	D_{IN}	Active

NOTE: 3090 tbl 03
1. H = V_{IH}, L = V_{IL}, X = Don't Care

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 3090 tbl 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 3090 tbl 05
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns, once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	VCC
Military	–55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

3090 tbl 06

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	6168SA15 Com'l.	6168SA15 Mil.	6168SA20 6168LA20 Com'l.	6168SA20 6168LA20 Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = 0(2)	SA	110	120	90	100	mA
		LA	—	—	70	80	
I_{CC2}	Dynamic Operating Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	SA	145	165	120	120	mA
		LA	—	—	100	110	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \ge V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}(2)	SA	55	60	45	45	mA
		LA	—	—	30	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \ge V_{HC}$, V_{CC} = Max., $V_{IN} \ge V_{HC}$ or $V_{IN} \le V_{LC}$, f = 0(2)	SA	20	20	20	20	mA
		LA	—	—	0.5	5	

3090 tbl 07

DC ELECTRICAL CHARACTERISTICS (CONTINUED)(1)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	6168SA25 6168LA25 Com'l.	6168SA25 6168LA25 Mil.	6168SA35 6168LA35 Com'l.	6168SA35 6168LA35 Mil.	6168SA45 6168LA45 Com'l.	6168SA45 6168LA45 Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = 0(2)	SA	90	100	90	—	—	100	mA
		LA	70	80	70	—	—	80	
I_{CC2}	Dynamic Operating Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	SA	110	120	100	—	—	110	mA
		LA	90	100	80	—	—	80	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \ge V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}(2)	SA	35	45	30	—	—	35	mA
		LA	25	30	20	—	—	25	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \ge V_{HC}$, V_{CC} = Max., $V_{IN} \ge V_{HC}$ or $V_{IN} \le V_{LC}$, f = 0(2)	SA	3	10	3	—	—	10	mA
		LA	0.5	0.3	0.5	—	—	0.3	

NOTES:

3090 tbl 08

1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC}, only address inputs are cycling at f_{MAX}. f = 0 means no address inputs are changing.

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT6168SA Min.	IDT6168SA Max.	IDT6168LA Min.	IDT6168LA Max.	Unit
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL	—	10	—	5	µA
			COM'L	—	2	—	2	
$\lvert I_{LO} \rvert$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL	—	10	—	5	µA
			COM'L	—	2	—	2	
V_{OL}	Output LOW Voltage	I_{OL} = 10mA, V_{CC} = Min.		—	0.5	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	
V_{OH}	Output HIGH Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	—	2.4	—	V

3090 tbl 09

DATA RETENTION CHARACTERISTICS (LA Version Only)

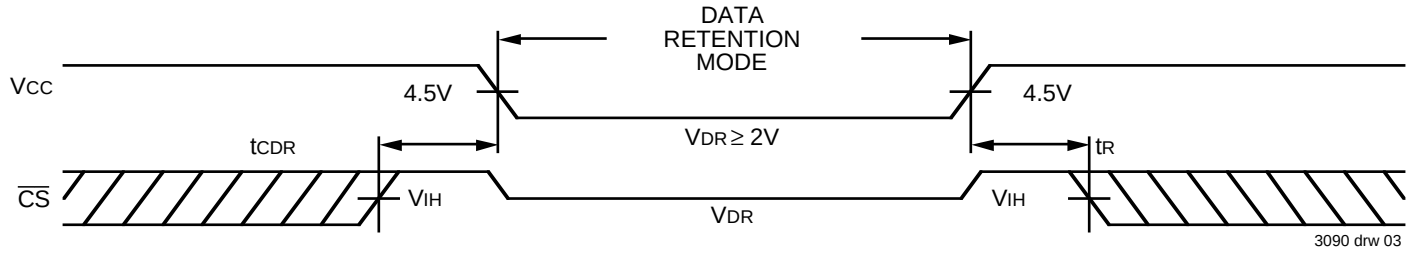
V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Condition		IDT6168LA Min.	IDT6168LA Typ.(1)	IDT6168LA Max.	Unit
V_{DR}	V_{CC} for Data Retention			2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	— —	0.5(2) 1.0(3)	100(2) 150(3)	µA
			COM'L.	— —	0.5(2) 1.0(3)	20(2) 30(3)	µA
t_{CDR}(5)	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(5)	Operation Recovery Time			t_{RC}(2)	—	—	ns

3090 tbl 10

NOTES:
1. T_A = +25°C.
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. t_{RC} = Read Cycle Time.
5. This parameter is guaranteed by device characterization, but is not production tested.

LOW V_{CC} DATA RETENTION WAVEFORM

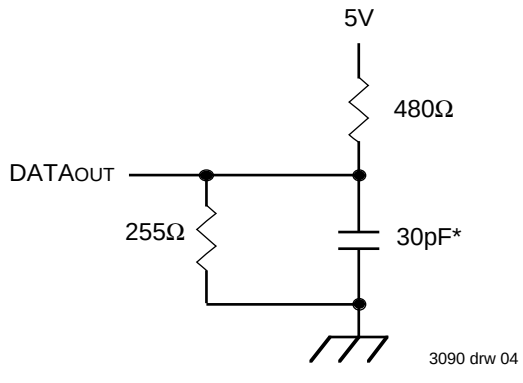


3090 drw 03

AC TEST CONDITIONS

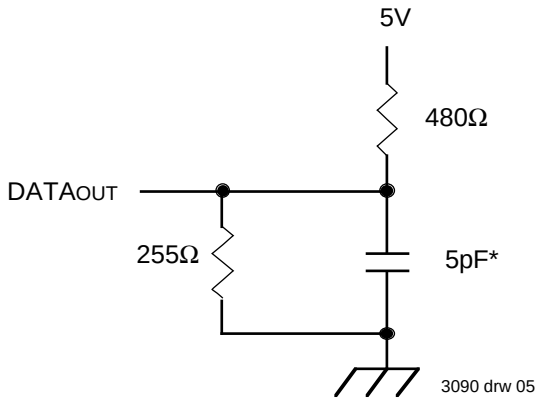
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

3090 tbl 11



3090 drw 04

Figure 1. AC Test Load



3090 drw 05

Figure 2. AC Test Load (for t_{CHZ}, t_{CLZ}, t_{WHZ} and t_{OW})

*Includes scope and jig capacitances

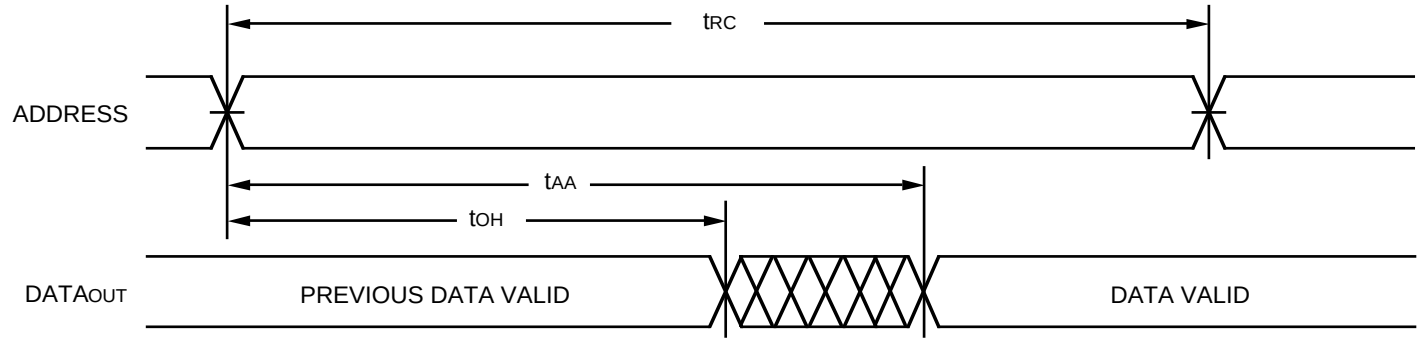
AC ELECTRICAL CHARACTERISTICS (CONTINUED) (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA15		6168SA20/25 6168LA20/25		6168SA35 6168LA35		6168SA45(1) 6168LA45(1)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	15	—	20/25	—	35	—	45	—	ns
t_{AA}	Address Access Time	—	15	—	20/25	—	35	—	45	ns
t_{ACS}	Chip Select Access Time	—	15	—	20/25	—	35	—	45	ns
t_{CLZ}(2)	Chip Select to Output in Low-Z	3	—	5	—	5	—	5	—	ns
t_{CHZ}(2)	Chip Deselect to Output in High-Z	—	8	—	10	—	15	—	25	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{PU}(2)	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}(2)	Chip Deselect to Power-Down Time	—	35	—	20/25	—	35	—	40	ns

3090 tbl 12

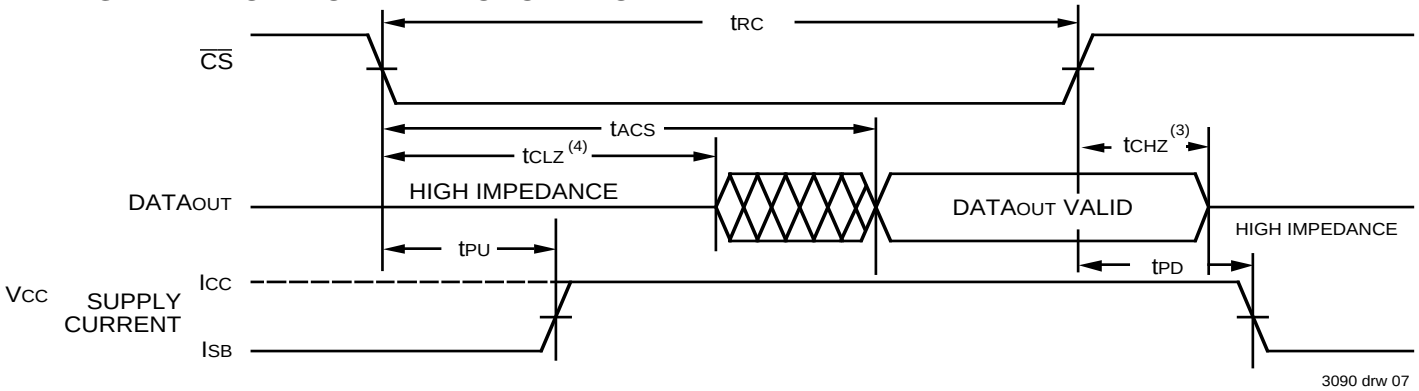
NOTES:
1. –55°C to +125°C temperature range only.
2. This parameter is guaranteed with AC Test load (Figure 2) by device characterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1, 2)



3090 drw 06

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 3)



3090 drw 07

NOTES:
1. $\overline{WE}$ is HIGH for Read cycle.
2. $\overline{CS}$ is LOW for Read cycle.
3. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. Transition is measured ±200mV from steady state.

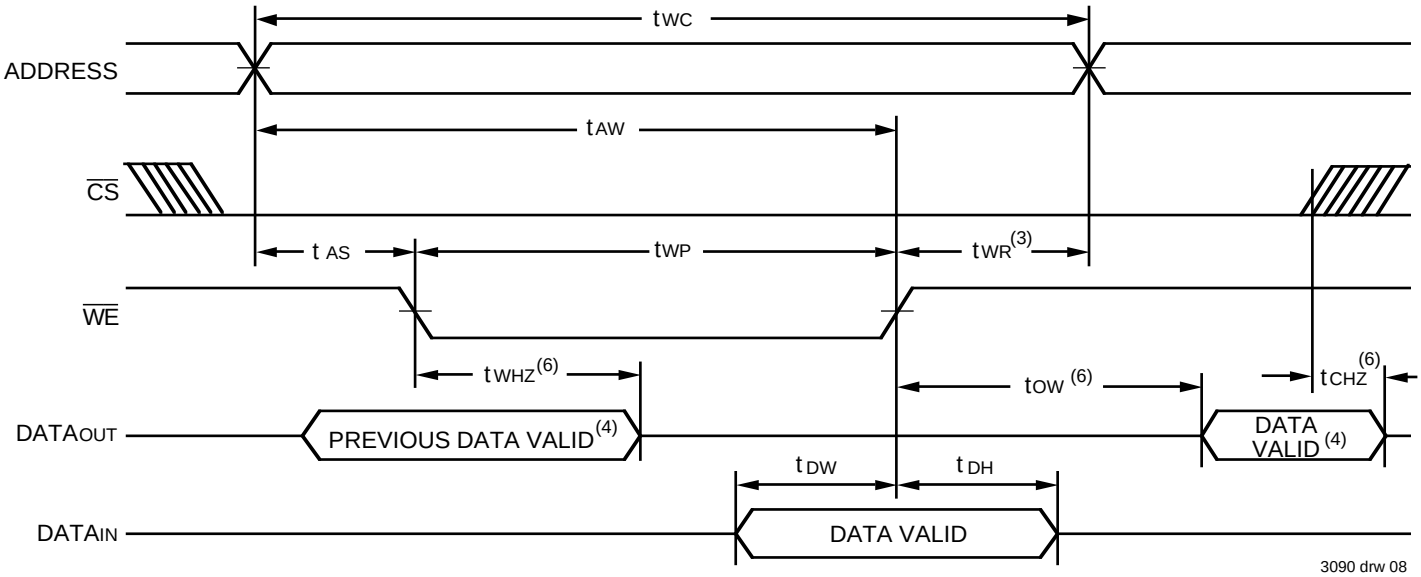
AC ELECTRICAL CHARACTERISTICS (CONTINUED) (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA15		6168SA20/25 6168LA20/25		6168SA35 6168LA35		6168SA45[2] 6168LA45[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle										
t_{WC}	Write Cycle Time	15	—	20	—	30	—	40	—	ns
t_{CW}	Chip Select to End-of-Write	15	—	20	—	30	—	40	—	ns
t_{AW}	Address Valid to End-of-Write	15	—	20	—	30	—	40	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	15	—	20	—	30	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	DataValid to End-of-Write	9	—	10	—	15	—	20	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	3	—	ns
t_{WHZ}[3]	Write Enable to Output in High-Z	—	6	—	7	—	13	—	20	ns
t_{OW}[3]	Output Active from End-of-Write	0	—	0	—	0	—	0	—	ns

NOTES:
3090 tbl 13

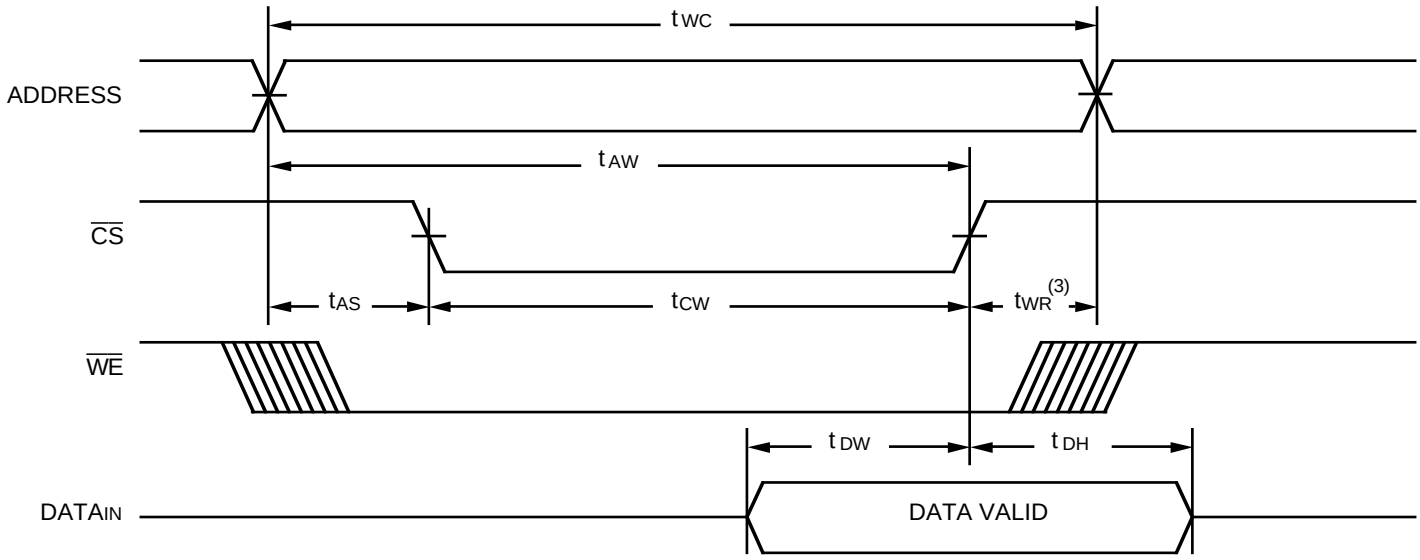
1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 5]



3090 drw 08

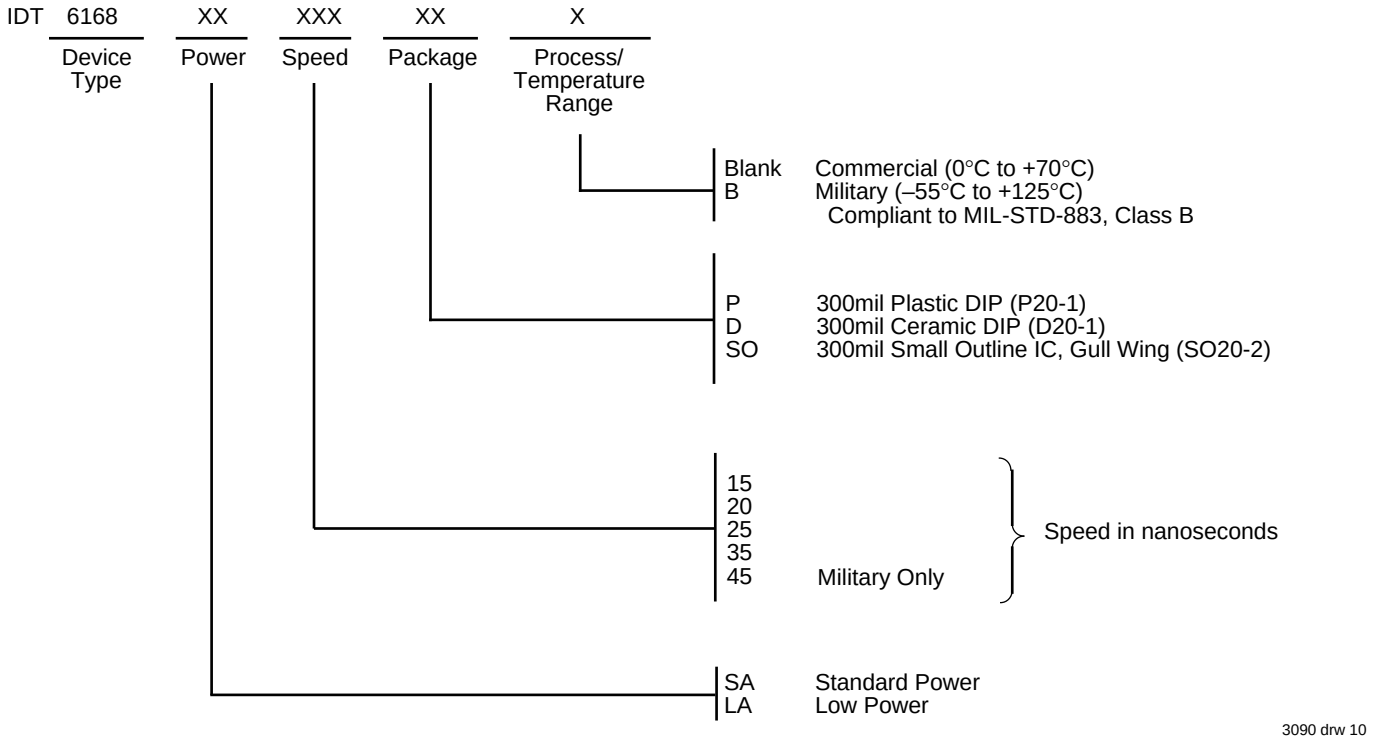
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 5)



3090 drw 09

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals should not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in the high impedance state.
6. Transition is measured ±200mV from steady state.

ORDERING INFORMATION



3090 drw 10