2912A
PCM TRANSMIT/RECEIVE FILTER

- **Low Power Consumption:**
  60 mW Typical without Power Amplifiers
  80 mW Typical with Power Amplifiers
  0.5 mW Typical Standby
- **Low Idle Channel Noise:**
  2 dBrnc0 Typical, Receive
  6 dBrnc0 Typical, Transmit
- **Excellent Power Supply Rejection:**
  40 dB Typical on V_{CC} @ 50 KHz
  30 dB Typical on V_{BB} @ 50 KHz
- **Transmit Filter Rejects Low Frequency Noise:**
  23 dB @ 60 Hz
  25 dB @ 50 Hz
  50 dB @ 16-2/3 Hz
- **Adjustable Gain in Both Directions**
- **Fully Compatible with the Industry Standard Intel 2912**
- **D3/D4 and CCITT G712 Compatible**
- **Common Mode Op Amp Input Rejection 75 dB Typical**
- **Direct Interface to the Intel 2910A/2911A PCM Codecs Including Stand-By Power Down Mode**
- **Direct Interface with Transformer or Electronic Hybrids**
- **Fabricated with Reliable N-Channel MOS Process**

The Intel 2912A 2nd generation PCM line filter is a fully integrated monolithic device containing the two filters of a PCM line or trunk termination. It has improved key parameters of power consumption, idle channel noise, and power supply rejection. A single part exceeds both AT&T* D3/D4 and CCITT transmission specs, exceeds digital Class 5 central office switching system stringent specifications, and is fully compatible with the 2912. The primary application for the 2912A is in telephone systems for transmission, switching, or remote concentration.

An advanced version of the switched capacitor technique used for the 2912 is used to implement the transmit and receive passband filter sections of the 2912A. The device is fabricated using Intel's reliable two layer polysilicon gate NMOS technology. (See Intel Reliability Report RR-24 on the 2910A, 2911A, and 2912.) The combination of advances in the switched capacitor techniques first used on the 2912 and the NMOS technology results in a monolithic 2912A filter which is packaged in a standard 16-pin DIP.

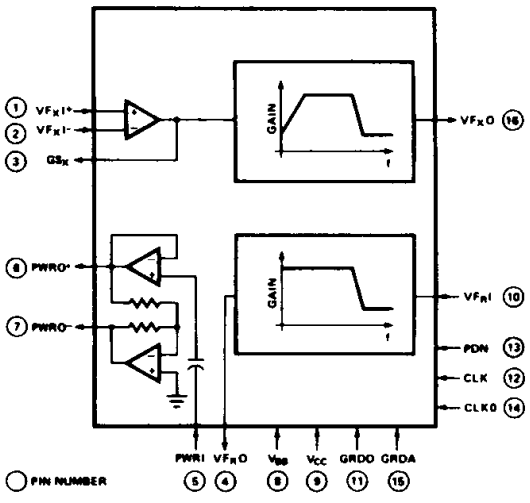

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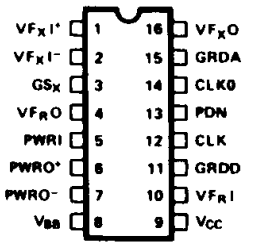
Figure 1. Block Diagram



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Pin Names

VF_XI^+, VF_XI^-	Analog Inputs
GS_X	Gain Control
VF_XO	Analog Output
VF_RI	Analog Input
VF_RO	Analog Output
PWRI	Driver Input
$PWRO^+$, $PWRO^-$	Driver Output
CLK	Clock Input
CLK0	Clock Selection
PDN	Power Down
V_{CC}	Power (+5V)
V_{BB}	Power (−5V)
GRDD	Digital Ground
GRDA	Analog Ground

Figure 2. Pin Configuration

*AT&T is a registered trademark of American Telephone and Telegraph Corporation.

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Order Number: 270159-002

Table 1. Pin Description

Symbol	Pin No.	Function	Description
VF_XI+	1	Input	Analog input of the transmit filter. The VF_XI+ signal comes from the 2 to 4 wire hybrid in the case of a 2 wire line and goes through the frequency rejection and the antialiasing filters before being sent to the Codec for encoding.
VF_XI-	2	Input	Inverting input of the gain adjustment operational amplifier on the transmit filter.
GS_X	3	Output	Output of the gain adjustment operational amplifier on the transmit filter. Used for gain setting of the transmit filter.
VF_RO	4	Output	Analog output of the receive filter. This output provides a direct interface to electronic hybrids. For a transformer hybrid application, VF_RO is tied to PRWI and a dual balanced output is provided on pins PWRO+ and PWRO−.
PWRI	5	Input	Input to the power driver amplifiers on the receive side for interface to transformer hybrids. High impedance input. When tied to V_{BB}, the power amplifiers are powered down.
PWRO+	6	Output	Non-inverting side of the power amplifiers. Power driver output capable of directly driving transformer hybrids.
PWRO−	7	Output	Inverting side of the power amplifiers. Power driver output capable of directly driving transformer hybrids.
V_{BB}	8	Power	−5V ±5% referenced to GRDA
V_{CC}	9	Power	+5V ±5% referenced to GRDA
VF_RI	10	Input	Analog input of the receive filter, interface to the Codec analog output for PCM applications. The receive filter provides the $\frac{Sinx}{x}$ correction needed for sample and hold type Codec outputs to give unity gain. The input voltage range is directly compatible with the Intel 2910A and 2911A Codecs.
GRDD	11	Ground	Digital ground return for internal clock generator.
CLK(1)	12	Input	Clock input. Three clock frequencies can be used: 1.536 MHz, 1.544 MHz or 2.048 MHz; pin 14, CLK0, has to be strapped accordingly. High impedance input, TTL voltage levels.
PDN	13	Input	Control input for the stand-by power down mode. An internal pull up to +5V is provided for interface to the Intel 2910A and 2911A PDN outputs. TTL voltage levels.
CLK0(1)	14	Input	Clock (pin 12, CLK) frequency selection. If tied to V_{BB}, CLK should be 1.536 MHz. If tied to Ground, CLK should be 1.544 MHz. If tied to V_{CC}, CLK should be 2.048 MHz.
GRDA	15	Ground	Analog return common to the transmit and receive analog circuits. Not connected to GRDD internally.
VF_XO	16	Output	Analog output of the transmit filter. The output voltage range is directly compatible with the Intel 2910A and 2911A Codecs.

NOTE:
1. The three clock frequencies are directly compatible with the Intel 2910A and 2911A Codecs. The following table should be observed in selecting the clock frequency.

Codec Clock	Clock Bits/Frame	CLK, Pin 12	CLK0, Pin 14
1.536 MHz	192	1.536 MHz	V_{BB} (−5V)
1.544 MHz	193	1.544 MHz	GRDD
2.048 MHz	256	2.048 MHz	V_{CC} (+5V)

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FUNCTIONAL DESCRIPTION

The 2912A provides the transmit and receive filters found on the analog termination of a PCM line or trunk. The transmit filter performs the anti-aliasing function needed for an 8 KHz sampling system, and the 50/60 Hz rejection. The receive filter has a low pass transfer characteristic and also provides the Sinx/x correction necessary to interface the Intel 2910A (μ Law) and 2911A (A Law) Codecs which have a non-return-to-zero output of the digital to analog conversion. Gain adjustment is provided in the receive and transmit directions.

A stand-by, power down mode is included in the 2912A and can be directly controlled by the 2910A/2911A Codecs.

The 2912A can interface directly with a transformer hybrid (2 to 4 wire conversion) or with electronic hybrids; in the latter case the power dissipation is reduced by powering down the output amplifier provided on the 2912A.

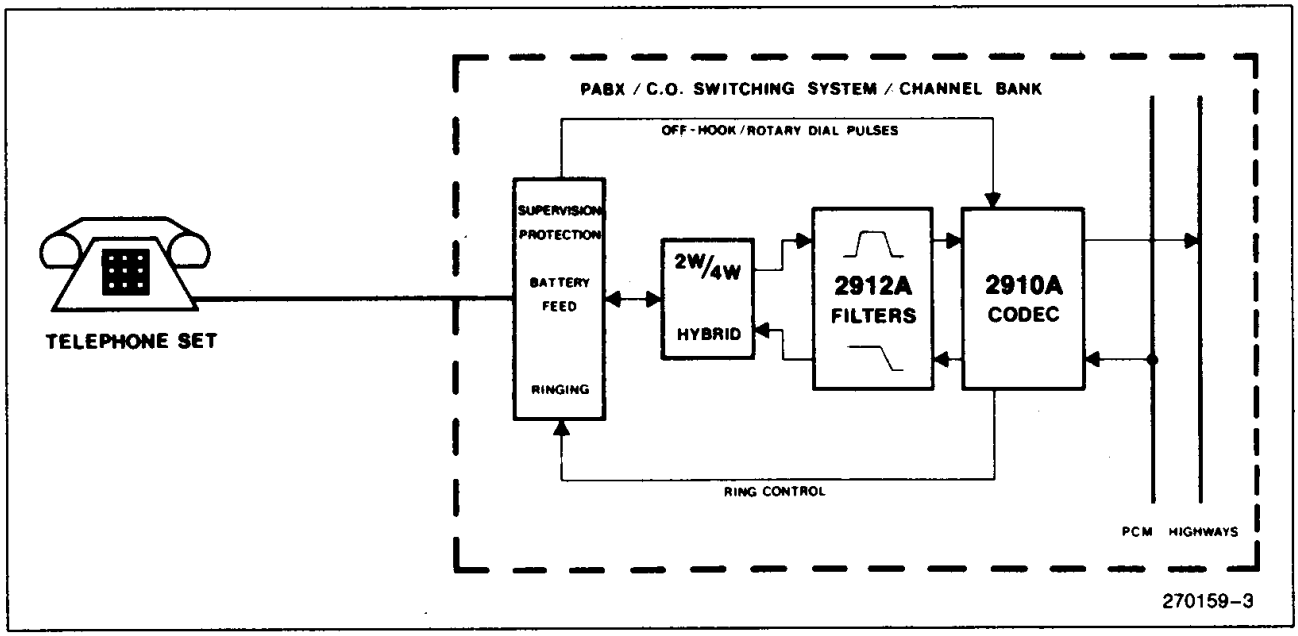

Figure 3. Typical Line Termination

FILTER OPERATION

Transmit Filter Input Stage

The input stage provides gain adjustment in the pass-band. The input operational amplifier has a common mode range of ±2.2 volts, a DC offset of less than 25 mV, a voltage gain greater than 3000 and a unity gain bandwidth of 1 MHz. It can be connected to provide a gain of 20 dB without degrading the noise performance of the filter. The load impedance connected to the amplifier output (GS_X) must be greater than 10K Ω in parallel with 25 pF. The input signal on lead VF_XI+ can be either AC or DC coupled. The input Op Amp can also be used in the inverting mode or differential amplifier mode. The remaining portion of the transmit filter provides a gain of +3 dB in the pass band.

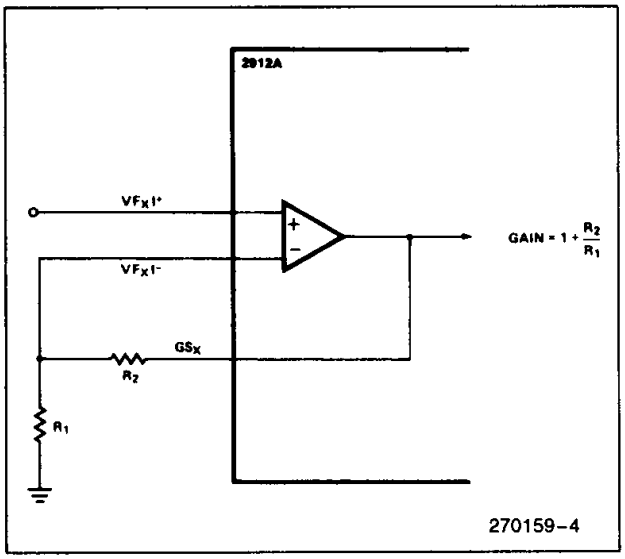

Figure 4. Transmit Filter Gain Adjustment

Receive Filter Output

The VF_RO lead is capable of driving high impedance electronic hybrids. The gain of the receive section from VF_RI to VF_RO is:

$$\frac{\left(\frac{\pi f}{8000}\right)}{\text{Sin}\left(\frac{\pi f}{8000}\right)}$$

which when multiplied by the output response of the Intel 2910A and 2911A Codecs results in a 0 dB gain in the pass band. The filter gain can be adjusted downward by a resistor voltage divider connected as shown in Figure 5. The total resistive load R_{LR} on VF_RO should not be less than 10K Ω.

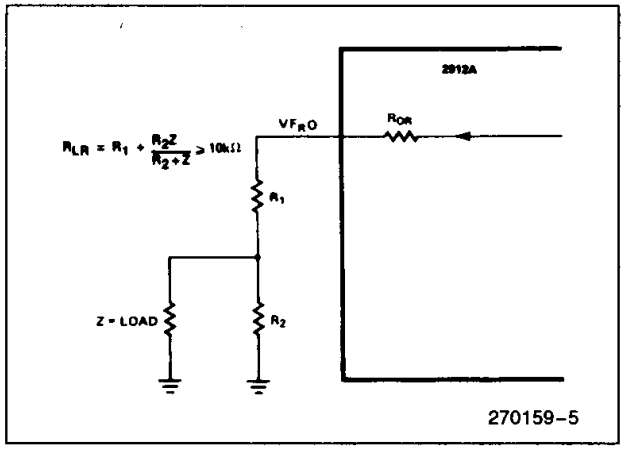

Figure 5. Receive Filter Output Gain Adjustment

Receive Filter Output Driver Amplifier Stage

A balanced power amplifier is provided in order to drive low-impedance loads in a bridged configuration. The receive filter output VF_RO is connected through gain setting resistors R_1 and R_2 to the amplifier input PWRI. The input voltage range on PWRI is ±3.2 volts and the gain is 6 dB for a bridged output.

With a 600Ω load connected between PWRO+ and PWRO−, the maximum voltage swing across the load is ±5.0 volts. The series combination of R_S and the hybrid transformer must present a minimum A.C. load resistance of 600Ω to the amplifier in the bridged configuration. A typical connection of the output driver amplifiers is shown in Figure 6. These amplifiers can also be used with loads connected to ground.

When the power amplifier is not needed it should be deactivated to save power. This is accomplished by tying the PWRI pin to V_{BB} before the device is powered up.

Power Down Mode

Pin 13, PDN, provides the power down control. When the signal on this lead is brought high, the 2912A goes into a standby, power down mode. Power dissipation is reduced to 0.5 mW. In the stand-by mode, all outputs go into a high impedance state. This feature allows multiple 2912As to drive the same analog bus on a time-shared basis.

When power is restored, the settling time of the 2912A is typically 15 ms.

The PDN interface is directly compatible with the Intel 2910A and 2911A PDN outputs. Only one command from the common control is then necessary to power down both the Codec and the Filters of the line or trunk interface.

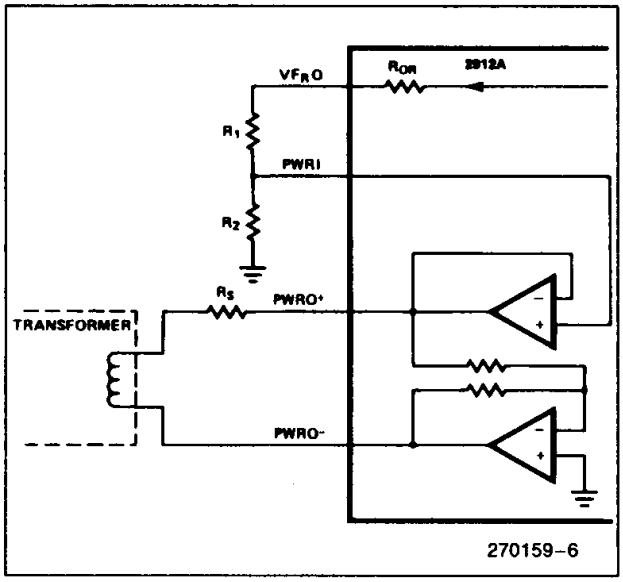

Figure 6. Typical Connection of Output Driver Amplifier

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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +150°C
Supply Voltage with Respect to V_{BB} ..... −0.3V to +14.0V
All Input and Output Voltages with Respect to V_{BB} ..... −0.3V to +14.0V
All Output Currents ..... ±50 mA
Power Dissipation ..... 1 Watt

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS T_A = 0°C to +70°C; V_{CC} = 5V ±5%; V_{BB} = −5V ±5%; GRDA = 0V; GRDD = 0V; unless otherwise specified

DIGITAL INTERFACE (CLK, CLK0, and PDN Pins)

Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
I_{LIC}	Input Load Current, CLK			10	μA	V_{IN} = GRDD to V_{CC}
I_{LIO}	Input Load Current, CLK0			10	μA	V_{IN} = V_{BB} to V_{CC}
I_{LIP}	Input Load Current, PDN			−100	μA	V_{IN} = GRDD to V_{CC}
V_{IL}	Input Low Voltage (except CLK0)			0.8	V	
V_{IH}	Input High Voltage (except CLK0)	2.0			V	
V_{IL0}	Input Low Voltage, CLK0	V_{BB}		V_{BB}+0.5	V	
V_{II0}	Input Intermediate Voltage, CLK0	GRDD−0.5		0.8	V	
V_{IH0}	Input High Voltage, CLK0	V_{CC}−0.5		V_{CC}	V	

POWER DISSIPATION

Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
I_{CC0}	V_{CC} Standby Current		50	100	μA	PDN = V_{IH} Min
I_{BB0}	V_{BB} Standby Current		50	100	μA	PDN = V_{IH} Min
I_{CC1}	V_{CC} Operating Current, Power Amplifiers Inactive		6	10	mA	PWRI = V_{BB}(2)
I_{BB1}	V_{BB} Operating Current, Power Amplifiers Inactive		6	10	mA	PWRI = V_{BB}(2)
I_{CC2}	V_{CC} Operating Current		8	14	mA	
I_{BB2}	V_{BB} Operating Current		8	14	mA	

NOTES:
1. Typical values are for T_A = 25°C and nominal power supply values.
2. To place the power amplifiers in the inactive mode PWRI must be tied to V_{BB} prior to power-up.

D.C. CHARACTERISTICS $T_A = 0°C$ to $+70°C$; $V_{CC} = 5V \pm 5\%$; $V_{BB} = -5V \pm 5\%$; GRDA = 0V; GRDD = 0V; unless otherwise specified (Continued)

ANALOG INTERFACE, TRANSMIT FILTER INPUT STAGE

Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
I_{BXI}	Input Leakage Current, VF_XI+, VF_XI-			100	nA	$-2.2V < V_{IN} < 2.2V$
R_{IXI}	Input Resistance, VF_XI+, VF_XI-	10			MΩ	
V_{OSXI}	Input Offset Voltage, VF_XI+, VF_XI-			25	mV	
CMRR	Common Mode Rejection, VF_XI+, VF_XI-	60	75		dB	$-2.2V < V_{IN} < 2.2V$, 0 dBm0 ≡ 1.1 V_{RMS}, Input at VF_XI-
A_{VOL}	DC Open Loop Voltage Gain, GS_X	3000				
f_C	Open Loop Unity Gain Bandwidth, GS_X		1		MHz	
V_{OXI}	Output Voltage Swing, GS_X	±2.5			V	$R_L \geq 10$ KΩ
C_{LXI}	Load Capacitance, GS_X			25	pF	
R_{LXI}	Minimum Load Resistance, GS_X	10			KΩ	Minimum R_L

ANALOG INTERFACE, TRANSMIT FILTER (See Figure 9)

Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
R_{OX}	Output Resistance, VF_XO		20	35	Ω	
V_{OSX}	Output DC Offset, VF_XO			100	mV	VF_XI+ Connected to GRDA, Input Op Amp at Unity Gain
$PSRR_1$	Power Supply Rejection of V_{CC} at 1 KHz, VF_XO	30	40		dB	Note 2
$PSRR_2$	Power Supply Rejection of V_{BB} at 1 KHz, VF_XO	25	30		dB	Note 2
C_{LX}	Load Capacitance, VF_XO			25	pF	
R_{LX}	Minimum Load Resistance, VF_XO	2.7			KΩ	Minimum R_L
V_{OX1}	Output Voltage Swing, 1 KHz, VF_XO	±3.2			V	$R_L \geq 10$ KΩ or with 2910A or 2911A
V_{OX2}	Output Voltage Swing, 1 KHz, VF_XO	±2.5			V	$R_L \geq 2.7$ KΩ

NOTES:
1. Typical values for $T_A = 25°C$ and nominal power supply values.
2. $PSRR_{1,2}$ include op amp in transmit section.

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D.C. CHARACTERISTICS T_A = 0°C to +70°C; V_{CC} = 5V ±5%; V_{BB} = −5V ±5%; GRDA = 0V; GRDD = 0V; unless otherwise specified (Continued)

ANALOG INTERFACE, RECEIVE FILTER (See Figure 10)

Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
I_{BR}	Input Leakage Current, VF_RI			3	μA	$-3.2V < V_{IN} < 3.2V$
R_{IR}	Input Resistance, VF_RI	1			MΩ	
R_{OR}	Output Resistance, VF_RO			100	Ω	
V_{OSR}	Output DC Offset VF_RO			100	mV	VF_RI Connected to GRDA
$PSRR_3$	Power Supply Rejection of V_{CC} at 1 KHz, VF_RO	30	45		dB	
$PSRR_4$	Power Supply Rejection of V_{BB} at 1 KHz, VF_RO	30	35		dB	
C_{LR}	Load Capacitance, VF_RO			25	pF	
R_{LR}	Minimum Load Resistance, VF_RO	10			KΩ	Minimum R_L
V_{OR}	Output Voltage Swing, VF_RO	±3.2			V	R_L = 10 KΩ

ANALOG INTERFACE, RECEIVE FILTER DRIVER AMPLIFIER STAGE

Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions	
I_{BRA}	Input Leakage Current, PWRI			3	μA	$-3.2V < V_{IN} < 3.2V$	
R_{IRA}	Input Resistance, PWRI	10			MΩ		
R_{ORA}	Output Resistance, PWRO+, PWRO−		1		Ω	$\|I_{OUT}\| < 10$ mA $-3.0V < V_{OUT} < 3.0V$	
V_{OSRA}	Output DC Offset, PWRO+, PWRO−			50	mV	PWRI Connected to GRDA	
C_{LRA}	Load Capacitance, PWRO+, PWRO−			100	pF		
V_{ORA1}	Output Voltage Swing Across R_L, PWRO+, PWRO− Single Ended Connection	±3.2			V	R_L = 10 KΩ	R_L Connected to GRDA fo ≥ 200 Hz
		±2.9			V	R_L = 600Ω	
		±2.5			V	R_L = 300Ω	
V_{ORA2}	Differential Output Voltage Swing, PWRO+, PWRO− Balanced Output Connection	±6.4			V	R_L = 20 KΩ	R_L Connected between PWRO + and PWRO − fo ≥ 200 Hz
		±5.8			V	R_L = 1200Ω	
		±5.0			V	R_L = 600Ω	

NOTE:
1. Typical values are for T_A = 25°C and nominal power supply values.

A.C. CHARACTERISTICS T_A = 0°C to +70°C; V_{CC} = 5V ±5%; V_{BB} = −5V ±5%; GRDA = 0V; GRDD = 0V; unless otherwise specified

Clock Input Frequency: CLK = 1.536 MHz ±0.1%; CLK0 = V_{IL0} (Tied to V_{BB})
CLK = 2.048 MHz ±0.1%; CLK0 = V_{IH0} (Tied to V_{CC})
CLK = 1.544 MHz ±0.1%; CLK0 = V_{II0} (Tied to GRDD)

TRANSMIT FILTER TRANSFER CHARACTERISTICS

(See Transmit Filter Transmit Characteristics, Figure 7)

Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
G_{RX}	Gain Relative to Gain at 1 KHz					0 dBm0 Input Signal
	16.67 Hz		−56	−50	dB	Gain Setting Op Amp
	50 Hz			−25	dB	Unity Gain
	60 Hz			−23	dB	
	200 Hz	−1.8		−0.125	dB	0 dBm0 Signal ≡ 1.1 V_{RMS}
	300 Hz to 3000 Hz	−0.125		0.125	dB	Input at VF_XI-
	3300 Hz	−0.35		0.03	dB	
	3400 Hz	−0.7		−0.1	dB	0 dBm0 Signal ≡ 1.6 V_{RMS}
	4000 Hz			−14	dB	Output at VF_XO
	4600 Hz and Above			−32	dB	
G_{AX}	Absolute Passband Gain at 1 KHz, VF_XO	2.9	3.0	3.1	dB	$R_L = \infty$ (3)
G_{AXT}	Gain Variation with Temperature at 1 KHz		0.0002	0.002	dB/°C	0 dBm0 Signal Level
G_{AXS}	Gain Variation with Supplies at 1 KHz		0.01	0.07	dB/V	0 dBm0 Signal Level, Supplies ±5%
CT_{RT}	Cross Talk, Receive to Transmit, Measured at VF_XO $20 \log \frac{VF_XO}{VF_RO}$		−75	−65	dB	VF_RI = 1.6 V_{RMS}, 1 KHz Input, VF_XI+, VF_XI- Connected to GS_X, GS_X Connected through 10 KΩ to GRDA
N_{CX1}	Total C Message Noise at Output, VF_XO		6	11	dBrnc0 (Note 2)	Gain Setting Op Amp at Unity Gain
N_{CX2}	Total C Message Noise at Output, VF_XO		9	13	dBrnc0 (Note 2)	Gain Setting Op Amp at 20 dB Gain
D_{DX}	Differential Envelope Delay, VF_XO 1 KHz to 2.6 KHz			60	μs	
D_{AX}	Absolute Delay at 1 KHz, VF_XO			110	μs	
DP_{X1}	Single Frequency Distortion Products			−48	dB	0 dBm0 Input Signal at 1 KHz
DP_{X2}	Single Frequency Distortion Products at Maximum Signal Level of +3 dBm0 at VF_XO			−45	dB	0.16 V_{RMS} 1 KHz Input Signal at VF_XI+; Gain Setting Op Amp at 20 dB Gain. The +3 dBm0 Signal at VF_XO is 2.26 V_{RMS}

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A.C. CHARACTERISTICS T_A = 0°C to +70°C; V_{CC} = 5V ±5%; V_{BB} = −5V ±5%; GRDA = 0V; GRDD = 0V; unless otherwise specified (Continued)

Clock Input Frequency: CLK = 1.536 MHz ±0.1%; CLK0 = V_{IL0} (Tied to V_{BB})
CLK = 1.544 MHz ±0.1%; CLK0 = V_{II0} (Tied to GRDD)
CLK = 2.048 MHz ±0.1%; CLK0 = V_{IH0} (Tied to V_{CC})

RECEIVE FILTER TRANSFER CHARACTERISTICS (See Receive Filter Transfer Characteristics, Figure 8)

Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
G_{RR}	Gain Relative to Gain at 1 KHz with Sinx/x Correction of 2910A or 2911A					0 dBm0 Input Signal
	Below 200 Hz			0.125	dB	0 dBm0 Signal ≡ 1.6 V_{RMS} × $\frac{\text{Sin}\left(\frac{\pi f}{8000}\right)}{\left(\frac{\pi f}{8000}\right)}$
	200 Hz	−0.5		0.125	dB	
	300 Hz to 3000 Hz	−0.125		0.125	dB	
	3300 Hz	−0.35		0.03	dB	Input at VF_RI
	3400 Hz	−0.7		−0.1	dB	
	4000 Hz			−14	dB	
	4600 Hz and Above			−30	dB	
G_{AR}	Absolute Passband Gain at 1 KHz, VF_RO	−0.1	0	+0.1	dB	R_L = ∞ (3, 4)
G_{ART}	Gain Variation with Temperature at 1 KHz		0.0002	0.002	dB/°C	0 dBm0 Signal Level
G_{ARS}	Gain Variation with Supplies at 1 KHz		0.01	0.07	dB/V	0 dBm0 Signal Level, Supplies ±5%
CT_{TR}	Cross Talk, Transmit to Receive, Measured at VF_RO; 20 log (VF_RO/VF_XO)		−70	−60	dB	VF_XI = 1.1 V_{RMS}, 1 KHz Output, VF_RI Connected to GRDA
N_{CR}	Total C Message Noise at Output, VF_RO		2	6	dBrnc0 (Note 2)	VF_RO Output or PWRO+ and PWRO− Connected with Unity Gain
D_{DR}	Differential Envelope Delay, VF_RO, 1 KHz to 2.6 KHz			100	μs	
D_{AR}	Absolute Delay at 1 KHz, VF_RO			110	μs	
DP_{R1}	Single Frequency Distortion Products			−48	dB	0 dBm0 Input Signal at 1 KHz
DP_{R2}	Single Frequency Distortion Products at Maximum Signal Level of +3 dBm0 at VF_RO			−45	dB	+3 dBm0 Signal Level of 2.26 V_{RMS}, 1 KHz Input at VF_RI

NOTES:
1. Typical Values are for T_A = 25°C and nominal power supply values.
2. A noise measurement of 12 dBrnc into a 600Ω load at the 2912A device is equivalent to 6 dBrnc0.
3. For gain under load refer to output resistance specs and perform gain calculation.
4. Output is non-inverting.

TRANSFER CHARACTERISTICS

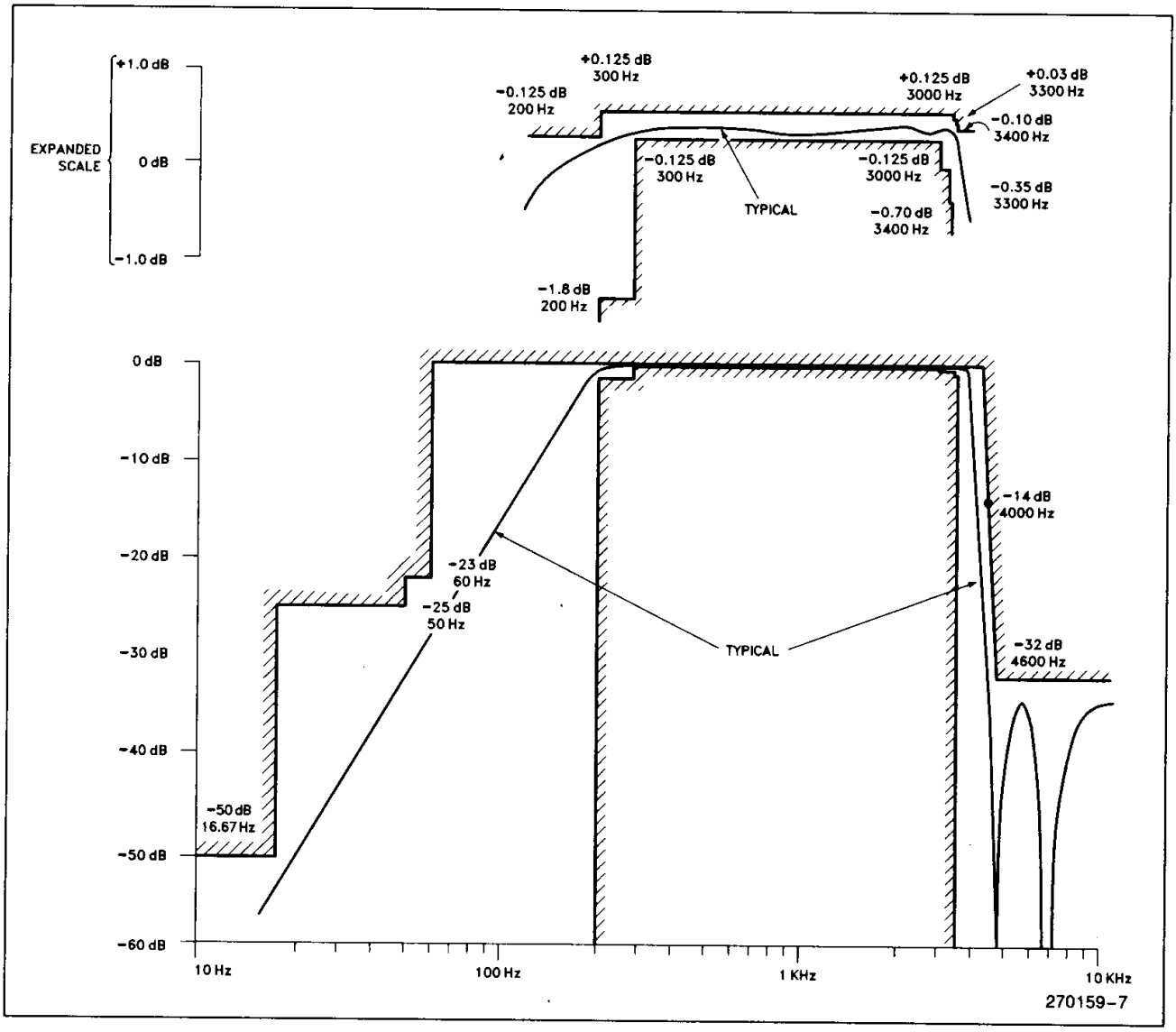

Figure 7. Transmit Filter

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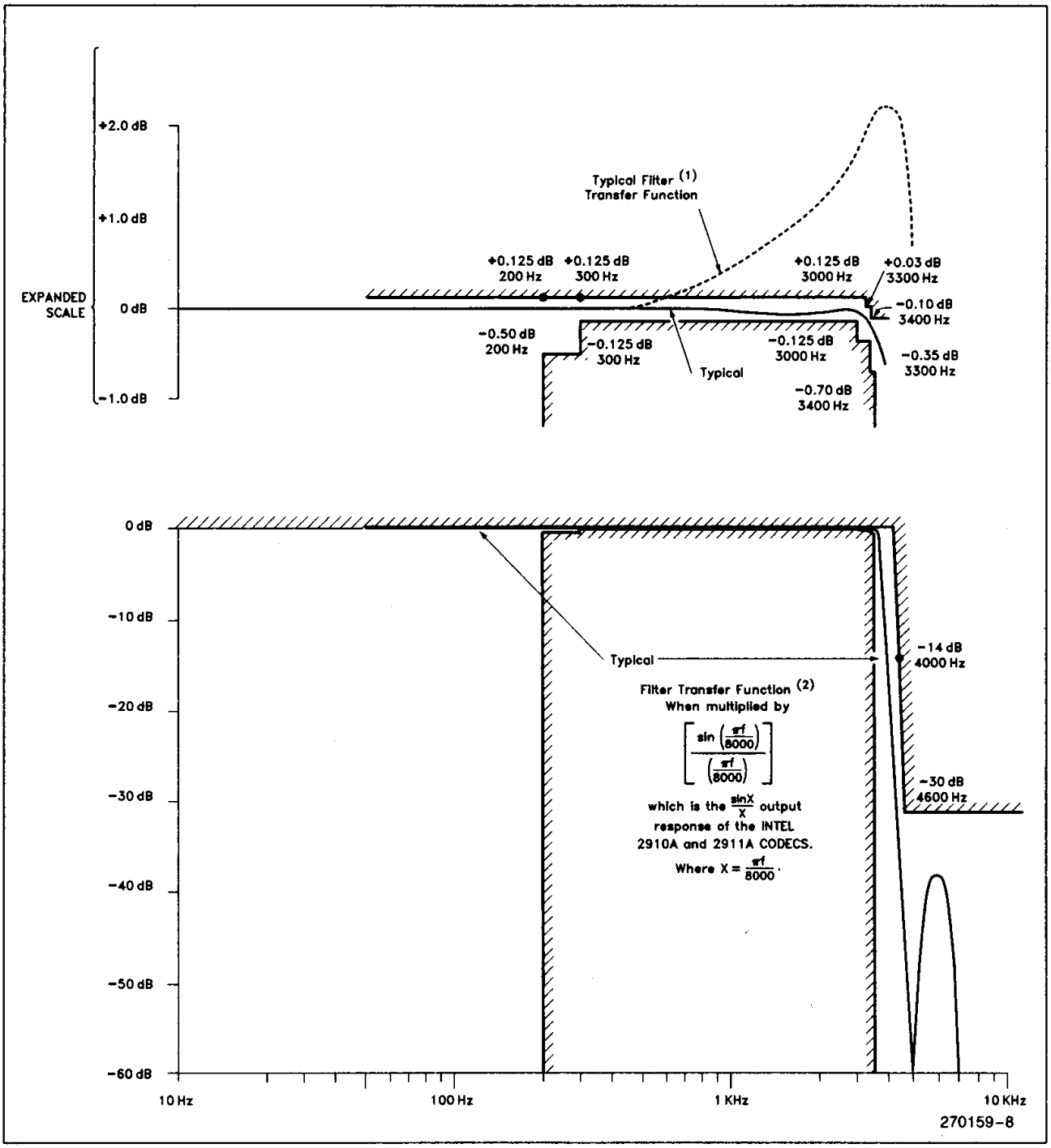

Figure 8. Receive Filter

NOTES:
1. Typical Transfer Function of the Receive Filter as a Separate Component.
2. Typical Transfer Function of the Receive Filter Driven by the Sample and Hold Output of the Intel 2910A and 2911A CODECS. The Combined Filter/CODEC Response Meets the Stated Specifications.

POWER SUPPLY REJECTION TYPICAL VALUES OVER 3 RANGES

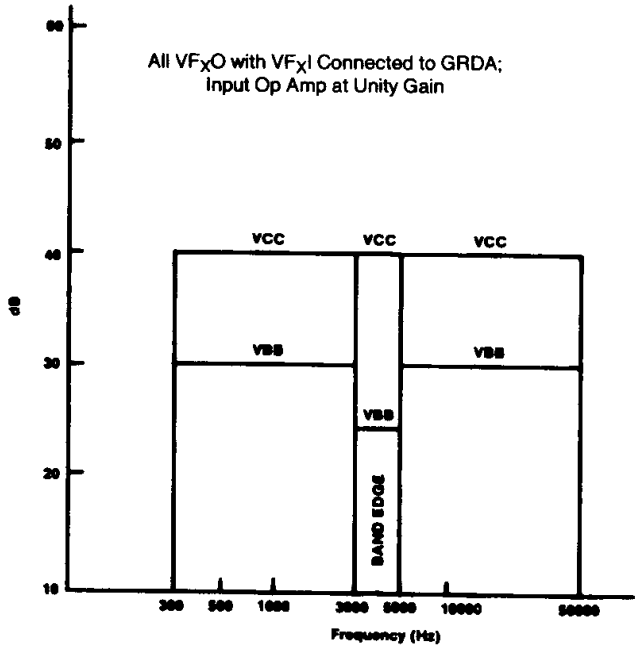

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Figure 9. Transmit Filter

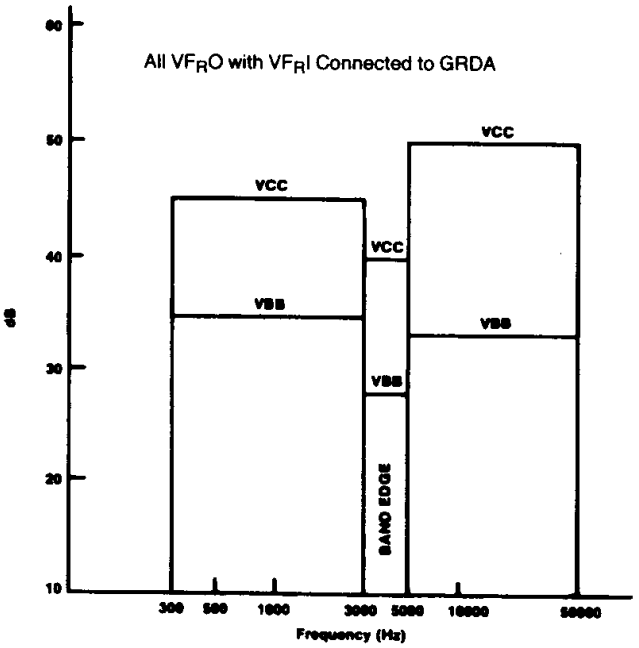

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Figure 10. Receive Filter

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