CMOS Single-Supply Rail-to-Rail Input/Output Operational Amplifier

OP150/OP250/OP450

FEATURES

- Single-Supply Operation: 2.7 V to 6 V
- High Output Current: ±250 mA
- Low Supply Current: 600 µA/Amp
- Wide Bandwidth: 4 MHz
- Slew Rate: 6.5 V/µs
- No Phase Reversal
- Low Input Currents
- Unity Gain Stable

APPLICATIONS

- Battery Powered Instrumentation
- Multi Media Audio
- Medical
- Remote Sensors
- ASIC Input or Output Amplifier
- Automotive
- Headphone Driver

GENERAL DESCRIPTION

The OP150, OP250 and OP450 are single, dual and quad *CMOS* single-supply, 4 MHz bandwidth amplifiers featuring *rail-to-rail inputs and outputs.* All are guaranteed to operate from a *3 volt single supply* as well as a +5 volt supply.

The OP150 family of amplifiers have very low input bias currents. The outputs are capable of driving 250 mA loads and are stable with capacitive loads as high as 500 pF.

Applications for these amplifiers include portable medical equipment, safety and security, and interface for transducers with high output impedances.

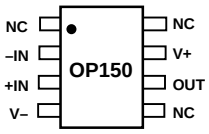
Supply current is only 600 µA per amplifier.

The ability to swing rail-to-rail at both the input and output enables designers to build multistage filters in single-supply systems and maintain high signal-to-noise ratios.

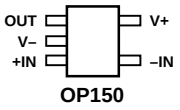
The OP150/OP250/OP450 are specified over the extended industrial (-40°C to +125°C) temperature range. The OP150 single amplifiers are available in 8-pin SO surface mount and the 5-pin SOT23-5 packages. The OP250 dual is available in 8-pin plastic DIPs and SO surface mount packages. The OP450 quad is available in 14-pin DIPs, TSSOP and narrow 14-pin SO packages. Consult factory for TSSOP availability.

PIN CONFIGURATIONS

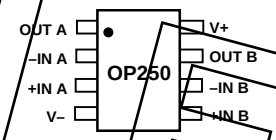
8-Lead Narrow-Body SO (S Suffix)



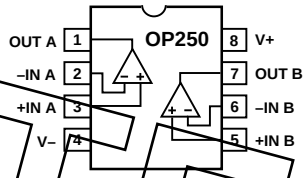
5-Lead SOT23-5 (RT Suffix)



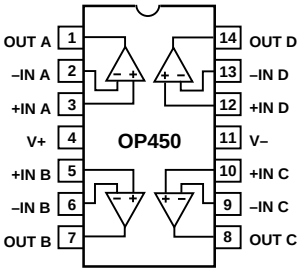
8-Lead Narrow-Body SO (S Suffix)



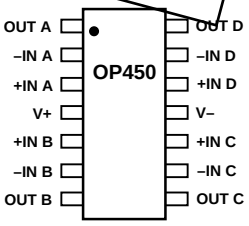
8 Lead Epoxy DIP (P Suffix)



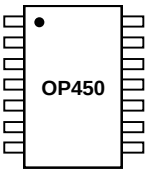
14-Lead Epoxy DIP (P Suffix)



14-Lead SO (S Suffix)



14-Lead TSSOP (RU Suffix)



This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

OP150/OP250/OP450–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = +3.0 V, V_{CM} = 0.05 V, V_O = 1.4 V, T_A = +25°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage OP150	V_{OS}				5	mV
		–40°C ≤ T_A ≤ +125°C				mV
Offset Voltage OP250/OP450	V_{OS}				5	mV
		–40°C ≤ T_A ≤ +125°C				mV
Input Bias Current	I_B			10	60	pA
		–40°C ≤ T_A ≤ +125°C				pA
Input Offset Current	I_{OS}			25		pA
		–40°C ≤ T_A ≤ +125°C				pA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 3 V	60			dB
		–40°C ≤ T_A ≤ +125°C				dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.3 V to 2.7 V		40		V/mV
		–40°C ≤ T_A ≤ +125°C				V/mV
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.3 V to 2.7 V		16		V/mV
Large Signal Voltage Gain	A_{VO}	R_L = 1 kΩ, V_O = 0.3 V to 2.7 V		10		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$					µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$					pA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$					pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 100 µA	2.95	2.99		V
		–40°C to +125°C				V
		I_L = 10 mA		2.95		V
		–40°C to +125°C				V
Output Voltage Low	V_{OL}	I_L = 100 µA		2	10	mV
		–40°C to +125°C				mV
		I_L = 10 mA		30	55	mV
		–40°C to +125°C				mV
Output Current	I_{OUT}			±250		mA
		–40°C to +125°C				mA
Open Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = 1				Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 6 V	70			dB
		–40°C ≤ T_A ≤ +125°C	68			dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		500	600	µA
		–40°C ≤ T_A ≤ +125°C		650		µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L =10 kΩ		2.7		V/µs
Settling Time	t_S	To 0.01%				µs
Gain Bandwidth Product	GBP			2		MHz
Phase Margin	Øo			75		Degrees
Channel Separation	CS	f = 1 kHz, R_L =10 kΩ				dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz				µV p-p
Voltage Noise Density	e_n	f = 1 kHz		55		nV/√Hz
Current Noise Density	i_n					pA/√Hz

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_S = +5.0 V, V_{CM} = 0.05 V, V_O = 1.4 V, T_A = +25°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage OP150	V_{OS}				5	mV
		–40°C ≤ T_A ≤ +125°C				mV
Offset Voltage OP250/OP450	V_{OS}				5	mV
		–40°C ≤ T_A ≤ +125°C				mV
Input Bias Current	I_B			30	50	pA
		–40°C ≤ T_A ≤ +125°C			60	pA
Input Offset Current	I_{OS}			0.1	8	pA
		–40°C ≤ T_A ≤ +125°C			16	pA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 5 V	60			dB
		–40°C ≤ T_A ≤ +125°C				dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.3 V to 4.7 V		40		V/mV
		–40°C ≤ T_A ≤ +125°C				V/mV
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.3 V to 2.7 V		16		V/mV
Large Signal Voltage Gain	A_{VO}	R_L = 1 kΩ, V_O = 0.3 V to 2.7 V		10		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	–40°C ≤ T_A ≤ +125°C		1.5		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			100		pA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			20		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 100 µA		4.99		V
		–40°C to +125°C				V
		I_L = 10 mA		4.95		V
		–40°C to +125°C				V
Output Voltage Low	V_{OL}	I_L = 100 µA		2		mV
		–40°C to +125°C				mV
		I_L = 10 mA		30		mV
		–40°C to +125°C				mV
Output Current	I_{OUT}			±250		mA
		–40°C to +125°C				mA
Open Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = 1				Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 6 V	75			dB
		–40°C ≤ T_A ≤ +125°C	70			dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V				µA
		–40°C ≤ T_A ≤ +125°C		550	650	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L =10 kΩ		6.5		V/µs
Full Power Bandwidth	BW_p	1% Distortion				kHz
Settling Time	t_S	To 0.01%				µs
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	Øo			75		Degrees
Channel Separation	CS	f = 1 kHz, R_L =10 kΩ				dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz				µV p-p
Voltage Noise Density	e_n	f = 1 kHz		55		nV/√Hz
Voltage Noise Density	e_n	f = 10 kHz		35		nV/√Hz
Current Noise Density	i_n					pA/√Hz

Specifications subject to change without notice.

WAFER TEST LIMITS (@ V_S = +5.0 V, V_{CM} = 0 V, T_A = +25°C unless otherwise noted.)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}		±10	mV max
Input Bias Current	I_B		50	pA max
Input Offset Current	I_{OS}		10	pA max
Input Voltage Range	V_{CM}		V– to V+	V min
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 10 V	60	dB min
Power Supply Rejection Ratio	PSRR	V = +2.7 V to +7 V	70	dB min
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ		V/mV min
Output Voltage High	V_{OH}	R_L = 2 kΩ to GND	2.9	V min
Output Voltage Low	V_{OL}	R_L = 2 kΩ to V+	55	mV max
Supply Current/Amplifier	I_{SY}	V_O = 0 V, R_L = ∞	650	µA max

NOTE
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . +7 V
Input Voltage . . . . . GND to V_S
Differential Input Voltage . . . . . 7 V
Output Short-Circuit Duration to GND[2] . . . . . Indefinite
Storage Temperature Range
P, S, RT, RU Package . . . . . –65°C to +150°C
Operating Temperature Range
OP150/OP250/OP450G . . . . . –40°C to +125°C
Junction Temperature Range
P, S, RT, RU Package . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
5-Pin SOT (RT)	325		°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W
8-Pin TSSOP (RU)	240	43	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
14-Pin SOIC (S)	120	36	°C/W
14-Pin TSSOP(RU)	180	35	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

ORDERING GUIDE

Model	Temperature Range	Package Option
OP150GS	–40°C to +125°C	8-Pin SOIC
OP150GRT	–40°C to +125°C	5-Pin SOT
OP150GBC	+25°C	DICE
OP250GP	–40°C to +125°C	8-Pin Plastic DIP
OP250GS	–40°C to +125°C	8-Pin SOIC
OP250GRU	–40°C to +125°C	8-Pin TSSOP
OP250GBC	+25°C	DICE
OP450GP	–40°C to +125°C	14-Pin Plastic DIP
OP450GS	–40°C to +125°C	14-Pin SOIC
OP450GRU	–40°C to +125°C	14-Pin TSSOP
OP450GBC	+25°C	DICE

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP150/OP250/OP450 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

DICE CHARACTERISTICS

OP150 Die Size 0.00 × 0.00 Inch, 00 Sq. Mils
Substrate (Die Backside) Is Connected to V–
Transistor Count, 00.
OP250 Die Size 0.044× 0.045 Inch, 1,980 Sq. Mils
Substrate (Die Backside) Is Connected to V–
Transistor Count, 0.
OP450 Die Size 0.052× 0.058 Inch, 3,016 Sq. Mils
Substrate (Die Backside) Is Connected to V–
Transistor Count, 127.

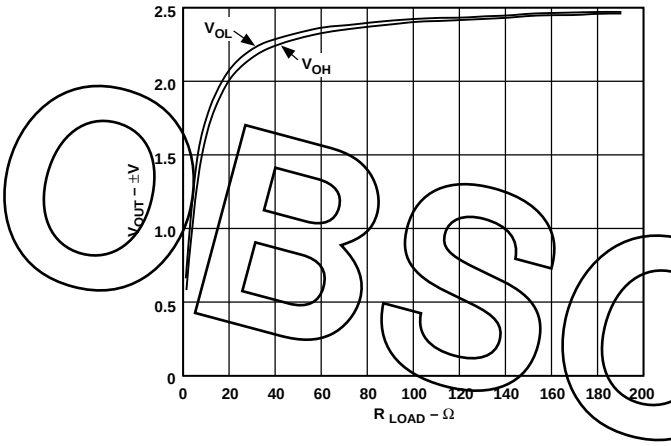


Figure 1. $\pm V_{OUT}$ vs. R_{LOAD}