5 MHz Single-Supply Operational Amplifier

OP183

FEATURES

Single supply: 3 V to 36 V
Wide bandwidth: 5 MHz
Low offset voltage: 1 mV
High slew rate: 10 V/µs
Low noise: 10 nV/√Hz
Unity gain stable
Input and output range includes GND
No phase reversal

APPLICATIONS

Multimedia
Telecom
ADC buffers
Wide band filters
Microphone preamplifiers

PIN CONNECTION

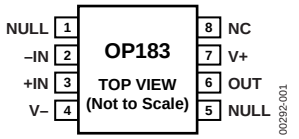


Figure 1. 8-Lead Narrow Body SOIC (S Suffix)

GENERAL DESCRIPTION

The OP183 is a single-supply, 5 MHz bandwidth amplifier with slew rates of 10 V/µs. It can operate from voltages as low as 3 V and up to 36 V. This combination of slew rate and bandwidth yields excellent single-supply ac performance, making this amplifier ideally suited for telecom and multimedia audio applications.

The OP183 also provides good dc performance with guaranteed 1 mV offset. Noise is a respectable 10 nV/√Hz. Supply current is only 1.2 mA per amplifier.

This amplifier is well suited for single-supply applications that require moderate bandwidth even when used in high gain configurations. This makes it useful in filters and instrumentation. The output drive capability and very wide full-power bandwidth of the OP183 make it a good choice for multimedia headphone drivers or microphone input amplifiers.

The OP183 is available in a SO-8 surface-mount package. It is specified over the extended industrial (−40°C to +85°C) temperature range.

Rev. D

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

5/05—Rev. C to Rev. D

Updated Format ..... Universal
Removed OP283 ..... Universal
Updated Outline Dimensions 16
Changes to Ordering Guide 16

2/02—Rev. B to Rev. C

Edits to FEATURES 1
Edits to GENERAL DESCRIPTION 1
Edits to SPECIFICATIONS 2–3
Edits to Package Type 4
Edits to ORDERING GUIDE 4
Edits to ABSOLUTE MAXIMUM RATINGS 4
Edits to OUTLINE DIMENSIONS 12

Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS @ V_S = 5 V

T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = 2.5 V, V_{OUT} = 2.5 V,		0.025	1.0	mV
		−40°C ≤ T_A ≤ +85°C			1.25	mV
Input Bias Current	I_B	V_{CM} = 2.5 V, V_{OUT} = 2.5 V,		350	600	nA
		−40°C ≤ T_A ≤ +85°C		430	750	nA
Input Offset Current	I_{OS}	V_{CM} = 2.5 V, V_{OUT} = 2.5 V,				nA
		−40°C ≤ T_A ≤ +85°C		11	±50	nA
Input Voltage Range			0		3.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 to 3.5 V				
		−40°C ≤ T_A ≤ +85°C	70	104		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, 0.2 ≤ V_O ≤ 3.8 V	100			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			4		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			−1.6		nA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ to GND	4.0	4.22		V
Output Voltage Low	V_{OL}	R_L = 2 kΩ to GND		50	75	mV
Short-Circuit Limit	I_{SC}	Source		25		mA
		Sink		30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 4 V to 6 V,				
		−40°C ≤ T_A ≤ +85°C	70	104		dB
Supply Current/Amplifier	I_{SY}	V_O = 2.5 V,				
		−40°C ≤ T_A ≤ +85°C		1.2	1.5	mA
Supply Voltage Range	V_S		3		±18	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	5	10		V/µs
Full Power Bandwidth	BWp	1% Distortion		>50		kHz
Settling Time	t_S	To 0.01%		1.5		µs
Gain Bandwidth Product	GBP			5		MHz
Phase Margin	ϕm			46		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz, V_{CM} = 2.5 V		10		nV/√Hz
Current Noise Density	i_n			0.4		pA/√Hz

ELECTRICAL CHARACTERISTICS @ V_S = 3 V

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = 1.5 V, V_{OUT} = 1.5 V,		0.3	1.0	mV
		−40°C ≤ T_A ≤ +85°C			1.25	mV
Input Bias Current	I_B	V_{CM} = 1.5 V, V_{OUT} = 1.5 V,		350	600	nA
		−40°C ≤ T_A ≤ +85°C			750	nA
Input Offset Current	I_{OS}	V_{CM} = 1.5 V, V_{OUT} = 1.5 V,				nA
		−40°C ≤ T_A ≤ +85°C		11	±50	nA
Input Voltage Range			0		1.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 1.5 V,				
		−40°C ≤ T_A ≤ +85°C	70	103		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, 0.2 ≤ V_O ≤ 1.8 V	100	260		V/mV
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ to GND	2.0	2.25		V
Output Voltage Low	V_{OL}	R_L = 2 kΩ to GND		90	125	mV
Short-Circuit Limit	I_{SC}	Source		25		mA
		Sink		30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.5 V to 3.5 V,				
		−40°C ≤ T_A ≤ +85°C	60	113		dB
Supply Current/Amplifier	I_{SY}	−40°C ≤ T_A ≤ +85°C, V_O = 1.5 V		1.2	1.5	mA
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBP			5		MHz
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz, V_{CM} = 1.5 V		10		nV/√Hz

ELECTRICAL CHARACTERISTICS @ V_S = ±15 V

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.01	1.0	mV
		−40°C ≤ T_A ≤ +85°C			1.25	mV
Input Bias Current	I_B			300	600	nA
		−40°C ≤ T_A ≤ +85°C		400	750	nA
Input Offset Current	I_{OS}	−40 ≤ T_A ≤ +85°C		11	±50	nA
Input Voltage Range			−15		+13.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −15 V to +13.5 V,				
		−40°C ≤ TA ≤ +85°C	70	86		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	100	1000		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			−1.6		nA/°C
Long-Term Offset Voltage	V_{OS}	Note[1]			1.5	mV
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ to GND, −40°C ≤ T_A ≤ +85°C	13.9	14.1		V
Output Voltage Low	V_{OL}	R_L = 2 kΩ to GND, −40°C ≤ T_A ≤ +85°C		−14.05	−13.9	V
Short-Circuit Limit	I_{SC}	Source		30		mA
		Sink		50		mA
Open-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = +1		15		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ± 2.5 V to ± 18 V,				
		−40°C ≤ T_A ≤ +85°C	70	112		dB
Supply Current/Amplifier	I_{SY}	V_S = ±18 V, V_O = 0 V,				
		−40°C ≤ T_A ≤ +85°C		1.2	1.75	mA
Supply Voltage Range	V_S		3		±18	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	10	15		V/µs
Full Power Bandwidth	BW_p	1% Distortion		50		kHz
Settling Time	t_S	To 0.01%		1.5		µs
Gain Bandwidth Product	GBP			5		MHz
Phase Margin	ϕm			56		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		10		nV/√Hz
Current Noise Density	i_n			0.4		pA/√Hz

[1] Long-term offset voltage is guaranteed by a 1,000 hour life test performed on three independent lots at 125°C, with an LTPD of 1.3.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	±18 V
Input Voltage	±18 V
Differential Input Voltage[1]	±7 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	
S Package	−65°C to +150°C
Operating Temperature Range	
OP183	−40°C to +85°C
Junction Temperature Range	
S Package	−65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	300°C

[1] For supply voltages less than ±7 V, the absolute maximum input voltage is equal to the supply voltage. Maximum input current should not exceed 2 mA.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply to packaged parts, unless otherwise noted.

Table 5.

Package Type	θ_{JA}[1]	θ_{JC}	Units
8-Lead SOIC (S)	158	43	°C/W

[1] θ_{JA} is specified for worst-case conditions; in other words, θ_{JA} is specified for device soldered in circuit board for SOIC packages.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

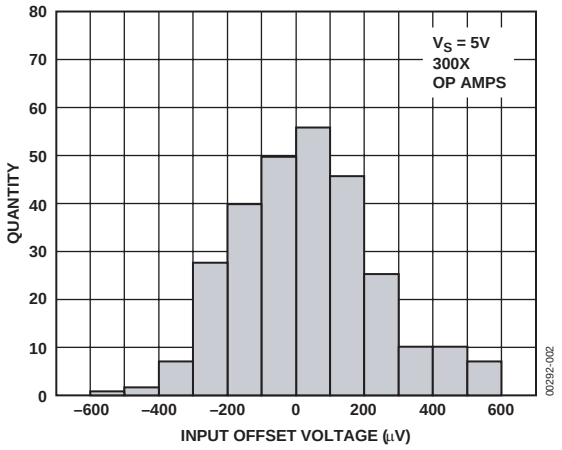


Figure 2. OP183 Input Offset Voltage Distribution @ 5 V

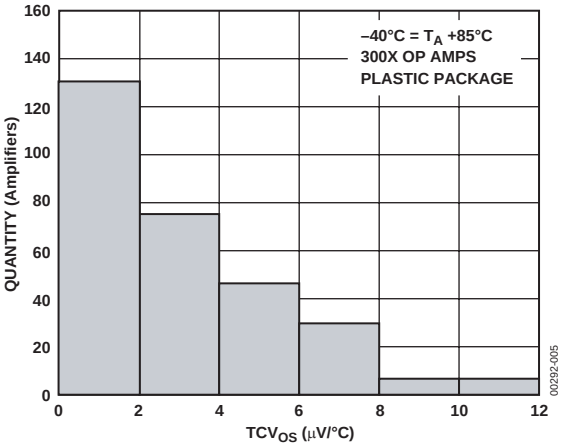


Figure 5. OP183 Input Offset Voltage Drift (TCV_{OS}) Distribution @ ±15 V

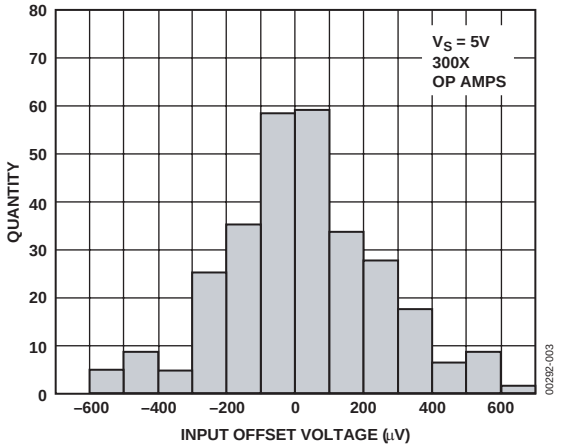


Figure 3. OP183 Input Offset Voltage Distribution @ ±15 V

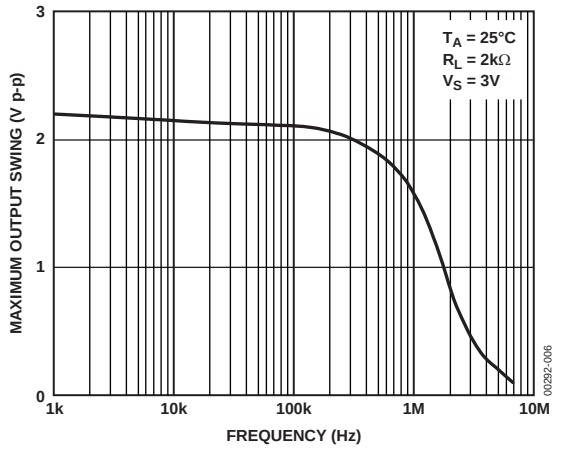


Figure 6. OP183 Maximum Output Swing vs. Frequency @ 3 V

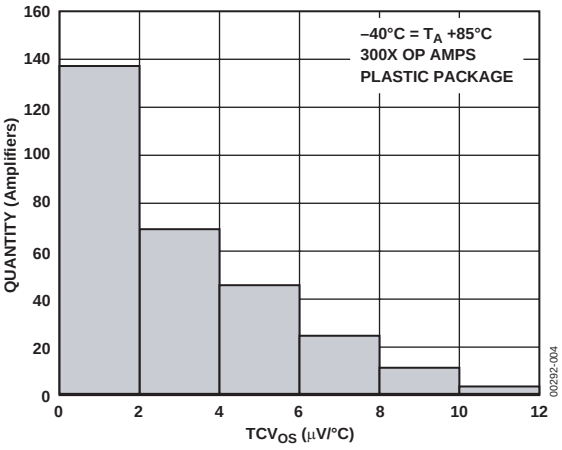


Figure 4. OP183 Input Offset Voltage Drift (TCV_{OS}) Distribution @ 5 V

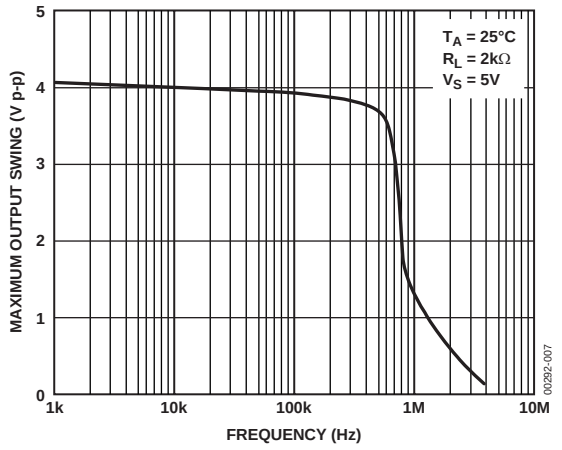


Figure 7. OP183 Maximum Output Swing vs. Frequency @ 5 V

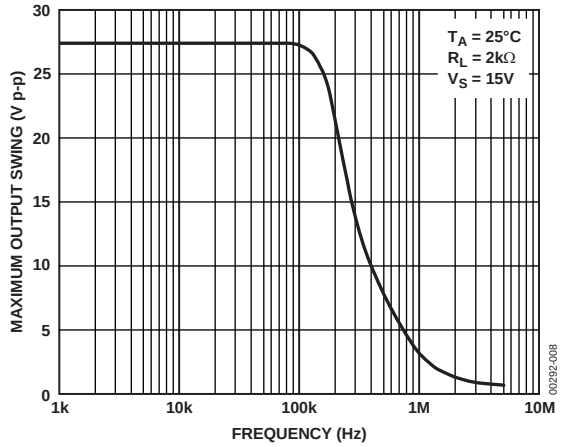


Figure 8. OP183 Maximum Output Swing vs. Frequency @ ±15 V

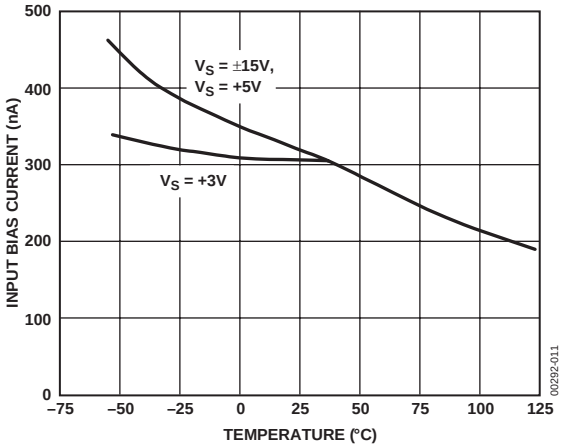


Figure 11. Input Bias Current vs. Temperature

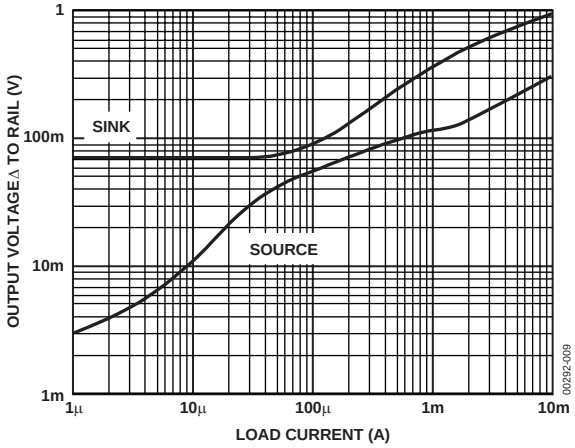


Figure 9. Output Voltage vs. Sink & Source Current

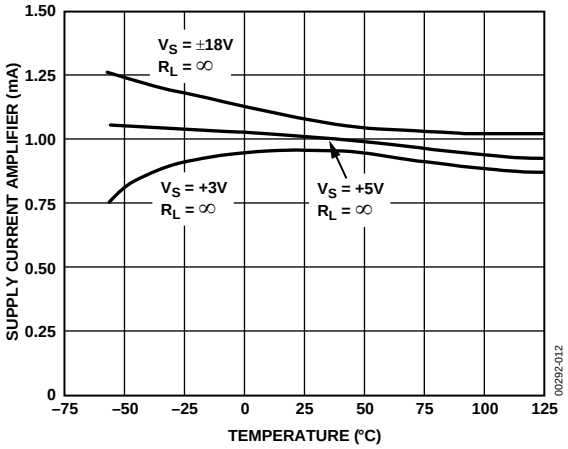


Figure 12. Supply Current per Amplifier vs. Temperature

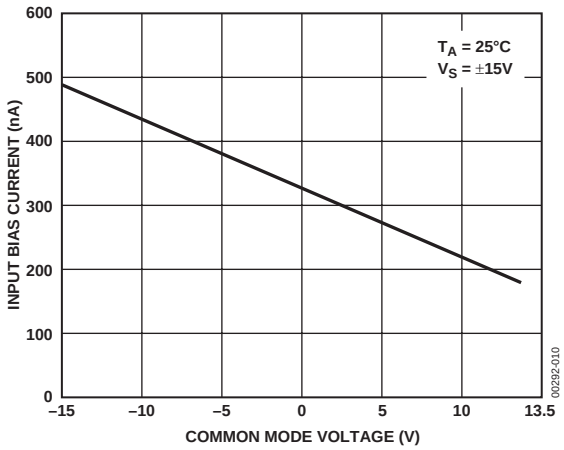


Figure 10. Input Bias Current vs. Common-Mode Voltage

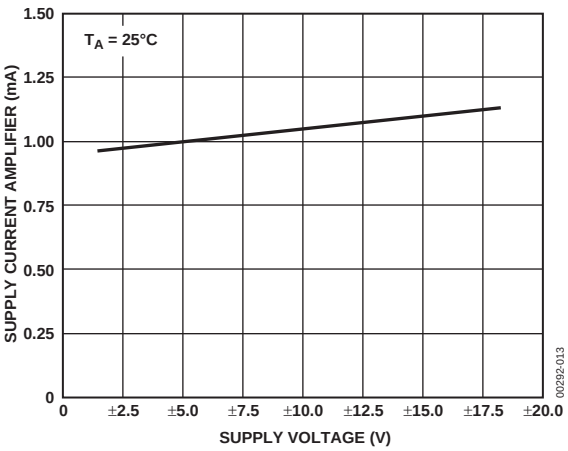


Figure 13. Supply Current per Amplifier vs. Supply Voltage

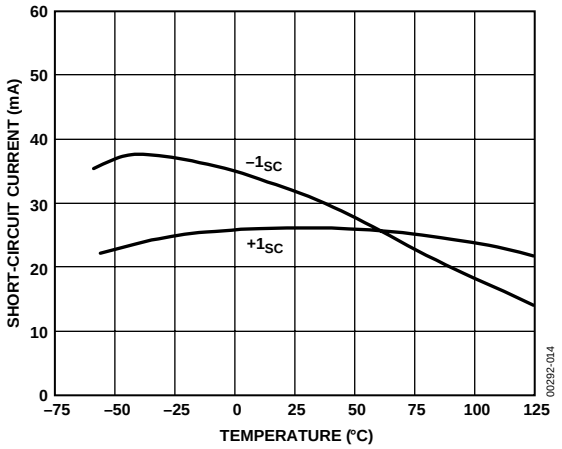


Figure 14. Short-Circuit Current vs. Temperature @ 5 V

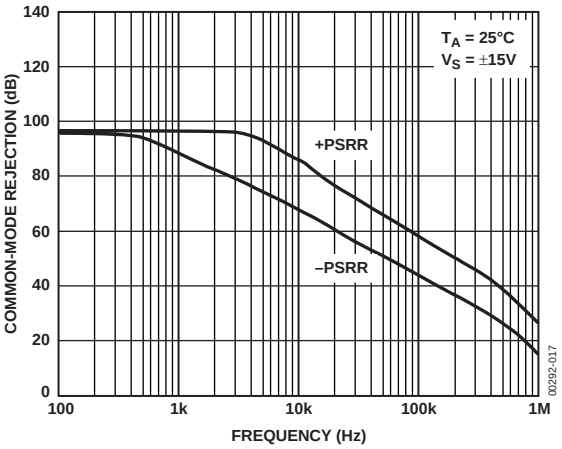


Figure 17. Power Supply Rejection vs. Frequency

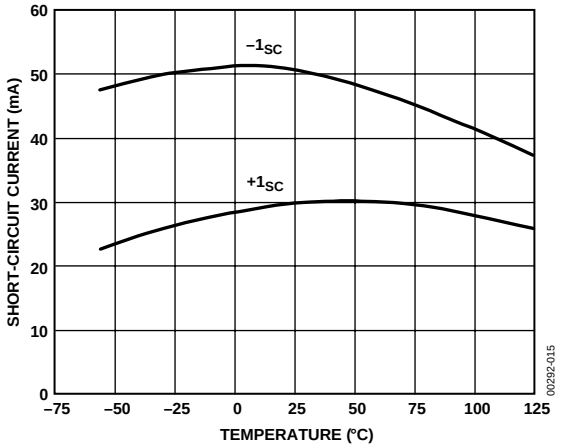


Figure 15. Short-Circuit Current vs. Temperature @ ±15 V

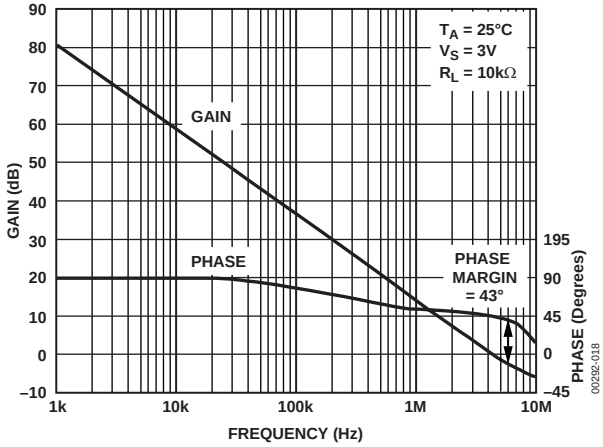


Figure 18. Open-Loop Gain and Phase vs. Frequency @ 3 V

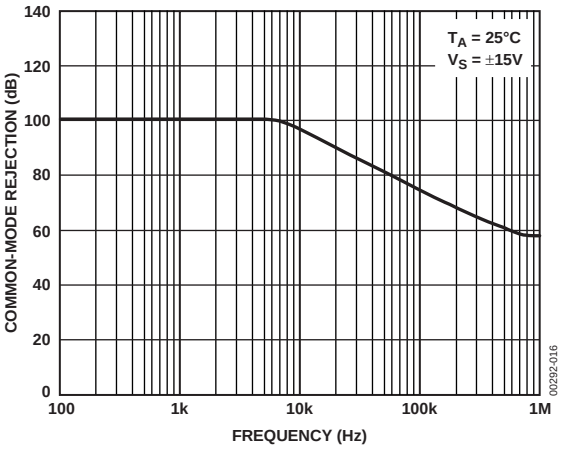


Figure 16. Common-Mode Rejection vs. Frequency

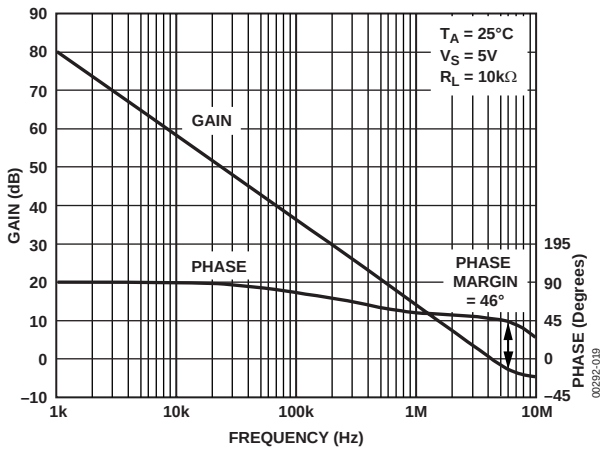


Figure 19. Open-Loop Gain and Phase vs. Frequency @ 5 V

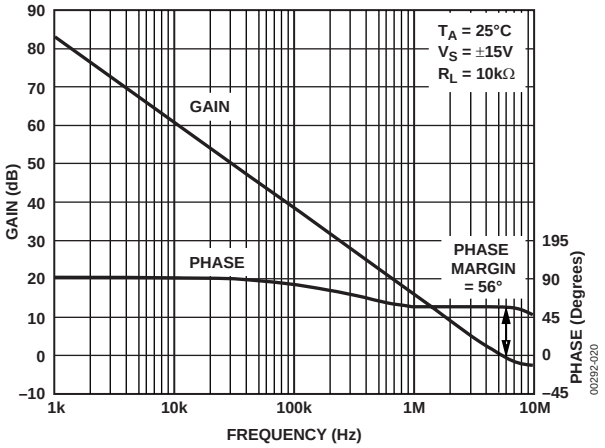


Figure 20. Open-Loop Gain and Phase vs. Frequency @ ±15 V

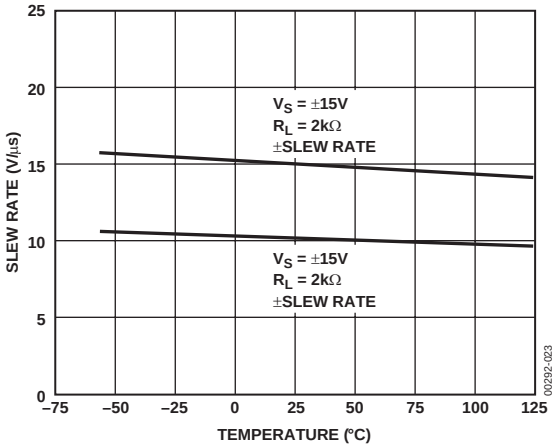


Figure 23. Slew Rate vs. Temperature

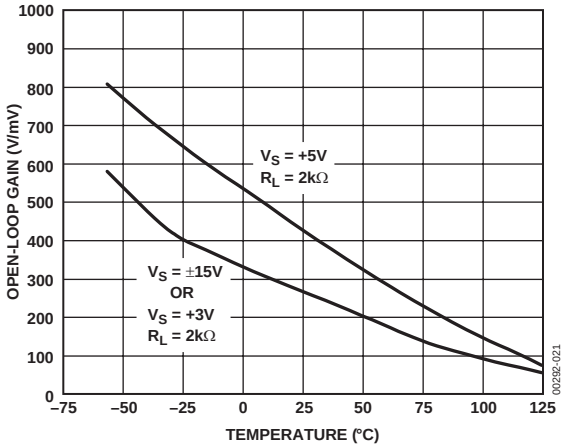


Figure 21. Open-Loop Gain vs. Temperature

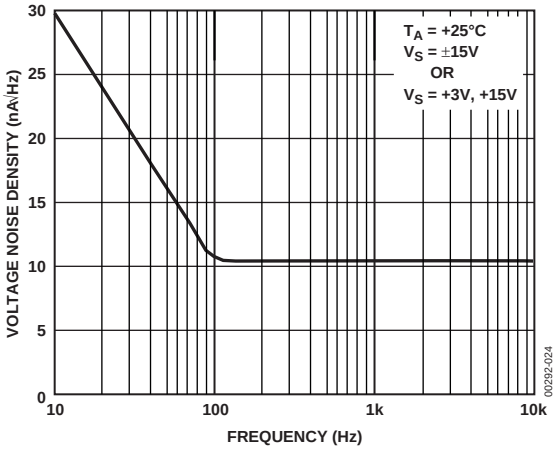


Figure 24. Voltage Noise Density vs. Frequency

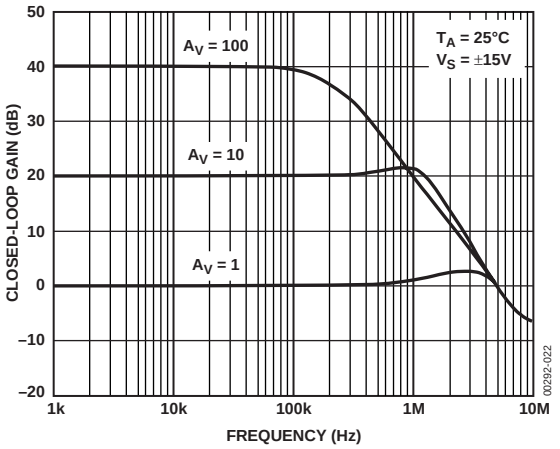


Figure 22. Closed-Loop Gain vs. Frequency

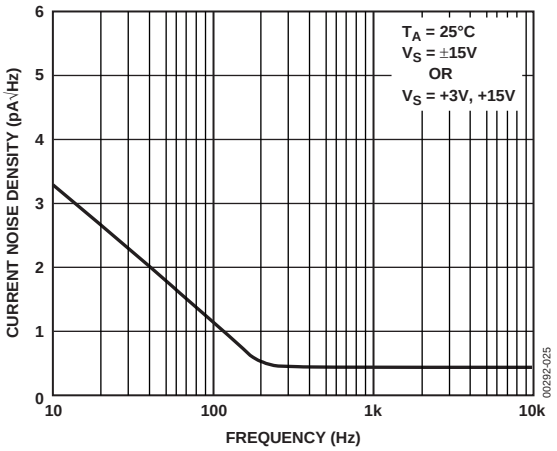


Figure 25. Current Noise Density vs. Frequency

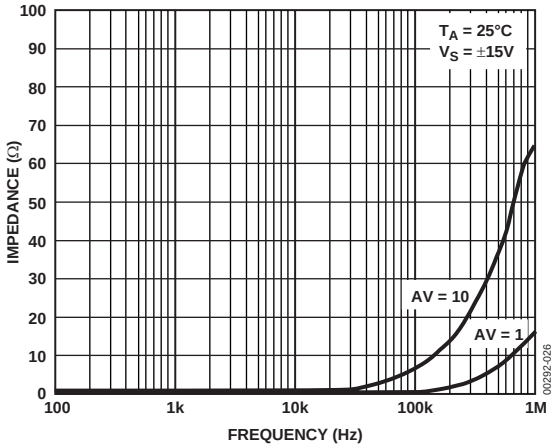


Figure 26. Closed-Loop Output Impedance vs. Frequency

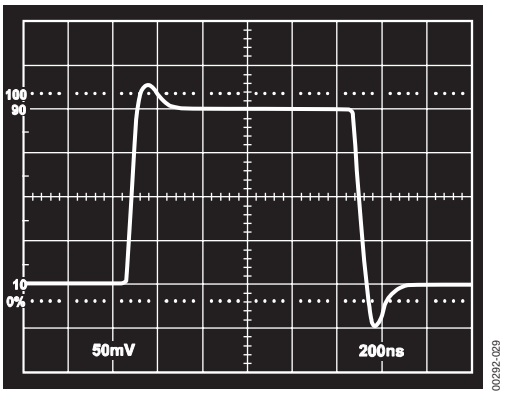


Figure 29. Small Signal Performance @ ±15 V

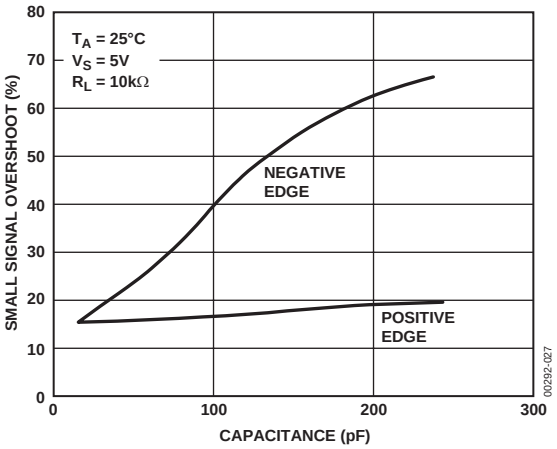


Figure 27. Small Signal Overshoot vs. Load Capacitance

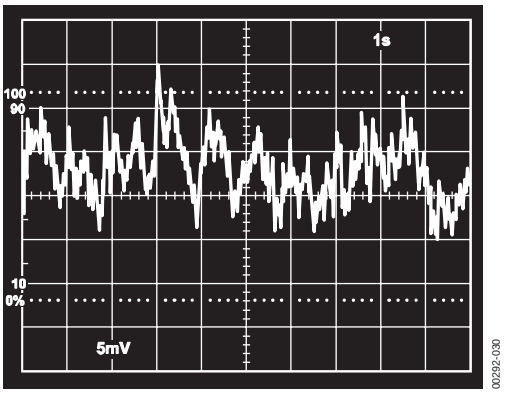


Figure 30. 0.1 Hz to 10 Hz Noise @ ±2.5 V

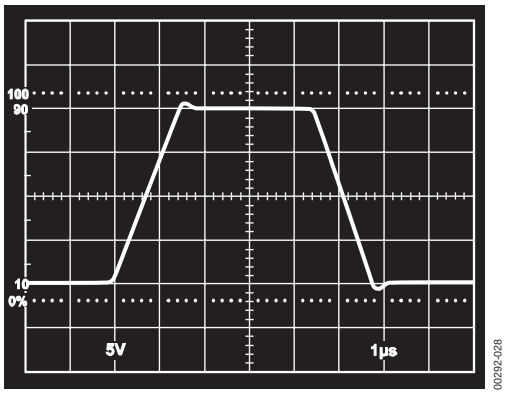


Figure 28. Large Signal Performance @ ±15 V

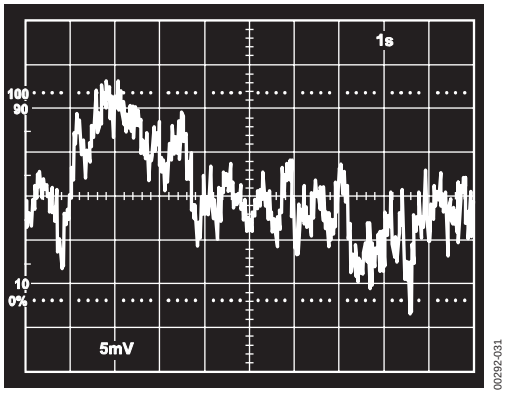


Figure 31. 0.1 Hz to 10 Hz Noise @ ±15 V

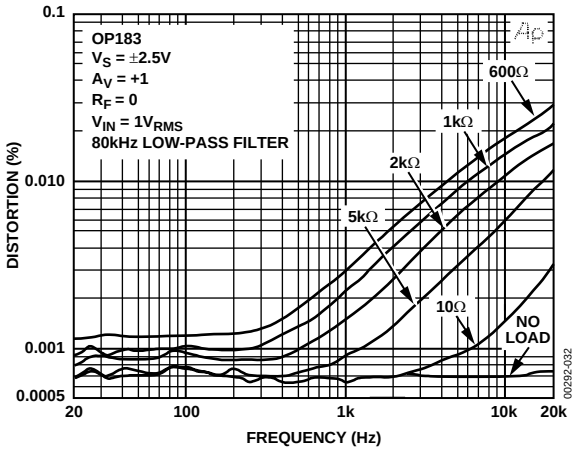


Figure 32. THD + Noise vs. Frequency for Various Loads

APPLICATIONS

OFFSET ADJUST

Figure 33 shows how the offset voltage of the OP183 can be adjusted by connecting a potentiometer between Pins 1 and 5, and connecting the wiper to V_{EE}. The recommended value for the potentiometer is 10 kΩ. This will give an adjustment range of approximately ±1 mV. If a larger adjustment span is desired, a 50 kΩ potentiometer will yield a range of ±2.5 mV.

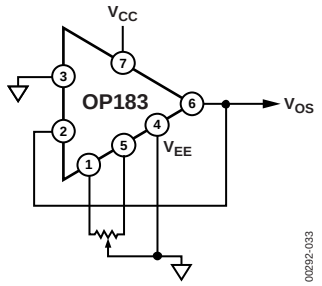


Figure 33. OP183 Offset Adjust

PHASE REVERSAL

The OP183 is protected against phase reversal as long as both of the inputs are within the range of the positive supply and the negative supply −0.6 V. If there is a possibility of either input going beyond these limits, however, the inputs should be protected with a series resistor to limit input current to 2 mA.

DIRECT ACCESS ARRANGEMENT

The OP183 can be used in a single supply direct access arrangement (DAA) as shown in Figure 34. This figure shows a portion of a typical DAA capable of operating from a single 5 V supply; with minor modifications it should also work on 3 V supplies. Amplifiers A2 and A3 are configured so that the transmit signal TxA is inverted by A2 and not inverted by A3. This arrangement drives the transformer differentially so that the drive to the transformer is effectively doubled over a single amplifier arrangement. This application takes advantage of the ability of the OP183 to drive capacitive loads and to save power in single-supply applications.

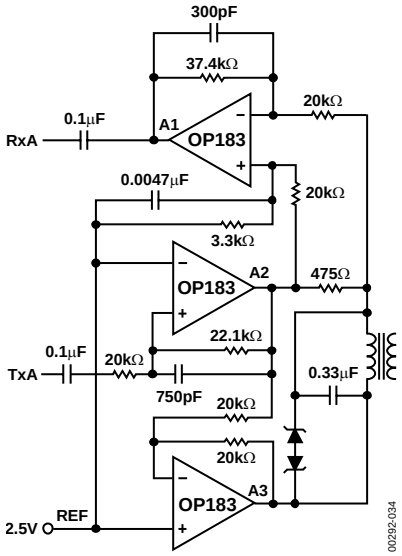


Figure 34. Direct Access Arrangement

5 V ONLY STEREO DAC FOR MULTIMEDIA

The low noise and single-supply capability of the OP183 are ideally suited for stereo DAC audio reproduction or sound synthesis applications, such as multimedia systems. Figure 35 shows an 18-bit stereo DAC output setup that is powered from a single 5 V supply. The low noise preserves the 18-bit dynamic range of the AD1868.

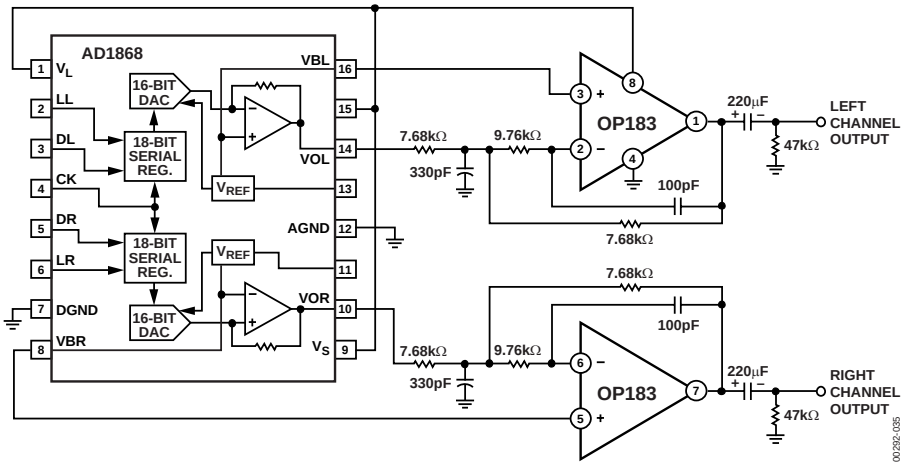


Figure 35. 5 V Only 18-Bit Stereo DAC

LOW VOLTAGE HEADPHONE AMPLIFIERS

Figure 36 shows a stereo headphone output amplifier for the AD1849 16-bit SoundPort® Stereo Codec device. The pseudoreference voltage is derived from the common-mode voltage generated internally by the AD1849, thus providing a convenient bias for the headphone output amplifiers.

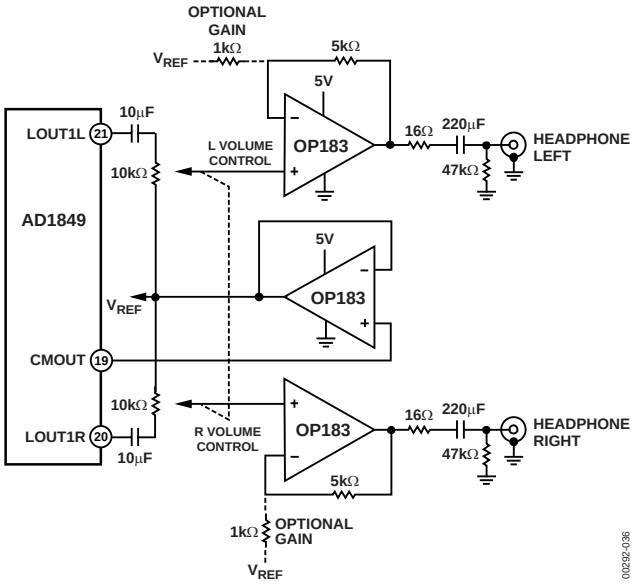


Figure 36. Headphone Output Amplifier for Multimedia Sound Codec

LOW NOISE MICROPHONE AMPLIFIER FOR MULTIMEDIA

The OP183 is ideally suited as a low noise microphone preamp for low voltage audio applications. Figure 37 shows a gain of 100 stereo preamp for the AD1849 16-bit SoundPort Stereo Codec chip. The common-mode output buffer serves as a phantom power driver for the microphones.

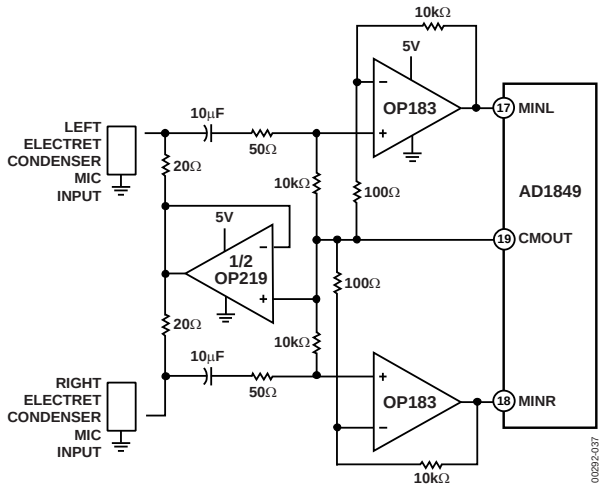


Figure 37. Low Noise Stereo Microphone Amplifier for Multimedia Sound Codec

3 V 50 HZ/60 HZ ACTIVE NOTCH FILTER WITH FALSE GROUND

To process ac signals, it may be easier to use a false-ground bias rather than the negative supply as a reference ground. This would reject the power line frequency interference which can often obscure low frequency physiological signals, such as heart rates, blood pressures, EEGs, and ECGs.

Figure 38 shows a 50 Hz/60 Hz active notch filter for eliminating line noise in patient monitoring equipment. It has several kilohertz bandwidth and is not sensitive to false-ground perturbations. The simple false-ground circuit shown achieves good rejection of low frequency interference using standard off-the-shelf components.

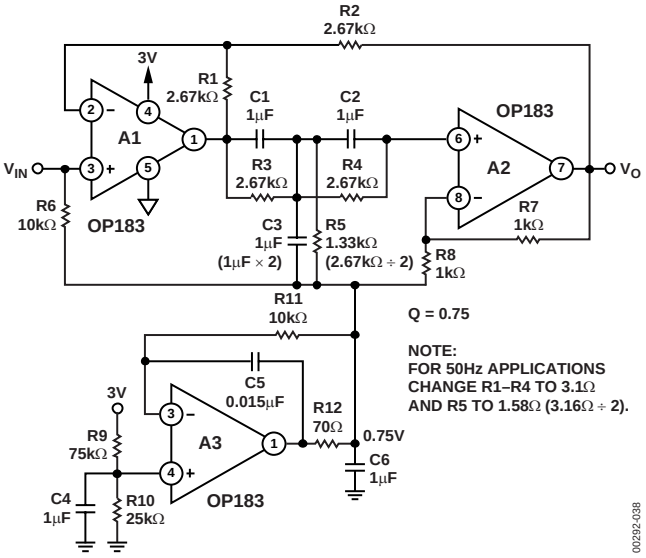


Figure 38. 3 V Supply 50 Hz/60 Hz Notch Filter with Pseudo Ground

Amplifier A3 biases A1 and A2 to the middle of their input common-mode range. When operating on a 3 V supply, the center of the common-mode range of the OP183 is 0.75 V. This notch filter effectively squelches 60 Hz pickup at a filter Q of 0.75. To reject 50 Hz interference, change the resistors in the twin-T section (R1 through R5) from 2.67 kΩ to 3.16 kΩ.

The filter section uses OP183 op amps in a twin-T configuration whose frequency selectivity is very sensitive to the relative matching of the capacitors and resistors in the twin-T section. Mylar is the material of choice for the capacitors, and the relative matching of the capacitors and resistors determines the filter's pass-band symmetry. Using 1% resistors and 5% capacitors produces satisfactory results.

LOW VOLTAGE FREQUENCY SYNTHESIZER FOR WIRELESS TRANSCEIVER

The low noise and low voltage operation capability of the OP183 serves well for the loop filter of a frequency synthesizer.

Figure 39 shows a typical application in a radio transceiver. The phase noise performance of the synthesizer depends on low noise contribution from each component in the loop as the noise is amplified by the frequency division factor of the prescaler.

The resistors used in the low-pass filter should be of low to moderate values to reduce noise contribution due to the input bias current as well as the resistors themselves. The filter cutoff frequency should be chosen to optimize the loop constant.

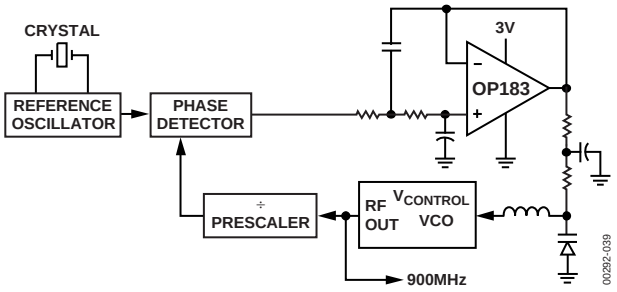


Figure 39. Low Voltage Frequency Synthesizer for a Wireless Transceiver

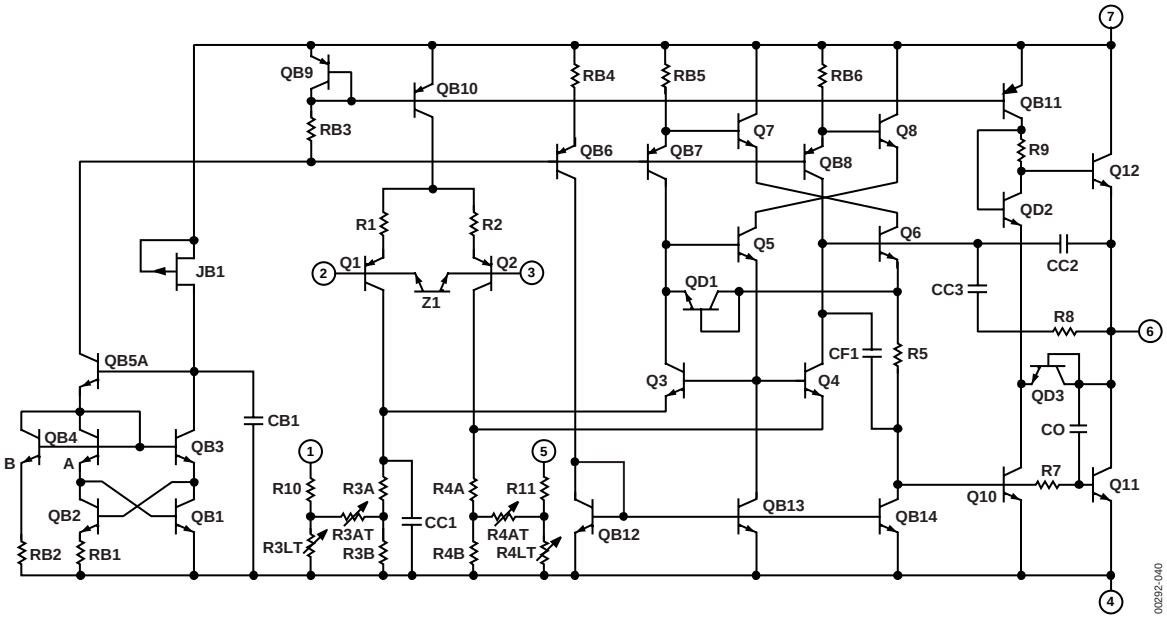
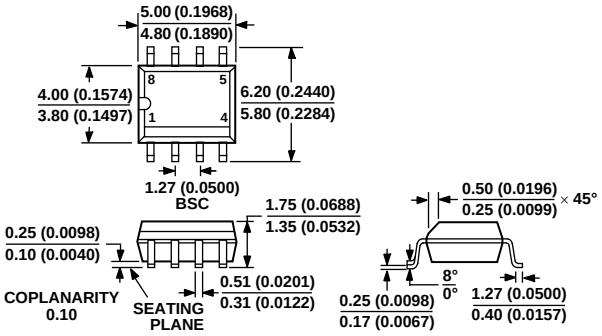


Figure 40. OP183 Simplified Schematic

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 41. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
S-Suffix
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP183GS	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)
OP183GS-REEL	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)
OP183GS-REEL7	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)
OP183GSZ[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)
OP183GSZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)
OP183GSZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)

[1]Z = Pb free part.

C00292-0-5/05(D)