Panel interface BU8310AK / BU8311KS / BU8313K

The BU8310AK, BU8311KS, and BU8313K are large-scale integrated circuits for telephones, which enable a serial input/output interface between the key input required for telephone panel boards and LED control functions. They reduce the number of wiring harnesses needed between the main board in the telephone and the panel board, and take some of the processing load off the main CPU.

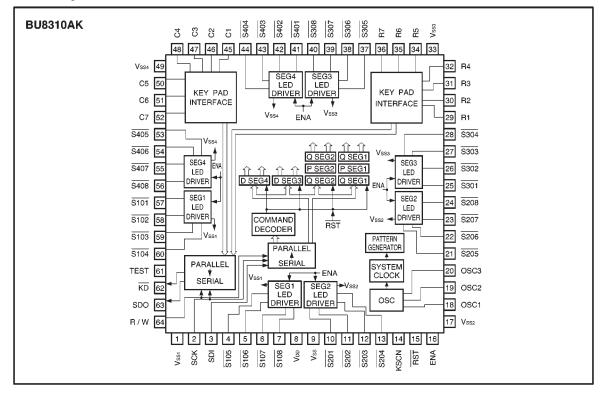
Applications
Telephones and cordless telephones

Features

- 1) Keypad matrix interface
 - (1) Key input is output as 16-bit serial data.
 - ② Internal chattering prevention circuit built into the key input circuit.
- 2) LED interface
 - ① LED control commands input as 16-bit serial data.
 - ② Bits with a pattern generator and pattern register can be assigned three independent flashing patterns in addition to being lighted or off.
 - ③ Power consumption can be reduced using RST pin input.
 - ④ LED on and off control can be initiated using ENA pin input or by commands setting all LEDs valid or invalid.

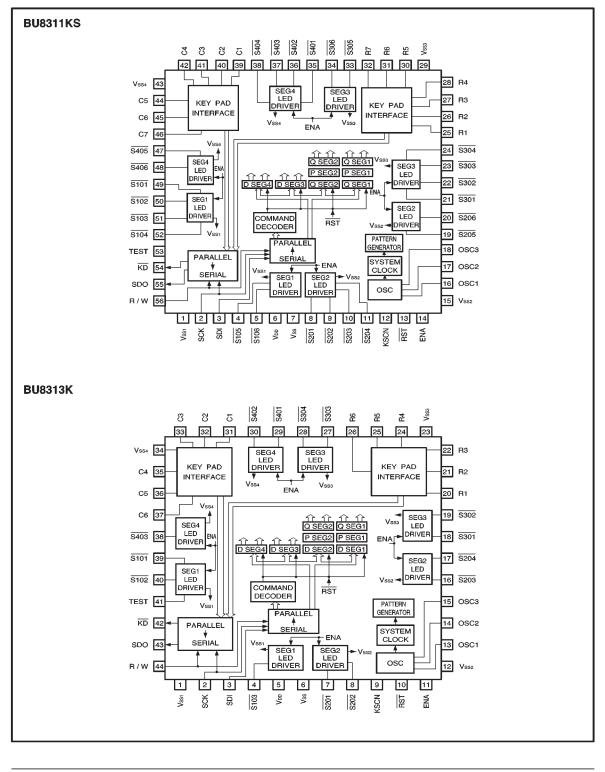
BU8310AK / BU8311KS / BU8313K

Block diagram



278

BU8310AK / BU8311KS / BU8313K



ROHM

BU8310AK / BU8311KS / BU8313K

Absolute maximum	ratings (Ta = 25°C)
------------------	---------------------

Parameter	Symbol	Limits	Unit	Conditions
Power supply voltage	VDD	7.0	V	-
Power dissipation	Pd	500	mW	*1
Operating temperature	Topr	-25~+60	C	_
Storage temperature	Tstg	-55~+125	C	_
Input voltage	VIN	Vss-0.3~Vdd+0.3	V	*2
Output voltage 1	Vout1	Vss-0.3~Vdd+0.3	V	*3
Output voltage 2	Vout2	Vss~7.0	V	*4
Output current	Іоит	20	mA	*4

*1 Reduced by 5mW for each increase in Ta of 1 $^\circ C$ over 25 $^\circ C.$

*2 SCK, SDI, ENA, RST, R/W, KSCN, and TEST pins

*3 SDO and KD pins

*4 LED drive output pins

Recommended operating conditions

Parameter	Symbol	Limits	Unit	Conditions
Power supply voltage	Vdd	1.8~5.5	V	_
Oscillation frequency	fosc	535	Hz	$R_i=2.2M\Omega$, $R_x=270k\Omega$ $C_x=3.3nF$
Key connection resistance	Rкс	0~5	kΩ	—

Pin descriptions

Pin No. BU8310AK	Pin No. BU8311KS	Pin No. BU8313K	Pin name	Function	I/O circuit
$57 \sim 60 \\ 4 \sim 7 \\ 10 \sim 13 \\ 21 \sim 24 \\ 25 \sim 28 \\ 37 \sim 40 \\ 41 \sim 44 \\ 53 \sim 56$	$\begin{array}{c} 49 \sim 52 \\ 4 \sim 5 \\ 8 \sim 11 \\ 19 \sim 20 \\ 21 \sim 24 \\ 33 \sim 34 \\ 35 \sim 38 \\ 47 \sim 48 \end{array}$	$39 \sim 40$ 4 7~ 8 16~17 18~19 27~28 29~30 38	$\overline{S101} \sim \overline{S108}$ $\overline{S201} \sim \overline{S208}$ $\overline{S301} \sim \overline{S308}$ $\overline{S401} \sim \overline{S408}$	These are the output pins for LED drive. They are "L" when "1" is applied to the data register (D), and "Z" (high impedance) at all other times.	D
29~32 34~36 45~48 50~52	25~28 30~32 39~42 44~46	20~22 24~26 31~33 35~37	R1 ~ R4 R5 ~ R7 C1 ~ C4 C5 ~ C7	These are the keypad input pins. They are used to connect a single-contact keypad.	с
62	54	42	KD	This is the output pin for the key press state. When a key is pressed, a "L" state is output. When no keys are pressed, these are "Z" (high impedance).	D
3	3	3	SDI	This is the serial data input pin. Data is output in the pertinent data format.	А
63	55	43	SDO	This is the serial data output pin. Data is output in the pertinent data format.	E
2	2	2	SCK	This is the shift clock input pin for serial data. Serial data is read from the SDO pin one bit at a time, at the rising edge, when R/W is "H". SDI is written one bit at a time, at the rising edge, when R/W is "L".	в

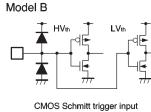
BU8310AK / BU8311KS / BU8313K

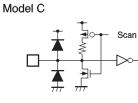
Pin No. BU8310AK	Pin No. BU8311KS	Pin No. BU8313K	Pin name	Function	I/O Circuit
64	56	44	R/W	This is the input pin which switches between the read and write modes. The read mode (serial output of key data) is accessed when this is "H". Key data is set to the output serial register at the falling edge. The write mode (serial input of data) is accessed when this key is "L". Serial data is taken up internally at the rising edge.	в
18~20	16~18	13~15	OSC1~OSC3	These are the I/O pins for the internal oscillator. The recommended values are as follows: $R_i=2.2M\Omega$, $R_x=270k\Omega$, $C_x=3.3nF$	F
14	12	9	KSCN	This is used for key scan control input. At "H", key scanning is carried out only when a key is pressed. At "L", key scanning is carried out at all times.	A
15	13	10	RST	This is the reset signal input pin. Normal operation is carried out when this pin is "H". When this pin is "L", all data in the internal registers is reset, and the internal oscillator stops.	в
16	14	11	ENA	This is the input pin for LED ON/OFF control. At "H", output for LED drive is valid. At "L", all LED drive output is turned off.	A
61	53	41	TEST	This is the test input pin, and is normally used at "L".	A
8	6	5	Vdd	This is the VDD pin	-
9	7	6	Vss	This is the Vss pin	-
1, 17, 33, 49	1, 15, 29, 43	1, 12, 23, 34	VSS1~VSS4	These are the Vss pins for segments 1 to 4 of the LED drive output.	-

Input/output circuits



CMOS input







Model D

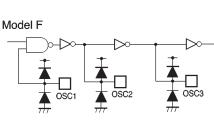




NMOS open drain output







Oscillation circuit input/output

Fig. 1

BU8310AK / BU8311KS / BU8313K

•Electrical characteristics

DC characteristics (unless otherwise noted,Ta = 25 $^{\circ}$ C, V_{DD} = 3 \sim 5V)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Supply current 1	IDD1	-	0.01	2.0	μA	At rest (RST =L)
Supply current 2	IDD2	—	7	20	μA	When operating VDD = 1.8V
Supply current 3	Ірдз	-	70	200	μA	When operating VDD =5.5V
Input high level voltage	Vін	0.8Vdd	_	VDD	V	*1
Input low level voltage	VIL	0	_	0.2VDD	V	*1
Input high level current	Ін	—	_	1	μA	*1
Input low level current	lı∟	-	_	1	μA	*1
Output high level voltage	Vон	0.9Vdd	_	Vdd	V	No load *2
Output low level voltage 1	Vol1	0	_	0.1VDD	V	No load *3
Output low level voltage 2	Vol2	0	_	0.5	V	*4

*1 SCK, SDI, ENA, RST, R/W, KSCN, and TEST pins

*2 SDO pin

*3 SDO and $\overline{\text{KD}}$ pins

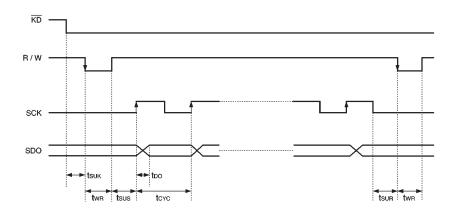
*4 Values for LED drive output pins are at VDD = 5 V, IOL = 20 mA

	Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
SDI	Setup time	tsui	100	—	—	ns	
501	Hold time	tHI	100	—	—	ns	
Serial of	clock cycle	tcvc	500	—	—	ns	DUTY=50%
SDO o	utput delay time	too	100	-	—	ns	
	Setup time R	tsun	100	—	—	ns	
	Setup time W	tsuw	100	—	—	ns	
R/W	Setup time K	tsuk	500	—	_	ns	
n / w	Setup time S	ts∪s	100	-	-	ns	
	Pulse width R	twr	500	-	-	ns	
	Pulse width W	tww	500	—	_	ns	
RST p	RST pulse width		500	—	—	ns	
Key de	bounce time	tов	—	30	—	ms	

AC characteristics (unless otherwise noted, Ta = 25 $^{\circ}$ C, V_{DD} = 3 \sim 5V)

BU8310AK / BU8311KS / BU8313K

Serial data output timing



Serial data input timing

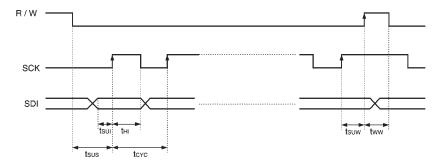


Fig. 2

BU8310AK / BU8311KS / BU8313K

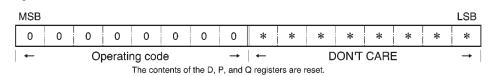
•Data formats (Serial data is input and output with the MSB coming first.)

MSB															LSB	
R7	R6	R5	R4	R3	R2	R1	0	C7	C6	C5	C4	СЗ	C2	C1	1	BU8310A BU8311K
-		ROW	key d	lata		->		←		CC)L key	[,] data		→		Decorri
R6	R5	R4	R3	R2	R1	0	0	C6	C5	C4	СЗ	C2	C1	0	1	BU8313k
-	RC	OW ke	y data	a	→			-	C	COL k	ey da	ta	→			
Data r	registe	r write	e comi	mand												
MSB															LSB	
0	0	0	1	S4	S3	S2	S1	08	07	06	05	04	03	02	01	BU8310A
←0	peratir	ng cod	le →	+	Segr	nent	→	←			Outp	out pin			→	
0	0	0	1	S4	S3	S2	S1	*	*	06	05	04	03	02	01	BU8311K
←0	peratir	ng cod	le →	-	Segr	nent	-	← DON'T	→ CARE	-		Outp	out pin	I	→	
0	0	0	1	S4	S3	S2	S1	*	* 04 03	03 03 *	*	*	02	01	*	BU8313
<u> </u>			. 1		:			u: 1	00		0					
		: The up		gment is			→ e middle	← e segme	nts are 2	2 and 3,	Outpu , and the		segmen	t is 4.	→ I LSB	
Patter MSB	Note n regit	ster w	pper seg rite cc	ommai	s Segme nd P	ent 1, the	e middle	e segme	nts are 2 07	2 and 3, 06	, and the	e lower s	segmen 03	t is 4. 02		BU8310/
Patter MSB	Note n regi:	ster w	pper seg rite cc	gment is ommai	s Segme	ent 1, the	e middle	e segme			, and the	e lower s			LSB	BU8310 <i>4</i>
Patter MSB	Note n regit	ster w	pper seg rite cc	gment is ommai	s Segme nd P	ent 1, the	e middle	e segme			, and the	e lower s			LSB	
Patter MSB 0 ↓ ← O	Note n regi: 0 peratir	ster w	pper seg rite cc 0 de →	gment is pmmai Q Pat	s Segme nd P tern	S2 Seg	e middle S1 ment S1 ment	e segme 08 ← *	07 * →	06 06 ←	, and the 05 Outp	04 04 04 04	03	02	LSB 01 →	
Patter MSB 0 ↓ ← O	Note n regis 0 peratir	ster w	pper seg rite cc 0 de →	gment is pmmai Q Pat	s Segme nd P tern P	S2 Seg	e middle S1 ment S1 ment	e segme 08 ← *	07 * →	06 06 ←	, and the 05 Outp	04 04 04 04	03	02	LSB 01 →	BU83111
Patter MSB 0 ↓ ← O	Note n regis 0 peratir 0 peratir	the up ster w 1 ng coc 1 ng coc	pper seq rite co 0 $de \rightarrow$ $de \rightarrow$ $de \rightarrow$	Q Pat Q Pat Q Pat	s Segme nd P tern P tern	S2 S2 Seg S2 S2 Seg S2 S2	e middle S1 ment S1 ment S1 ment	08 ← ← DON'T ←	07 * CARI * 04	06 06 ← 03	, and the 05 Outp 05 * Outp	04 04 04 04 04 04 04 04	03 03 put pin	02	LSB 01 → 01	BU83111
Patter MSB 0 ↓ ← O	Note n regis 0 peratir 0 peratir	The up ster w 1 ng coc 1 ng coc	pper seg rite cc 0 $de \rightarrow$ $de \rightarrow$ $de \rightarrow$	Q Pat Q Pat Q Pat Note: T	s Segme nd P tern P tern	S2 S2 Seg S2 S2 Seg S2 S2	e middle S1 ment S1 ment S1 ment	- segme 08 ← ← DON'T *	07 * CARI * 04	06 06 ← 03	, and the 05 Outp 05 * Outp	04 04 04 04 04 04 04 04	03 03 put pin	02	LSB 01 → 01	BU83111
Patter MSB 0 ↓ ← O	Note n regis 0 peratir 0 peratir 0 peratir	The up ster w 1 ng coc 1 ng coc	pper seg rite cc 0 $de \rightarrow$ $de \rightarrow$ $de \rightarrow$	Q Pat Q Pat Q Pat Note: T	s Segme nd P tern P tern	S2 S2 Seg S2 S2 Seg S2 S2	e middle S1 ment S1 ment S1 ment	08 ← ← DON'T ←	07 * CARI * 04	06 06 ← 03	, and the 05 Outp 05 * Outp	04 04 04 04 04 04 04 04	03 03 put pin	02	LSB 01 → 01	BU83111
Patter MSB 0 ↓ ← O ↓ ← O	Note n regis 0 peratir 0 peratir 0 peratir	The up ster w 1 ng coc 1 ng coc	pper seg rite cc 0 $de \rightarrow$ $de \rightarrow$ $de \rightarrow$	Q Pat Q Pat Q Pat Note: T	s Segme nd P tern P tern	S2 S2 Seg S2 S2 Seg S2 S2	e middle S1 ment S1 ment S1 ment	08 ← ← DON'T ←	07 * CARI * 04	06 06 ← 03	, and the 05 Outp 05 * Outp	04 04 04 04 04 04 04 04	03 03 put pin	02	LSB 01 → 01 →	BU8311F
Patter MSB 0 ↓ ← O ↓ ← O ↓ ← O All LE MSB	Note n regis peratir 0 peratir peratir Ds val	The up ster w 1 ng coc 1 ng coc 1 ng coc lid cor	pper seg rite cc i 0 de \rightarrow de \rightarrow de \rightarrow de \rightarrow	Q Pat Q Pat Q Pat Note: T d	s Segme nd P tern P tern he uppe	S2 S2 S2 S2 S2 S2 S2 S2 S2 S2 S2	e middle S1 ment S1 ment S1 ment ent is Se	e segme 08 ← × ← DON'T * egment	07 * → CARE * 04 1, and th	06 06 ← 03 ne lower	, and the 05 0utp 05 * Outp segme	04 out pin 04 Outp 04 Outp not s 2.	03 03 0ut pin 02	02	LSB 01 → 01 → × LSB	BU8311F
Patter MSB 0 ↓ ← 0 0 ↓ ← 0 All LE MSB 0 ↓ ←	Note n regis peratir 0 peratir peratir Ds val	The up ster w 1 ng coc 1 ng coc 1 ng coc lid cor 0 Op	pper seg rite co 0 $de \rightarrow$ 0 $de \rightarrow$ nmano $0peratir$	Q Pat Q Pat Q Pat Note: T d	s Segme nd P tern P tern he uppe	S2 S2 S2 S2 S2 S2 S2 S2 S2 S2 S2	e middle S1 ment S1 ment S1 ment ent is Se	e segme 08 ← * ← DON'T * ← egment *	07 * → CARE * 04 1, and th	06 06 ← 03 ne lower	, and the 05 0utp 05 * Outp segme	04 out pin 04 Outr 04 Outr 04 Vutr not is 2.	03 03 0ut pin 02	02	LSB 01 → 01 → × LSB	BU8311F
Patter MSB 0 ↓ ← 0 0 ↓ ← 0 All LE MSB 0 ↓ ←	Note n regis 0 peratir 0 peratir Ds val	The up ster w 1 ng coc 1 ng coc 1 ng coc lid cor 0 Op	pper seg rite co 0 $de \rightarrow$ 0 $de \rightarrow$ nmano $0peratir$	Q Pat Q Pat Q Pat Note: T d	s Segme nd P tern P tern he uppe	S2 S2 S2 S2 S2 S2 S2 S2 S2 S2 S2	e middle S1 ment S1 ment S1 ment ent is Se	e segme 08 ← * ← DON'T * ← egment *	07 * → CARE * 04 1, and th	06 06 ← 03 ne lower	, and the 05 0utp 05 * Outp segme	04 out pin 04 Outr 04 Outr 04 Vutr not is 2.	03 03 0ut pin 02	02	LSB 01 → 01 → × LSB	BU8311F
Patter MSB 0 ↓ ← O ↓ ← O ↓ ← O All LE MSB 0 ↓ ←	Note n regis 0 peratir 0 peratir Ds val	The up ster w 1 ng coc 1 ng coc 1 ng coc lid cor 0 Op	pper seg rite co 0 $de \rightarrow$ 0 $de \rightarrow$ nmano $0peratir$	Q Pat Q Pat Q Pat Note: T d	s Segme nd P tern P tern he uppe	S2 S2 S2 S2 S2 S2 S2 S2 S2 S2 S2	e middle S1 ment S1 ment S1 ment ent is Se	e segme 08 ← * ← DON'T * ← egment *	07 * → CARE * 04 1, and th	06 06 ← 03 ne lower	, and the 05 0utp 05 * Outp segme	04 out pin 04 Outr 04 Outr 04 Vutr not is 2.	03 03 0ut pin 02	02	LSB 01 → 01 → LSB * →	BU83104 BU83114 BU83134

ROHM

BU8310AK / BU8311KS / BU8313K

(6) Register reset command



Entering data settings

(1) Setting operands

S1~S4	These are used to select the segment. "1" selects a segment and "0" de-selects it. More than one segment can be selected at the same time. With pattern register writing, S3 and S4 are not used.
P, Q	These are used to specify the pattern. The lighted state, non-lighted state, and three different flashing patterns can be assigned independently to the 16 bits of segments 1 and 2.
01~08	These are used to select the output pin. "1" selects a pin and "0" de-selects it. More than one output pin can be selected at the same time.

(2) Setting the blink cycle

	р	Blink cy	vcle (sec)
Q	F	ON	OFF
0	0	Lighted	Lighted
1	0	0.5	0.5
0	1	1.0	1.0
1	1	0.125	0.125

Driver internal equivalent circuit (for 1 bit)

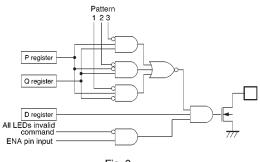
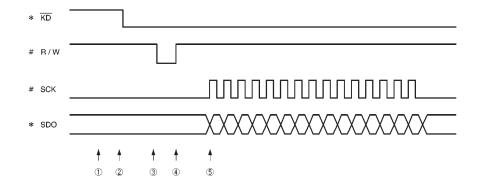


Fig. 3

Recommended method for inputting/outputting data

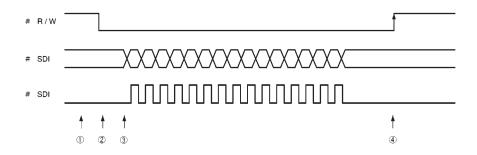
(1) Serial output of key data

State	CPU Operation (#)	BU8310AK Series Operation (*)
1	At standby, R/W = HIGH, SCK = LOW	
2		KD goes LOW when key is pressed.
3	Supplied at falling edge of R/W (key data setting)	
4	R/W set to HIGH (read mode)	
5	SCK rising edges supplied in sequence	Serial data is output in sequential order.



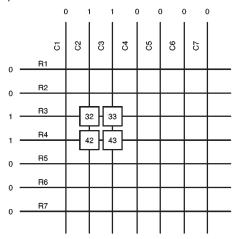
(2) Serial input of LED control commands

State	CPU Operation #
1	At standby, R/W = HIGH, SCK = LOW R/W set to LOW (write mode)
3	SDI input sequentially at rising edge of SCK _o
(4)	After all 16-bit data has been input, R/W rising edge is supplied, and data is taken in internally.



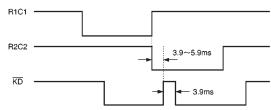
Operation notes

(1) Serial output of key data when several keys are pressed at the same is as shown below.



The key data when 32 and 43 are pressed at the same time will be the same as the key data when 33 and 42 are pressed at the same time.

(2) Pressing different keys



When a different key is pressed from the one already pressed, $\overline{\text{KD}}$ is turned temporarily to provide notification of the change.

(6) Operation states in response to RST, KSCN and ENA pin input

Pin setting			BU	3310AK series state				
RST	KSCN	ENA	Master oscillator	Key scan	LED output	Usage examples		
L	Does not matter		Stopped	Stopped	OFF	Power failure when on hook		
н	L	L	Running	Normal operation	OFF	Power failure when off hook, or normal key scan		
н	L	Н	Running	Normal operation	ON	Power on, or normal key scan		
н	н	L	Running	Runs when key is pressed	OFF	Power failure when off hook, or key pressed to start key scan		
н	Н	н	Running	Runs when key is pressed	ON	Power on, or key pressed to start key scan		

ROHM

BU8310AK / BU8311KS / BU8313K

(3) When the power supply is turned on, the internal registers should be reset using either \overline{RST} pin input or the register reset command.

(4) If the RST pin is set to LOW or the register reset command is executed while data is being output, the SDO output logic is not reset.

(5) If the D, P, and Q registers are rewritten, all eight bits should be written, and not just the pertinent bits.

	D8	D7	D6	D5	D4	D3	D2	D1			
(Ex.)Contents of D register	0	1	0	0	0	0	0	0			
↓ To change D6 to "1"											

Data written to D register 0 1 1 0 0 0 0 0

BU8310AK / BU8311KS / BU8313K

External dimensions (Units: mm)

