Audio ICs

I^{2}C bus line buffer IC
BA8274 / F

BA8274, BA8274F are buffer ICs that can lengthen the bus line retaining all features and operating mode of I^{2}C bus system. Adoption of this buffer in data and clock line enable to improve the drive capacity and to lengthen the bus line with using standard wire at a low price.

●**Applications**

Mini-component stereo, Micro-component stereo and Television.

●**Features**

1) Dual, bi-directional, unity voltage gain buffer.
2) I^{2}C bus compatible.
3) 1:10 impedance transformation.
4) Logic signal levels may include both supply and ground.
5) Power supply voltage range is large.

●**Absolute maximum ratings** (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	Vcc	13.0	V
Power dissipation	Pd	800* / 550*	mW
Operating temperature	Topr	−40 to +85	°C
Storage temperature	Tstg	−55 to +125	°C

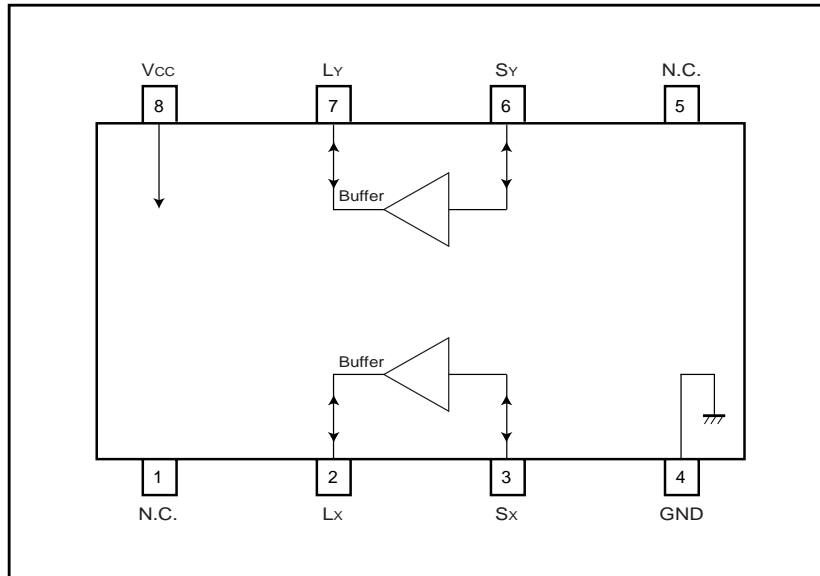∗ For Ta=25°C or more it is reduced at 5.5mW/°C(SOP), 8.0mW/°C (DIP).

●**Recommended operating conditions** (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	Vcc	4.5	–	12	V

∗ I^{2}C bus is a trademark of Philips.

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● **Block diagram**

● **Pin descriptions and input output circuits**

Pin No.	Pin Name	Equivalent circuit	Pin description
2 7	Lx Ly		A pin for outputting a buffer.
3 6	Sx Sy		A pin for inputting a buffer.
4	GND	–	A ground pin.
8	Vcc	–	Power supply pin.

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●**Electrical characteristics** (unless otherwise noted, Ta=25°C, VCC=5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply current 1	I_{Q1}	–	16	30	mA	
Supply current 2	I_{Q2}	–	17	30	mA	VCC=12V
Supply current 3	I_{Q3}	–	30	40	mA	Both I^{2}C inputs LOW, both buffered outputs sinking 30mA.
Drive current 1	ISX, ISY	2.0	2.7	–	mA	ISX, ISY LOW=0.4V VLX, VLY LOW on buffered bus=0.3V.
Drive current 2	ILX, ILY	20	27	–	mA	ILX, ISY LOW=0.4V VSX, VSY LOW on I^{2}C bus=0.3V.
Input current 1	ISX, ISY	–	2.8	3.5	mA	ILX, ILY sink on buffered bus=30mA.
Input current 2	ILX, ILY	–	3.0	3.3	mA	ISX, ISY sink on I^{2}C bus=3mA.
Leakage current	ILX, ILY	–	–	200	μA	VLX, VLY=VCC and VSX, VSY=VCC.
Input/Output impedance	ZIN / ZOUT	8	10	13	–	

●**Measurement circuit**
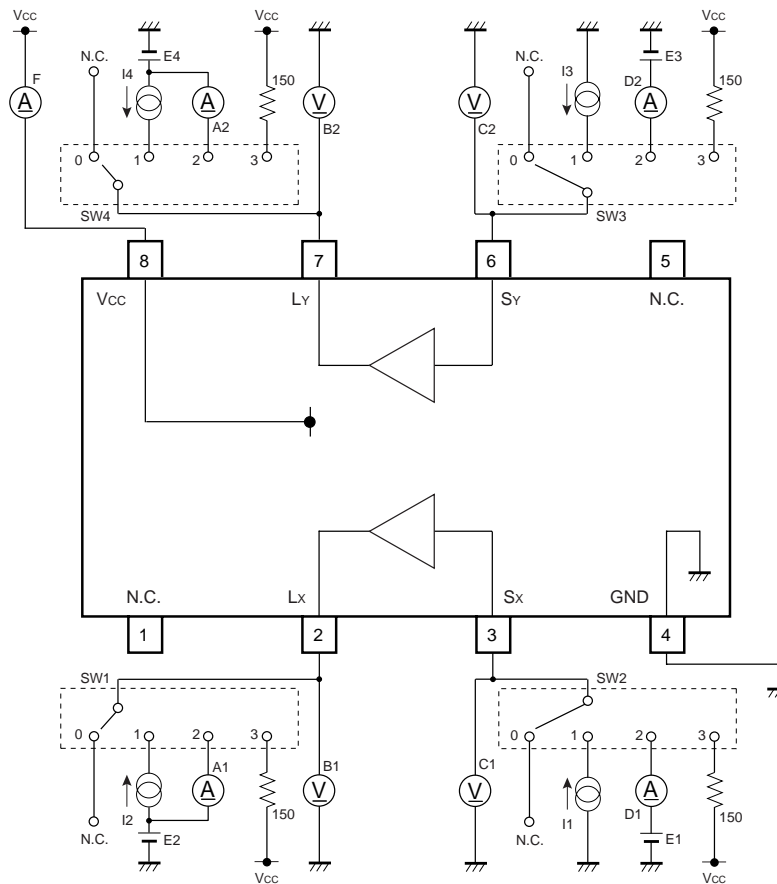

Fig.1

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●**Circuit operation**

BA8274/F contains two identical buffer circuits which enable I^2C and similar bus systems to be extended over long distances without degradation of system performance or requiring the use of special cables.

The buffer has an effective current gain of about 10 from I^2C bus to buffered bus. When current is flowing out of the I^2C bus side, about 10 times that current will be flowing into the buffered bus side (See Fig.2).

As a consequence of this amplification the system is able to drive capacitive load up to about 6 times the standard limit on the buffered bus side. This current based buffering approach preserves the bi-directional, open collector / open-drain characteristic of the I^2C SDA/SCL lines.

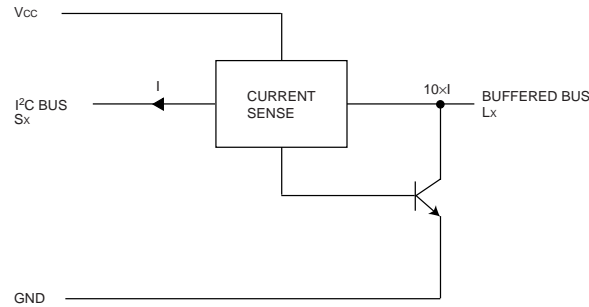To minimize interference and ensure stability, current rise and fall rates are internally controlled.
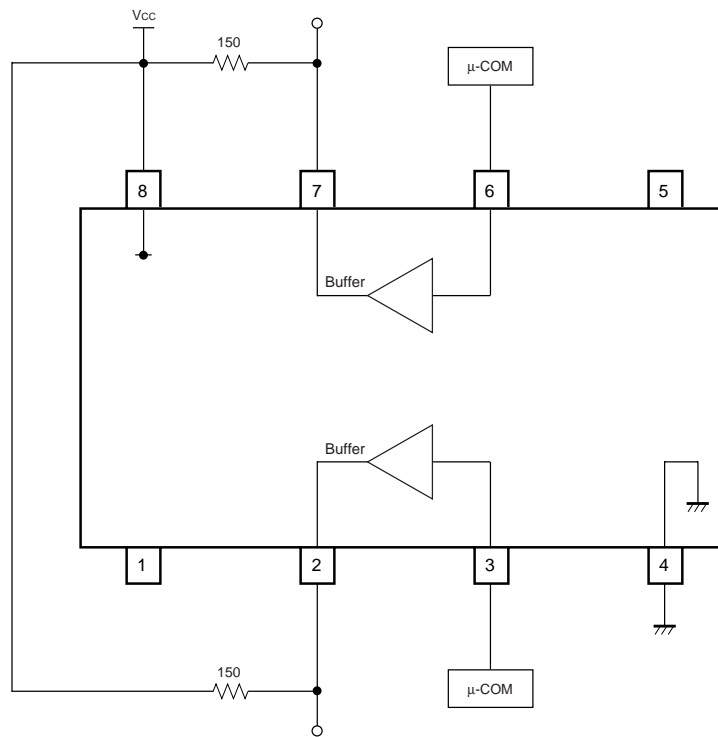
Fig.2

●**Application circuit**

Fig.3

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●**Attached components**

1. Selection of external components

(1) Pull-up resistance calculation

In practical system the pull-up resistance is determined by the rise time limit for I^2C systems. As an approximation this limit will be satisfied if the time constant (product of the net resistance and net capacitance) of the total system is set to 1 microsecond.

The total time constant may either be set by considering each bus node individually (i.e., the I^2C nodes, and the buffered bus node) and choosing pull-up resistors to give time constants of 1 microsecond for each node; or by combining the capacitances into an equivalent capacitive loading on the buffered bus, and calculating the buffered bus pull-up resistor required by this equivalent capacitance.

For each separate bus the pull-up resistor may be calculated as follows:

$$R = \frac{1\mu sec}{C_{device} + C_{wiring}}$$

Where : C_{device} = Sum of device capacitances connected to each bus.

C_{wiring} = Total wiring and stray capacitance on each bus.

If these capacitances are not know then a good approximation is to assume that each device presents 10pF of load capacitance and 10pF of wiring capacitance.

The capacitance figures for one or more individual I^2C bus nodes should be multiplied by a factor of about 10 times, and then added to the buffered bus capacitance. Calculation of a new buffered bus pull-up resistor will allow this single pull-up resistor to act for both the included I^2C bus nodes and the buffered bus. Thus it is possible to combine some or all of these separate pull-up resistors into a signal resistor on the buffered bus (the value of which is calculated from the sum of the scaled capacitances on the buffered bus.) If the buffer is to be permanently connected into the system then all the separate pull-up resistors should be combined. But if it is to be connected by adding it onto an existing system, then only those on the additional I^2C bus system can be combined onto to the buffered bus if the original system is required to be able to still operate on a stand-alone basis.

A further restriction is that the maximum pull-up current, with the bus LOW, should not exceed the I^2C bus specification maximum of 3mA, or 30mA on buffered bus. The following formula applies:

$$30mA > \frac{V_{CC}-0.4}{R_p}$$

Where : R_p = Scaled parallel combination of all pull-up resistors.

If this condition is met, the fall time specifications will also be met.

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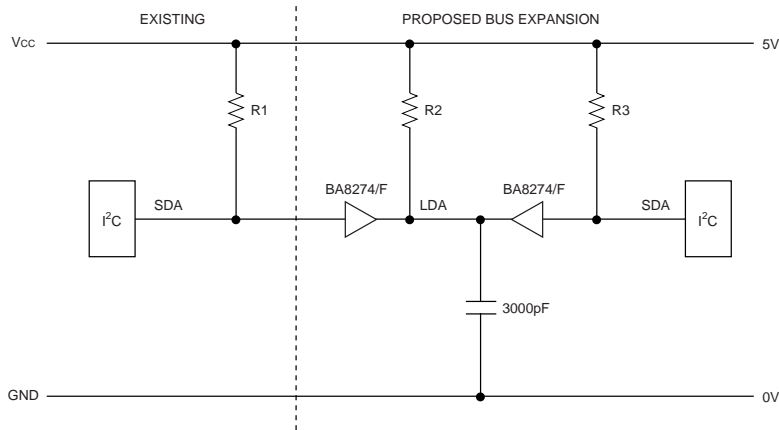2. Loading calculations for the expanded I^2C bus.

EXISTING   PROPOSED BUS EXPANSION

Vcc ——————————————————————————————————— 5V

R1   R2   R3

I^2C   SDA   BA8274/F   LDA   BA8274/F   SDA I^2C

3000pF

GND ——————————————————————————————————— 0V

Fig.4

Effective capacitance
Near I^2C devices

2 × I^2C Devices	20pF
Strays	20pF
BA8274 Buffer	10pF
Total Cap.	50pF

Effective capacitance
Buffered line

Wiring Cap.	3000pF
Total Cap.	3000pF

Effective capacitance
Remote I^2C devices

1 × I^2C Devices	10pF
Strays	10pF
BA8274 Buffer	10pF
Total Cap.	30pF

I^2C pull-up

$$R1 = \frac{1\mu sec}{50pF} = 20k\Omega$$

Buffered bus pull-up

$$R2 = \frac{1\mu sec}{3000pF} = 333k\Omega$$

I^2C pull-up

$$R3 = \frac{1\mu sec}{30pF} = 33k\Omega$$

As an addition to an existing system:

$$R1 = 20k\Omega \qquad R2 = \frac{R2 \times 0.1R3}{R2 + 0.1R3} = 300\Omega$$

R3 not required since buffer always connected.

For a permanent system:

$$R2 = \frac{1}{\frac{1}{0.1R1} + \frac{1}{0.1R2} + \frac{1}{0.1R3}} = 262\Omega$$

R1 and R3 not required since buffer always connected.

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Note): R1, R2 and R3 are calculated from the capacitive loading and a 1μsec time constant on each bus node. For an addition to an existing system, R2 (the new value for R2) is shown as being calculated from the parallel combination of R2 and the scaled value of R3; while for a permanent system R2, and scaled values of R1 and R3 have been used. Note that this example has used scaled resistor values and combined the node and cable capacitances.

Check for maximum pull-up current:

$$\frac{(5-0.4)V}{260\Omega} = 17.6mA < 30mA$$

● **Operation notes**

1. About operation voltage supply range
   Within operation voltage supply range, basic circuit function operation is guaranteed within operation ambient temp.
   But please confirm set up of constant and element, voltage set up and temp set up on use.

2. About operation temp range
   If it within recommended operation voltage range, circuit function operation is guaranteed within operation temp.
   It corralled to conditions of power dissipation to temp.
   Please watch out except condition stipulated by electrical characteristics within the range, it cannot guarantee standard value of electrical characteristics. But it retains original function.

3. S_X, S_Y, I^{2}C BUS, SDA or SCL
   Because the two buffer circuits in the BA8274/F are identical either input pin can be used as the I^{2}C BUS SDA data line,
   or the SCL clock line.

4. L_X, L_Y, Buffered bus, LDA or LCL
   On the buffered low impedance line side, the corresponding output becomes LDA and LCL.
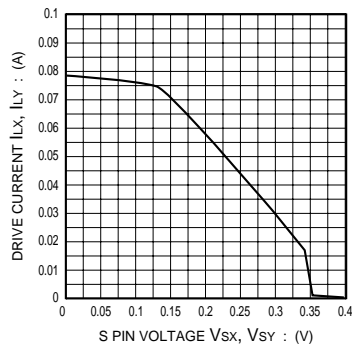
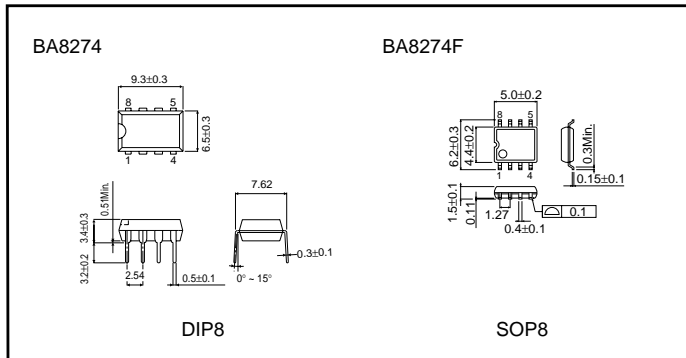● **Electrical characteristic curves**

Fig.5 S pin voltage-drive current I_{LX}, I_{LY}

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●**External dimensions** (Unit: mm)

BA8274

9.3±0.3

8   5

6.5±0.3

1   4

0.5Min.

3.4±0.3

3.2±0.2

2.54

0.5±0.1

7.62

0.3±0.1

0° ~ 15°

DIP8

BA8274F

5.0±0.2

8

1   4

6.2±0.3

4.4±0.2

0.3Min.

0.15±0.1

1.5±0.1

0.1

1.27

0.4±0.1

0.1

SOP8

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Appendix1-Rev1.0