

Structure : Silicon Monolithic Integrated Circuit
 Product Name : Power Driver For CD-ROM
 Device Name : **BA5912BFP**

- Features :
- Driver exclusively for the 2-ch BTL
 - Use of an HSOP25PIN power package can achieve downsizing of the set.
 - A wide dynamic range
 - Using an external mute terminal, the output current can be muted. (CH1, CH2 independently muted.)
 - Muting both 2CHs will lead to the standby mode.
 - Three power supply systems provided.(PreVcc, CH1 PowVcc, CH2 PowVcc)
 - Two built-in general OP-AMPS installed.
 - A built-in thermal shutdown circuit installed.

○ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power Supply Voltage	Vcc	13.5	V
Power Dissipation	Pd	1.45*1	W
Operating Temperature Range	Topr	-35 to 85	°C
Storage Temperature Range	Tstg	-55 to 150	°C

*1 When mounted on the glass/epoxy board with the size: 70 mm×70 mm, the thickness: 1.6 mm, and the rate of copper foil occupancy area: 3% or less.
 Over Ta=25°C, derating at the rate of 11.6mW/°C.

○ RECOMMENDED OPERATING CONDITIONS (To determine a power supply voltage, the power dissipation must be taken into consideration.)

Parameter	Symbol	Limits	Unit
Pre-stage Power Supply Voltage	PreVcc	4.5 to 13.2	V
Power-stage Power Supply Voltage	PowVcc	4.5 to PreVcc	V

This product has not been checked for the strategic materials (or service) defined in the Foreign Exchange and Foreign Trade Control Law of Japan so that a verification work is required before exporting it.

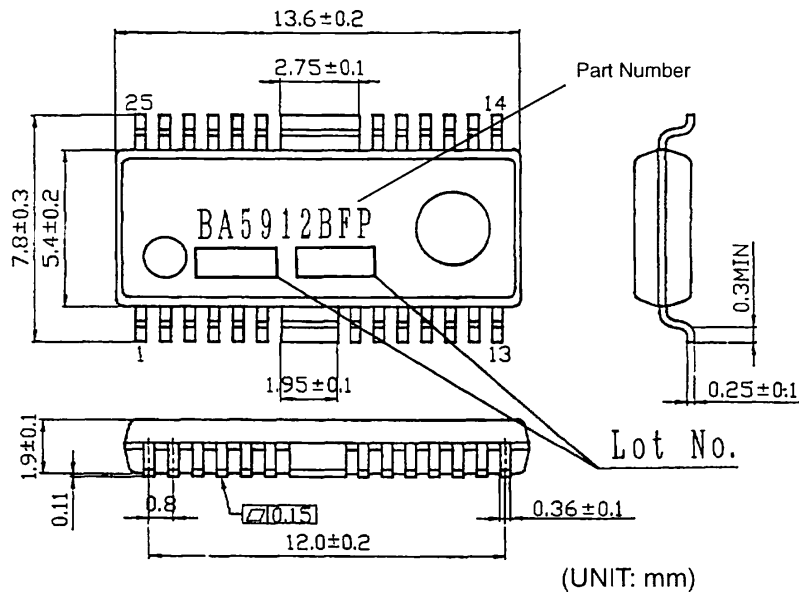
Not designed for radiation resistance.

○ ELECTRIC CHARACTERISTICS (Ta=25°C, Pre, Pow Vcc=5V, BIAS=2.5V, RL=8Ω, unless otherwise noted.)

◎ The items except Maximum Output Amplitude and Standby Circuit Current have the constant limit values regardless of the voltage value of VREF.

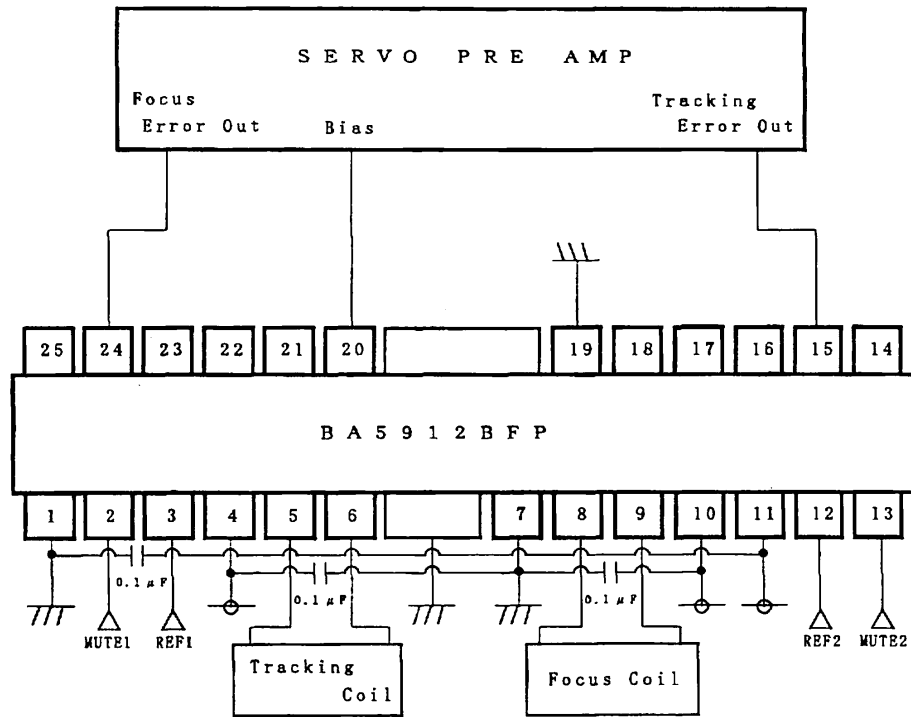
Parameter	Symbol	MIN.	TYP	MAX.	Unit	Condition
Consumption Current (at no signal)	Icc	-	9.0	14.0	MA	when no load applied, REF1,2 ≥ 2.0V
Standby Circuit Current	Isc	-	0	100	μA	When no load applied, REF1,2 ≤ 0.5V
<Driver Part>						
Output Offset Voltage	Voo	-50	0	50	MV	
Maximum Output Amplitude 1	VOM1	3.2	3.5	-	V	REF1,2 ≤ 0.5V
Maximum Output Amplitude 2	VOM2	3.7	4.0	-	V	Pre Vcc=12V, Pow Vcc=5V REF1,2 > 2.0V
Closed Circuit Voltage Gain	Gvc	10.0	11.5	13.0	DB	VIN=BIAS ± 0.5V
Mute ON Voltage	VMON	GND	-	0.5	V	
Mute OFF Voltage	VMOFF	2.0	-	Vcc	V	
Vref Switching Voltage 1	VREF1	GND	-	0.5	V	Pre Vcc=Pow Vcc
Vref Switching Voltage 2	VREF2	2.0	-	Vcc	V	Pre Vcc > Pow Vcc+VF
<OP-AMP Part>						
Offset Voltage	VOFOP	-5	0	5	MV	
Input Bias Current	IBOP	-	-	300	NA	
High-level Output Voltage	VOHOP	4.00	4.36	-	V	
Low-level Output Voltage	VOLOP	-	0.74	1.1	V	
Output Driving Current Sink	ISINK	10	50	-	MA	Vcc with 50 Ω attached
Output Driving Current Source	ISOURCE	10	40	-	MA	GND with 50 Ω attached
Slew Rate	SROP	-	1	-	V/μs	100KHz square wave, 4Vp-p output

○ OUTLINE DIMENSIONS, SYMBOLS



Rev.B

○ APPLICATION CIRCUIT DIAGRAM



When used at $Pre Vcc > Pow Vcc + VF$ and in the standby mode, REF1 (PIN3) and REF2 (PIN12) must be set to open, or 0.5V or less. When used with REF1 (PIN3) and REF2 (PIN12) shorted; or MUTE1 (PIN2) and MUTE2 (PIN13) shorted, each microcomputer output must be able to supply a current of 300µA or so.

○ PIN NUMBERS, PIN NAMES

No.	Pin Name	Description	No.	Pin Name	Description
1	GND	Substrate GND	14	IN2'	CH2 input terminal for gain control
2	MUTE1	CH1 mute terminal	15	IN2	CH2 input terminal with gain fixed
3	REF1	CH1Vref switching terminal	16	OP1-OUT	Operational amplifier 1 output
4	Pow Vcc1	Pow Vcc(CH1)	17	OP1-IN-	Operational amplifier 1- input
5	OUT 1 -	CH1 negative output terminal	18	OP-IN+	Operational amplifier 1+ input
6	OUT1+	CH1 positive output terminal	19	GND	Substrate GND
7	GND	Substrate GND	20	BIAS	Bias input terminal
8	OUT2+	CH2 positive output terminal	21	OP2-IN+	Operational amplifier 2+ input
9	OUT2-	CH2 negative output terminal	22	OP2-IN-	Operational amplifier 2- input
10	Pow Vcc2	Pow Vcc(CH2)	23	OP2-OUT	Operational amplifier 2 output
11	Pre Vcc	Pre Vcc	24	IN1	CH1 input terminal with gain fixed
12	REF2	CH2Vref switching terminal	25	IN1'	CH1 input terminal for gain control
13	MUTE2	CH2 mute terminal			

* The positive or negative polarity on an output terminal is determine by the input polarity.

○ CAUTIONS ON USE

- (1) When the mute terminal voltage (at pin 2 and pin 13) is set to open or dropped to 0.5V (typ.) or less, the output current (CH1, CH2) can be muted individually. Under conditions of normal use, the pin 2 and pin 13 should be pulled-up to 2.0V or above. Setting both mute terminals (pin 2 and pin 13) to open, or 0.5V or less will automatically enter the standby mode.
- (2) On the Bias terminal (pin 20), the applied voltage of 0.7V (typ.) or less will activate a mute function. Under conditions of normal use, it should be set to 1.0V or above.
- (3) When the power supply voltage drops to 3.5V (typ.) or less, the internal circuit will turn OFF and, when recovering to 4.0V (Typ.) or above, the internal circuit will startup.
- (4) Thermal shutdown (TSD), mute ON, bias terminal voltage drop, or power supply voltage drop will activate the mute function, where only the driver part can be muted. While muting, the voltage at the output terminal will equal to the internal bias voltage.
- (5) When $Pre\ V_{cc}=Pow\ V_{cc}$, the Vref switching terminal must be set to open or 0.5V or less (internal bias voltage= $(Pow\ V_{CC} - VF)/2$); or, when $Pre\ V_{cc}>Pow\ V_{cc}+VF$, the Vref switching terminal must be pulled up to 2.0V or above (internal bias voltage= $Pow\ V_{CC}/2$).
- (6) Even though a radiating fin is connected to the GND inside of the package, it must be connected to the external GND.
- (7) About absolute maximum ratings
Exceeding the absolute maximum ratings, such as the applied voltage or the operating temperature range, may cause permanent device damage. As these cases cannot be limited to the broken short mode or the open mode, if a special mode where the absolute maximum ratings may be exceeded is assumed, it is recommended to take mechanical safety measures such as attaching fuses.
- (8) About power supply lines
As a measure against the back current regenerated by a counter electromotive force of the motor, a capacitor to be used as a regenerated-current path can be installed between the power supply and GND and its capacitance value should be determined after careful check that any problems, for example, a leak capacitance of the electrolytic capacitor at low temperature, are not found in various characteristics.
- (9) About GND potential
The electric potential of the GND terminal must be kept lowest in the circuitry at any operation states.
- (10) About thermal design
With consideration of the power dissipation (Pd) under conditions of actual use, a thermal design provided with an enough margin should be done.
- (11) About operations in a strong electric field
When used in a strong electric field, note that a malfunction may occur.
- (12) ASO
When using this IC, the output Tr. must be set not to exceed the values specified in the absolute maximum ratings and ASO.
- (13) Thermal shutdown circuit
This IC incorporates a thermal shutdown circuit (TSD circuit). When the chip temperature reaches the value shown below, the coil output to the motor will be set to open. The thermal shutdown circuit is designed only to shut off the IC from a thermal runaway and not intended to protect or guarantee the entire IC functions. Therefore, users cannot assume that the TSD circuit once activated can be used continuously in the subsequent operations.

TSD ON Temperature [°C] (typ.)	Hysteresis Temperature [°C] (typ.)
175	25

- (14) About earth wiring patterns
When a small signal GND and a large current GND are provided, it is recommended that the large current GND pattern and the small signal GND pattern should be separated and grounded at a single point of the reference point of the set in order to prevent the voltage of the small signal GND from being affected by a voltage change caused by the resistance of the pattern wiring and the large current. Make sure that the GND wiring patterns of the external components will not change, too.

- (15) This IC is a monolithic IC which has a P⁺ isolations and P substrate to isolate elements each other. This P layer and an N layer in each element form a PN junction to construct various parasitic elements. Due to the IC structure, the parasitic elements are inevitably created by the potential relationship.

Activation of the parasitic elements can cause interference between circuits and may result in a malfunction or, consequently, a fatal damage. Therefore, make sure that the IC must not be used under conditions that may activate the parasitic elements, for example, applying the lower voltage than the ground level (GND, P substrate) to the input terminals.

In addition, do not apply the voltage to input terminals without applying the power supply voltage to the IC. Also while applying the power supply voltage, the voltage of each input terminal must not be over the power supply voltage, or within the guaranteed values in the electric characteristics.

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