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BU2040/BU2040F

Serial I/O Expander

FEATURES

- 12-bit Serial/Parallel Conversion
- Low Quiescent Current Due To CMOS Configuration
- Output Open Drain
- I_{SINK} = 20mA
- Default High-Z On At Power Up
- No External Latching Required

APPLICATIONS

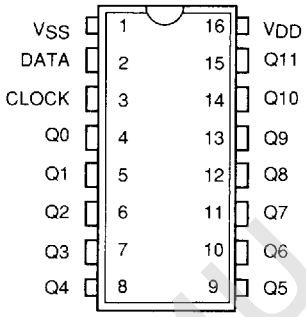
- Microprocessor port expansion
- Serial/Parallel conversion
- Computer peripheral

DESCRIPTION

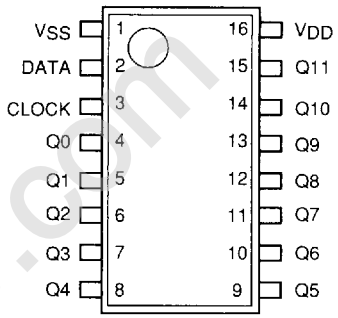
The BU2040 is a 12-bit serial/parallel converter which can be used to expand the input or output capability of a microcontroller or microprocessor. It has the particular benefit that latching is derived from the clock and data inputs and does not require a separate input.

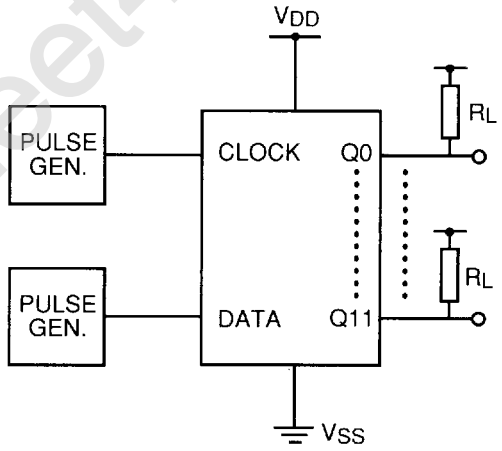
PIN CONFIGURATION

BU2040 (DIP 16-Pin)



BU2040F (MF 16-Pin) Surface Mount

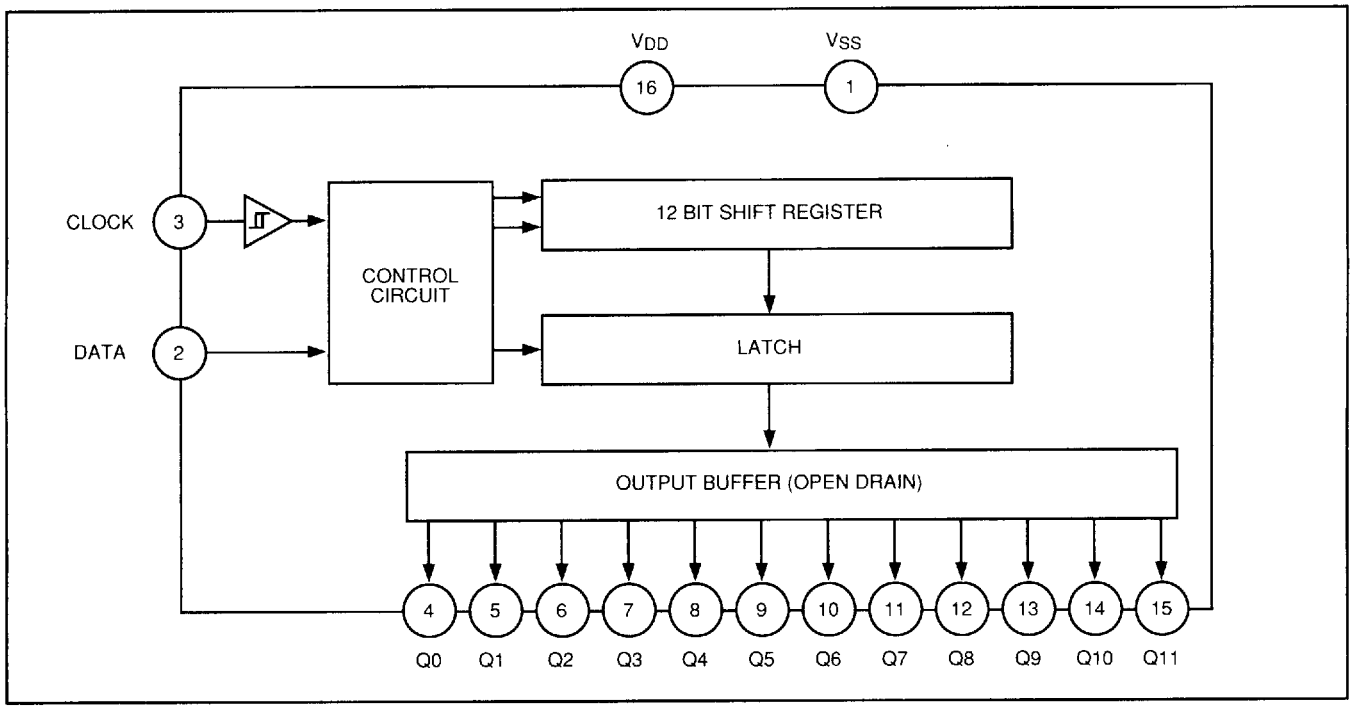




PIN NAMES

V_{SS}	Steady State Voltage
DATA	Serial DATA Input
CLOCK	Clock Input
Q0-Q11	Outputs
V_{DD}	Supply Voltage

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

T_A = 25°C, V_{SS} = 0V

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage	-0.3 to +7.0	V
P_d	Power Dissipation	1100(DIP)/500(MF)	mW
T_{opr}	Operating Temperature Range	-25 to +75	°C
T_{stg}	Storage Temperature Range	-55 to +125	°C
V_{IN}	Input Voltage	V_{SS} -0.3 to V_{DD} +0.3	V
V_O	Output Voltage	V_{SS} to 7.0	V
I_O	DC Output Current	20	mA

Notes:

1. Absolute Maximum Ratings are values below which the device will not sustain damage and does not guarantee operation.
2. Power dissipation is done at 11mW/°C for operation above T_A = 25°C.

RECOMMENDED OPERATING CONDITIONS

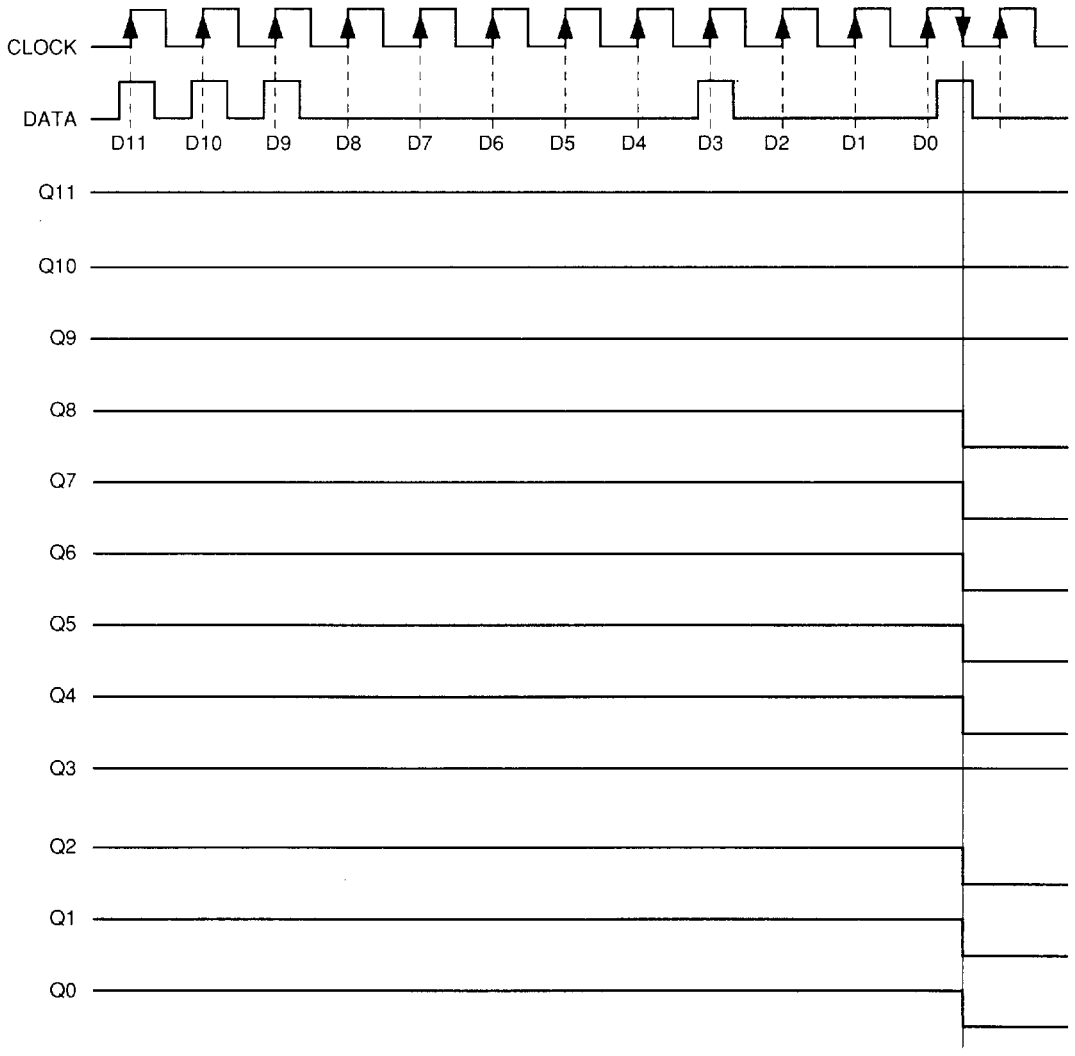
T_A = 25°C, V_{SS} = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input Voltage (High Level)	0.7 x V_{DD}	V_{DD}	V_{DD}	V
V_{IL}	Input Voltage (Low Level)	0	0	0.3 x V_{DD}	V

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, V_{SS} = 0V

Symbol	Parameter	BU2040/BU2040F			Unit	Test Conditions
		Min.	Typ.	Max.		
V_{OL}	Output Voltage (Low Level)	—	—	2	V	I_{OL} = 20mA
I_{OZH}	Output Disable Current (High Level)	—	—	7	µA	V_O = 7.0V
I_{OZL}	Output Disable Current (Low Level)	—	—	-5	µA	V_O = 0V
I_{DD}	Quiescent Supply Current	—	—	5	µA	V_{IN} = V_{SS} or V_{DD}
t_w	Minimum Clock Pulse Width	500	—	—	ns	



NOTE: If the data is 'high' as the clock pulse falls, the contents of the shift register is transferred to the latch circuit.

FIGURE 1. TIMING DIAGRAM

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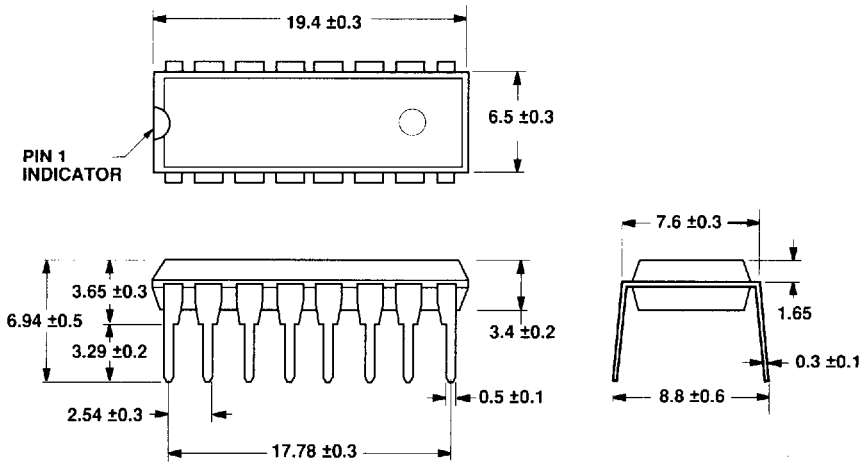
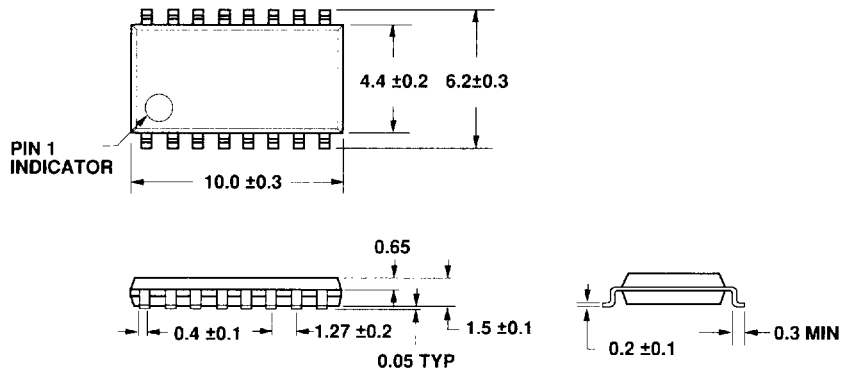
PACKAGE DIAGRAMS

Plastic Dual-in-line Package (PDIP 16-pin)

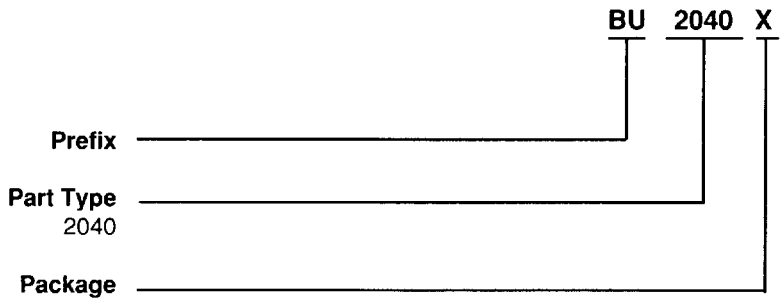


Plastic Surface Mount Package (MF 16-pin)



ORDERING INFORMATION

Part Numbers:



Plastic DIP — No Designation
Small Outline — F

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