

## High-Voltage Transistor Arrays

The CA3146A, CA3146, CA3183A, and CA3183 are general purpose high voltage silicon NPN transistor arrays on a common monolithic substrate.

Types CA3146A and CA3146 consist of five transistors with two of the transistors connected to form a differentially connected pair. These types are recommended for low power applications in the DC through VHF range. (CA3146A and CA3146 are high voltage versions of the popular predecessor type CA3046.)

Types CA3183A and CA3183 consist of five high current transistors with independent connections for each transistor. In addition two of these transistors ( $Q_1$  and  $Q_2$ ) are matched at low current (i.e., 1mA) for applications where offset parameters are of special importance. A special substrate terminal is also included for greater flexibility in circuit design. (CA3183A and CA3183 are high voltage versions of the popular predecessor type CA3083.)

The types with an "A" suffix are premium versions of their non-"A" counterparts and feature tighter control of breakdown voltages making them more suitable for higher voltage applications.

For detailed application information, see companion Application Note AN5296 "Application of the CA3018 Integrated Circuit Transistor Array."

## Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3146AE	-40 to 85	14 Ld PDIP	E14.3
CA3146AM (3146A)	-40 to 85	14 Ld SOIC	M14.15
CA3146E	-40 to 85	14 Ld PDIP	E14.3
CA3146M (3146)	-40 to 85	14 Ld SOIC	M14.15
CA3146M96 (3146)	-40 to 85	14 Ld SOIC Tape and Reel	M14.15
CA3183AE	-40 to 85	16 Ld PDIP	E16.3
CA3183AM96 (3183A)	-40 to 85	16 Ld SOIC Tape and Reel	M16.15
CA3183E	-40 to 85	16 Ld PDIP	E16.3
CA3183M (3183)	-40 to 85	16 Ld SOIC	M16.15
CA3183M96 (3183)	-40 to 85	16 Ld SOIC Tape and Reel	M16.15

## Features

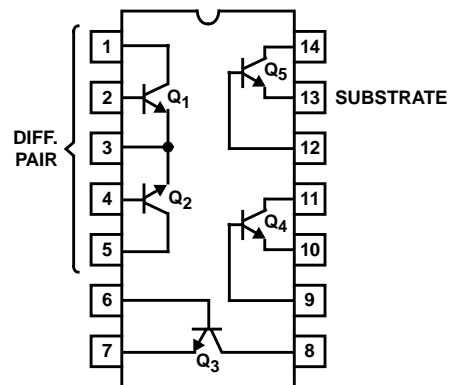
- Matched General Purpose Transistors
  - $V_{BE}$  Match .....  $\pm 5mV$  (Max)
- Operation from DC to 120MHz (CA3146, CA3146A)
- Low Noise Figure ..... 3.2dB (CA3146, CA3146A)
- High  $I_C$  ..... 75mA (Max) (CA3183, CA3183A)

## Applications

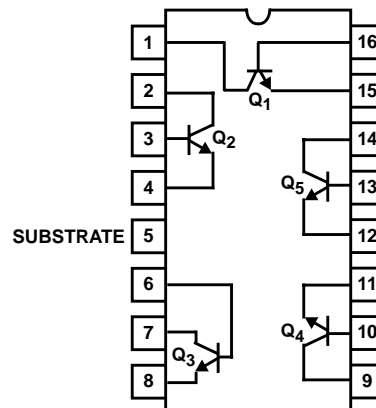
- General Use in Signal Processing Systems in DC through VHF Range
- Custom Designed Differential Amplifiers
- Temperature Compensated Amplifiers
- Lamp and Relay Drivers (CA3183, CA3183A)
- Thyristor Firing (CA3183, CA3183A)

## Pinouts

CA3146, CA3146A (PDIP, SOIC)  
TOP VIEW



CA3183, CA3183A (PDIP, SOIC)  
TOP VIEW



# CA3146, CA3146A, CA3183, CA3183A

## Absolute Maximum Ratings

Collector-to-Emitter Voltage ( $V_{CE0}$ )	
CA3146A, CA3183A	40V
CA3146, CA3183	30V
Collector-to-Base Voltage ( $V_{CBO}$ )	
CA3146A, CA3183A	50V
CA3146, CA3183	40V
Collector-to-Substrate Voltage ( $V_{CIO}$ , Note 1)	
CA3146A, CA3183A	50V
CA3146, CA3183	40V
Emitter to Base Voltage ( $V_{EBO}$ ) all types	5V
Collector Current	
CA3146A, CA3146	50mA
CA3183A, CA3183	75mA
Base Current ( $I_B$ ) - CA3183A, CA3183	20mA

## Thermal Information

Thermal Resistance (Typical, Note 2)	$\theta_{JA}$ ( $^{\circ}C/W$ )
14 Ld PDIP Package	100
14 Ld SOIC Package	200
16 Ld PDIP Package	95
16 Ld SOIC Package	175
Maximum Power Dissipation (Any One Transistor, Note 3)	
CA3146A, CA3146	300mW
CA3183A, CA3183	500mW
Maximum Junction Temperature (Die)	175 $^{\circ}C$
Maximum Junction Temperature (Plastic Package)	150 $^{\circ}C$
Maximum Storage Temperature Range (all types)	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}C$ (SOIC - Lead Tips Only)

## Operating Conditions

Temperature Range . . . . . -40 $^{\circ}C$  to 85 $^{\circ}C$

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTES:

- The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors, and to provide for normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.
- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.
- Care must be taken to avoid exceeding the maximum junction temperature. Use the total power dissipation (all transistors) and thermal resistances to calculate the junction temperature.

## Electrical Specifications CA3146 Series

PARAMETER	SYMBOL	TEST CONDITIONS	TYPICAL PERF. CURVE FIG. NO.	CA3146			CA3146A			UNITS
		$T_A = 25^{\circ}C$		MN	TYP	MAX	MIN	TYP	MAX	
<b>DC CHARACTERISTICS FOR EACH TRANSISTOR</b>										
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu A, I_E = 0$	-	40	72	-	50	72	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA, I_B = 0$	-	30	56	-	40	56	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_{CI} = 10\mu A, I_B = 0, I_E = 0$	-	40	72	-	50	72	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu A, I_C = 0$	-	5	7	-	5	7	-	V
Collector-Cutoff Current	$I_{CEO}$	$V_{CE} = 10V, I_B = 0$	1	-	See Curve	5	-	See Curve	5	$\mu A$
Collector-Cutoff Current	$I_{CBO}$	$V_{CB} = 10V, I_E = 0$	2	-	0.002	100	-	0.002	100	nA
DC Forward-Current Transfer Ratio	$h_{FE}$	$V_{CE} = 5V, I_C = 10mA$	3	-	85	-	-	85	-	-
		$V_{CE} = 5V, I_C = 1mA$	3	30	100	-	30	100	-	-
		$V_{CE} = 5V, I_C = 10\mu A$	3	-	90	-	-	90	-	-
Base-to-Emitter Voltage	$V_{BE}$	$V_{CE} = 3V, I_C = 1mA$	4	0.63	0.73	0.83	0.63	0.73	0.83	V
Collector-to-Emitter Saturation Voltage	$V_{CE SAT}$	$I_C = 10mA, I_B = 1mA$	5	-	0.33	-	-	0.33	-	V
<b>DC CHARACTERISTICS FOR TRANSISTORS Q<sub>1</sub> AND Q<sub>2</sub> (As A Differential Amplifier)</b>										
Magnitude of Input Offset Voltage $ V_{BE1} - V_{BE2} $	$ V_{IO} $	$V_{CE} = 5V, I_E = 1mA$	6, 7	-	0.48	5	-	0.48	5	mV
Magnitude of Base-to-Emitter Temperature Coefficient	$\left  \frac{\Delta V_{BE}}{\Delta T} \right $	$V_{CE} = 5V, I_E = 1mA$	-	-	1.9	-	-	1.9	-	mV/ $^{\circ}C$

## CA3146, CA3146A, CA3183, CA3183A

### Electrical Specifications CA3146 Series (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	TYPICAL PERF. CURVE FIG. NO.	CA3146			CA3146A			UNITS
		$T_A = 25^\circ\text{C}$		MIN	TYP	MAX	MIN	TYP	MAX	
Magnitude of $V_{IO}$ ( $V_{BE1} - V_{BE2}$ ) Temperature Coefficient	$\left  \frac{\Delta V_{IO}}{\Delta T} \right $	$V_{CE} = 5V,$ $I_{C1} = I_{C2} = 1mA$	-	-	1.1	-	-	1.1	-	$\mu\text{V}/^\circ\text{C}$
Magnitude of Input Offset Current $ I_{IO1} - I_{IO2} $ (CA3146AE and CA3146E Only)	$I_{IO}$	$V_{CE} = 5V,$ $I_{C1} = I_{C2} = 1mA$	8	-	0.3	2	-	0.3	2	$\mu\text{A}$
<b>DYNAMIC CHARACTERISTICS</b>										
Low Frequency Noise Figure	NF	$f = 1\text{kHz}, V_{CE} = 5V,$ $I_C = 100\mu\text{A},$ Source Resistance = $1\text{k}\Omega$	10	-	3.25	-	-	3.25	-	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:										
Forward-Current Transfer Ratio	$h_{FE}$	$f = 1\text{kHz}, V_{CE} = 5V,$ $I_C = 1mA$	12	-	100	-	-	100	-	-
Short-Circuit Input Impedance	$h_{IE}$	$f = 1\text{kHz}, V_{CE} = 5V,$ $I_C = 1mA$	12	-	3.5	-	-	2.7	-	$\text{k}\Omega$
Open-Circuit Output Impedance	$h_{OE}$	$f = 1\text{kHz}, V_{CE} = 5V,$ $I_C = 1mA$	12	-	15.6	-	-	15.6	-	$\mu\text{S}$
Open-Circuit Reverse Voltage Transfer Ratio	$h_{RE}$	$f = 1\text{kHz}, V_{CE} = 5V,$ $I_C = 1mA$	12	-	$1.8 \times 10^{-4}$	-	-	$1.8 \times 10^{-4}$	-	-
Admittance Characteristics:										
Forward Transfer Admittance	$Y_{FE}$	$f = 1\text{MHz}, V_{CE} = 5V,$ $I_C = 1mA$	13	-	31-j1.5	-	-	31-j1.5	-	mS
Input Admittance	$Y_{IE}$	$f = 1\text{MHz}, V_{CE} = 5V,$ $I_C = 1mA$	14	-	$0.3 + j0.04$	-	-	$0.35 + j0.04$	-	mS
Output Admittance	$Y_{OE}$	$f = 1\text{MHz}, V_{CE} = 5V,$ $I_C = 1mA$	15	-	$0.001 + j0.03$	-	-	$0.001 + j0.03$	-	mS
Reverse Transfer Admittance	$Y_{RE}$	$f = 1\text{MHz}, V_{CE} = 5V,$ $I_C = 1mA$	16	-	See Curve	-	-	See Curve	-	mS
Gain-Bandwidth Product	$f_T$	$V_{CE} = 5V, I_C = 3mA$	17	300	500	-	300	500	-	MHz
Emitter-to-Base Capacitance	$C_{EB}$	$V_{EB} = 5V, I_E = 0$	18	-	0.70	-	-	0.70	-	pF
Collector-to-Base Capacitance	$C_{CB}$	$V_{CB} = 5V, I_C = 0$	18	-	0.37	-	-	0.37	-	pF
Collector-to-Substrate Capacitance	$C_{CI}$	$V_{CI} = 5V, I_C = 0$	18	-	2.2	-	-	2.2	-	pF

### Electrical Specifications CA3183 Series

PARAMETER	SYMBOL	TEST CONDITIONS	TYPICAL PERF. CURVE FIG. NO.	CA3183			CA3183A			UNITS
		$T_A = 25^\circ\text{C}$		MIN	TYP	MAX	MIN	TYP	MAX	
<b>DC CHARACTERISTICS FOR EACH TRANSISTOR</b>										
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 100\mu\text{A}, I_E = 0$	-	40	-	-	50	-	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA, I_B = 0$	-	30	-	-	40	-	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_{CI} = 100\mu\text{A}, I_B = 0,$ $I_E = 0$	-	40	-	-	50	-	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 500\mu\text{A}, I_C = 0$	-	5	-	-	5	-	-	V
Collector-Cutoff Current	$I_{CEO}$	$V_{CE} = 10V, I_B = 0$	19	-	-	10	-	-	10	$\mu\text{A}$

# CA3146, CA3146A, CA3183, CA3183A

## Electrical Specifications CA3183 Series (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	TYPICAL PERF. CURVE FIG. NO.	CA3183			CA3183A			UNITS
		$T_A = 25^\circ\text{C}$		MIN	TYP	MAX	MIN	TYP	MAX	
Collector-Cutoff Current	$I_{CBO}$	$V_{CB} = 10\text{V}, I_E = 0$	20	-	-	1	-	-	1	$\mu\text{A}$
DC Forward-Current Transfer Ratio	$h_{FE}$	$V_{CE} = 3\text{V}, I_C = 10\text{mA}$	21, 22	40	-	-	40	-	-	-
		$V_{CE} = 5\text{V}, I_C = 50\text{mA}$	-	40	-	-	40	-	-	-
Base-to-Emitter Voltage	$V_{BE}$	$V_{CE} = 3\text{V}, I_C = 10\text{mA}$	23	0.65	0.75	0.85	0.65	0.75	0.85	V
Collector-to-Emitter Saturation Voltage	$V_{CE\text{ SAT}}$ (Note 3)	$I_C = 50\text{mA}, I_B = 5\text{mA}$	24	-	1.7	3.0	-	1.7	3.0	V
<b>FOR TRANSISTORS Q<sub>1</sub> AND Q<sub>2</sub> (AS A DIFFERENTIAL AMPLIFIER)</b>										
Absolute Input Offset Voltage	$ V_{IO} $	$V_{CE} = 3\text{V}, I_C = 1\text{mA}$	25	-	0.47	5	-	0.47	5	mV
Absolute Input Offset Current	$ I_{IO} $	$V_{CE} = 3\text{V}, I_C = 1\text{mA}$	26	-	0.78	2.5	-	0.78	2.5	$\mu\text{A}$

## Typical Performance Curves DC Characteristics - CA3146 Series

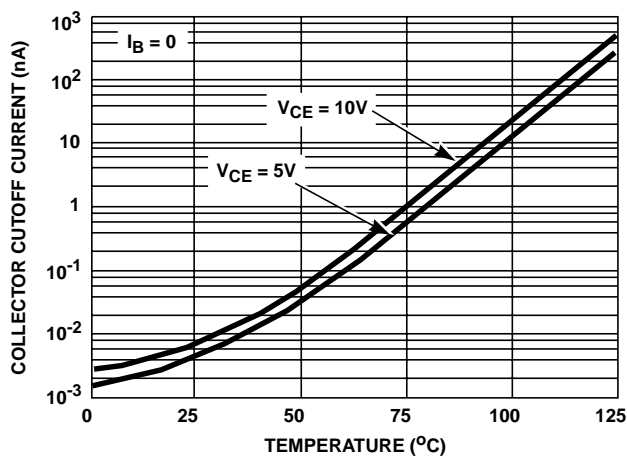


FIGURE 1.  $I_{CEO}$  vs TEMPERATURE FOR ANY TRANSISTOR

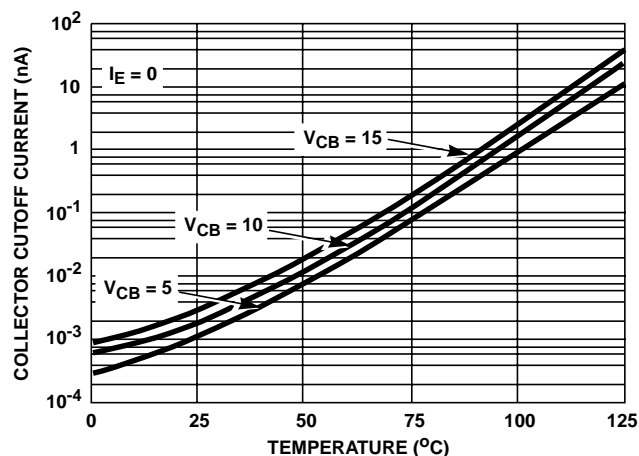


FIGURE 2.  $I_{CBO}$  vs TEMPERATURE FOR ANY TRANSISTOR

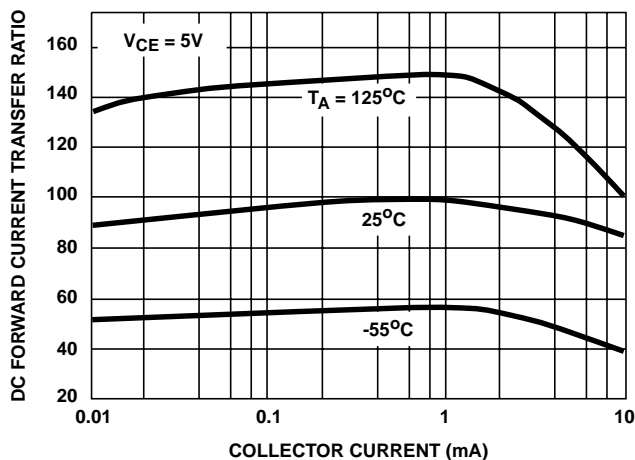


FIGURE 3.  $h_{FE}$  vs  $I_C$  FOR ANY TRANSISTOR

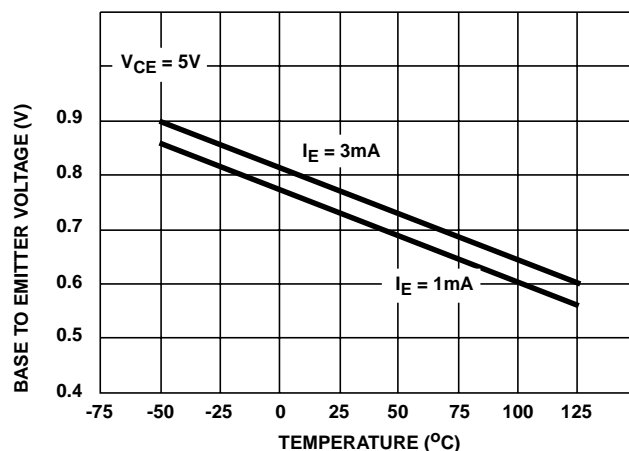


FIGURE 4.  $V_{BE}$  vs TEMPERATURE FOR ANY TRANSISTOR

Typical Performance Curves DC Characteristics - CA3146 Series (Continued)

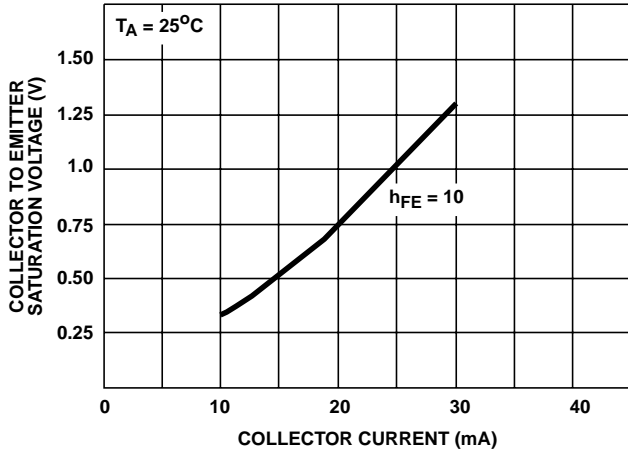


FIGURE 5.  $V_{CE SAT}$  vs  $I_C$  FOR ANY TRANSISTOR

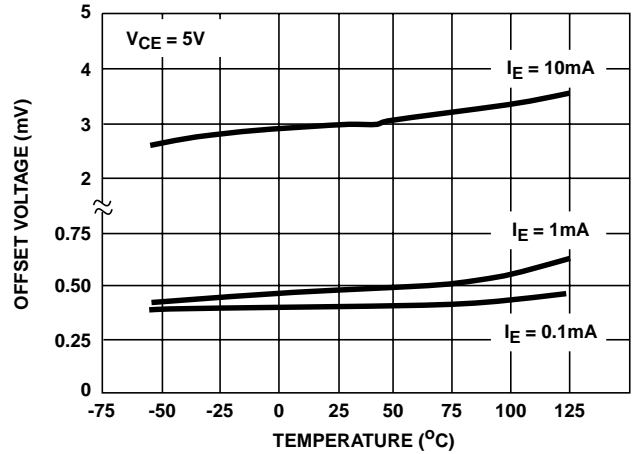


FIGURE 6.  $V_{IO}$  vs TEMPERATURE FOR  $Q_1$  AND  $Q_2$

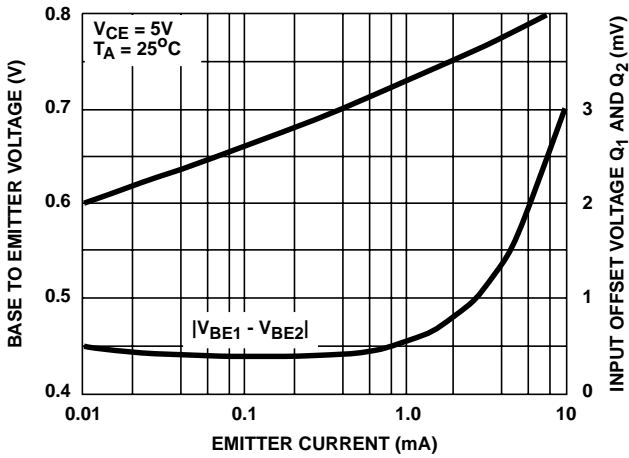


FIGURE 7.  $V_{BE}$  AND  $V_{IO}$  vs  $I_E$  FOR  $Q_1$  AND  $Q_2$

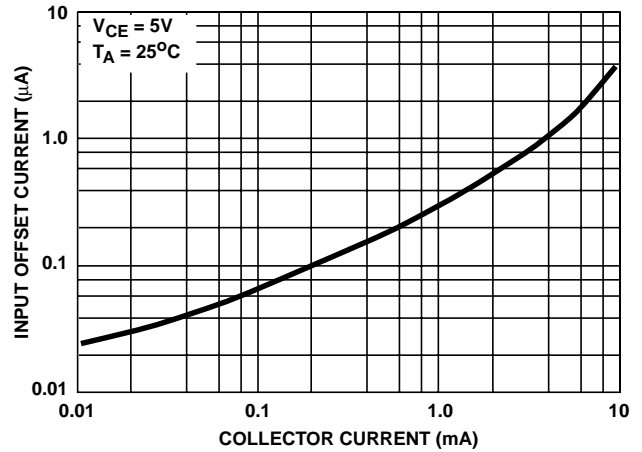


FIGURE 8.  $I_{IO}$  vs  $I_C$  FOR  $Q_1$  AND  $Q_2$

Typical Performance Curves Dynamic Characteristics (For Any Transistor) - CA3146 Series

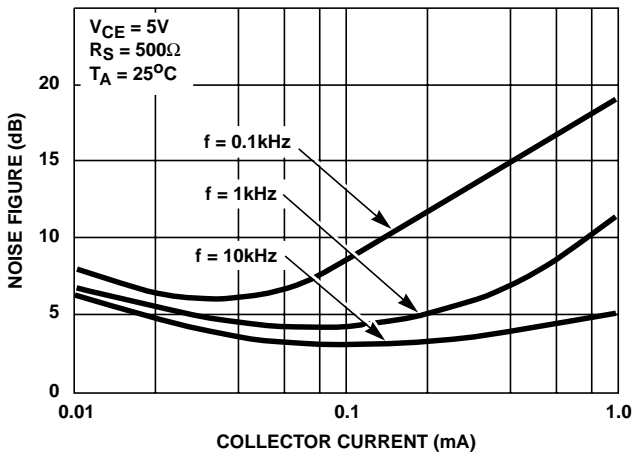


FIGURE 9. NF vs  $I_C$  AT  $R_S = 500\Omega$

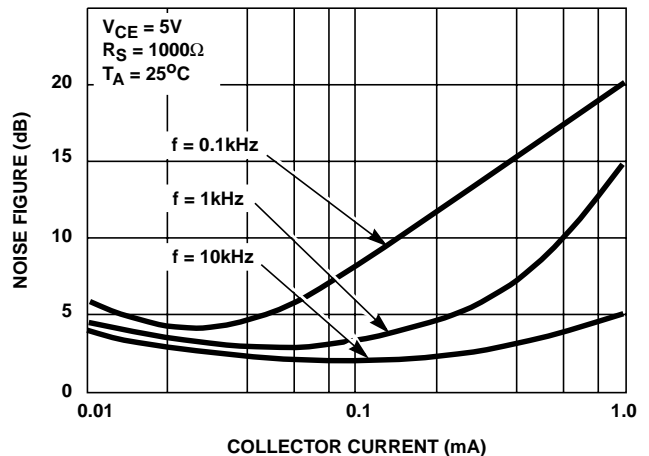


FIGURE 10. NF vs  $I_C$  AT  $R_S = 1k\Omega$

Typical Performance Curves Dynamic Characteristics (For Any Transistor) - CA3146 Series (Continued)

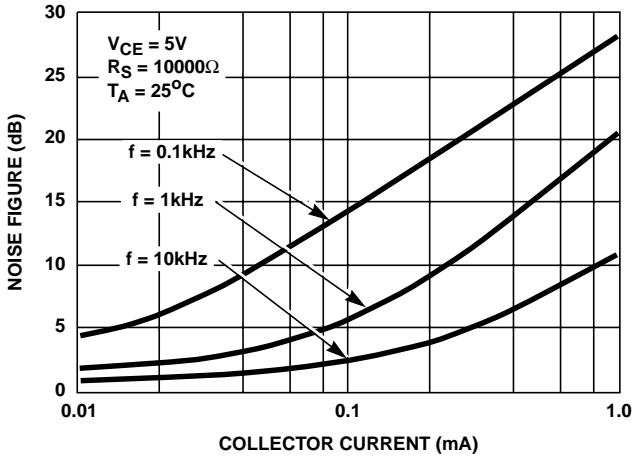


FIGURE 11. NF vs  $I_C$  AT  $R_S = 10k\Omega$

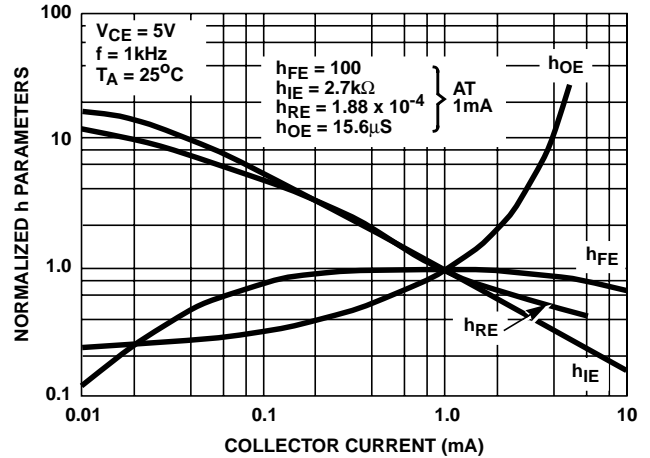


FIGURE 12.  $h_{FE}$ ,  $h_{IE}$ ,  $h_{OE}$ ,  $h_{RE}$  vs  $I_C$

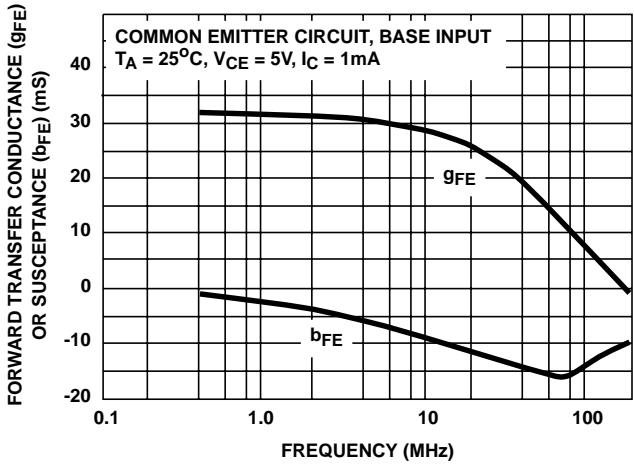


FIGURE 13.  $y_{FE}$  vs FREQUENCY

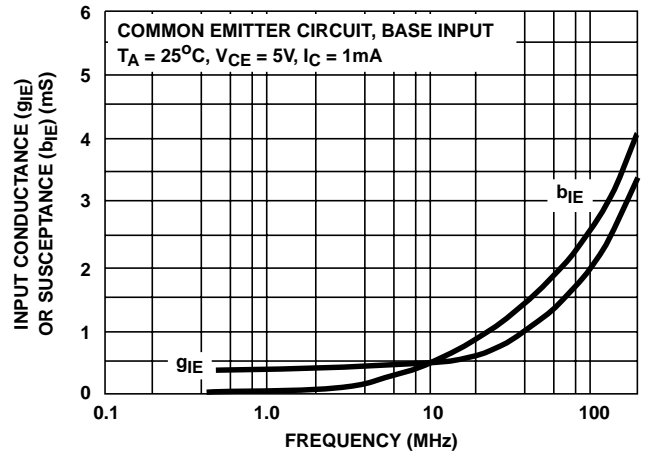


FIGURE 14.  $y_{IE}$  vs FREQUENCY

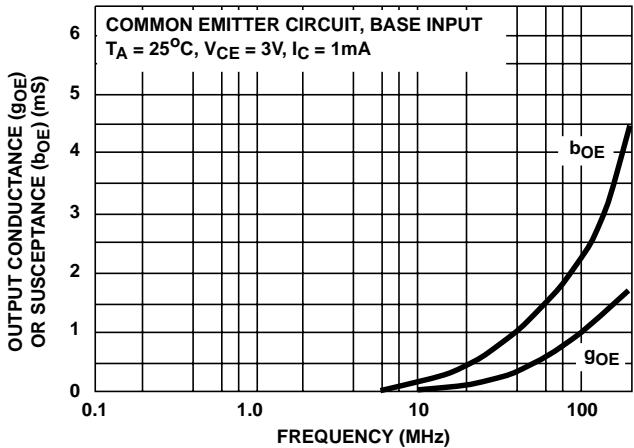


FIGURE 15.  $y_{OE}$  vs FREQUENCY

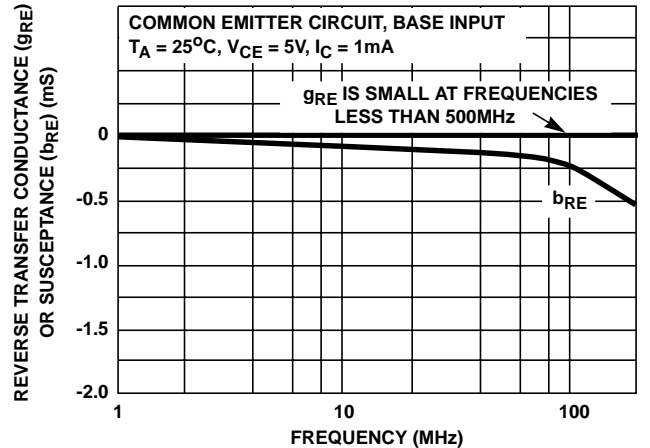


FIGURE 16.  $y_{RE}$  vs FREQUENCY

**Typical Performance Curves** Dynamic Characteristics (For Any Transistor) - CA3146 Series (Continued)

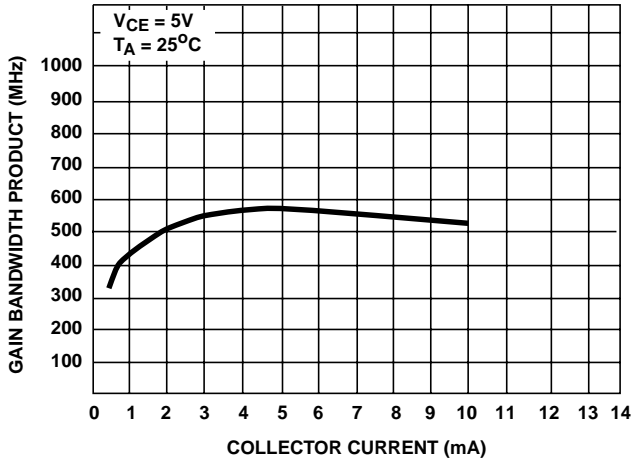


FIGURE 17.  $f_T$  vs  $I_C$

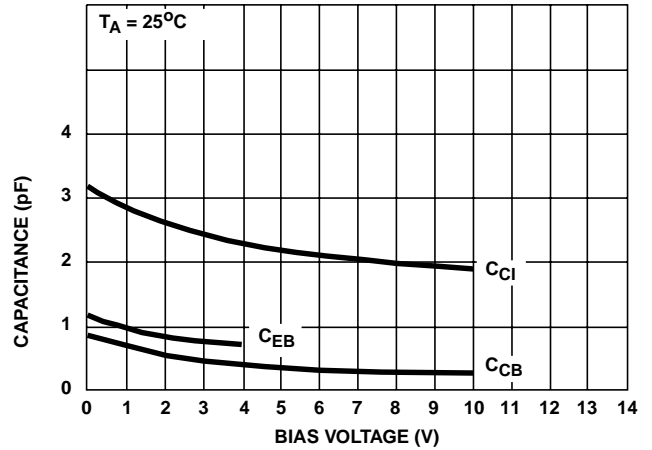


FIGURE 18.  $C_{EB}$ ,  $C_{CB}$ ,  $C_{CI}$  vs BIAS VOLTAGE

**Typical Performance Curves** DC Characteristics - CA3183 Series

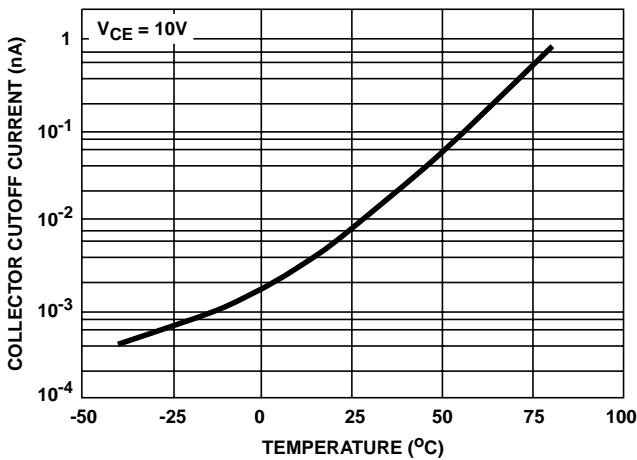


FIGURE 19.  $I_{CEO}$  vs TEMPERATURE FOR ANY TRANSISTOR

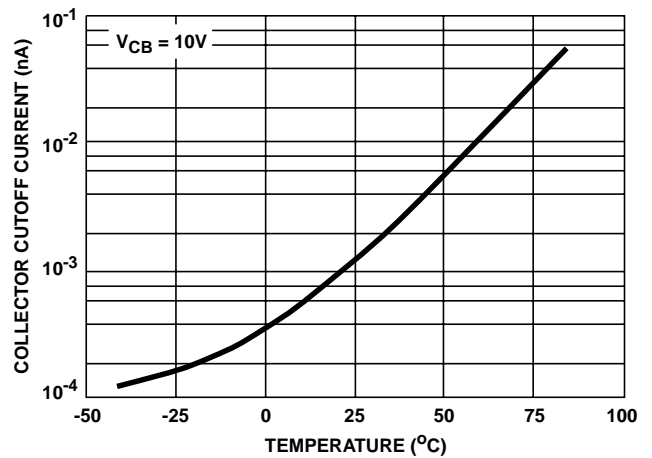


FIGURE 20.  $I_{CBO}$  vs TEMPERATURE FOR ANY TRANSISTOR

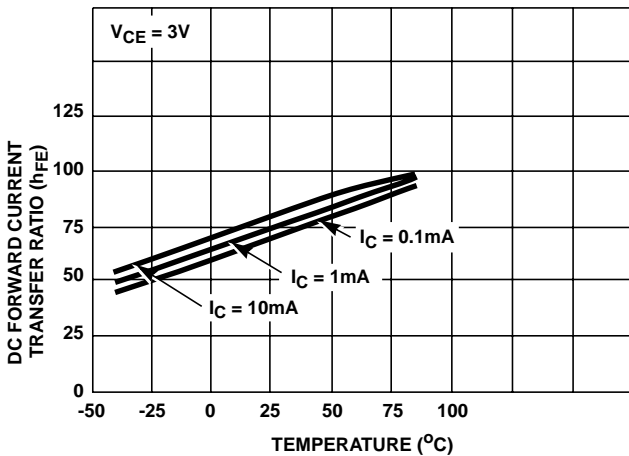


FIGURE 21.  $h_{FE}$  vs TEMPERATURE FOR ANY TRANSISTOR

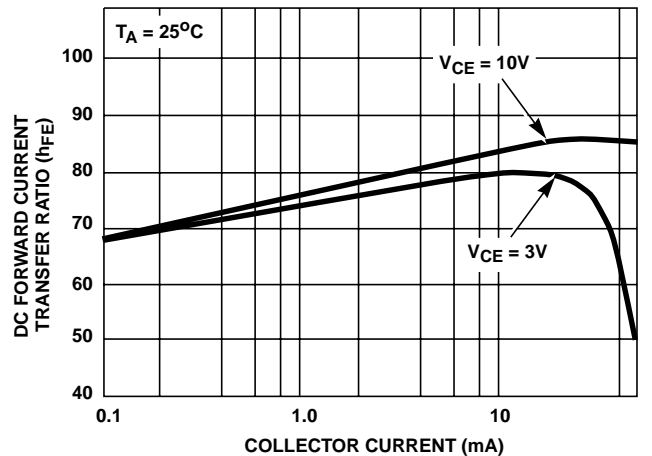


FIGURE 22.  $h_{FE}$  vs  $I_C$  FOR ANY TRANSISTOR

Typical Performance Curves DC Characteristics - CA3183 Series (Continued)

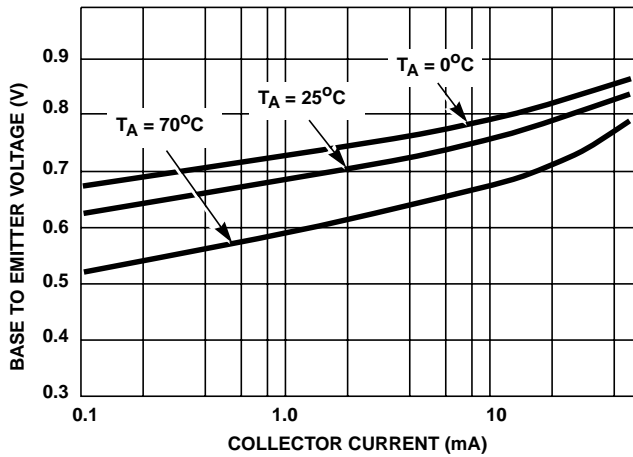


FIGURE 23.  $V_{BE}$  vs  $I_C$  FOR ANY TRANSISTOR

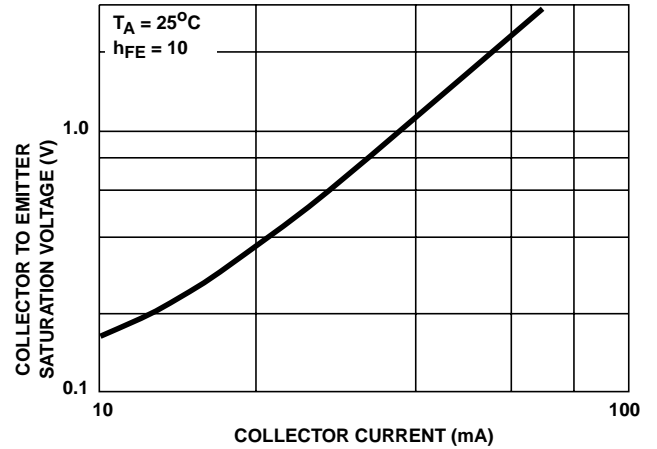


FIGURE 24.  $V_{CE\text{ SAT}}$  vs  $I_C$  FOR ANY TRANSISTOR

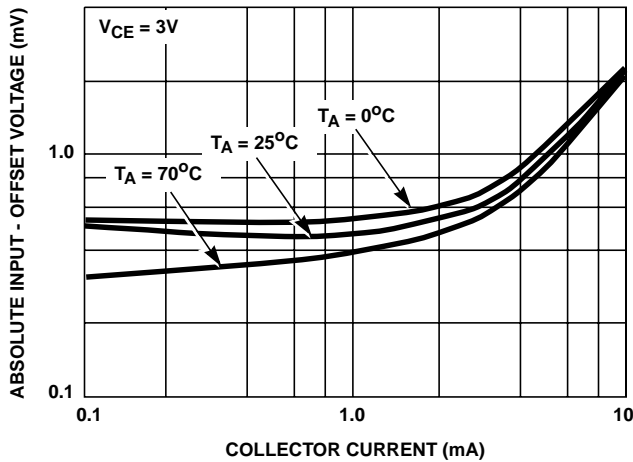


FIGURE 25.  $|V_{IO}|$  vs  $I_C$  FOR DIFFERENTIAL AMPLIFIER (Q<sub>1</sub> AND Q<sub>2</sub>)

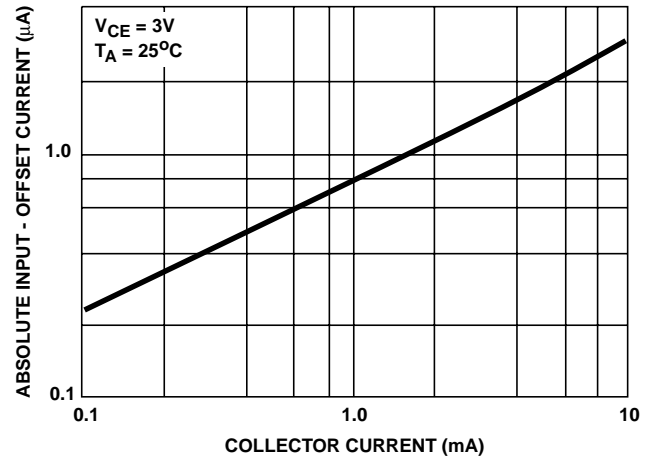
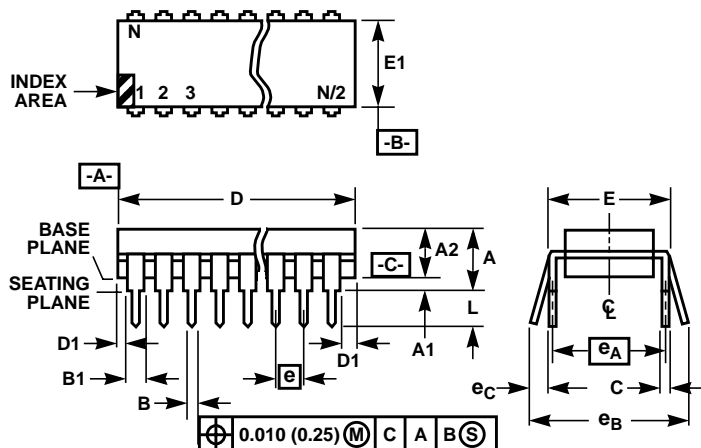


FIGURE 26.  $|I_{IO}|$  vs  $I_C$  FOR DIFFERENTIAL AMPLIFIER (Q<sub>1</sub> AND Q<sub>2</sub>)



Dual-In-Line Plastic Packages (PDIP)



NOTES:

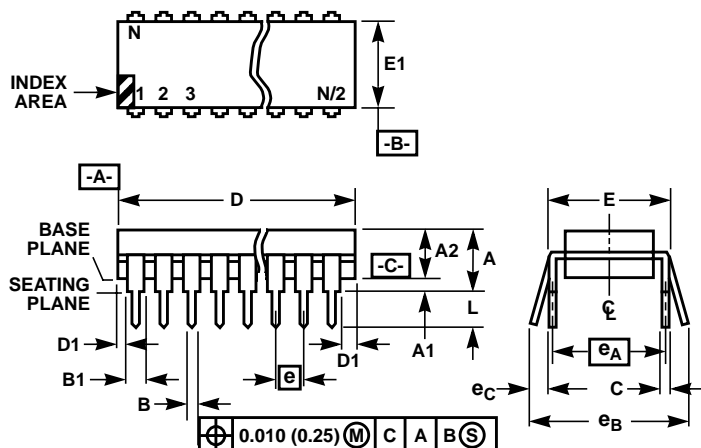
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and  $e_A$  are measured with the leads constrained to be perpendicular to datum [-C-].
7.  $e_B$  and  $e_C$  are measured at the lead tips with the leads unconstrained.  $e_C$  must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E14.3 (JEDEC MS-001-AA ISSUE D)  
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
$e_A$	0.300 BSC		7.62 BSC		6
$e_B$	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	14		14		9

Rev. 0 12/93

Dual-In-Line Plastic Packages (PDIP)



NOTES:

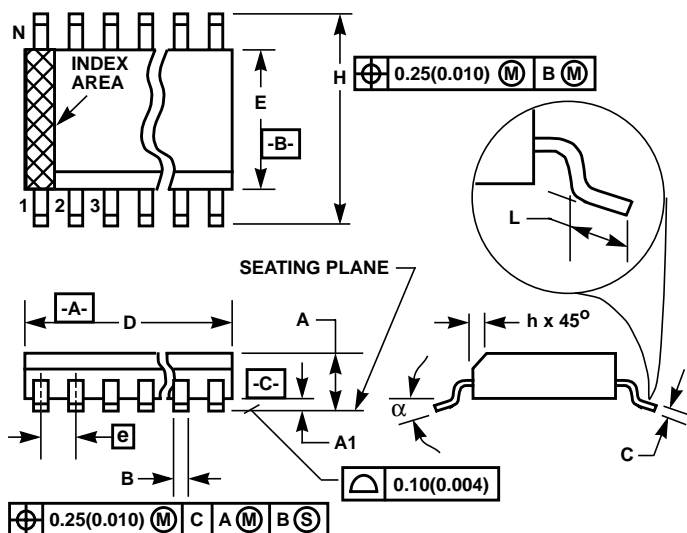
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and  $e_A$  are measured with the leads constrained to be perpendicular to datum  $-C-$ .
7.  $e_B$  and  $e_C$  are measured at the lead tips with the leads unconstrained.  $e_C$  must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)  
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
$e_A$	0.300 BSC		7.62 BSC		6
$e_B$	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

Rev. 0 12/93

Small Outline Plastic Packages (SOIC)



**M14.15 (JEDEC MS-012-AB ISSUE C)**  
**14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

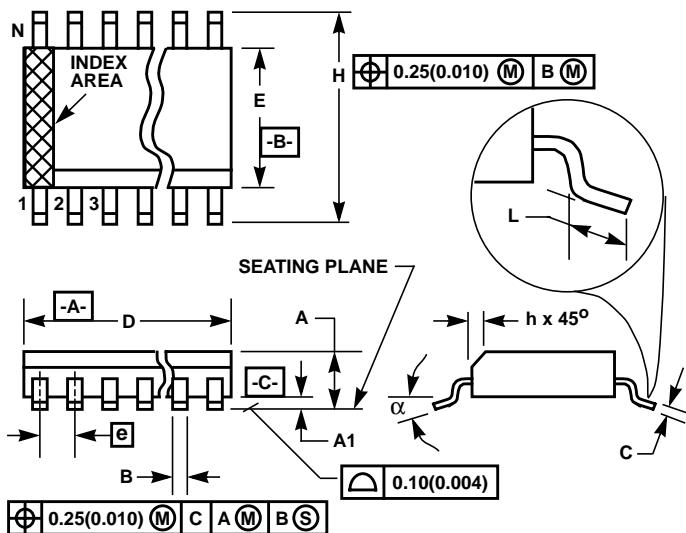
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3367	0.3444	8.55	8.75	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0°	8°	0°	8°	-

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Rev. 0 12/93

Small Outline Plastic Packages (SOIC)



**M16.15 (JEDEC MS-012-AC ISSUE C)**  
**16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Rev. 0 12/93

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

*Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see web site [www.intersil.com](http://www.intersil.com)

**Sales Office Headquarters**

**NORTH AMERICA**  
 Intersil Corporation  
 P. O. Box 883, Mail Stop 53-204  
 Melbourne, FL 32902  
 TEL: (321) 724-7000  
 FAX: (321) 724-7240

**EUROPE**  
 Intersil SA  
 Mercure Center  
 100, Rue de la Fusee  
 1130 Brussels, Belgium  
 TEL: (32) 2.724.2111  
 FAX: (32) 2.724.22.05

**ASIA**  
 Intersil (Taiwan) Ltd.  
 7F-6, No. 101 Fu Hsing North Road  
 Taipei, Taiwan  
 Republic of China  
 TEL: (886) 2 2716 9310  
 FAX: (886) 2 2715 3029