

# DATA SHEET

## **BGY284**

power amplifier with integrated  
control loop for GSM850,  
EGSM900, DCS1800 & PCS1900

Preliminary specification

2003 Aug 20

# power amplifier with integrated control loop for GSM850, EGSM900, DCS1800 & PCS1900

## BGY284

### FEATURES

- Quad band GSM amplifier
- Very small size (8 x 8 mm).
- Suited for GPRS class 12 (duty cycle 4 : 8)
- Integrated power control loop
- 3.5 V nominal supply voltage
- 35 dBm controlled output power for GSM850/EGSM900
- 32.5 dBm controlled output power for DCS1800/PCS1900
- Easy on/off and band select by digital control voltage
- Internal input and output matching
- Specification based on 3GPP TS 45.005.

### APPLICATIONS

- Digital cellular radio systems with Time Division Multiple Access (TDMA) operation (GSM systems) in four frequency bands: 824 to 849 MHz, 880 to 915 MHz, 1710 to 1785 MHz and 1850 to 1910 MHz.

### DESCRIPTION

The BGY284 is a power amplifier module in a SOT775 surface mounted package with a plastic cap.

The module consists of two separated line-ups, one for low band (LB, GSM850/EGSM900) and one for high band (HB, DCS1800/PCS1900) with internal power detection function, power control loop, input and output matching. See the simplified internal circuit on page 4.

The power control circuit ensures a stable power output set by the level of  $V_{DAC}$  and stabilised to compensate variations of supply voltage, input power and temperature, with a control range fully compliant with ETSI time mask and power spectrum requirements

### QUICK REFERENCE DATA

RF performance at  $T_{mb} = 25\text{ °C}$  (mounting base temperature);  $V_{BAT} = 3.5\text{ V}$ ;  $V_{STAB} = 2.8\text{ V}$ ;  $Z_S = Z_L = 50\text{ }\Omega$ ;  $P_D = 0\text{ dBm}$ ;  $\delta = 2:8$

MODE OF OPERATION	f (MHz)	$P_L$ (dBm)	$\eta$ (%)
Typical pulsed, controlled output power	824 to 849	34	50
	880 to 915	34	50
	1710 to 1785	31.3	45
	1850 to 1910	31.3	45

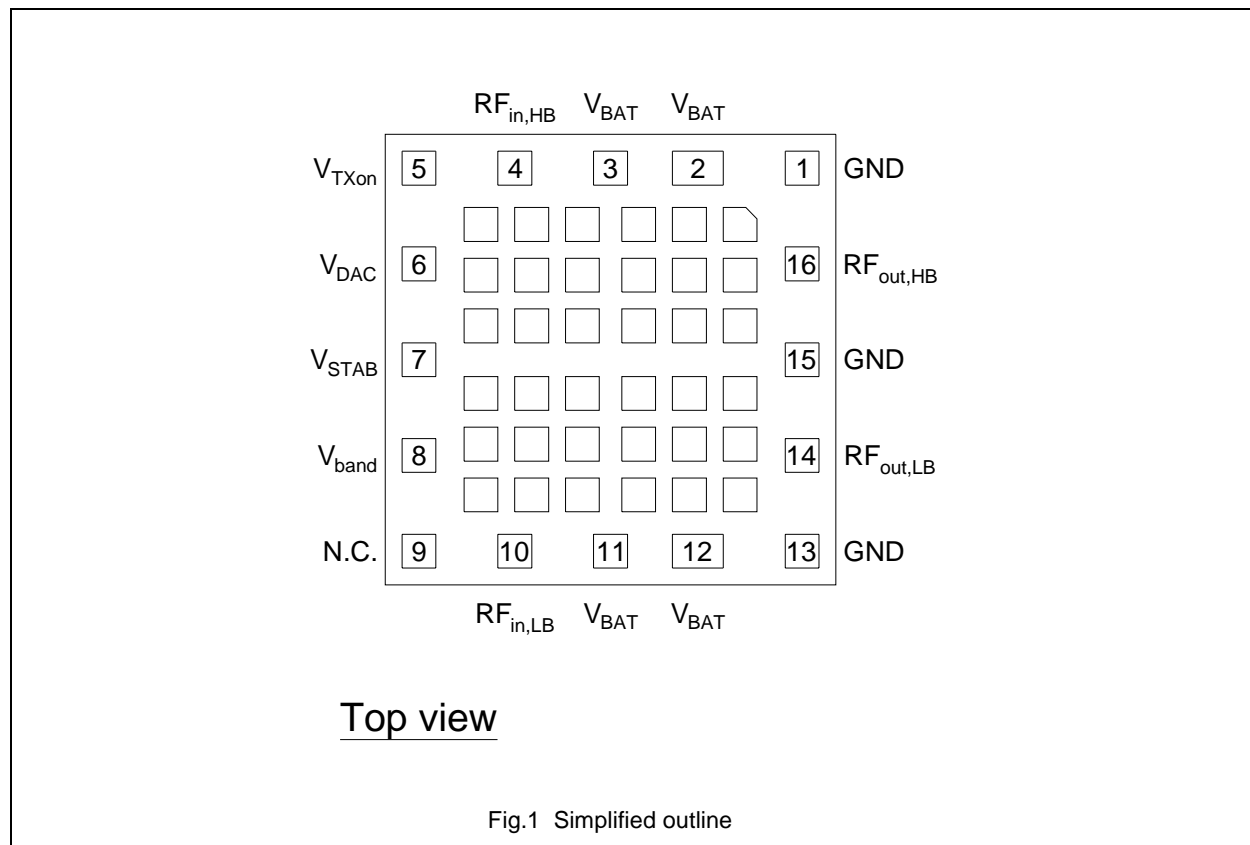
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**PINNING - SOT775**

SYMBOL	PIN NUMBER	PIN TYPE	DESCRIPTION
GND	1, 13, 15	ground	ground
V <sub>BAT</sub>	2, 3	supply	battery connection of DCS1800/PCS1900
V <sub>BAT</sub>	11, 12	supply	battery connection of GSM850/EGSM900 line-up
RF <sub>in,HB</sub>	4	input, analog	DCS1800/PCS1900 transmit RF input
V <sub>TXon</sub>	5	input, logic	power control enable input
V <sub>DAC</sub>	6	input, analog	RF power control input
V <sub>STAB</sub>	7	supply	stabilized supply voltage
V <sub>band</sub>	8	input, logic	LB (GSM850/EGSM900) HB (DCS1800/PCS1900) band select input
	9		not connected
RF <sub>in,LB</sub>	10	input, analog	GSM850/EGSM900 transmit RF input
RF <sub>out,LB</sub>	14	output, analog	GSM850/EGSM900 transmit RF output
RF <sub>out,HB</sub>	16	output, analog	DCS1800/PCS1900 transmit RF output
	inner pads	ground	ground

Note: V<sub>BAT</sub> signals (pin numbers 2, 3, 11, 12) are not internally connected and must all be connected to the battery supply voltage



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INTERNAL CIRCUIT

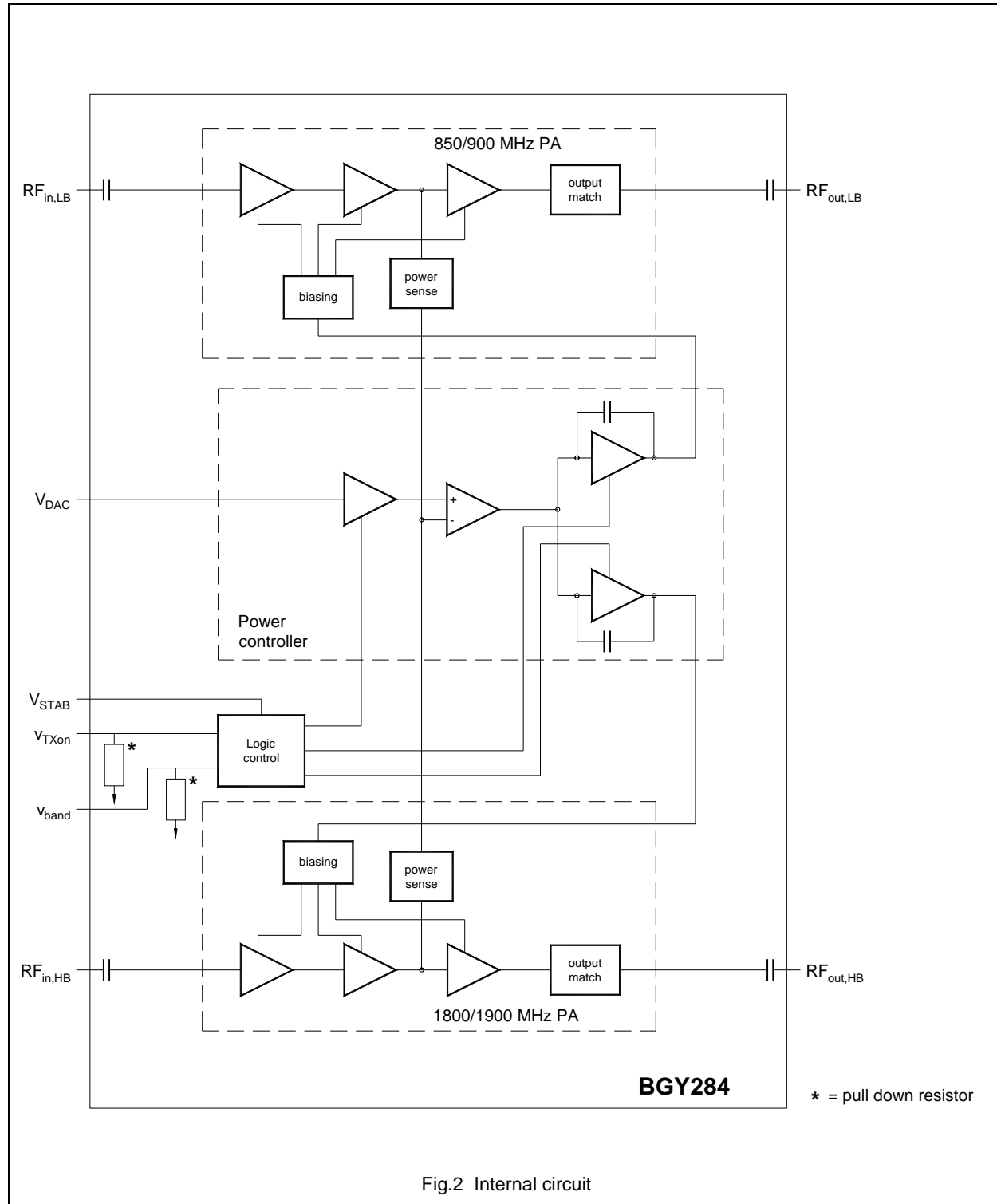


Fig.2 Internal circuit

# power amplifier with integrated control loop for GSM850, EGSM900, DCS1800 & PCS1900

## BGY284

### FUNCTIONAL DESCRIPTION

#### Operating conditions

The BGY284 is designed to meet the 3GPP TS 45.005 technical specification for the European Telecommunication Standards Institute (ETSI).

#### Power amplifier

The low band (GSM850 and EGSM900) and the high band (DCS1800 and PCS1900) power amplifiers both consist of 3 cascaded gain stages. Input and output matching as well as harmonic filters are integrated in the module. The output power is controlled by means of an internal control signal (generated in the power controller block) that is used to adapt the biasing of the 3 stages of an amplifier.

For every line-up the power amplifier block generates a detected output power signal, that is an input to the power control block.

#### Control logic

In the control logic block the various signals are generated to control the complete BGY284 out of  $V_{TXon}$  and  $V_{band}$ , as indicated in the mode control table. The  $V_{STAB}$  is used as supply for the control logic. When  $V_{STAB} = 0$  V the BGY284 is in idle mode and the battery current consumption is almost zero.

The  $V_{TXon}$  signal "HIGH" enables the power control block. When  $V_{band}$  signal is "LOW" the low band (GSM850/EGSM900) line-up is enabled, when the  $V_{band}$  signal is "HIGH" the high band (DCS1800/PCS1900) channel is enabled.

On both  $V_{TXon}$  and  $V_{band}$  inputs there are pull down resistors of approximately 1 M $\Omega$ .

#### Power controller

Main inputs to the power controller block are the  $V_{DAC}$  and the internal generated detected output power signals from the power amplifier block.

The  $V_{DAC}$  signal is the reference voltage for the requested output power level, and usually is generated by an external digital analog converter.

The  $V_{DAC}$  signal is buffered and compared to the detected output power signal. The error signal is then further amplified by the integrator.

Dependent on the  $V_{band}$  signal one of the integrators are selected. The output of the selected integrator is the internal control signal that sets the biasing circuits of the selected channel.

#### Mode control

MODE	Mode description	$V_{STAB}$ (V)	$V_{TXon}$	$V_{band}$	$V_{DAC}$ (V)
Idle	complete PA off, minimal leakage current	0	0	0	<0.15
Standby	control logic functioning, PA off	2.6...3	0	logic 1 or logic 0	<0.15
LB TX	low band transmit mode	2.6...3	1	0	<2.5
HB TX	high band transmit mode	2.6...3	1	1	<2.5

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## TIMING DIAGRAM

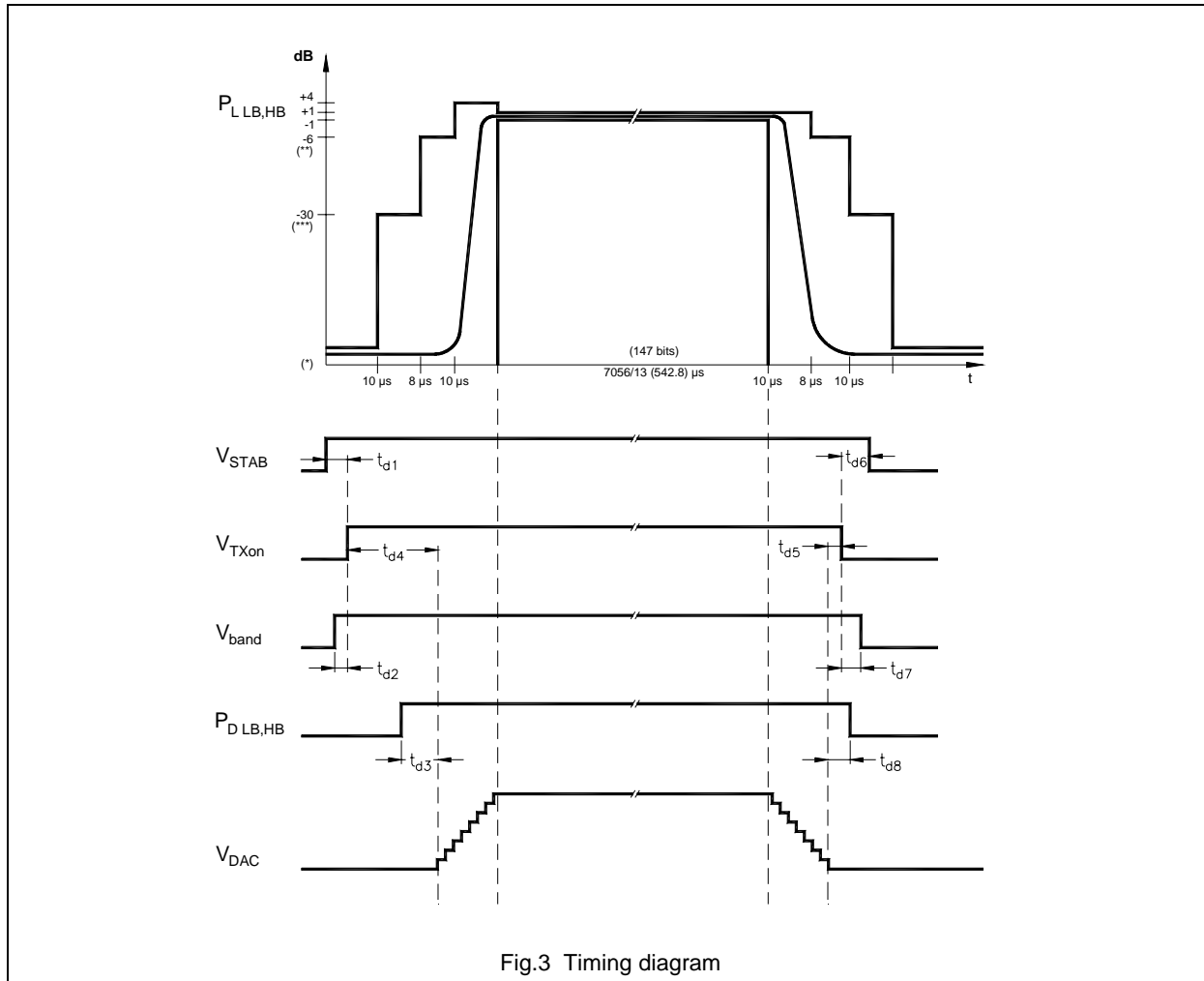


Fig.3 Timing diagram

## TIMING CHARACTERISTICS

$Z_S = Z_L = 50 \Omega$ ;  $-3 \leq P_{D,HB,LB} \leq 3 \text{ dBm}$ ;  $3.1 \leq V_{BAT} \leq 4.6 \text{ V}$ ;  $2.6 \leq V_{STAB} \leq 3.0 \text{ V}$ ;  $-20 \leq T_{mb} \leq 85 \text{ }^\circ\text{C}$ ;  $1 : 8 \leq \delta \leq 4 : 8$ ; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$t_{d1}$	delay time; $V_{STAB}$ high voltage input power before transition $V_{TXon}$ to logic 1	0	—	—	$\mu\text{s}$
$t_{d2}$	delay time; $V_{band}$ to logic 0 or logic 1 before $V_{TXon}$ transition to logic 1	0	—	—	$\mu\text{s}$
$t_{d3}$	delay time; RF signal on $RF_{in,HB,LB}$ before $V_{DAC}$ ramp	0	—	—	$\mu\text{s}$
$t_{d4}$	delay time; voltage step on $V_{DAC}$ after transition $V_{TXon}$ to logic 1	10	—	—	$\mu\text{s}$
$t_{d5}$	delay time; transition of $V_{TXon}$ to logic 0 after $V_{DAC}$ signal to off	0	—	—	$\mu\text{s}$
$t_{d6}$	delay time; $V_{STAB}$ to 0, after $V_{TXon}$ to logic 0	10	—	—	$\mu\text{s}$
$t_{d7}$	delay time; change of $V_{band}$ after $V_{TXon}$ to logic 0	0	—	—	$\mu\text{s}$
$t_{d8}$	delay time; removal of RF signal on $RF_{in,HB,LB}$ after $V_{DAC}$ signal to off	0	—	—	$\mu\text{s}$

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**BGY284****DESCRIPTION RAMP-UP**

Minimum  $t_{d1}$  before  $V_{TX\ on}$  becomes high (control loop becomes active) the  $V_{STAB}$  must be available.

The  $V_{band}$  signal will select the correct transmit channel (LB = GSM850/EGSM900, or HB = DCS1800/PCS1900). The  $V_{band}$  signal must be at the correct value no later than the rising edge of the  $V_{TX\ on}$  signal.

The  $V_{TX\ on}$  signal going high enables the power control loop. To set-up the right internal biasing conditions and charge the integration capacitors to the right starting value there is a set-up time of  $V_{TX\ on}$  before the first increase of  $V_{DAC}$ . Before  $V_{DAC}$  signal is ramping high there has to be RF power on the input of the selected channel ( $P_{D\ LB,HB}$ ).

$V_{DAC}$  has to step up to the voltage level to get the required power level. Sequence of  $V_{DAC}$  steps can be chosen to have approximately a quarter cosine wave ramp-up of  $P_{L\ LB,HB}$  in such a way that there is no violation of the GSM power mask, and that in the same time there is no violation of the spectrum due to transients.

To avoid violation of the lowest power level in the GSM power mask (indicated by \*), the BGY284 has to give sufficient isolation in following condition:  $V_{TX\ on}$  high,  $V_{DAC}$  minimum value, RF power on input of PA.

For GSM850/EGSM900 the system specification for maximum output power level of the handset in this condition is -36 dBm.

For DCS1800/PCS1900 the system specification in this condition is -48 dBm.

In the handset the antenna switch can still be in Rx mode and therefore still provide isolation between the PA and the antenna. This situation is accounted in the isolation conditions in electrical characteristics transmit mode.

**DESCRIPTION RAMP-DOWN**

$V_{DAC}$  will step down from the voltage level for the current power level to offstate. Sequence of  $V_{DAC}$  steps can be chosen to have approximately a quarter cosine wave ramp-down of  $P_{L\ LB,HB}$  in such a way that there is no violation of the GSM power mask, and that in the same time there is no violation of the spectrum due to transients.

The control loop can be switched off ( $V_{TX\ on}$  signal going to logic 0) as soon as the  $V_{DAC}$  has reached the offstate level. At the same time also the  $V_{band}$  signal is allowed to change polarity and the RF input power ( $P_{D\ LB,HB}$ ) at the selected channel can be removed. Because there is no input power anymore there is no additional isolation specification required to meet the GSM system specification.

For GSM850/EGSM900 the system specification for maximum output power level of the handset in this condition is -54 dBm.

For DCS1800/PCS1900 the system specification in this condition is -48 dBm.

$t_{d6}$  after  $V_{TX\ on}$  signal going to logic 0 (control loop is switched off) and all charge in the internal capacitors of the control loop has been removed the BGY284 can go into idle mode ( $V_{STAB}$  can go to 0 V).

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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>BAT</sub>	DC supply voltage	idle mode	–	7	V
		HB TX or LB TX mode	–	5.3	V
V <sub>STAB</sub>	DC supply voltage		–0.5	3.3	V
I <sub>STAB</sub>	supply current		–	2	mA
V <sub>DAC</sub>	DC output power control voltage		–	3	V
I <sub>DAC</sub>	current into output power control input		–2	+2	mA
P <sub>D HB</sub> , P <sub>D LB</sub>	input drive power on RF <sub>in HB, LB</sub>		–	10	dBm
P <sub>L LB</sub>	load power from RF <sub>out LB</sub>		–	37	dBm
P <sub>L HB</sub>	load power from RF <sub>out HB</sub>		–	35	dBm
V <sub>band</sub>	band switch voltage		–0.5	+3.3	V
I <sub>band</sub>	band switch current		–2	+2	mA
V <sub>TXon</sub>	transmit control signal		–0.5	+3.3	V
I <sub>TXon</sub>	current into transmit control input		–2	+2	mA
P <sub>BAT</sub>	power from supply during pulse	HB TX mode	–	4	W
		LB TX mode	–	7	W
I <sub>BAT</sub>	current from supply during pulse	HB TX mode	–	1.4	A
		LB TX mode	–	2.2	A
T <sub>stg</sub>	storage temperature		–40	+100	°C
T <sub>mb</sub>	operating mounting base temperature	δ = 2 : 8	–30	+100	°C
		δ = 4 : 8	–30	+90	°C



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**DC CHARACTERISTICS**

$Z_S = Z_L = 50 \Omega$ ;  $P_{D\text{ HB, LB}} = 0 \text{ mW}$ ;  $V_{\text{BAT}} = 3.5 \text{ V}$ ;  $V_{\text{STAB}} = 2.8 \text{ V}$ ;  $T_{\text{mb}} = 25 \text{ }^\circ\text{C}$ ; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>VOLTAGE SUPPLY</b>						
$V_{\text{BAT}}$	battery supply voltage	Note 1	2.9	–	3.1	V
		typical operating range	3.1	3.6	4.6	V
		Note 2	4.6	–	5.2	V
$I_{\text{BAT}}$	leakage current	standby mode	–	–	25	$\mu\text{A}$
		idle mode	–	–	10	$\mu\text{A}$
$V_{\text{STAB}}$	supply voltage	standby, HB TX or LB TX mode	2.6	2.8	3.0	V
		idle mode	0	–	0.2	V
$I_{\text{STAB}}$	current consumption	HB TX or LB TX mode	–	–	1	mA
		standby mode	–	–	10	$\mu\text{A}$

$Z_S = Z_L = 50 \Omega$ ;  $-3 \leq P_{D\text{ HB, LB}} \leq 3 \text{ dBm}$ ;  $3.1 \leq V_{\text{BAT}} \leq 4.6 \text{ V}$ ;  $2.6 \leq V_{\text{STAB}} \leq 3.0 \text{ V}$ ;  $-20 \leq T_{\text{mb}} \leq 85 \text{ }^\circ\text{C}$ ;  $1 : 8 \leq \delta \leq 4 : 8$ ; unless otherwise specified

<b>DIGITAL INPUTS: <math>V_{\text{TXon}}</math>, <math>V_{\text{band}}</math></b>						
$V_{\text{il}}$	logic low voltage		0	–	0.5	V
$V_{\text{ih}}$	logic high voltage		0.9	–	3	V
$I_{\text{il}}$	current at low voltage		–	–	3	$\mu\text{A}$
$I_{\text{ih}}$	current at high voltage		–	–	15	$\mu\text{A}$
$C_{\text{i}}$	input capacitance		–	4	–	pF
<b>ANALOG INPUTS: <math>V_{\text{DAC}}</math></b>						
$V_{\text{DAC}}$	power control voltage		0	–	2.5	V
$I_{\text{DAC}}$	power control current		–100	–	–	$\mu\text{A}$
$C_{\text{DAC}}$	input capacitance of $V_{\text{DAC}}$		–	4	–	pF
$R_{\text{DAC}}$	input resistance of $V_{\text{DAC}}$		–	1.2	–	M $\Omega$

**Note**

1. PA is functional from 2.9 to 3.1 V, but will not meet all electrical specification points.
2. PA is functional from 4.6 to 5.2 V under 50  $\Omega$  conditions, but will not meet all electrical specification points.

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**ELECTRICAL CHARACTERISTICS GSM850 AND EGSM900 TRANSMIT MODE**

$Z_S = Z_L = 50 \Omega$ ;  $V_{BAT} = 3.6 V$ ;  $V_{STAB} = 2.8 V$ ;  $T_{mb} = 25 \text{ }^\circ\text{C}$ ;  $1 : 8 \leq \delta \leq 4 : 8$ ;  $575 \leq t_p \leq 2300 \mu\text{s}$ ;  $P_{DLB} = 0 \text{ dBm}$ ;  
spurious on  $P_{DLB} < -50 \text{ dBm}$ ; LB TX mode selected;  
 $f = 824 \text{ to } 849 \text{ MHz}$  for GSM850;  $f = 880 \text{ to } 915 \text{ MHz}$  for EGSM900; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$P_{DLB}$	RF input power		-2	0	+2	dBm
$V_{DAC}$	reference voltage to set output power	$f = 897.5 \text{ MHz}$ for EGSM900; $f = 836.5 \text{ MHz}$ for GSM850; $P_{LLB} = 35 \text{ dBm}$	-	-	2	V
		$f = 897.5 \text{ MHz}$ for EGSM900; $f = 836.5 \text{ MHz}$ for GSM850; $P_{LLB} = 5 \text{ dBm}$	0.2	-	-	V
$P_{LLB}$	available output power	$V_{DAC} = 2.2 V$	35.2	36	-	dBm
		$V_{DAC} = 2.2 V$ ; $V_{BAT} = 3.2 V$ ; $P_{DLB} = -2 \text{ dBm}$ ; $T_{mb} = 85 \text{ }^\circ\text{C}$	34.1	-	-	dBm
$\eta$	efficiency GSM850	saturated power	-	55	-	%
		$P_{LLB} = 34 \text{ dBm}$	-	50	-	%
	efficiency EGSM900	saturated power	-	50	-	%
		$P_{LLB} = 34 \text{ dBm}$	-	45	-	%
$\Delta P_{LLB}$	output power variation at nominal temperature	$V_{DAC}$ set to have $31 \leq P_{LLB} \leq 34 \text{ dBm}$ ; see note 1 and 2	-1	-	1	dB
		$V_{DAC}$ set to have $13 \leq P_{LLB} \leq 31 \text{ dBm}$ ; see note 1 and 2	-1.5	-	1.5	dB
		$V_{DAC}$ set to have $7 \leq P_{LLB} \leq 13 \text{ dBm}$ ; see note 1 and 2	-3	-	2	dB
	output power variation at extreme temperature	$V_{DAC}$ set to have $31 \leq P_{LLB} \leq 34 \text{ dBm}$ ; see note 1 and 3	-1.5	-	1.5	dB
		$V_{DAC}$ set to have $13 \leq P_{LLB} \leq 31 \text{ dBm}$ ; see note 1 and 3	-2	-	2	dB
		$V_{DAC}$ set to have $7 \leq P_{LLB} \leq 13 \text{ dBm}$ ; see note 1 and 3	-4	-	3	dB
	output power variation vs frequency	$V_{DAC}$ set to have $31 \leq P_{LLB} \leq 34 \text{ dBm}$ ; see note 1 and 4	-0.3	-	0.3	dB
$H_2$ to $H_{13}$	harmonics	$P_{LLB} \leq 34 \text{ dBm}$	-	-	-5	dBm
	isolation $H_2$ into DCS1800/PCS1900	measured at $RF_{out HB}$ ; $P_{LLB} = 34 \text{ dBm}$	-	-	-15	dBm
	isolation $H_3$ into DCS1800/PCS1900	measured at $RF_{out HB}$ ; $P_{LLB} = 34 \text{ dBm}$	-	-	-25	dBm
	isolation	$P_{DLB} = 2 \text{ dBm}$ ; $V_{DAC} = 0.15 V$ ; standby mode	-	-	-36	dBm
		$P_{DLB} = 2 \text{ dBm}$ ; $V_{DAC} = 0.15 V$ ; LB TX mode	-	-	-36	dBm
$VSWR_{in}$	input VSWR	$P_{LLB} < 5 \text{ dBm}$	-	-	6:1	
$VSWR_{in}$	input VSWR	$5 \leq P_{LLB} \leq 34 \text{ dBm}$ ;	-	2:1	3:1	

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$P_n$	noise power	RBW = 100 kHz; $f_0 = 897.5$ MHz for EGSM900; $f_0 = 836.5$ MHz for GSM850; $f_0 + 10$ MHz; $P_{L\text{ LB}} < 34$ dBm; $f_0 + 20$ MHz; $P_{L\text{ LB}} < 34$ dBm; $f \geq 1805$ MHz; $P_{L\text{ LB}} < 34$ dBm;	–	–	–73	dBm
			–	–	–82	dBm
			–	–	–77	dBm
CG	conversion gain	$f_0 = 915$ MHz for EGSM900; $f_0 = 849$ MHz for GSM850; $5 \leq P_{L\text{ LB}} \leq 34$ dBm; $f_{SS1} = f_0 - 20$ MHz; $P_{SS1} = -40$ dBm; $CG = P_{L\text{ CON}} - P_{SS1}$ ; see fig. 4	–	–	28	dB
SSG	small signal gain	$f_0 = 915$ MHz for EGSM900; $f_0 = 849$ MHz for GSM850; $5 \leq P_{L\text{ LB}} \leq 34$ dBm; $f_{SS2} = f_0 + 20$ MHz; $P_{SS2} = -40$ dBm; $SSG = P_{L\text{ SS2}} - P_{SS2}$ ; see fig. 5	–	–	31	dB
AM/AM	AM/AM conversion	$5 \leq P_{L\text{ LB}} \leq 34$ dBm; 6.5 % AM modulation with $f_{\text{mod}} = 67$ kHz at $RF_{\text{in LB}}$	–	8	12	%
		$5 \leq P_{L\text{ LB}} \leq 34$ dBm; 6.5 % AM modulation with $f_{\text{mod}} = 140$ kHz at $RF_{\text{in LB}}$	–	12	15	%
		$5 \leq P_{L\text{ LB}} \leq 34$ dBm; 6.5 % AM modulation with $f_{\text{mod}} = 271$ kHz at $RF_{\text{in LB}}$	–	18	20	%
AM/PM	AM/PM conversion	$-0.5 \leq P_{D\text{ LB}} \leq 0.5$ dBm; $5 \leq P_{L\text{ LB}} \leq 34$ dBm	–	–	4	deg/dB
	maximum control slope	$5 \leq P_{L\text{ LB}} \leq 34$ dBm	–	–	250	dB/V
$t_r, t_f$	carrier rise and fall time	$P_{L\text{ LB}} 5$ dBm to 34 dBm or vice versa	–	–	2	$\mu\text{s}$
$f_{\text{CL}}$	control loop bandwidth		–	200	–	kHz
	stability	$P_{L\text{ LB}} \leq 34$ dBm; $V_{\text{SWR}} \leq 8 : 1$ through all phases; $3.2 \leq V_{\text{BAT}} \leq 4.6$ V	–	–	–36	dBm
	ruggedness	$3.2 \leq V_{\text{BAT}} \leq 4.6$ V; $P_{L\text{ LB}} \leq 34$ dBm; $\delta = 4 : 8$ ; $V_{\text{SWR}} \leq 8 : 1$ through all phases	no degradation			

**Note**

- Condition to set  $V_{\text{DAC}}$ :  $V_{\text{BAT}} = 3.6$  V;  $\delta = 2 : 8$ ;  $P_{D\text{ LB}} = 0$  dBm;  $T_{\text{mb}} = 25$  °C;  $f = 897.5$  MHz for EGSM900;  
 $f = 836.5$  MHz for GSM850
- Conditions for power variation:  $-2 \leq P_{D\text{ LB}} \leq +2$  dBm;  $f = 824$  to 849 MHz for GSM850;  
 $f = 880$  to 915 MHz for EGSM900;  $15 \leq T_{\text{mb}} \leq 70$  °C;  $3.2 \leq V_{\text{BAT}} \leq 4.2$  V;  $V_{\text{STAB}} = 2.8$  V  $\pm$  10 mV
- Conditions for power variation:  $-2 \leq P_{D\text{ LB}} \leq +2$  dBm;  $f = 824$  to 849 MHz for GSM850;  
 $f = 880$  to 915 MHz for EGSM900;  $-10 \leq T_{\text{mb}} \leq 90$  °C;  $3.2 \leq V_{\text{BAT}} \leq 4.2$  V;  $V_{\text{STAB}} = 2.8$  V  $\pm$  10 mV
- Conditions for power variation:  $P_{D\text{ LB}} = 0$  dBm;  $f = 824$  to 849 MHz for GSM850;  
 $f = 880$  to 915 MHz for EGSM900;  $T_{\text{mb}} = 25$  °C;  $V_{\text{BAT}} = 3.6$  V;  $V_{\text{STAB}} = 2.8$  V  $\pm$  10 mV

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**ELECTRICAL CHARACTERISTICS DCS1800/PCS1900 TRANSMIT MODE**

$Z_S = Z_L = 50 \Omega$ ;  $V_{BAT} = 3.6 \text{ V}$ ;  $V_{STAB} = 2.8 \text{ V}$ ;  $T_{mb} = 25 \text{ }^\circ\text{C}$ ;  $1 : 8 \leq \delta \leq 4 : 8$ ;  $575 \leq t_p \leq 2300 \mu\text{s}$ ;  $P_{DHB} = 0 \text{ dBm}$ ;  
spurious on  $P_{DHB} < -50 \text{ dBm}$ ; HB TX mode selected;  
 $f = 1710 \text{ to } 1785 \text{ MHz}$  for DCS1800;  $f = 1850 \text{ to } 1910 \text{ MHz}$  for PCS1900; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT	
$P_{DHB}$	RF input power		-2	0	+2	dBm	
$V_{DAC}$	reference voltage to set output power	$f = 1747.6 \text{ MHz}$ for DCS1800; $f = 1880 \text{ MHz}$ for PCS1900; $P_{LHB} = 32.5 \text{ dBm}$	-	-	2	V	
		$f = 1747.6 \text{ MHz}$ for DCS1800; $f = 1880 \text{ MHz}$ for PCS1900; $P_{LHB} = 0 \text{ dBm}$	0.2	-	-	V	
$P_{LHB}$	available output power	$V_{DAC} = 2.2 \text{ V}$	32.7	33.5	-	dBm	
		$V_{DAC} = 2.2 \text{ V}$ ; $V_{BAT} = 3.2 \text{ V}$ ; $P_{DHB} = -3 \text{ dBm}$ ; $T_{mb} = 85 \text{ }^\circ\text{C}$	31.8	-	-	dBm	
$\eta$	efficiency DCS1800	saturated power	-	50	-	%	
		$P_{LHB} = 31.3 \text{ dBm}$	-	45	-	%	
	efficiency PCS1900	saturated power	-	50	-	%	
		$P_{LHB} = 31.3 \text{ dBm}$	-	45	-	%	
$\Delta P_{LHB}$	output power variation at nominal temperature	$V_{DAC}$ set to have $30 \leq P_{LHB} \leq 32 \text{ dBm}$ ; see note 1 and 2	-1	-	1	dB	
		$V_{DAC}$ set to have $15 \leq P_{LHB} \leq 30 \text{ dBm}$ ; see note 1 and 2	-1.5	-	1.5	dB	
		$V_{DAC}$ set to have $5 \leq P_{LHB} \leq 15 \text{ dBm}$ ; see note 1 and 2	-2	-	2	dB	
		$V_{DAC}$ set to have $2 \leq P_{LHB} \leq 5 \text{ dBm}$ ; see note 1 and 2	-3	-	3	dB	
	output power variation at extreme temperature	$V_{DAC}$ set to have $30 \leq P_{LHB} \leq 32 \text{ dBm}$ ; see note 1 and 3	-1.5	-	1.5	dB	
		$V_{DAC}$ set to have $15 \leq P_{LHB} \leq 30 \text{ dBm}$ ; see note 1 and 3	-2	-	2	dB	
		$V_{DAC}$ set to have $5 \leq P_{LHB} \leq 15 \text{ dBm}$ ; see note 1 and 3	-2.5	-	2.5	dB	
		$V_{DAC}$ set to have $2 \leq P_{LHB} \leq 5 \text{ dBm}$ ; see note 1 and 3	-3.5	-	3.5	dB	
	output power variation vs frequency	$V_{DAC}$ set to have $30 \leq P_{LHB} \leq 32 \text{ dBm}$ ; see note 1 and 4	-0.3	-	0.3	dB	
	$H_2$ to $H_7$	harmonics	$P_{LHB} \leq 32 \text{ dBm}$	-	-	-4.5	dBm
		isolation	$P_{DHB} = 2 \text{ dBm}$ ; $V_{DAC} = 0.15 \text{ V}$ ; standby mode	-	-	-36	dBm
			$P_{DHB} = 2 \text{ dBm}$ ; $V_{DAC} = 0.15 \text{ V}$ ; HB TX mode	-	-	-36	dBm
$VSWR_{in}$	input VSWR	$P_{LHB} < 2 \text{ dBm}$	-	-	6:1		
$VSWR_{in}$	input VSWR	$2 \leq P_{LHB} \leq 32 \text{ dBm}$	-	2:1	3:1		

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$P_n$	noise power	RBW = 100 kHz $f_0 = 1747.5$ MHz for DCS1800; $f_0 = 1880$ MHz for PCS1900; $f_0 + 20$ MHz; $P_{L\text{ HB}} < 32$ dBm	–	–	–77	dBm
CG	conversion gain	$f_0 = 1785$ MHz for DCS1800; $f_0 = 1910$ MHz for PCS1900; $0 \leq P_{L\text{ HB}} \leq 32$ dBm; $f_{SS1} = f_0 - 20$ MHz; $P_{SS1} = -40$ dBm; $CG = P_{L\text{ CON}} - P_{SS1}$ ; see fig. 4	–	–	25.5	dB
SSG	small signal gain	$f_0 = 1785$ MHz for DCS1800; $f_0 = 1910$ MHz for PCS1900; $0 \leq P_{L\text{ HB}} \leq 32$ dBm; $f_{SS2} = f_0 + 20$ MHz; $P_{SS2} = -40$ dBm; $SSG = P_{L\text{ SS2}} - P_{SS2}$ ; see fig. 5	–	–	31	dB
AM/AM	AM/AM conversion	$0 \leq P_{L\text{ HB}} \leq 32$ dBm; 6.5 % AM modulation with $f_{\text{mod}} = 67$ kHz at $RF_{\text{in HB}}$	–	8	12	%
		$0 \leq P_{L\text{ HB}} \leq 32$ dBm; 6.5 % AM modulation with $f_{\text{mod}} = 140$ kHz at $RF_{\text{in HB}}$	–	12	15	%
		$0 \leq P_{L\text{ HB}} \leq 32$ dBm; 6.5 % AM modulation with $f_{\text{mod}} = 271$ kHz at $RF_{\text{in HB}}$	–	18	20	%
AM/PM	AM/PM conversion	$-0.5 \leq P_{D\text{ HB}} \leq 0.5$ dBm; $0 \leq P_{L\text{ HB}} \leq 32$ dBm	–	–	4	deg/dB
	maximum control slope	$0 \leq P_{L\text{ HB}} \leq 32$ dBm	–	–	250	dB/V
$t_r, t_f$	carrier rise and fall time	$P_{L\text{ HB}}$ from 0 dBm to 32 dBm and vice versa	–	–	2	$\mu\text{s}$
$f_{\text{CL}}$	control loop bandwidth		–	200	–	kHz
	stability	$P_{L\text{ HB}} \leq 32$ dBm; $V_{\text{SWR}} \leq 8 : 1$ through all phases; $3.2 \leq V_{\text{BAT}} \leq 4.6$ V	–	–	–36	dBm
	ruggedness	$3.2 \leq V_{\text{BAT}} \leq 4.6$ V; $P_{L\text{ HB}} \leq 32$ dBm; $\delta = 4 : 8$ ; $V_{\text{SWR}} \leq 8 : 1$ through all phases	no degradation			

**Note**

- Condition to set  $V_{\text{DAC}}$ :  $V_{\text{BAT}} = 3.6$  V;  $\delta = 2 : 8$ ;  $P_{D\text{ HB}} = 0$  dBm;  $T_{\text{mb}} = 25$  °C;  $f = 1747.6$  MHz for DCS1800;  
 $f = 1880$  MHz for PCS1900
- Conditions for power variation:  $-2 \leq P_{D\text{ HB}} \leq +2$  dBm;  $f = 1710$  to 1785 MHz for DCS1800;  
 $f = 1850$  to 1910 MHz for PCS1900;  $15 \leq T_{\text{mb}} \leq 70$  °C;  $3.2 \leq V_{\text{BAT}} \leq 4.2$  V;  $V_{\text{STAB}} = 2.8$  V  $\pm$  10 mV
- Conditions for power variation:  $-2 \leq P_{D\text{ HB}} \leq +2$  dBm;  $f = 1710$  to 1785 MHz for DCS1800;  
 $f = 1850$  to 1910 MHz for PCS1900;  $-10 \leq T_{\text{mb}} \leq 90$  °C;  $3.2 \leq V_{\text{BAT}} \leq 4.2$  V;  $V_{\text{STAB}} = 2.8$  V  $\pm$  10 mV
- Conditions for power variation:  $P_{D\text{ HB}} = 0$  dBm;  $f = 1710$  to 1785 MHz for DCS1800;  
 $f = 1850$  to 1910 MHz for PCS1900;  $T_{\text{mb}} = 25$  °C;  $V_{\text{BAT}} = 3.6$  V;  $V_{\text{STAB}} = 2.8$  V  $\pm$  10 mV

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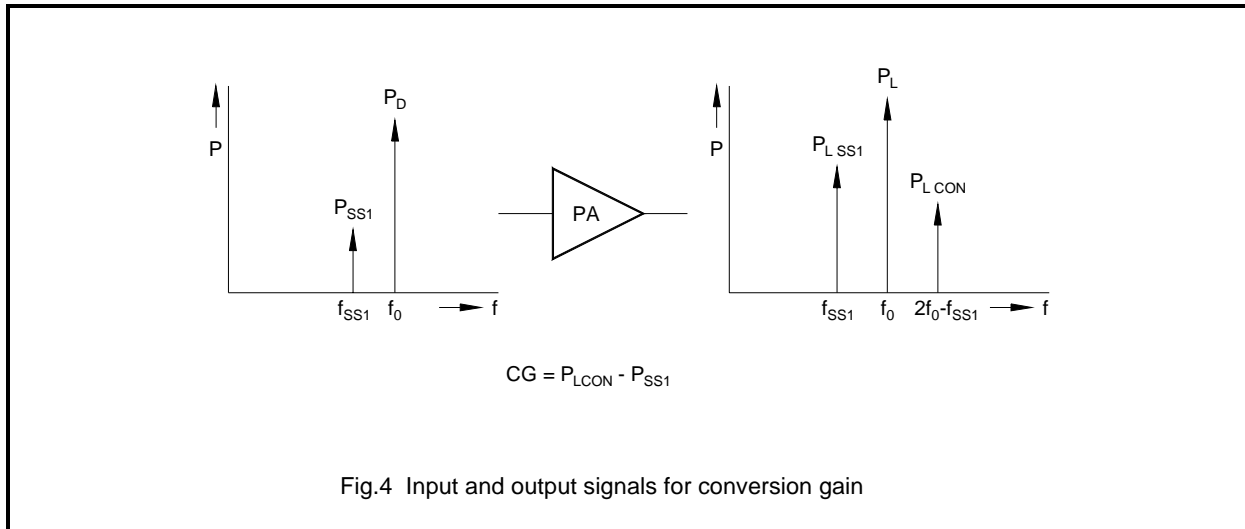


Fig.4 Input and output signals for conversion gain

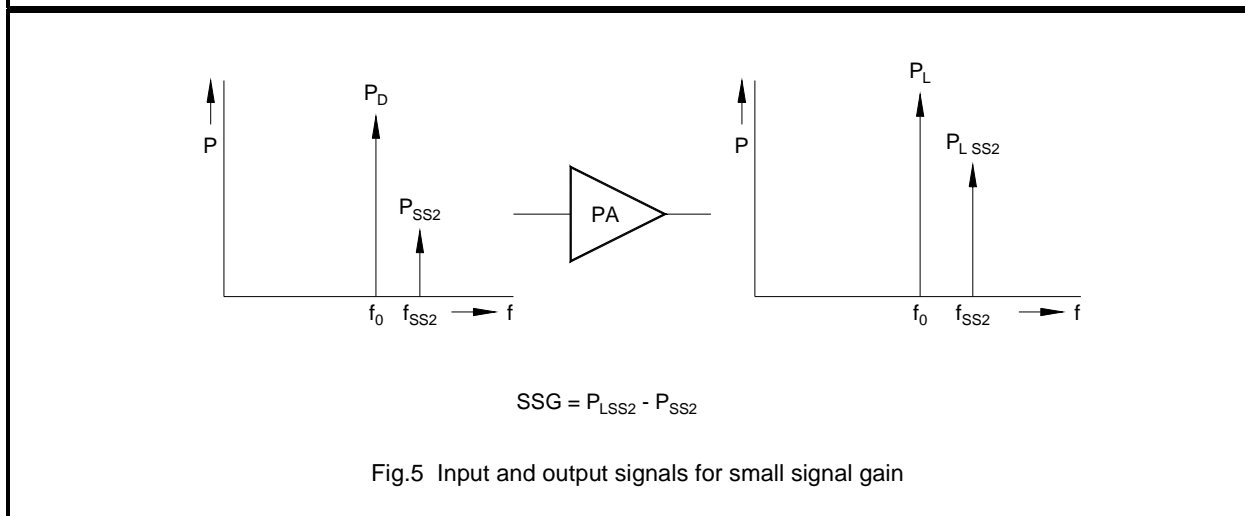


Fig.5 Input and output signals for small signal gain

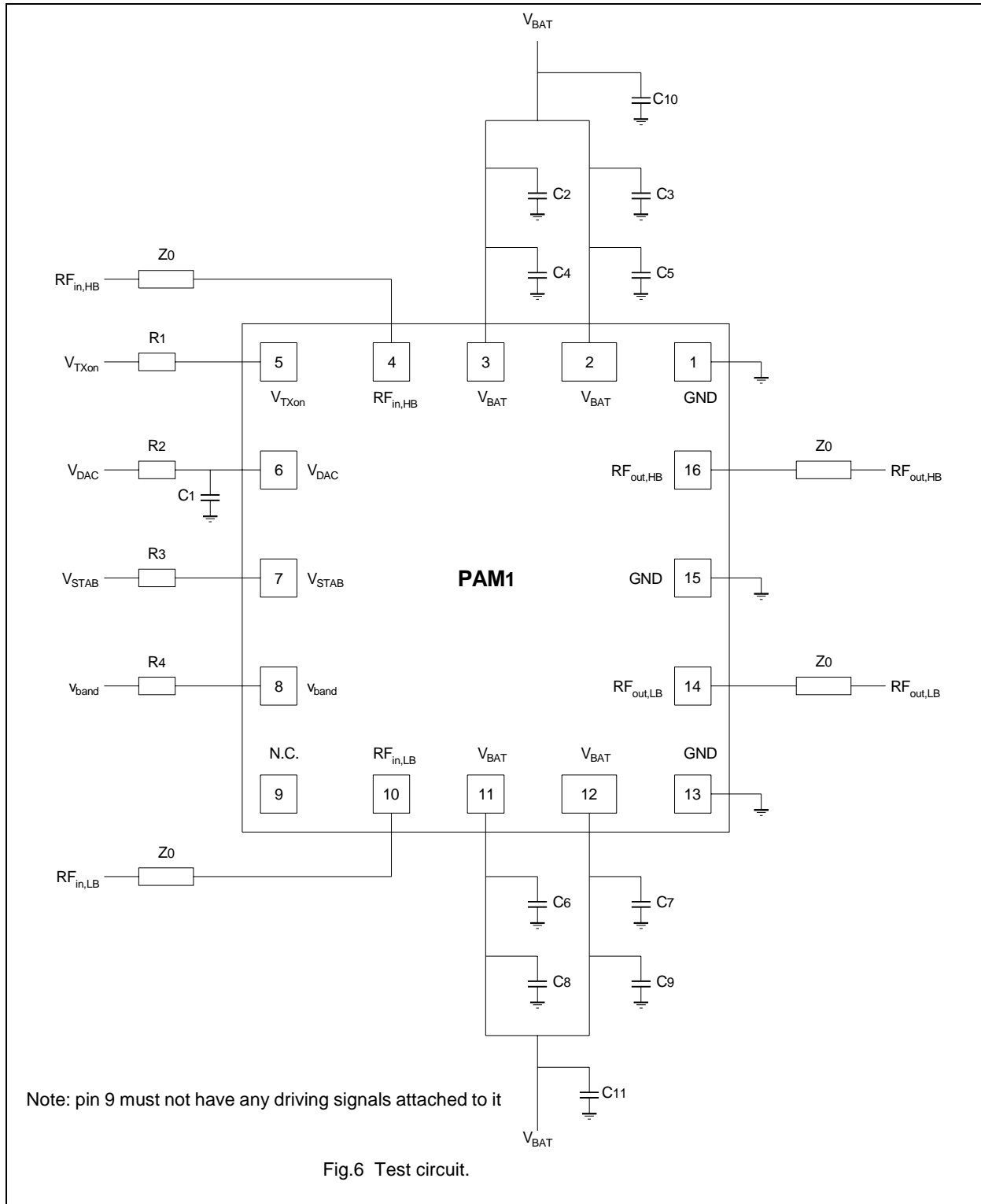
Note 1: total noise at the output of the PA is the summation of three sources:

- 1) the noise present at the input of the PA at  $f_{SS1}$  amplified by the conversion gain
- 2) the noise present at the input of the PA at  $f_{SS2}$  amplified by the small signal gain
- 3) the noise generated by the PA itself, when the noise at the input of the PA is 0

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APPLICATION INFORMATION



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## List of components

QUANTITY	LOCATION	VALUE / TYPE	DESCRIPTION	REMARK	SUPPLIER
1		PB005H1	PCB		Roland Haeefele
1	PAM1	BGY284	Power amplifier module		
4	CON1, CON2, CON3, CON4		Jack assembly end launch SMA connector	Type no. 142-0701-881	Johnson Components
1	CON5		DC conector 5 pin		
1	CON6		solder ring		
1	C1	2.7 nF	0603 size SMD capacitor		
4	C2, C3, C8, C9	100 nF	0805 size SMD capacitor		
2	C4, C5	10 pF	0603 size SMD capacitor		
2	C6, C7	33 pF	0603 size SMD capacitor		
2	C10, C11	47 $\mu$ F / 35 V	Electrol. capacitor	note 2	Matsushita
4	R1, R3, R4, R5	0 $\Omega$	0603 size SMD resistor		
1	R2	1k Ohms / 0.1 W	0603 size SMD resistor		
4	Z0	50 $\Omega$	stripline; note 1	width 1.4 mm	

## Note

1. The striplines are on a double etched printed circuit board ( $\epsilon_r = 4.6$ ); thickness 0.8 mm
2. C<sub>10</sub> and C<sub>11</sub> have been added to smoothen V<sub>BAT</sub>



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PCB Design PB005H1

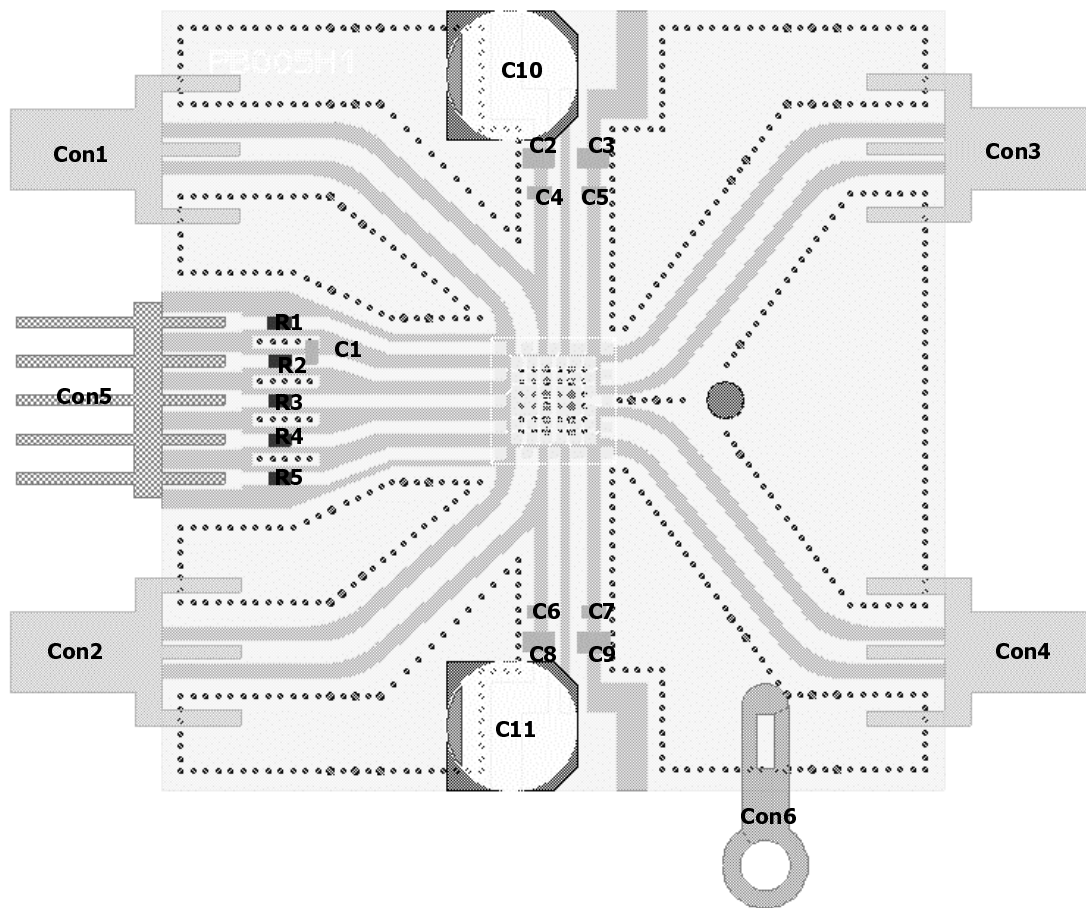


Fig.7 PCB testcircuit.

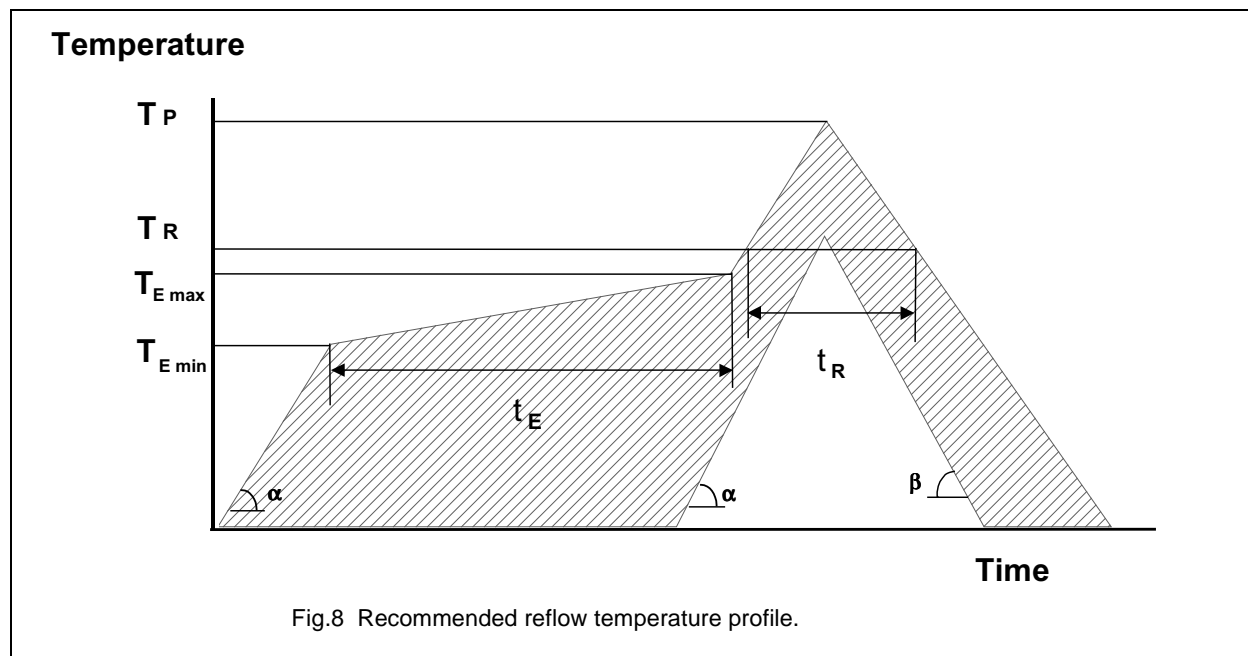
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**SOLDERING RECOMMENDATIONS****Reflow profile:**

The BGY284 is a laminate based PA module in a LGA package. The module can be assembled using a standard SMT reflow process in a convection or IR-oven.

In the graph below (see Fig.8) the minimum and maximum limits of the temperature profile are given. The actual profile has to be within these limits, and will depend on the PCB material, the number and size of the components to be assembled, and the type of solder which is being used.



It is recommended to use a standard no-clean solder paste like SnPb (in case of a profile for a lead containing solder) or SnAgCu (in case of a lead free assembly process). In the table the corresponding values are given for SnPb and for SnAgCu solder.

PARAMETER	SnPb SOLDER	SnAgCu SOLDER
Temperature gradient ( $\alpha$ ) ( $^{\circ}\text{C/s}$ )	$\leq 3$	$\leq 3$
Preheat (soak) temperature ( $T_E$ ) ( $^{\circ}\text{C}$ )	100 - 150	150 - 200
Preheat time ( $t_E$ ) (s)	60 - 120	60 - 180
Reflow temperature ( $T_R$ ) ( $^{\circ}\text{C}$ )	$> 183$	$> 217$
Reflow time ( $t_R$ ) (s)	60 - 150	60 - 150
Maximum peak temperature ( $T_P$ ) ( $^{\circ}\text{C}$ )	240	260
Temperature gradient ( $\beta$ ) ( $^{\circ}\text{C/s}$ )	$< 5$	$< 5$
Time 25 $^{\circ}\text{C}$ to peak temperature	6 minutes max.	8 minutes max.

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**BGY284****PCB layout:**

The PCB footprint layout is a copy of the metal pattern on the backside of the LGA package. It is recommended to design a big ground plane on the PCB, and to make the solder lands of the ground plane solder mask defined. A drawing of the footprint is included in the "Footprint layout SOT775A" drawing.

**Stencil design:**

The dimensions of the solder stencil are also given in the "Footprint layout SOT775A" drawing. The recommendation is based on a stencil thickness of 125  $\mu\text{m}$ . If a thinner or thicker stencil is being used, the dimensions of the stencil apertures have to be adjusted.

**Moisture sensitivity level:**

The BGY284 is tested according to the JEDEC standard JESD 22-A113C. The BGY284 is classified on MSL3 for a lead containing soldering profile with a peak temperature of 240  $^{\circ}\text{C}$ , and on MSL4 for a lead free soldering profile with a peak temperature of 260  $^{\circ}\text{C}$ .

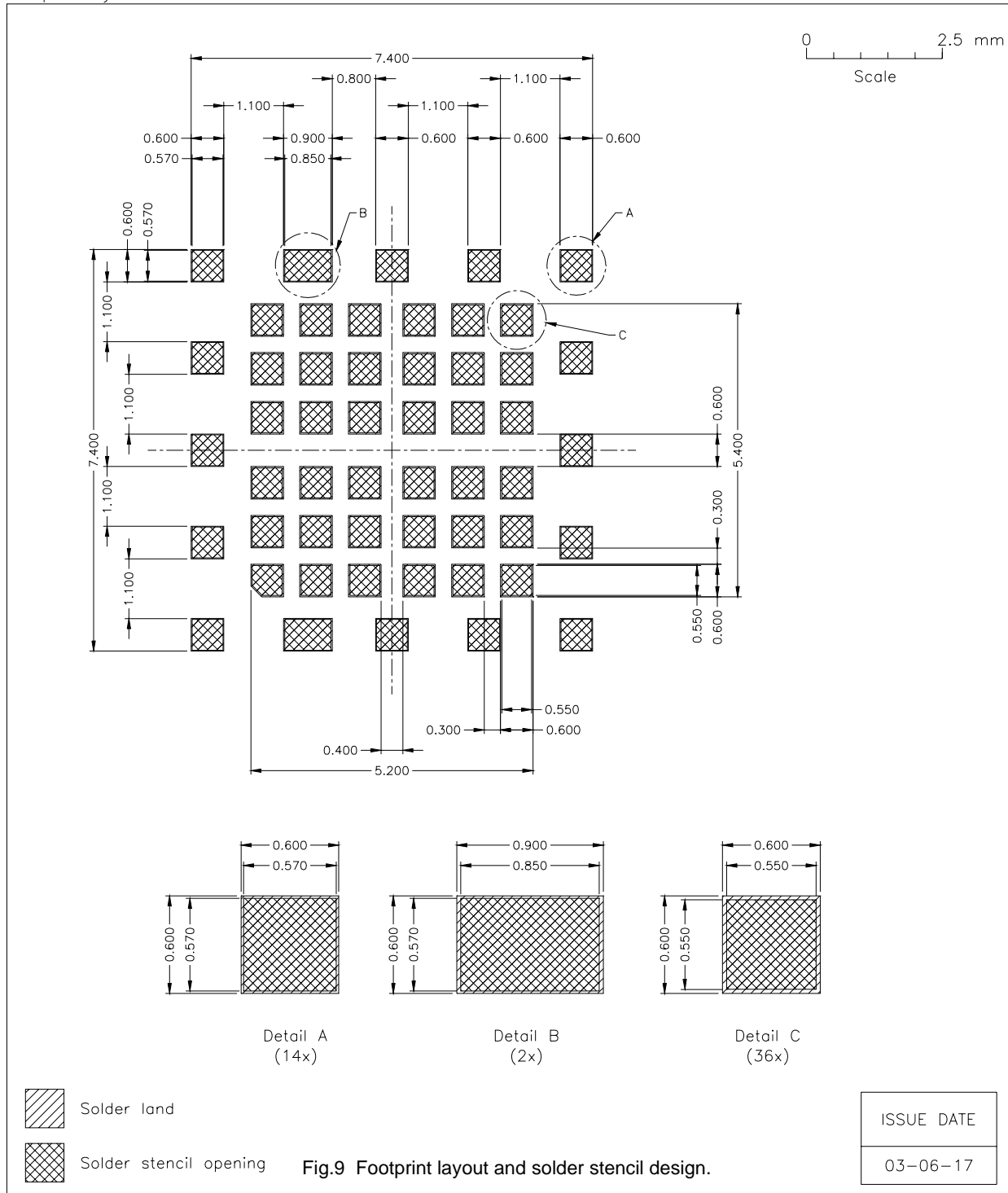
**Rework:**

If rework is needed it is recommended to use a BGA rework station with a programmable top and bottom heater. The first step of the rework process is preheating the PCB with the bottom heater of the rework station. When the board has reached the preheat temperature then the top heater can be used to increase the temperature above the melting point of the solder. The component which has to be replaced can be picked up with a vacuum nozzle. Before placing a new component the remaining solder on the board has to be removed. Fresh solder can be dispensed, a new component can be placed, and the board can be heated in a similar way as described before.

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Footprint layout SOT775A

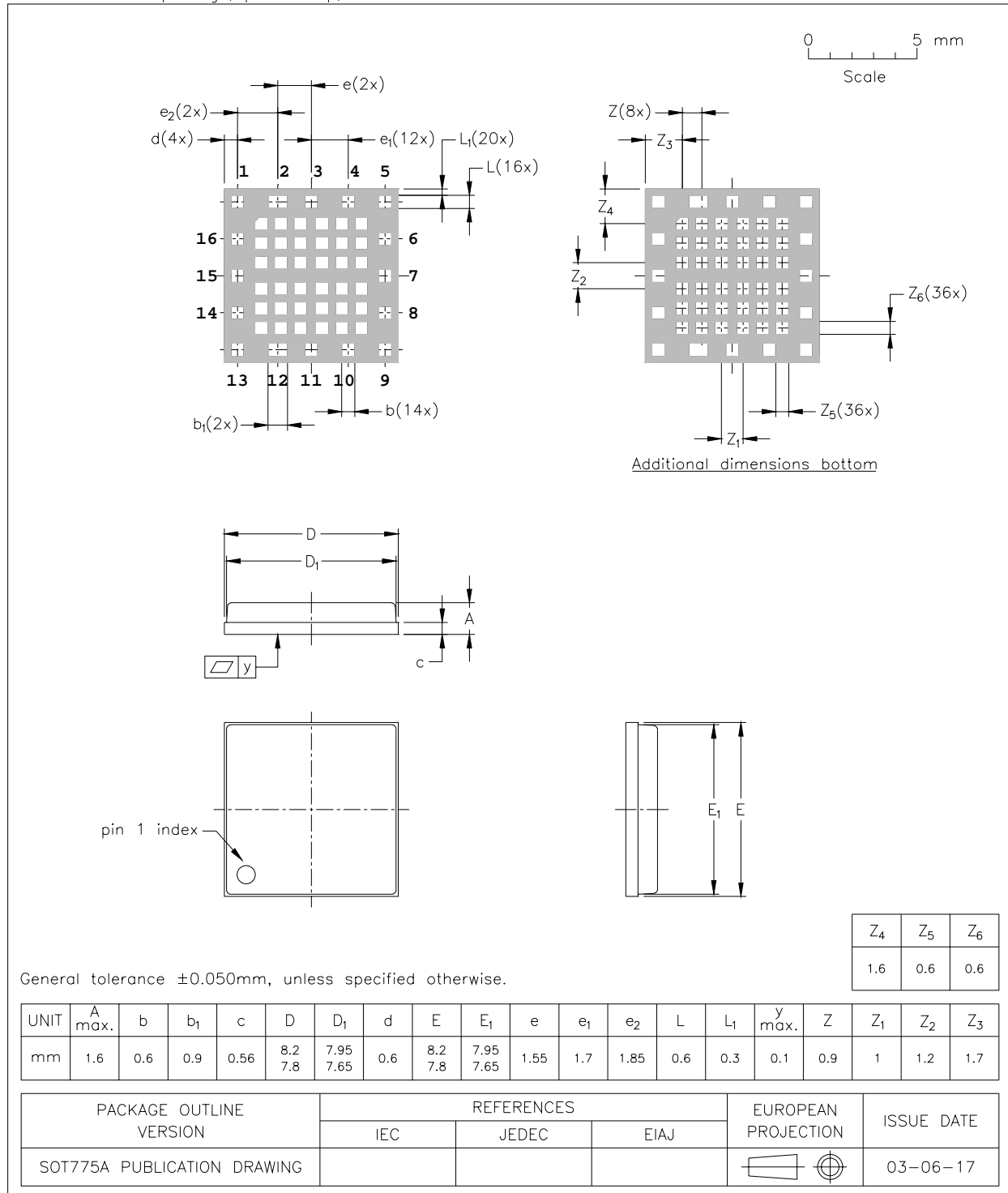


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PACKAGE OUTLINE

Surface mounted package; plastic cap; 16 terminations



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## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Printed in The Netherlands

budgetnum/printrun/ed/pp23

Date of release: 2003 Aug 20

Document order number: 9397 750 11968

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