Ordering number: EN3003B

CMOS LSI

SANYO No.3003B

LC7385, 7385M

DTMF Receiver

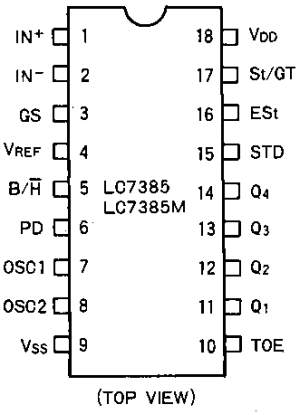
Overview

The LC7385, 7385M CMOS DTMF Receiver LSIs integrate bandsplit filter and digital decoder functions for the 16 DTMF digits used in touch-tone telephone systems.

Features

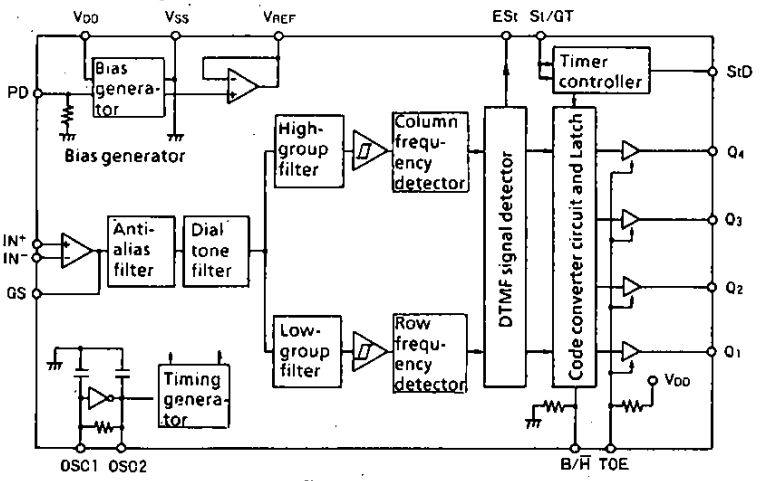
① Single +5V power supply
② Decodes all 16 DTMF digits.
③ Built-in differential input amplifier
④ On-chip filters, including
- Dial tone filter
- High-group filter
- Low-group filter

⑤ User-selectable acquisition and release times
⑥ Pin-selectable 4-bit hexadecimal or binary-coded 2-of-8 output
⑦ 3-state data outputs facilitate microcontroller or other peripheral interfaces.
⑧ Standby mode
⑨ Low-power double-poly CMOS process
⑩ LC7385 : 18-pin DIP package
LC7385M : 18-pin MFP package

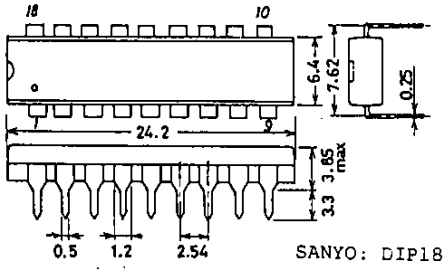


Pin Assignment

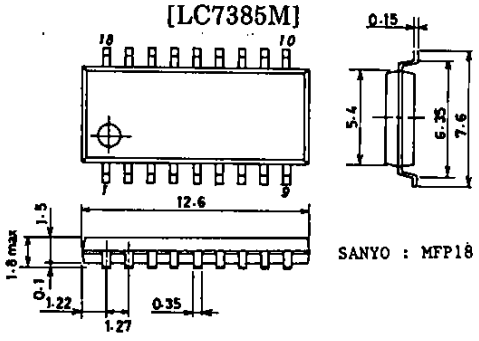
Block Diagram



Package Dimensions (unit: mm) 3007A [LC7385]



Package Dimensions (unit: mm) 3095 [LC7385M]



SANYO Electric Co.,Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10,1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

Pin Functions

Pin No.	Name	I/O	Description
1	IN+	I	Input amp non-inverting input
2	IN−	I	Input amp inverting input
3	GS	O	Input amp output
4	V_{REF}	O	Reference voltage output ($V_{DD}/2$)
5	B/$\overline{H}$	I	Q1 to Q4 output format selection: Binary 2-of-8 when HIGH Hexadecimal when LOW
6	PD	I	Standby mode when set to HIGH
7 8	OSC1 OSC2	I O	Clock pins. 3.579545MHz crystal is connected between OSC1 and OSC2.
9	V_{SS}		Power supply. Normally 0V
10	TOE	I	Q1 to Q4 3-state output selection: Enabled when HIGH High-impedance when LOW
11	Q_1	O	3-state data output
12	Q_2		
13	Q_3		
14	Q_4		
15	StD	O	Goes HIGH when valid tone pair duration exceeds set guard time.
16	ESt	O	Goes HIGH when valid tone pair is detected.
17	St/GT	I/O	Used to set guard time.
18	V_{DD}		Power supply. Normally 5V

Absolute Maximum Ratings at Ta = 25 ± 2°C, V_{SS} = 0V

Parameter	Symbol	Condition	Rating		unit
Maximum Supply Voltage	V_{DD} max		−0.3 to +7.0		V
Input Voltage	V_{IN}		−0.3 to V_{DD}+0.3		V
Input Current	I_{IN}		−10 to +10		mA
Output Voltage	V_{OUT}		−0.3 to V_{DD}+0.3		V
Power Dissipation	P_D	−40°C ≦ Ta ≦ +85°C	DIP-18	250	mW
			MFP-18	180	
Operating Temperature	Topr		−40 to +85		°C
Storage Temperature	Tstg		−50 to +125		°C

Allowable Operating Conditions at Ta = −40 to +85°C, V_{SS} = 0V

Parameter	Symbol	Condition	min	typ	max	unit	Pin No.
Operating Voltage	V_{DD}		4.75		5.25	V	
Input 'H'-Level Voltage	V_{IH}		0.7V_{DD}			V	6,10
			0.85V_{DD}			V	5
Input 'L'-Level Voltage	V_{IL}				0.3V_{DD}	V	6.10
					0.15V_{DD}	V	5

Note : When soldering the 18-pin MFP package, solder it manually or use the infrared reflow method. Do not use the dip-soldering method. The conditions for the infrared reflow method are 235°C max., 10sec.

DC Electrical Characteristics at $Ta = 25 \pm 2°C, V_{DD} = 5V, V_{SS} = 0V$

Parameter	Symbol	Condition	min	typ	max	unit	Pin No.
Operating Supply Current	I_{DD} (op)			3.0	7.0	mA	
Standby Supply Current	I_{DD} (st)	PD=5V			100	μA	
Output 'H'-Level Current	I_{OH}	V_{OUT}=4.6V		−0.8	−0.4	mA	11,12,13 14,15,16
				−3.0	−1.2	mA	17
Output 'L'-Level Current	I_{OL}	V_{OUT}=0.4V	1.0	2.5		mA	11.12.13 14.15.16
			1.2	3.0		mA	17
OFF-State Output Current	I_{OZH}	TOE=0V, V_{OUT}=5V			10	μA	11,12,13
	I_{OZL}	TOE=0V, V_{OUT}=5V	−10			μA	14
Input 'H'-Level Current	I_{IH}	V_{IN}=5V			10	μA	1,2,10
Input 'L'-Level Current	I_{IL}	V_{IN}=0V	−10			μA	1,2,5,6
Pull-up (source) Current	I_{SO}	TOE=0V	−15	−5		μA	10
Pull-down (sink) Current	I_{SI}	PD,B/H=5V		5	15	μA	5,6
St/GT Threshold Voltage	V_{TST}			2.35		V	17
V_{REF} Output Voltage	V_{REF}	No load	2.4		2.7	V	4
V_{REF} Output Resistance	R_{REF}			1		kΩ	4

Input Amplifier Characteristics at $Ta = 25 \pm 2°C, V_{DD} = 5V, V_{SS} = 0V$

Parameter	Symbol	Condition	min	typ	max	unit
Input Offset Voltage	V_{IO}		−25		+25	mV
Input Offset Current	I_{IO}	$V_{SS} \leqq V_{IN} \leqq V_{DD}$		±100		nA
Power Supply Rejection	PSRR	1kHz		60		dB
Common Mode Rejection	CMRR			60		dB
Open-Loop Voltage Gain	A_O			65		dB
0dB Gain Bandwidth	f_T			1.5		MHz
Maximum Output Voltage	V_O	$R_L \geqq 100k\Omega$		4.5		Vp-p
Tolerable Capacitive Load	C_L			100		pF
Tolerable Resistive Load	R_L			50		kΩ
Common Mode Range	V_{CM}	No load		3.0		Vp-p

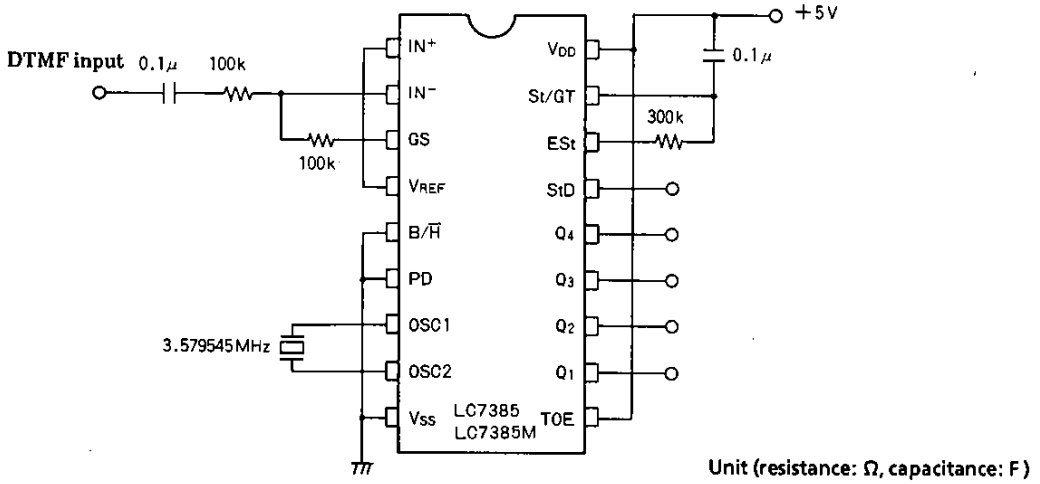
AC Characteristics at Ta = 25 ± 2°C, V_{DD} = 5V, V_{SS} = 0V, f_{OSC} = 3.579545MHz

Parameter	Symbol	Condition	min	typ	max	unit
Valid Input Signal Level		1, 2, 3, 5, 6, 9	−29		1.1	dBm
Twist Accept Limit		2, 3, 6, 9, 11		±10		dB
Frequency Deviation Accept Limit		2, 3, 5, 9			±1.5% ±2Hz	
Frequency Deviation Accept Limit		2, 3, 5	±3.5			%
Third Tone Tolerance		2, 3, 4, 5, 9, 10		−16		dB
Dial tone Tolerance		2, 3, 4, 5, 8, 9, 10		+18		dB
Noise Tolerance		2, 3, 4, 5, 7, 9, 10		−12		dB
Tone Present Detection Time	t_{DP}	See timing diagram.	5	11	14	ms
Tone Absent Detection Time	t_{DA}		0.5	4.0	8.5	ms
Tone Duration Accept	t_{REC}	Adjustable. See Guard Time Adjustment.	40			ms
Tone Duration Reject	t_{REJ}				20	ms
Interdigit Pause Accept	t_{ID}		40			ms
Interdigit Pause Reject	t_{DO}				20	ms
Propagation Delay (St→Q)	t_{PQ}	TOE = 5V, No load		8	11	μs
Propagation Delay (St→StD)	t_{PSTD}	TOE = 5V, No load		12		μs
Output Data Set-Up (Q→StD)	t_{QSTD}	TOE = 5V, No load		4.5		μs
Output Enable Delay	t_{PTE}	R_L = 10k, C_L = 50pF		50	100	ns
Output Disable Delay	t_{PTD}	R_L = 10k, C_L = 50pF		300		ns
Clock Frequency	f_{OSC}		3.5759	3.5795	3.5831	MHz
Clock Capacitive Load	C_{XO}	OSC2			30	pF

Conditions

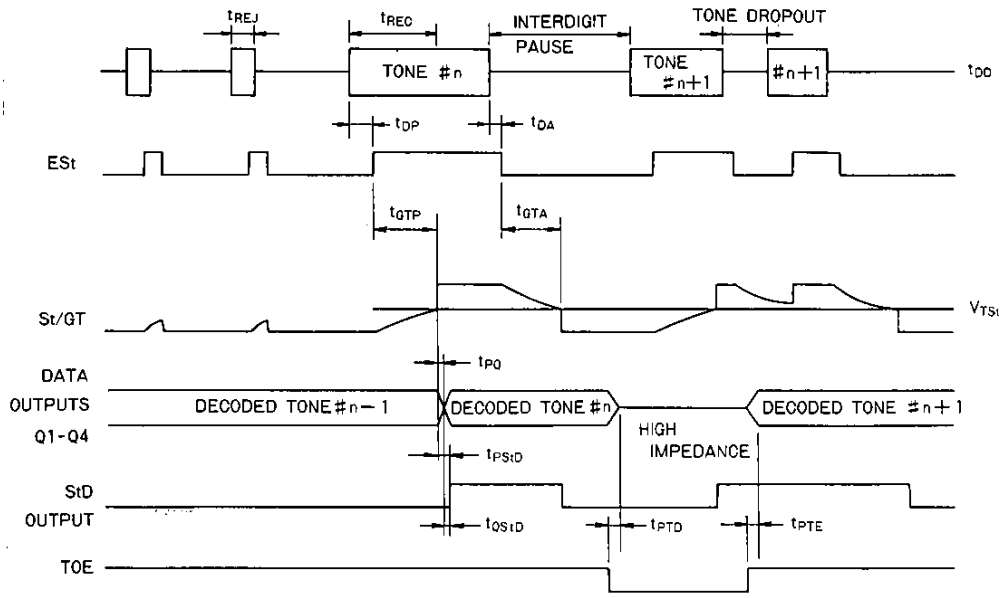
1. dBm = decibels above or below a reference power of 1mW into a 600Ω load
2. All 16 DTMF tones
3. 40ms DTMF tone duration and 40ms pause duration
4. Nominal DTMF frequencies
5. Both tones in composite signal have an equal amplitude.
6. Tone pair deviated by ±1.5% ±2Hz
7. Bandwidth limited (0 to 3kHz) Gaussian noise
8. 350Hz and 440Hz +2% dial tone frequencies
9. Error rate better than 1 in 10,000
10. Referenced to lowest level frequency component in DTMF signal
11. Twist = ratio of high-frequency tone level to low-frequency tone level

Single-Ended Input Configuration

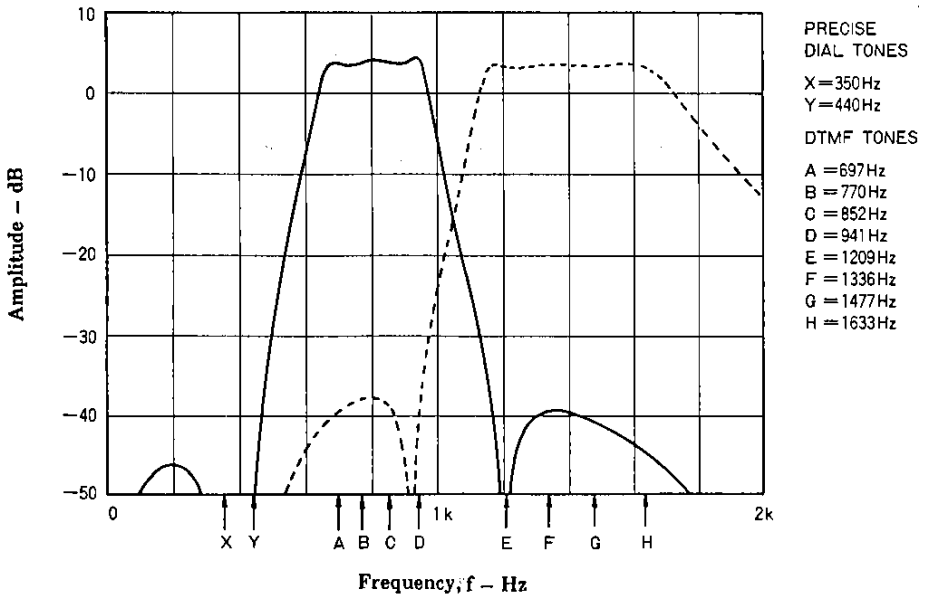


Unit (resistance: Ω, capacitance: F)

Timing Diagram



Typical Filter Characteristics

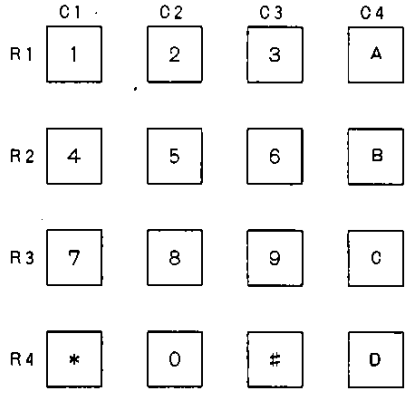


Decode Table

FL	FH	KEY	TOE	B/H="L"				B/H="H"			
				Q4	Q3	Q2	Q1	Q4	Q3	Q2	Q1
697	1209	1	H	L	L	L	H	L	L	L	L
697	1336	2	H	L	L	H	L	L	L	L	H
697	1477	3	H	L	L	H	H	L	L	H	L
770	1209	4	H	L	H	L	L	L	H	L	L
770	1336	5	H	L	H	L	H	L	H	L	H
770	1477	6	H	L	H	H	L	L	H	H	L
852	1209	7	H	L	H	H	H	H	L	L	L
852	1336	8	H	H	L	L	L	H	L	L	H
852	1477	9	H	H	L	L	H	H	L	H	L
941	1336	0	H	H	L	H	L	H	H	L	H
941	1209	*	H	H	L	H	H	H	H	L	L
941	1477	#	H	H	H	L	L	H	H	H	L
697	1633	A	H	H	H	L	H	L	L	H	H
770	1633	B	H	H	H	H	L	L	H	H	H
852	1633	C	H	H	H	H	H	H	L	H	H
941	1633	D	H	L	L	L	L	H	H	H	H
—	—	—	L	Z	Z	Z	Z	Z	Z	Z	Z
								ROW m		COL n	

Note : Z=High impedance

DTMF Dialing Matrix



Guard Time Setting

Component values are chosen using the following formula:

$t_{REC} = t_{DP} + t_{GTP}$

$t_{ID} = t_{DA} + t_{GTA}$

(a) Basic Circuit

$t_{GTP} = RC \cdot \ln [\, V_{DD} / (V_{DD} - V_{TST}) \,]$

$t_{GTA} = RC \cdot \ln (V_{DD} / V_{TST})$

(b) $t_{GTP} < t_{GTA}$

$t_{GTP} = R_1 R_2 / (R_1 + R_2) \cdot C \cdot \ln [\, V_{DD} / (V_{DD} - V_{TST}) \,]$

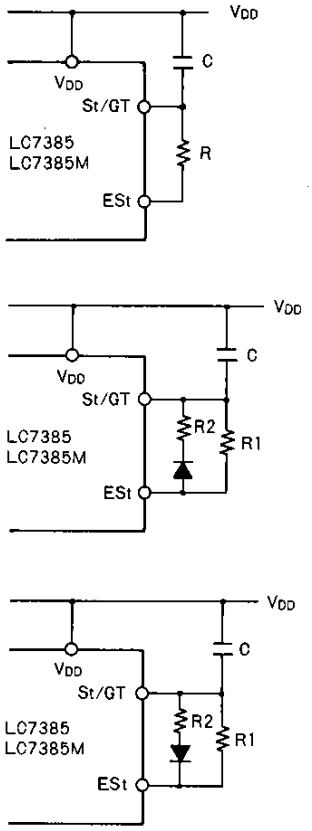
$t_{GTA} = R_1 C \cdot \ln (V_{DD} / V_{TST})$

(c) $t_{GTP} > t_{GTA}$

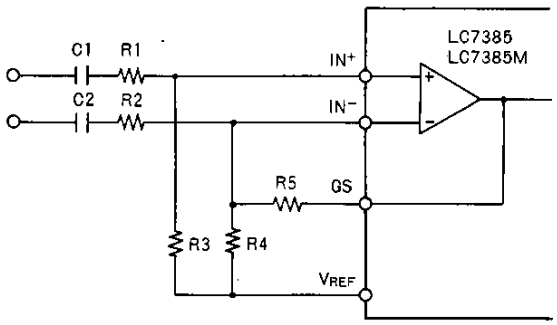
$t_{GTP} = R_1 C \cdot \ln [\, V_{DD} / (V_{DD} - V_{TST}) \,]$

$t_{GTA} = R_1 R_2 / (R_1 + R_2) \cdot C \cdot \ln (V_{DD} / V_{TST})$

Guard Time Adjustment



Differential Input Configuration



Example of component values

$C_1 = C_2 = 0.01\mu F$

$R_1 = R_2 = R_5 = 100k\Omega$

$R_4 = 60k\Omega$, $R_3 = 37.5k\Omega$

$$R_3 = \frac{R_4 R_5}{R_4 + R_5}$$

Voltage gain : $Av = \dfrac{R_5}{R_1}$

Input impedance = $2\sqrt{R_1^2 + \left(\dfrac{1}{2\pi f c_1}\right)^2}$