ADVANCE INFORMATION

WORD-WIDE
FlashFile™ MEMORY FAMILY
28F160S3, 28F320S3

Includes Extended Temperature Specifications

- **Two 32-Byte Write Buffers**
  - **2.7 µs per Byte Effective Programming Time**
- **Low Voltage Operation**
  - **2.7V or 3.3V V_{CC}**
  - **2.7V, 3.3V or 5V V_{PP}**
- **100 ns Read Access Time (16 Mbit)**
  110 ns Read Access Time (32 Mbit)
- **High-Density Symmetrically-Blocked Architecture**
  - **32 64-Kbyte Erase Blocks (16 Mbit)**
  - **64 64-Kbyte Erase Blocks (32 Mbit)**
- **System Performance Enhancements**
  - **STS Status Output**
- **Industry-Standard Packaging**
  - **µBGA* package, SSOP, and TSOP (16 Mbit)**
  - **µBGA* package and SSOP (32 Mbit)**
- **Cross-Compatible Command Support**
  - **Intel Standard Command Set**
  - **Common Flash Interface (CFI)**
  - **Scaleable Command Set (SCS)**
- **100,000 Block Erase Cycles**
- **Enhanced Data Protection Features**
  - **Absolute Protection with V_{PP} = GND**
  - **Flexible Block Locking**
  - **Block Erase/Program Lockout during Power Transitions**
- **Configurable x8 or x16 I/O**
- **Automation Suspend Options**
  - **Program Suspend to Read**
  - **Block Erase Suspend to Program**
  - **Block Erase Suspend to Read**
- **ETOX™ V Nonvolatile Flash Technology**

Intel's Word-Wide FlashFile™ memory family provides high-density, low-cost, non-volatile, read/write storage solutions for a wide range of applications. The Word-Wide FlashFile memories are available at various densities in the same package type. Their symmetrically-blocked architecture, flexible voltage, and extended cycling provide highly flexible components suitable for resident flash arrays, SIMMs, and memory cards. Enhanced suspend capabilities provide an ideal solution for code or data storage applications. For secure code storage applications, such as networking, where code is either directly executed out of flash or downloaded to DRAM, the Word-Wide FlashFile memories offer three levels of protection: absolute protection with V_{PP} at GND, selective block locking, and program/erase lockout during power transitions. These alternatives give designers ultimate control of their code security needs.

This family of products is manufactured on Intel's 0.4 µm ETOX™ V process technology. It comes in the industry-standard 56-lead SSOP and µBGA packages. In addition, the 16-Mb device is available in the industry-standard 56-lead TSOP package.

June 1997

Order Number: 290608-001

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The 28F160S3 and 28F320S3 may contain design defects or errors known as errata. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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REVISION HISTORY

Number	Description
-001	Original version

1.0 INTRODUCTION

This datasheet contains 16- and 32-Mbit Word-Wide FlashFile™ memory (28F160S3 and 28F320S3) specifications. Section 1 provides a flash memory overview. Sections 2, 3, 4, and 5 describe the memory organization and functionality. Section 6 covers electrical specifications for extended temperature product offerings.

1.1 New Features

The Word-Wide FlashFile memory family maintains basic compatibility with Intel's 28F016SA and 28F016SV. Key enhancements include:

- Common Flash Interface (CFI) Support
- Scaleable Command Set (SCS) Support
- Low Voltage Technology
- Enhanced Suspend Capabilities

They share a compatible Status Register, basic software commands, and pinout. These similarities enable a clean migration from the 28F016SA or 28F016SV. When upgrading, it is important to note the following differences:

- Because of new feature and density options, the devices have different manufacturer and device identifier codes. This allows for software optimization.
- New software commands.
- To take advantage of low voltage on the 28F160S3 and 28F320S3, allow V_{PP} connection to V_{CC}. The 28F160S3 and 28F320S3 do not support a 12V V_{PP} option.

1.2 Product Overview

The Word-Wide FlashFile memory family provides density upgrades with pinout compatibility for the 16- and 32-Mbit densities. They are high-performance memories arranged as 1 Mword and 2 Mwords of 16 bits or 2 Mbyte and 4 Mbyte of 8 bits. This data is grouped in thirty-two and sixty-four 64-Kbyte blocks that can be erased, locked and unlocked in-system. Figure 1 shows the block diagram, and Figure 5 illustrates the memory organization.

This family of products are optimized for fast factory programming and low power designs. Specifically designed for 3V systems, the 28F160S3 and 28F320S3 support read operations at 2.7V–3.6V Vcc with block erase and program operations at 2.7V–3.6V and 5V V_{PP}. High programming performance is achieved through highly-optimized write buffers. A 5V V_{PP} option is available for even faster factory programming. For a simple low power design, V_{CC} and V_{PP} can be tied to 2.7V. Additionally, the dedicated V_{PP} pin gives complete data protection when $V_{PP} \leq V_{PPLK}$.

Internal V_{PP} detection circuitry automatically configures the device for optimized write operations.

A Common Flash Interface (CFI) permits OEM-specified software algorithms to be used for entire families of devices. This allows device-independent, JEDEC ID-independent, and forward- and backward-compatible software support for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

Scaleable Command Set (SCS) allows a single, simple software driver in all host systems to work with all SCS-compliant flash memory devices, independent of system-level packaging (e.g., memory card, SIMM, or direct-to-board placement). Additionally, SCS provides the highest system/device data transfer rates and minimizes device and system-level implementation costs.

A Command User Interface (CUI) serves as the interface between the system processor and internal device operation. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase, program, and lock-bit configuration operations.

A block erase operation erases one of the device's 64-Kbyte blocks typically within $t_{WHQV2/EHQV2}$ independent of other blocks. Each block can be independently erased 100,000 times. Block erase suspend mode allows system software to suspend block erase to read or write data from any other block.

Data is programmed in byte, word or page increments. Program suspend mode enables the system to read data or execute code from any other flash memory array location.

The device incorporates two Write Buffers of 32 bytes (16 words) to allow optimum-performance data programming. This feature can improve system program performance by up to four times over non-buffer programming.

Individual block locking uses a combination of block lock-bits to lock and unlock blocks. Block lock-bits gate block erase, full chip erase, program and write to buffer operations. Lock-bit configuration operations (Set Block Lock-Bit and Clear Block Lock-Bits commands) set and clear lock-bits.

The Status Register and the STS pin in RY/BY# mode indicate whether or not the device is busy executing an operation or ready for a new command. Polling the Status Register, system software retrieves WSM feedback. STS in RY/BY# mode gives an additional indicator of WSM activity by providing a hardware status signal. Like the Status Register, RY/BY#-low indicates that the WSM is performing a block erase, program, or lock-bit operation. RY/BY#-high indicates that the WSM is ready for a new command, block erase is suspended (and program is inactive), program is suspended, or the device is in deep power-down mode.

The Automatic Power Savings (APS) feature substantially reduces active current when the device is in static mode (addresses not switching).

The BYTE# pin allows either x8 or x16 read/writes to the device. BYTE# at logic low selects 8-bit mode with address A_0 selecting between the low byte and high byte. BYTE# at logic high enables 16-bit operation with address A_1 becoming the lowest order address. Address A_0 is not used in 16-bit mode.

When one of the CE_X# pins (CE_0#, CE_1#) and RP# pins are at V_{CC}, the component enters a CMOS standby mode. Driving RP# to GND enables a deep power-down mode which significantly reduces power consumption, provides write protection, resets the device, and clears the Status Register. A reset time (t_{PHQV}) is required from RP# switching high until outputs are valid. Likewise, the device has a wake time (t_{PHEL}) from RP#-high until writes to the CUI are recognized.

1.3 Pinout and Pin Description

The 16-Mbit device is available in the 56-lead TSOP, 56-lead SSOP and µBGA packages. The 32- Mb device is available in the 56-lead SSOP and µBGA packages. The pinouts are shown in Figures 2, 3 and 4.

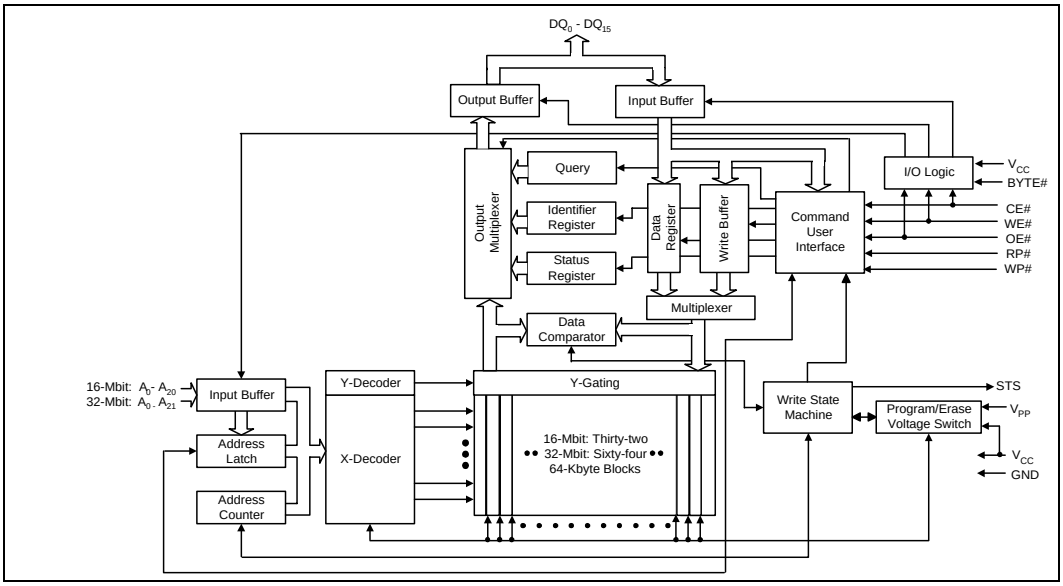

Figure 1. Block Diagram

Table 1. Pin Descriptions

Sym	Type	Name and Function
A_0–A_{21}	INPUT	**ADDRESS INPUTS:** Address inputs for read and write operations are internally latched during a write cycle. A_0 selects high or low byte when operating in x8 mode. In x16 mode, A_0 is not used; input buffer is off. 16-Mbit → A_0–A_{20} 32-Mbit → A_0–A_{21}
DQ_0–DQ_{15}	INPUT/ OUTPUT	**DATA INPUTS/OUTPUTS:** Inputs data and commands during CUI write cycles; outputs data during memory array, Status Register, query and identifier code read cycles. Data pins float to high-impedance when the chip is deselected or outputs are disabled. Data is internally latched during a write cycle.
CE_0#, CE_1#	INPUT	**CHIP ENABLE:** Activates the device's control logic, input buffers, decoders, and sense amplifiers. With CE_0# or CE_1# high, the device is deselected and power consumption reduces to standby levels. Both CE_0# and CE_1# must be low to select the device. Device selection occurs with the latter falling edge of CE_0# or CE_1#. The first rising edge of CE_0# or CE_1# disables the device.
RP#	INPUT	**RESET/DEEP POWER-DOWN:** When driven low, RP# inhibits write operations which provides data protection during system power transitions, puts the device in deep power-down mode, and resets internal automation. RP#-high enables normal operation. Exit from deep power-down sets the device to read array mode.
OE#	INPUT	**OUTPUT ENABLE:** Gates the device's outputs during a read cycle.
WE#	INPUT	**WRITE ENABLE:** Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of the WE# pulse.
STS	OPEN DRAIN OUTPUT	**STATUS:** Indicates the status of the internal state machine. When configured in level mode (default), it acts as a RY/BY# pin. For this and alternate configurations of the STATUS pin, see the Configuration command. Tie STS to V_{CC} with a pull-up resistor.
WP#	INPUT	**WRITE PROTECT:** Master control for block locking. When V_{IL}, locked blocks cannot be erased or programmed, and block lock-bits cannot be set or cleared.
BYTE#	INPUT	**BYTE ENABLE:** Configures x8 mode (low) or x16 mode (high).
V_{PP}	SUPPLY	**BLOCK ERASE, PROGRAM, LOCK-BIT CONFIGURATION POWER SUPPLY:** Necessary voltage to perform block erase, program, and lock-bit configuration operations. Do not float any power pins.
V_{CC}	SUPPLY	**DEVICE POWER SUPPLY:** Do not float any power pins. Do not attempt block erase, program, or block-lock configuration with invalid V_{CC} values.
GND	SUPPLY	**GROUND:** Do not float any ground pins.
NC		**NO CONNECT:** Lead is not internally connected; it may be driven or floated.

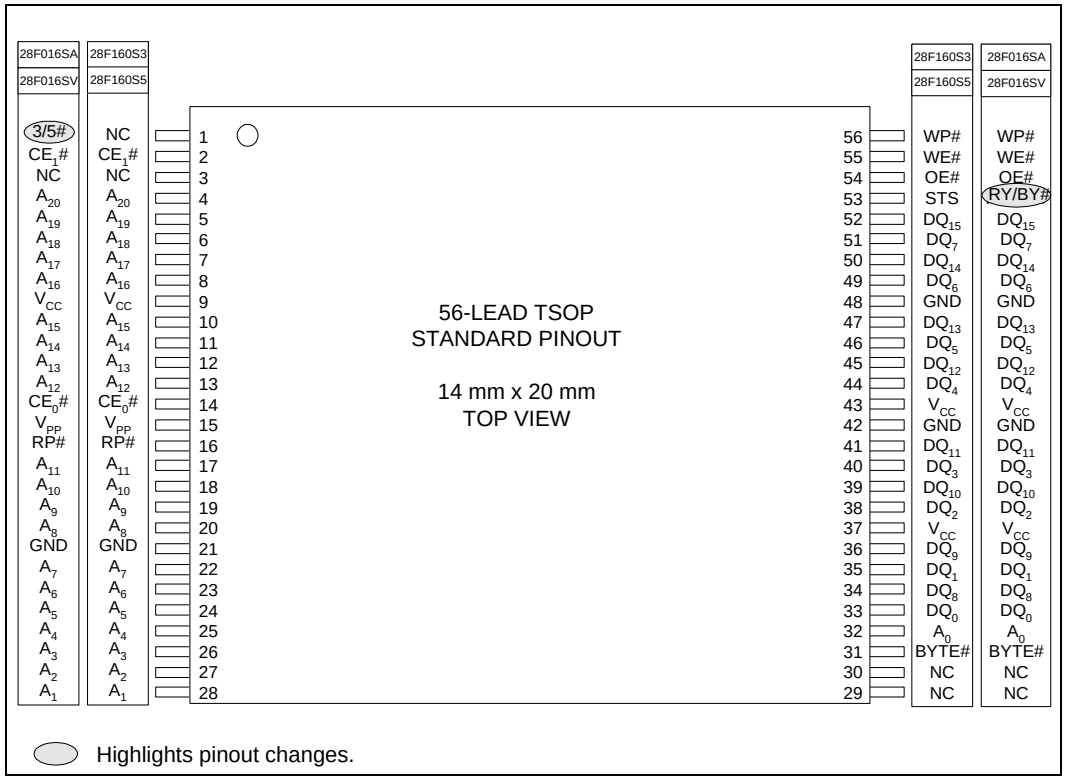

Figure 2. TSOP 56-Lead Pinout

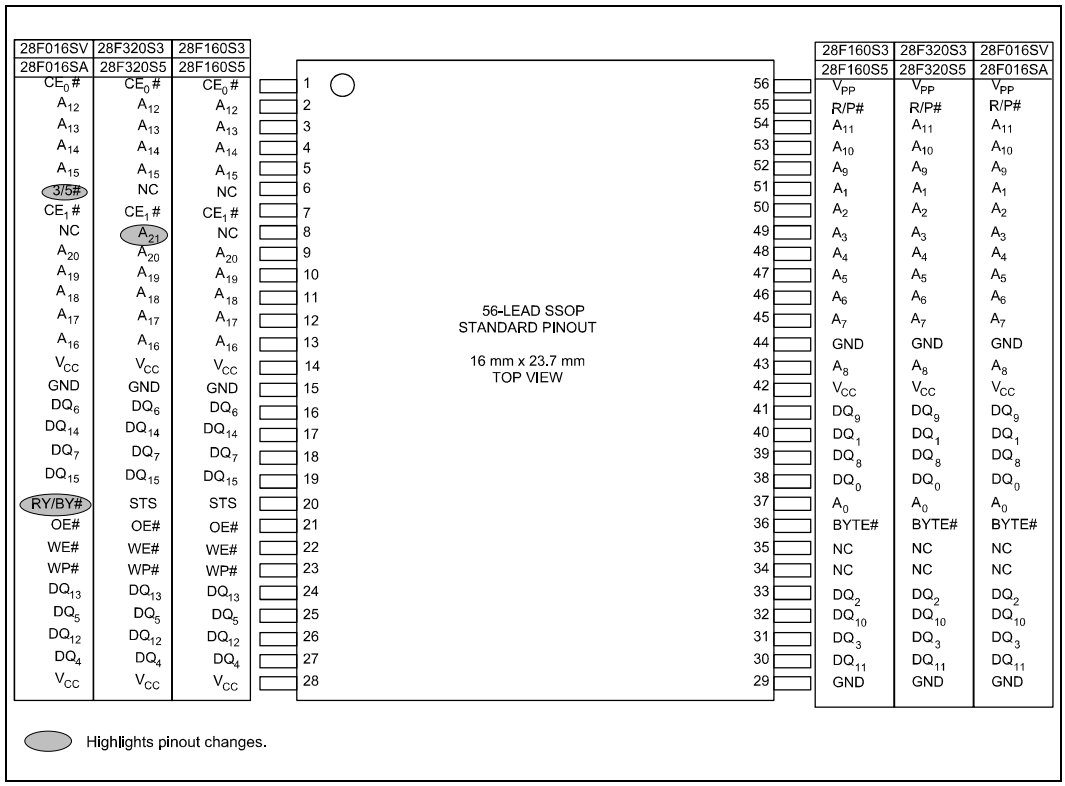

Figure 3. SSOP 56-Lead Pinout

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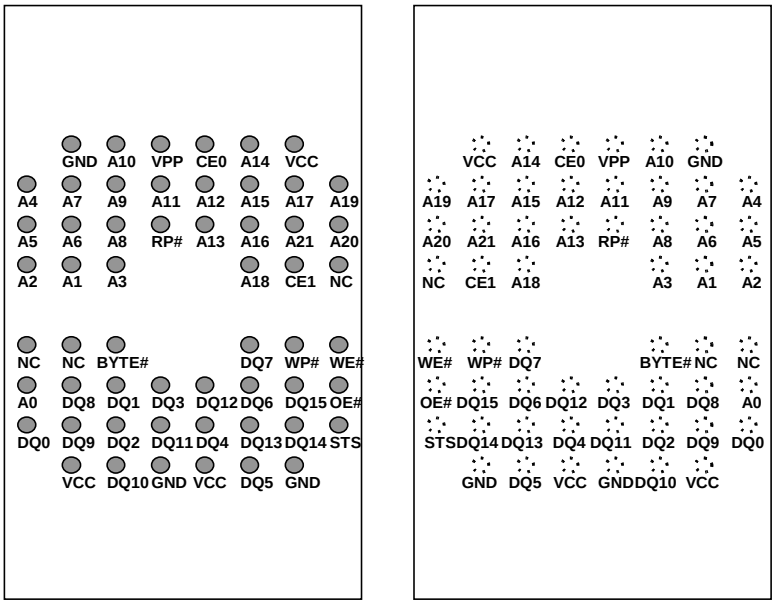


Bottom View

This is the view of the package as surface mounted on the board. Note that the signals are mirror imaged.

NOTES:

1. Figures are not drawn to scale.
2. Address A_{21} is not included in the 28F160S3.
3. More information on µBGA* packages is available by contacting your Intel/Distribution sales office.

Figure 4. µBGA* Package Pinout

2.0 PRINCIPLES OF OPERATION

The word-wide memories include an on-chip Write State Machine (WSM) to manage block erase, program, and lock-bit configuration functions. It allows for: 100% TTL-level control inputs, fixed power supplies during block erasure, programming, lock-bit configuration, and minimal processor overhead with RAM-like interface timings.

After initial device power-up or return from deep power-down mode (see Bus Operations), the device defaults to read array mode. Manipulation of external memory control pins allow array read, standby, and output disable operations.

Read Array, Status Register, query, and identifier codes can be accessed through the CUI independent of the V_{PP} voltage. Proper programming voltage on V_{PP} enables successful block erasure, program, and lock-bit configuration. All functions associated with altering memory contents—block erase, program, lock-bit configuration—are accessed via the CUI and verified through the Status Register.

Commands are written using standard microprocessor write timings. The CUI contents serve as input to the WSM that controls the block erase, programming, and lock-bit configuration. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification, and margining of data. Addresses and data are internally latched during write cycles. Writing the appropriate command outputs array data, identifier codes, or Status Register data.

Interface software that initiates and polls progress of block erase, programming, and lock-bit configuration can be stored in any block. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the Read Array command. Block erase suspend allows system software to suspend a block erase to read or write data from any other block. Program suspend allows system software to suspend a program to read data from any other flash memory array location.

2.1 Data Protection

Depending on the application, the system designer may choose to make the V_{PP} power supply switchable or hardwired to $V_{PPH1/2}$. The device supports either design practice, and encourages optimization of the processor-memory interface.

When $V_{PP} \leq V_{PPLK}$, memory contents cannot be altered. When high voltage is applied to V_{PP}, the two-step block erase, program, or lock-bit configuration command sequences provide protection from unwanted operations. All write functions are disabled when V_{CC} voltage is below the write lockout voltage V_{LKO} or when RP# is at V_{IL}. The device's block locking capability provides additional protection from inadvertent code or data alteration.

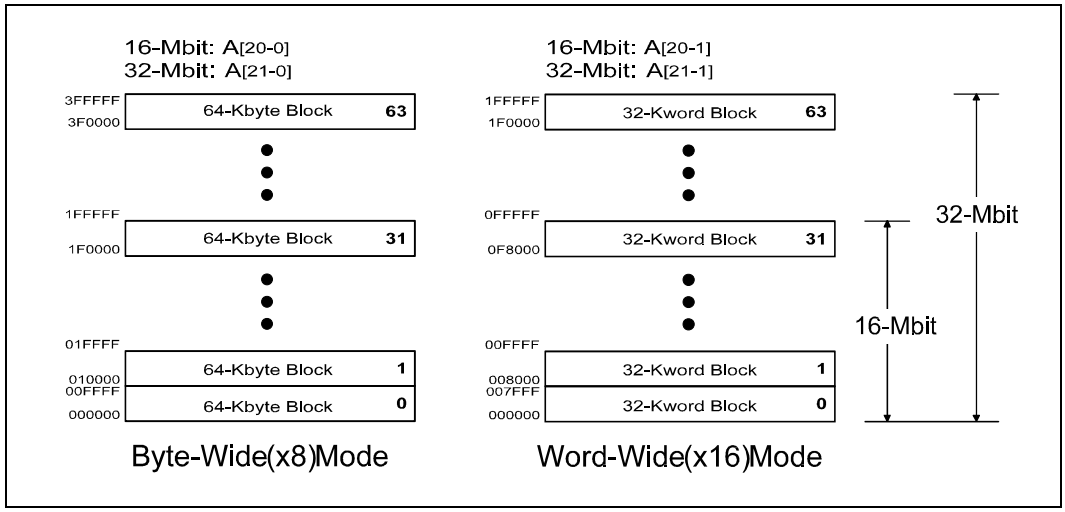


Figure 5. Memory Map

3.0 BUS OPERATION

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

3.1 Read

Block information, query information, identifier codes and Status Registers can be read independent of the V_{PP} voltage.

The first task is to place the device into the desired read mode by writing the appropriate read-mode command (Read Array, Query, Read Identifier Codes, or Read Status Register) to the CUI. Upon initial device power-up or after exit from deep power-down mode, the device automatically resets to read array mode. Control pins dictate the data flow in and out of the component. CE_0#, CE_1# and OE# must be driven active to obtain data at the outputs. CE_0# and CE_1# are the device selection controls, and, when both are active, enable the selected memory device. OE# is the data output (DQ_0–DQ_{15}) control: When active it drives the selected memory data onto the I/O bus. WE# must be at V_{IH} and RP# must be at V_{IH}. Figure 17 illustrates a read cycle.

3.2 Output Disable

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. Output pins DQ_0–DQ_{15} are placed in a high-impedance state.

3.3 Standby

CE_0# or CE_1# at a logic-high level (V_{IH}) places the device in standby mode, substantially reducing device power consumption. DQ_0–DQ_{15} (or DQ_0– DQ_7 in x8 mode) outputs are placed in a high-impedance state independent of OE#. If deselected during block erase, programming, or lock-bit configuration, the device continues functioning and consuming active power until the operation completes.

3.4 Deep Power-Down

RP# at V_{IL} initiates the deep power-down mode.

In read mode, RP#-low deselects the memory, places output drivers in a high-impedance state, and turns off all internal circuits. RP# must be held low for time t_{PLPH}. Time t_{PHQV} is required after return from power-down until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI resets to read array mode, and the Status Register is set to 80H.

During block erase, programming, or lock-bit configuration modes, RP#-low will abort the operation. STS in RY/BY# mode remains low until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially corrupted after programming or partially altered after an erase or lock-bit configuration. Time t_{PHWL} is required after RP# goes to logic-high (V_{IH}) before another command can be written.

It is important in any automated system to assert RP# during system reset. When the system comes out of reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during block erase, programming, or lock-bit configuration modes. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. Intel's Flash memories allow proper CPU initialization following a system reset through the use of the RP# input. In this application, RP# is controlled by the same RESET# signal that resets the system CPU.

3.5 Read Query Operation

The read query operation outputs block status, Common Flash Interface (CFI) ID string, system interface, device geometry, and Intel-specific extended query information.

3.6 Read Identifier Codes Operation

The read-identifier codes operation outputs the manufacturer code, device code, and block lock configuration codes for each block configuration (see Figure 6). Using the manufacturer and device codes, the system software can automatically match the device with its proper algorithms. The block-lock configuration codes identify each block's lock-bit setting.

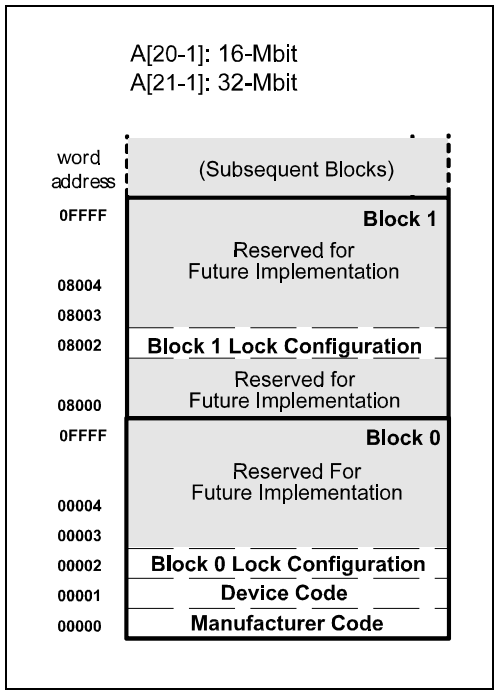


Figure 6. Device Identifier Code Memory Map

3.7 Write

Writing commands to the CUI enables reading of device data, query, identifier codes, inspection and clearing of the Status Register. Additionally, when $V_{PP} = V_{PPH1/2}$, block erasure, programming, and lock-bit configuration can also be performed.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Byte/Word Write command requires the command and address of the location to be written. Set Block Lock-Bit commands require the command and address within the block to be locked. The Clear Block Lock-Bits command requires the command and an address within the device.

The CUI does not occupy an addressable memory location. It is written when WE#, CE_0#, and CE_1# are active and OE# = V_{IH}. The address and data needed to execute a command are latched on the rising edge of WE# or CE_X# (CE_0#, CE_1#), whichever goes high first. Standard microprocessor write timings are used. Figure 18 illustrates a write operation.

4.0 COMMAND DEFINITIONS

V_{PP} voltage ≤ V_{PPLK} enables read operations from the Status Register, identifier codes, or memory blocks. Placing $V_{PPH1/2}$ on V_{PP} enables successful block erase, programming, and lock-bit configuration operations.

Device operations are selected by writing specific commands into the CUI. and Table 3 define these commands.

Table 2. Bus Operations

Mode	Notes	RP#	CE_0#	CE_1#	OE#(11)	WE#(11)	Address	V_{PP}	DQ(8)	STS(3)
Read	1,2	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	X	D_{OUT}	X
Output Disable		V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z	X
Standby		V_{IH}	V_{IL} V_{IH} V_{IH}	V_{IH} V_{IL} V_{IH}	X	X	X	X	High Z	X
Reset/Power-Down Mode	10	V_{IL}	X	X	X	X	X	X	High Z	High Z(9)
Read Identifier Codes	4	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	See Figure 6	X	D_{OUT}	High Z(9)
Read Query	5	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	See Table 6	X	D_{OUT}	High Z(9)
Write	3,6,7	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	$V_{PPH1/2}$	D_{IN}	X

NOTES:

1. Refer to Table 19. When $V_{PP} \le V_{PPLK}$, memory contents can be read, but not altered.
2. X can be V_{IL} or V_{IH} for control and address input pins and V_{PPLK} or $V_{PPH1/2}$ for V_{PP}. See Table 19, for V_{PPLK} and $V_{PPH1/2}$ voltages.
3. STS in level RY/BY# mode (default) is V_{OL} when the WSM is executing internal block erase, programming, or lock-bit configuration algorithms. It is V_{OH} when the WSM is not busy, in block erase suspend mode (with programming inactive), program suspend mode, or deep power-down mode.
4. See Section 4.3 for read identifier code data.
5. See Section 4.2 for read query data.
6. Command writes involving block erase, write, or lock-bit configuration are reliably executed when $V_{PP} = V_{PPH1/2}$ and $V_{CC} = V_{CC1/2}$ (see Section 6.2).
7. Refer to Table 3 for valid D_{IN} during a write operation.
8. DQ refers to $DQ_{0–7}$ if BYTE# is low and $DQ_{0–15}$ if BYTE# is high.
9. High Z will be V_{OH} with an external pull-up resistor.
10. RP# at GND ± 0.2V ensures the lowest deep power-down current.
11. OE# = V_{IL} and WE# = V_{IL} concurrently is an undefined state and should not be attempted.

Table 3. Word-Wide FlashFile™ Memory Command Set Definitions(13)

Command	Scaleable or Basic Command Set(14)	Bus Cycles Req'd	Notes	First Bus Cycle			Second Bus Cycle		
				Oper(1)	Addr(2)	Data(3,4)	Oper(1)	Addr(2)	Data(3,4)
Read Array	SCS/BCS	1		Write	X	FFH			
Read Identifier Codes	SCS/BCS	≥2	5	Write	X	90H	Read	IA	ID
Read Query	SCS	≥ 2		Write	X	98H	Read	QA	QD
Read Status Register	SCS/BCS	2		Write	X	70H	Read	X	SRD
Clear Status Register	SCS/BCS	1		Write	X	50H			
Write to Buffer	SCS	> 2	8, 9, 10	Write	BA	E8H	Write	BA	N
Word/Byte Program	SCS/BCS	2	6,7	Write	X	40H or 10H	Write	PA	PD
Block Erase	SCS/BCS	2	6,10	Write	X	20H	Write	BA	D0H
Block Erase, Word/Byte Program Suspend	SCS/BCS	1	6	Write	X	B0H			
Block Erase, Word/Byte Program Resume	SCS/BCS	1	6	Write	X	D0H			
STS pin Configuration	SCS	2		Write	X	B8H	Write	X	CC
Set Block Lock-Bit	SCS	2	11	Write	X	60H	Write	BA	01H
Clear Block Lock-Bits	SCS	2	12	Write	X	60H	Write	X	D0H
Full Chip Erase	SCS	2	10	Write	X	30H	Write	X	D0H

NOTES:

1. Bus operations are defined in Table 2.
2. X = Any valid address within the device.
   BA = Address within the block being erased or locked.
   IA = Identifier Code Address: see Table 12.
   QA = Query database Address.
   PA = Address of memory location to be programmed.
3. ID = Data read from Query database.
   SRD = Data read from Status Register. See Table 15 for a description of the Status Register bits.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of WE#.
   CC = Configuration Code. (See Table 14.)
4. The upper byte of the data bus (DQ_{8-15}) during command writes is a “Don’t Care” in x16 operation.
5. Following the Read Identifier Codes command, read operations access manufacturer, device, and block-lock codes. See Section 4.3 for read identifier code data.
6. If a block is locked (i.e., the block’s lock-bit is set to 0), WP# must be at V_{IH} in order to perform block erase, program and suspend operations. Attempts to issue a block erase, program and suspend operation to a locked block while WP# is V_L will fail.
7. Either 40H or 10H are recognized by the WSM as the byte/word program setup.
8. After the Write to Buffer command is issued, check the XSR to make sure a Write Buffer is available.
9. N = byte/word count argument such that the number of bytes/words to be written to the input buffer = N + 1. N = 0 is 1 byte/word length, and so on. Write to Buffer is a multi-cycle operation, where a byte/word count of N + 1 is written to the correct memory address (WA) with the proper data (WD). The Confirm command (D0h) is expected after exactly N + 1 write cycles; any other command at that point in the sequence aborts the buffered write. Writing a byte/word count outside the buffer boundary causes unexpected results and should be avoided.
10. The write to buffer, block erase, or full chip erase operation does not begin until a Confirm command (D0h) is issued. Confirm also reactivates suspended operations.
11. A block lock-bit can be set only while WP# is V_{IH}.
12. WP# must be at V_{IH} to clear block lock-bits. The clear block lock-bits operation simultaneously clears all block lock-bits.
13. Commands other than those shown above are reserved for future use and should not be used.
14. The Basic Command Set (BCS) is the same as the 28F008SA Command Set or Intel Standard Command Set. The Scaleable Command Set (SCS) is also referred to as the Intel Extended Command Set.

4.1 Read Array Command

Upon initial device power-up and after exit from deep power-down mode, the device defaults to read array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal WSM has started block erase, program, or lock-bit configuration, the device will not recognize the Read Array command until the WSM completes its operation—unless the WSM is suspended via an Erase-Suspend or Program-Suspend command. The Read Array command functions independently of the V_{PP} voltage.

4.2 Read Query Mode Command

This section defines the data structure or "database" returned by the Common Flash Interface (CFI) Query command. System software should parse this structure to gain critical information such as block size, density, x8/x16, and electrical specifications. Once this information has been obtained, the software will know which command sets to use to enable flash writes, block erases, and otherwise control the flash component. The Query is part of an overall specification for multiple command set and control interface descriptions called Common Flash Interface, or CFI.

4.2.1 QUERY STRUCTURE OUTPUT

The Query "database" allows system software to gain critical information for controlling the flash component. This section describes the device's CFI-compliant interface that allows the host system to access Query data.

Query data are always presented on the lowest-order data outputs (DQ_{0-7}) only. The numerical offset value is the address relative to the maximum bus width supported by the device. On this device, the Query table device starting address is a 10h word address, since the maximum bus width is x16.

For this word-wide (x16) device, the first two bytes of the Query structure, "Q" and "R" in ASCII, appear on the low byte at word addresses 10h and 11h. This CFI-compliant device outputs 00H data on upper bytes. Thus, the device outputs ASCII "Q" in the low byte (DQ_{0-7}) and 00h in the high byte (DQ_{8-15}).

Since the device is x8/x16 capable, the x8 data is still presented in word-relative (16-bit) addresses. However, the "fill data" (00h) is not the same as driven by the upper bytes in the x16 mode. As in x16 mode, the byte address (A_0) is ignored for Query output so that the "odd byte address" (A_0 high) repeats the "even byte address" data (A_0 low). Therefore, in x8 mode using byte addressing, the device will output the sequence "Q", "Q", "R", "R", "Y", "Y", and so on, beginning at byte-relative address 20h (which is equivalent to word offset 10h in x16 mode).

At Query addresses containing two or more bytes of information, the least significant data byte is presented at the lower address, and the most significant data byte is presented at the higher address.

Table 4. Summary of Query Structure Output as a Function of Device and Mode

Device Type/Mode	Word Addressing		Byte Addressing	
	Location	Query Data Hex, ASCII	Location	Query Data Hex, ASCII
x16 device/ x16 mode	10h 11h 12h	0051h “Q” 0052h “R” 0059h “Y”	20h 21h 22h	51h “Q” 00h null 52h “R”
x16 device/ x8 mode	N/A(1)	N/A	20h 21h 22h	51h “Q” 51h “Q” 52h “R”

NOTE:

1. The system must drive the lowest order addresses to access all the device’s array data when the device is configured in x8 mode. Therefore, word addressing where lower addresses are not toggled by the system is“Not Applicable” for x8-configured devices.

Table 5. Example of Query Structure Output of a x16- and x8-Capable Device

Device Address	Word Addressing: Query Data	Byte Address	Byte Addressing: Query Data
A_{16}–A_1	D_{15}–D_0	A_7–A_0	D_7–D_0
0010h 0011h 0012h 0013h 0014h 0015h 0016h 0017h 0018h ...	0051h “Q” 0052h “R” 0059h “Y” P_ID_{LO} PrVendor P_ID_{HI} ID # P_{LO} PrVendor P_{HI} TblAdr A_ID_{LO} AltVendor A_ID_{HI} ID # ...	20h 21h 22h 23h 24h 25h 26h 27h 28h ...	51h “Q” 51h “Q” 52h “R” 52h “R” 59h “Y” 59h “Y” P_ID_{LO} PrVendor P_ID_{LO} ID # P_ID_{HI} “ ...

4.2.2 QUERY STRUCTURE OVERVIEW

The Query command causes the flash component to display the Common Flash Interface (CFI) Query structure or “database.” The structure sub-sections and address locations are summarized in Table 8.

The following sections describe the Query structure sub-sections in detail.

Table 6. Query Structure(1)

Offset	Sub-Section Name	Description
00h		Manufacturer Code
01h		Device Code
(BA+2)h(2)	Block Status Register	Block-specific information
04-0Fh	*Reserved*	*Reserved for vendor-specific information*
10h	CFI Query Identification String	Command set ID and vendor data offset
1Bh	System Interface Information	Device timing & voltage information
27h	Device Geometry Definition	Flash device layout
P(3)	Primary Intel-Specific Extended Query Table	Vendor-defined additional information specific to the Primary Vendor Algorithm

NOTES:

1. Refer to Section 4.2.1 and Table 4 for the detailed definition of offset address as a function of device word width and mode.
2. BA = The beginning location of a Block Address (i.e., 08000h is the beginning location of block 1 when the block size is 32 Kword).
3. Offset 15 defines “P” which points to the Primary Intel-specific Extended Query Table.

4.2.3 BLOCK STATUS REGISTER

The Block Status Register indicates whether an erase operation completed successfully or whether a given block is locked or can be accessed for flash program/erase operations.

Block Erase Status (BSR.1) allows system software to determine the success of the last block erase operation. BSR.1 can be used just after power-up to verify that the V_{CC} supply was not accidentally removed during an erase operation. This bit is only reset by issuing another erase operation to the block. The Block Status Register is accessed from word address 02h within each block.

Table 7. Block Status Register

Offset	Length (bytes)	Description	28F320S3/ 28F160S3 x16 Device/Mode
(BA+2)h(1)	01h	Block Status Register	BA+2: 0000h or 0001h
		BSR.0 = Block Lock Status 1 = Locked 0 = Unlocked	BA+2 (bit 0): 0 or 1
		BSR.1 = Block Erase Status 1 = Last erase operation did not complete successfully 0 = Last erase operation completed successfully	BA+2 (bit 1): 0 or 1
		BSR 2-7 Reserved for future use	BA+2 (bits 2-7): 0

NOTE:

1. BA = The beginning location of a Block Address (i.e., 008000h is the beginning location of block 1 in word mode.)

4.2.4 CFI QUERY IDENTIFICATION STRING

The Identification String provides verification that the component supports the Common Flash Interface specification. Additionally, it indicates which version of the specification and which vendor-specified command set(s) is (are) supported.

Table 8. CFI Identification

Offset	Length (Bytes)	Description	28F320S3/ 28F160S3
10h	03h	Query-Unique ASCII string “QRY“	10: 0051h 11: 0052h 12: 0059h
13h	02h	Primary Vendor Command Set and Control Interface ID Code 16-bit ID Code for Vendor-Specified Algorithms	13: 0001h 14: 0000h
15h	02h	Address for Primary Algorithm Extended Query Table Offset value = ***P*** = 31h	15: 0031h 16: 0000h
17h	02h	Alternate Vendor Command Set and Control Interface ID Code Second Vendor-Specified Algorithm Supported **Note: 0000h means none exists**	17: 0000h 18: 0000h
19h	02h	Address for Secondary Algorithm Extended Query Table **Note: 0000h means none exists**	19: 0000h 1A: 0000h

4.2.5 SYSTEM INTERFACE INFORMATION

The following device information can be useful in optimizing system interface software.

Table 9. System Interface Information

Offset	Length (bytes)	Description	28F320S3/ 28F160S3
1Bh	01h	V_{CC} Logic Supply Minimum Program/Erase Voltage bits 7–4 BCD volts bits 3–0 BCD 100 mv	1B: 0030h
1Ch	01h	V_{CC} Logic Supply Maximum Program/Erase Voltage bits 7–4 BCD volts bits 3–0 BCD 100 mv	1C: 0055h
1Dh	01h	V_{PP} [Programming] Supply Minimum Program/Erase Voltage bits 7–4 HEX volts bits 3–0 BCD 100 mv	1D: 0030h
1Eh	01h	V_{PP} [Programming] Supply Maximum Program/Erase Voltage bits 7–4 HEX volts bits 3–0 BCD 100 mv	1E: 0055h
1Fh	01h	Typical Time-Out per Single Byte/Word Program, 2^N µ-sec	1F: 0003h
20h	01h	Typical Time-Out for Max. Buffer Write, 2^N µ-sec	20: 0006h
21h	01h	Typical Time-Out per Individual Block Erase, 2^N m-sec	21: 000Ah
22h	01h	Typical Time-Out for Full Chip Erase, 2^N m-sec	22: 000Fh
23h	01h	Maximum Time-Out for Byte/Word Program, 2^N Times Typical	23: TBD
24h	01h	Maximum Time-Out for Buffer Write, 2^N Times Typical	24: TBD
25h	01h	Maximum Time-Out per Individual Block Erase, 2^N Times Typical	25: TBD
26h	01h	Maximum Time-Out for Chip Erase, 2^N Times Typical	26: TBD

4.2.6 DEVICE GEOMETRY DEFINITION

This field provides critical details of the flash device geometry.

Table 10. Device Geometry Definition

Offset	Length (bytes)	Description	28F320S3/ 28F160S3
27h	01h	Device Size = 2^N in Number of Bytes	27: 0015h (16Mb) 27: 0016h (32Mb)
28h	02h	Flash Device Interface Description value meaning 0002h x8/x16 asynchronous	28: 0002h 29: 0000h
2Ah	02h	Maximum Number of Bytes in Write Buffer = 2^N	2A: 0005h 2B: 0000h
2Ch	01h	Number of Erase Block Regions within Device: **bits 7–0 = x** = # of Erase Block Regions	2C: 0001h
2Dh	04h	Erase Block Region Information **bits 15–0 = y**, Where y+1 = Number of Erase Blocks of Identical Size within Region **bits 31–16 = z**, Where the Erase Block(s) within This Region are (z) × 256 Bytes	y: 32 Blk (16Mb) 2D: 001Fh 2E: 0000h y: 64 Blk (32Mb) 2D: 003Fh 2E: 0000h z: 64-KB 2F: 0000h 30: 0001h

4.2.7 INTEL-SPECIFIC EXTENDED QUERY TABLE

Certain flash features and commands are optional. The Intel-Specific Extended Query table specifies this and other similar types of information.

Table 11. Primary-Vendor Specific Extended Query

Offset(1)	Length (bytes)	Description	Data
(P)h	03h	Primary Extended Query Table Unique ASCII String “PRI“	31: 0050h 32: 0052h 33: 0049h
(P+3)h	01h	Major Version Number, ASCII	34: 0031h
(P+4)h	01h	Minor Version Number, ASCII	35: 0030h
(P+5)h	04h	Optional Feature & Command Support bit 0 Chip Erase Supported (**1=yes**, 0=no) bit 1 Suspend Erase Supported (**1=yes**, 0=no) bit 2 Suspend Program Supported (**1=yes**, 0=no) bit 3 Lock/Unlock Supported (**1=yes**, 0=no) bit 4 Queued Erase Supported (1=yes, **0=no**) *bits 5–31 Reserved for future use; undefined bits are “0”*	36: 000Fh 37: 0000h 38: 0000h 39: 0000h
(P+9)h	01h	Supported Functions after Suspend Read Array, Status, and Query are always supported during suspended Erase or Program operation. This field defines other operations supported. bit 0 Program Supported after Erase Suspend (**1=yes**, 0=no) *bits 1-7 Reserved for future use; undefined bits are “0”*	3A: 0001h
(P+A)h	02h	Block Status Register Mask Defines which bits in the Block Status Register section of Query are implemented. bit 0 Block Status Register Lock-Bit [BSR.0] active (**1=yes**, 0=no) bit 1 Block Erase Status Bit [BSR.1] active (**1=yes**, 0=no) *bits 2-15 Reserved for future use; undefined bits are “0”*	3B: 0003h 3C: 0000h

NOTES:

1. The variable P is a pointer which is defined at offset 15h in Table 8.

Table 11. Primary-Vendor Specific Extended Query (Continued)

Offset	Length (bytes)	Description	Data
(P+C)h	01h	V_{CC} Logic Supply Optimum Program/Erase voltage (highest performance) bits 7–4 BCD value in volts bits 3–0 BCD value in 100 mv	3D: 0050h
(P+D)h	01h	V_{PP} [Programming] Supply Optimum Program/Erase voltage bits 7–4 HEX value in volts bits 3–0 BCD value in 100 mv	3E: 0050h
(P+E)h	*reserved*	*Reserved for future use*	

Table 12. Identifier Codes

Code		Address(2)	Data
Manufacturer Code		000000	B0
Device Code	16 Mbit	000001	D0
	32 Mbit	000001	D4
Block Lock Configuration		x0002(1)	
• Block is Unlocked			$DQ_0 = 0$
• Block is Locked			$DQ_0 = 1$
• Reserved for Future Use			DQ_{2-7}
Block Erase Status		x0002(1)	
• Last erase completed successfully			$DQ_1 = 0$
• Last erase did not complete successfully			$DQ_1 = 1$
• Reserved for Future Use			DQ_{2-7}

NOTES:

1. X selects the specific block lock configuration code. See Figure 6 for the device identifier code memory map.
2. A_0 should be ignored in this address. The lowest order address line is A_1 in both word and byte mode.

4.3 Read Identifier Codes Command

The identifier code operation is initiated by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Figure 6 retrieve the manufacturer, device, block lock configuration, and block erase status codes (see Table 12 for identifier code values). To terminate the operation, write another valid command. Like the Read Array command, the Read Identifier Codes command functions independently of the V_{PP} voltage. Following the Read Identifier Codes command, the information in Table 12 can be read.

4.4 Read Status Register Command

The Status Register may be read to determine when programming, block erasure, or lock-bit configuration is complete and whether the operation completed successfully. It may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the Status Register until another valid command is written. The Status Register contents are latched on the falling edge of OE#, CE_0#, or CE_1# whichever occurs last. OE# or CE_X# must toggle to V_{IH} to update the Status Register latch. The Read Status Register command functions independently of the V_{PP} voltage.

Following a program, block erase, set block lock-bit, or clear block lock-bits command sequence, only SR.7 is valid until the Write State Machine completes or suspends the operation. Device I/O pins DQ_{0-6} and DQ_{8-15} are invalid. When the operation completes or suspends (SR.7 = 1), all contents of the Status Register are valid when read.

The eXtended Status Register (XSR) may be read to determine Write Buffer availability (see Table 16). The XSR may be read at any time by writing the Write to Buffer command. After writing this command, all subsequent read operations output data from the XSR, until another valid command is written. The contents of the XSR are latched on the falling edge of OE# or CE_X# whichever occurs last in the read cycle. Write to buffer command must be re-issued to update the XSR latch.

4.5 Clear Status Register Command

Status Register bits SR.5, SR.4, SR.3, and SR.1 are set to "1"s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 15). By allowing system software to reset these bits, several operations (such as cumulatively erasing or locking multiple blocks or programming several bytes/words in sequence) may be performed. The Status Register may be polled to determine if an error occurred during the sequence.

To clear the Status Register, the Clear Status Register command is written. It functions independently of the applied V_{PP} voltage. This command is not functional during block erase or program suspend modes.

4.6 Block Erase Command

Block Erase is executed one block at a time and initiated by a two-cycle command. A Block Erase Setup command is written first, followed by a Confirm command. This command sequence requires appropriate sequencing and an address within the block to be erased (erase changes all block data to FFH). Block preconditioning, erase, and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs Status Register data when read (see Figure 10). The CPU can detect block erase completion by analyzing STS in level RY/BY# mode or Status Register bit SR.7. Toggle OE#, CE_0#, or CE_1# to update the Status Register.

When the block erase is complete, Status Register bit SR.5 should be checked. If a block erase error is detected, the Status Register should be cleared before system software attempts corrective actions. The CUI remains in read Status Register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both Status Register bits SR.4 and SR.5 being set to "1." Also, reliable block erasure can only occur when $V_{CC} = V_{CC1/2}$ and $V_{PP} = V_{PPH1/2}$. In the absence of these voltages, block contents are protected against erasure. If block erase is attempted while $V_{PP} \leq V_{PPLK}$, SR.3 and SR.5 will be set to "1." Successful block erase requires that the corresponding block lock-bit be cleared, or WP# = V_{IH}. If block erase is attempted when the corresponding block lock-bit is set and WP# = V_{IL}, the block erase will fail and SR.1 and SR.5 will be set to "1."

4.7 Full Chip Erase Command

The Full Chip Erase command followed by a Confirm command erases all unlocked blocks. After the Confirm command is written, the device erases all unlocked blocks from block 0 to block 31 (or 63) sequentially. Block preconditioning, erase, and verify are handled internally by the WSM. After the Full Chip Erase command sequence is written to the CUI, the device automatically outputs the Status Register data when read. The CPU can detect full chip erase completion by polling the STS pin in level RY/BY# mode or Status Register bit SR.7.

When the full chip erase is complete, Status Register bit SR.5 should be checked to see if the operation completed successfully. If an erase error occurred, the Status Register should be cleared before issuing the next command. The CUI remains in read Status Register mode until a new command is issued. If an error is detected while erasing a block during a full chip erase operation, the WSM skips the remaining cells in that block and proceeds to erase the next block. Reading the block valid status code by issuing the Read Identifier Codes command or Query command informs the user of which block(s) failed to erase.

This two-step command sequence of setup followed by execution ensures that block contents are not accidentally erased. An invalid Full Chip Erase command sequence will result in both Status Register bits SR.4 and SR.5 being set to 1. Also, reliable full chip erasure can only occur when $V_{CC} = V_{CC1/2}$ and $V_{PP} = V_{PPH1/2}$. In the absence of these voltages, block contents are protected against erasure. If full chip erase is attempted while $V_{PP} \leq V_{PPLK}$, SR.3 and SR.5 will be set to 1. When WP# = V_{IL}, only unlocked blocks are erased. Full chip erase cannot be suspended.

4.8 Write to Buffer Command

To program the flash device via the write buffers, a Write to Buffer command sequence is initiated. A variable number of bytes or words, up to the buffer size, can be written into the buffer and programmed to the flash device. First, the Write to Buffer setup command is issued along with the Block Address. At this point, the eXtended Status Register information is loaded and XSR.7 reverts to the "buffer available" status. If XSR.7 = 0, no write buffer is available. To retry, continue monitoring XSR.7 by issuing the Write to Buffer setup command with the Block Address until XSR.7 = 1. When XSR.7 transitions to a "1," the buffer is ready for loading.

Now a Word/Byte count is issued at an address within the block. On the next write, a device start address is given along with the write buffer data. For maximum programming performance and lower power, align the start address at the beginning of a Write Buffer boundary. Subsequent writes must supply additional device addresses and data, depending on the count. All subsequent addresses must lie within the start address plus the count.

After the final buffer data is given, a Write Confirm command is issued. This initiates the WSM to begin copying the buffer data to the flash memory. If a command other than Write Confirm is written to the device, an "Invalid Command/Sequence" error will be generated and Status Register bits SR.5 and SR.4 will be set to "1." For additional buffer writes, issue another Write to Buffer setup command and check XSR.7. The write buffers can be loaded while the WSM is busy as long as XSR.7 indicates that a buffer is available. Refer to Figure 7 for the Write to Buffer flowchart.

If an error occurs while writing, the device will stop programming, and Status Register bit SR.4 will be set to a "1" to indicate a program failure. Any time a media failure occurs during a program or an erase (SR.4 or SR.5 is set), the device will not accept any more Write to Buffer commands. Additionally, if the user attempts to write past an erase block boundary with a Write to Buffer command, the device will abort programming. This will generate an "Invalid Command/Sequence" error and Status Register bits SR.5 and SR.4 will be set to "1." To clear SR.4 and/or SR.5, issue a Clear Status Register command.

Reliable buffered programming can only occur when $V_{CC} = V_{CC1/2}$ and $V_{PP} = V_{PPH1/2}$. If programming is attempted while $V_{PP} \leq V_{PPLK}$, Status Register bits SR.4 and SR.5 will be set to "1." Programming attempts with invalid V_{CC} and V_{PP} voltages produce spurious results and should not be attempted. Finally, successful programming requires that the corresponding Block Lock-Bit be cleared, or WP# = V_{IH}. If a buffered write is attempted when the corresponding Block Lock-Bit is set and WP# = V_{IL}, SR.1 and SR.4 will be set to "1."

4.9 Byte/Word Program Commands

Byte/Word programming is executed by a two-cycle command sequence. Byte/Word Program setup (standard 40H or alternate 10H) is written, followed by a second write that specifies the address and data (latched on the rising edge of WE#). The WSM then takes over, controlling the program and verify algorithms internally. After the write sequence is written, the device automatically outputs Status Register data when read. The CPU can detect the completion of the program event by analyzing STS in level RY/BY# mode or Status Register bit SR.7.

When programming is complete, Status Register bit SR.4 should be checked. If a programming error is detected, the Status Register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully program to "0"s. The CUI remains in read Status Register mode until it receives another command. Refer to Figure 8 for the Word/Byte Program flowchart.

Also, Reliable byte/word programming can only occur when $V_{CC} = V_{CC1/2}$ and $V_{PP} = V_{PPH1/2}$. In the absence of this high voltage, contents are protected against programming. If a byte/word program is

attempted while $V_{PP} \leq V_{PPLK}$, Status Register bits SR.4 and SR.3 will be set to "1." Successful byte/word programming requires that the corresponding block lock-bit be cleared. If a byte/word program is attempted when the corresponding block lock-bit is set and WP# = V_{IL}, SR.1 and SR.4 will be set to "1."

4.10 STS Configuration Command

The Status (STS) pin can be configured to different states using the STS pin Configuration command. Once the STS pin has been configured, it remains in that configuration until another configuration command is issued or RP# is low. Initially, the STS pin defaults to level RY/BY# operation where STS low indicates that the state machine is busy. STS high indicates that the state machine is ready for a new operation or suspended.

To reconfigure the Status (STS) pin to other modes, the STS pin Configuration command is issued followed by the desired configuration code. The three alternate configurations are all pulse mode for use as a system interrupt as described in Table 14. For these configurations, bit 0 controls Erase Complete interrupt pulse, and bit 1 controls Write Complete interrupt pulse. When the device is configured in one of the pulse modes, the STS pin pulses low with a typical pulse width of 250 ns. Supplying the 00h configuration code with the Configuration command resets the STS pin to the default RY/BY# level mode. Refer to Table 14 for configuration coding definitions. The Configuration command may only be given when the device is not busy or suspended. Check SR.7 for device status. An invalid configuration code will result in both Status Register bits SR.4 and SR.5 being set to "1."

4.11 Block Erase Suspend Command

The Block Erase Suspend command allows block-erase interruption to read or program data in another block of memory. Once the block erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. The device outputs Status Register data when read after the Block Erase Suspend command is written. Polling Status Register bit SR.7 can determine when the block erase operation has been suspended. When SR.7 = 1, SR.6 should also be set to "1," indicating that the device is in the erase suspend mode. STS in level RY/BY# mode will also transition to V_{OH}. Specification t_{WHRH2} defines the block erase suspend latency.

At this point, a Read Array command can be written to read data from blocks other than that which is suspended. A Program command sequence can also be issued during erase suspend to program data in other blocks. Using the Program Suspend command (see Section 4.12), a program operation can also be suspended. During a program operation with block erase suspended, Status Register bit SR.7 will return to "0" and STS in RY/BY# mode will transition to V_{OL}. However, SR.6 will remain "1" to indicate block erase suspend status.

The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and STS in RY/BY# mode will return to V_{OL}. After the Erase Resume command is written, the device automatically outputs Status Register data when read (see Figure 11). V_{PP} must remain at $V_{PPH1/2}$ and V_{CC} must remain at $V_{CC1/2}$ (the same V_{PP} and V_{CC} levels used for block erase) while block erase is suspended. RP# must also remain at V_{IH} (the same RP# level used for block erase). Block erase cannot resume until program operations initiated during block erase suspend have completed.

4.12 Program Suspend Command

The Program Suspend command allows program interruption to read data in other flash memory locations. Once the programming process starts, writing the Program Suspend command requests that the WSM suspend the program sequence at a predetermined point in the algorithm. The device continues to output Status Register data when read after the Program Suspend command is written. Polling Status Register bits SR.7 can determine when the programming operation has been suspended. When SR.7 = 1, SR.2 should also be set to "1", indicating that the device is in the program suspend mode. STS in level RY/BY# mode will also transition to V_{OH}. Specification t_{WHRH1} defines the program suspend latency.

At this point, a Read Array command can be written to read data from locations other than that which is suspended. The only other valid commands while programming is suspended are Read Status Register and Program Resume. After a Program Resume command is written, the WSM will continue the programming process. Status Register bits SR.2 and SR.7 will automatically clear and STS in RY/BY# mode will return to V_{OL}. After the Program Resume command is written, the device automatically outputs Status Register data when read. V_{PP} must remain at $V_{PPH1/2}$ and V_{CC} must remain at $V_{CC1/2}$ (the same V_{PP} and V_{CC} levels used for programming) while in program suspend mode. RP# must also remain at V_{IH} (the same RP# level used for programming). Refer to Figure 9 for the Program Suspend/Resume flowchart.

4.13 Set Block Lock-Bit Command

A flexible block locking and unlocking scheme is enabled via a combination of block lock-bits. The block lock-bits gate program and erase operations. With WP# = V_{IH}, individual block lock-bits can be set using the Set Block Lock-Bit command.

Set block lock-bit is initiated using a two-cycle command sequence. The Set Block Lock-Bit setup along with appropriate block or device address is written followed by the Set Block Lock-Bit Confirm and an address within the block to be locked. The WSM then controls the set lock-bit algorithm. After the sequence is written, the device automatically outputs Status Register data when read. The CPU can detect the completion of the set lock-bit event by analyzing STS in level RY/BY# mode or Status Register bit SR.7.

When the set lock-bit operation is complete, Status Register bit SR.4 should be checked. If an error is detected, the Status Register should be cleared. The CUI will remain in read Status Register mode until a new command is issued.

This two-step sequence of setup followed by execution ensures that lock-bits are not accidentally set. An invalid Set Block Lock-Bit command will result in Status Register bits SR.4 and SR.5 being set to “1.” Also, reliable operations occur only when V_{CC} = $V_{CC1/2}$ and V_{PP} = $V_{PPH1/2}$. In the absence of these voltages, lock-bit contents are protected against alteration.

A successful set block lock-bit operation requires that WP# = V_{IH}. If it is attempted with WP# = V_{IL}, the operation will fail and SR.1 and SR.4 will be set to “1.” See Table 13 for write protection alternatives. Refer to Figure 12 for the Set Block Lock-Bit flowchart.

4.14 Clear Block Lock-Bits Command

All set block lock-bits are cleared in parallel via the Clear Block Lock-Bits command. This command is valid only when WP# = V_{IH}.

The clear block lock-bits operation is initiated using a two-cycle command sequence. A Clear Block Lock-Bits setup command is written followed by a Confirm command. Then, the device automatically outputs Status Register data when read (see Figure 13). The CPU can detect completion of the clear block lock-bits event by analyzing STS in level RY/BY# mode or Status Register bit SR.7.

This two-step sequence of set-up followed by execution ensures that block lock-bits are not accidentally cleared. An invalid Clear Block Lock-Bits command sequence will result in Status Register bits SR.4 and SR.5 being set to “1.” Also, a reliable clear block lock-bits operation can only occur when V_{CC} = $V_{CC1/2}$ and V_{PP} = $V_{PPH1/2}$. If a clear block lock-bits operation is attempted while $V_{PP} \le V_{PPLK}$, SR.3 and SR.5 will be set to “1.” In the absence of these voltages, the block lock-bits contents are protected against alteration. A successful clear block lock-bits operation requires that WP# = V_{IH}.

If a clear block lock-bits operation is aborted due to V_{PP} or V_{CC} transitioning out of valid range or RP# or WP# active transition, block lock-bit values are left in an undetermined state. A repeat of clear block lock-bits is required to initialize block lock-bit contents to known values.

When the operation is complete, Status Register bit SR.5 should be checked. If a clear block lock-bit error is detected, the Status Register should be cleared. The CUI will remain in read Status Register mode until another command is issued.

Table 13. Write Protection Alternatives

Operation	Block Lock-Bit	WP#	Effect
Program and Block Erase	0	V_{IL} or V_{IH}	Block erase and programming enabled
	1	V_{IL}	Block is locked. Block erase and programming disabled
		V_{IH}	Block Lock-Bit override. Block erase and programming enabled
Full Chip Erase	0,1	V_{IL}	All unlocked blocks are erased
	X	V_{IH}	Block Lock-Bit override. All blocks are erased
Set or Clear Block Lock-Bit	X	V_{IL}	Set or clear block lock-bit disabled
		V_{IH}	Set or clear block lock-bit enabled

Table 14. Configuration Coding Definitions

Reserved	Pulse on Write Complete	Pulse on Erase Complete
bits 7–2	bit 1	bit 0

DQ7–DQ2 = Reserved

DQ1/DQ0 = STS Pin Configuration Codes

00 = default, level mode RY/BY# (device ready) indication

01 = pulse on Erase complete

10 = pulse on Flash Program complete

11 = pulse on Erase or Program Complete

Configuration Codes 01b, 10b, and 11b are all pulse mode such that the STS pin pulses low then high when the operation indicated by the given configuration is completed.

Configuration Command Sequences for STS pin configuration (masking bits D7–D2 to 00h) are as follows:

Default RY/BY# level mode B8h, 00h
ER INT (Erase Interrupt): B8h, 01h
Pulse-on-Erase Complete
PR INT (Program Interrupt): B8h, 02h
Pulse-on-Flash-Program Complete
ER/PR INT (Erase or Program Interrupt): B8h, 03h
Pulse-on-Erase or Program Complete

DQ7–DQ2 are reserved for future use.

default (DQ1/DQ0 = 00) RY/BY#, level mode —used to control HOLD to a memory controller to prevent accessing a flash memory subsystem while any flash device's WSM is busy.

configuration 01 ER INT, pulse mode(1) —used to generate a system interrupt pulse when any flash device in an array has completed a block erase or sequence of queued block erases. Helpful for reformatting blocks after file system free space reclamation or 'cleanup'

configuration 10 PR INT, pulse mode(1) —used to generate a system interrupt pulse when any flash device in an array has complete a program operation. Provides highest performance for servicing continuous buffer write operations.

configuration ER/PR INT, pulse mode(1) —used to generate system interrupts to trigger servicing of flash arrays when either erase or flash program operations are completed when a common interrupt service routine is desired.

NOTE:

1. When the device is configured in one of the pulse modes, the STS pin pulses low with a typical pulse width of 250 ns.

Table 15. Status Register Definition

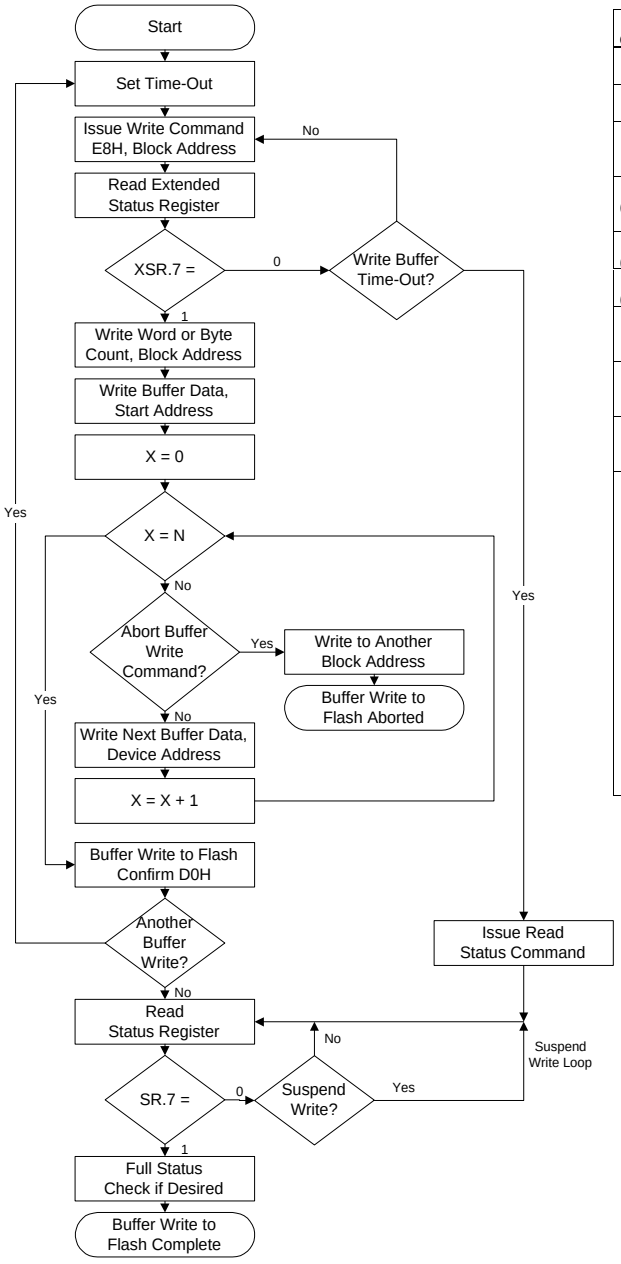
WSMS	ESS	ECLBS	BWSLBS	VPPS	BWSS	DPS	R
7	6	5	4	3	2	1	0

	NOTES:
SR.7 = WRITE STATE MACHINE STATUS 1 = Ready 0 = Busy	Check STS in RY/BY# mode or SR.7 to determine block erase, programming, or lock-bit configuration completion. SR.6-0 are invalid while SR.7 = "0."
SR.6 = ERASE SUSPEND STATUS 1 = Block erase suspended 0 = Block erase in progress/completed	
SR.5 = ERASE AND CLEAR LOCK-BITS STATUS 1 = Error in block erasure or clear lock-bits 0 = Successful block erase or clear lock-bits	If both SR.5 and SR.4 are "1"s after a block erase or lock-bit configuration attempt, an improper command sequence was entered.
SR.4 = PROGRAM AND SET LOCK-BIT STATUS 1 = Error in program or block lock-bit 0 = Successful program or set block lock-bit	
SR.3 = V_{PP} STATUS 1 = V_{PP} low detect, operation abort 0 = V_{PP} OK	SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after a block erase, program, or lock-bit configuration operation. SR.3 reports accurate feedback only when $V_{PP} = V_{PPH1/2}$.
SR.2 = PROGRAM SUSPEND STATUS 1 = Program suspended 0 = Program in progress/completed	
SR.1 = DEVICE PROTECT STATUS 1 = Block Lock-Bit and/or RP# lock detected, operation abort 0 = Unlock	SR.1 does not provide a continuous indication of block lock-bit values. The WSM interrogates the block lock-bit, and WP# only after a block erase, program, or lock-bit configuration operation. It informs the system, depending on the attempted operation, if the block lock-bit is set.
SR.0 = RESERVED FOR FUTURE ENHANCEMENTS	SR.0 is reserved for future use and should be masked when polling the Status Register.

Table 16. Extended Status Register Definition

WBS	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

	NOTES:
XSR.7 = WRITE BUFFER STATUS 1 = Write to buffer available 0 = Write to buffer not available	After a Write to buffer command, XSR.7 indicates that another Write to buffer command is possible.
XSR.6 = RESERVED FOR FUTURE ENHANCEMENTS	SR.6–0 are reserved for future use and should be masked when polling the status register

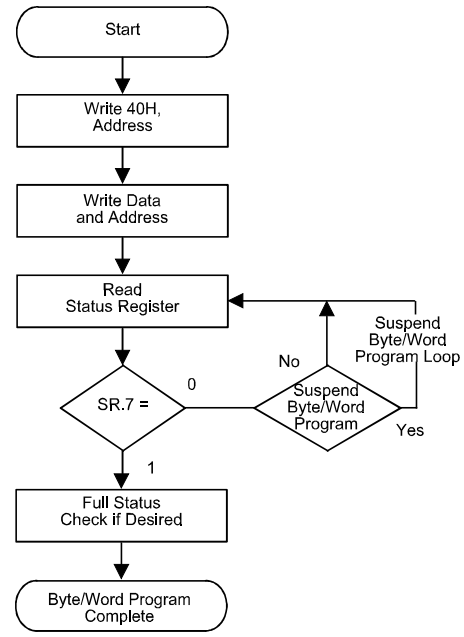


Bus Operation	Command	Comments
Write	Write to Buffer	Data = E8h Addr = Block Address
Read		XSR.7=valid Addr = X
Standby		Check XSR.7 1 = Write buffer available 0 = Write buffer not available
Write (Note 1, 2)		Data = N = word/byte count N = 0 corresponds to count = 1 Addr = Block Address
Write (Note 3, 4)		Data = write buffer data Addr = device start address
Write (Note 5, 6)		Data = write buffer data Addr = device address
Write	Buffer write to flash confirm	Data = D0h Addr = X
Read		Status Register data CE# & OE# low updates SR Addr = X
Standby		Check SR.7 1 = WSM ready 0 = WSM busy

1. Byte- or word-count values on DQ_{0-7} are loaded into the Count register.
2. The device now outputs the Status Register when read (XSR is no longer available).
3. Write Buffer contents will be programmed at the device start address or destination flash address.
4. Align the start address on a Write Buffer boundary for maximum programming performance.
5. The device aborts the Write to Buffer command if the current address is outside of the original block address.
6. The Status Register indicates an "improper command sequence" if the Write to Buffer command is aborted. Follow this with a Clear Status Register command.

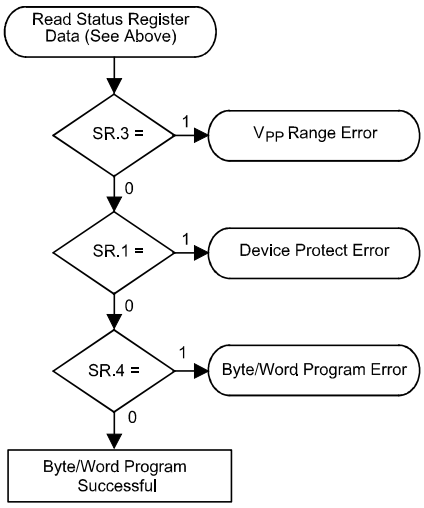
   Full status check can be done after all Erase and Write sequences complete. Write FFh after the last operation to reset the device to Read Array mode.

Figure 7. Write to Buffer Flowchart



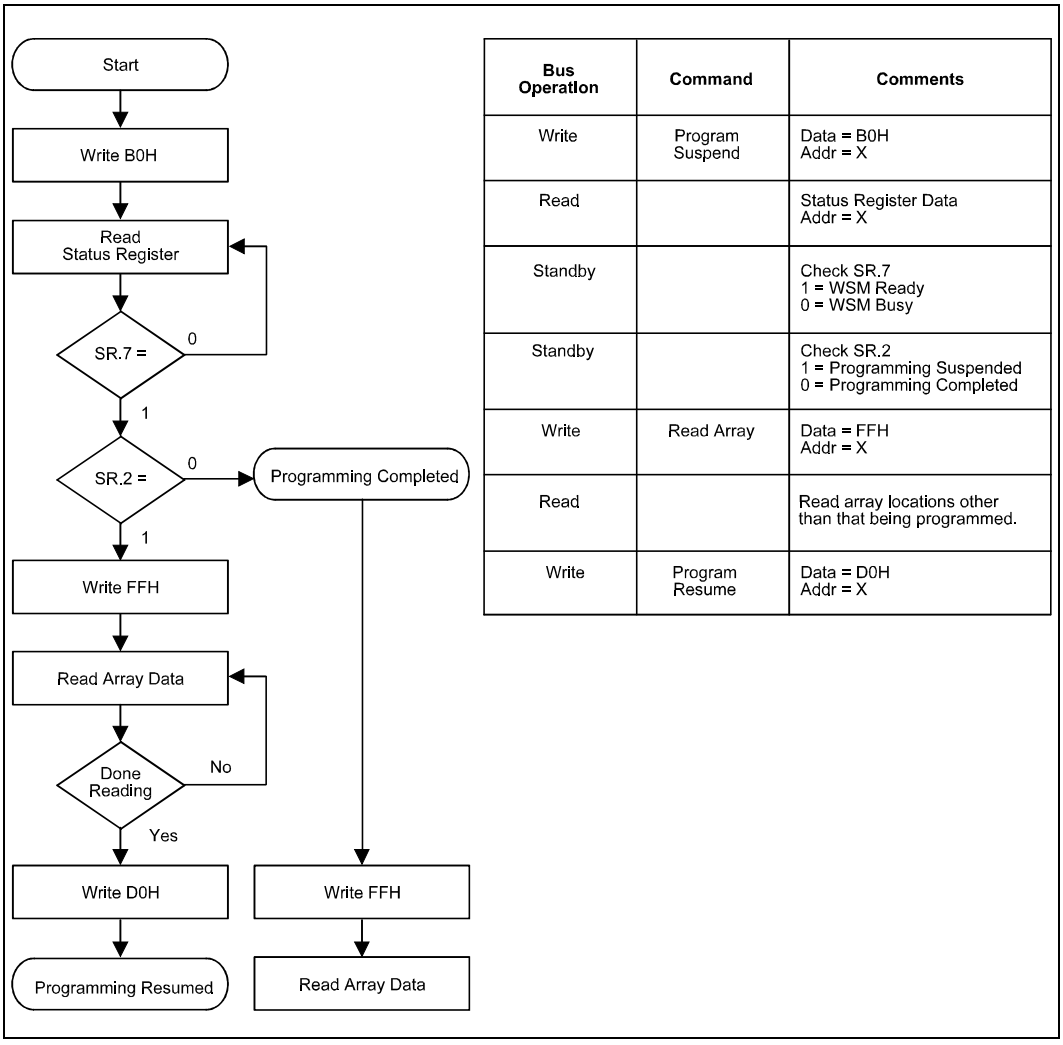
Bus Operation	Command	Comments
Write	Setup Byte/Word Program	Data = 40H Addr = Location to Be Written
Write	Byte/Word Program	Data = Data to Be Written Addr = Location to Be Written
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent byte/word programs Full status register check can be done after each byte/word program or after a sequence of byte/word programs. Write FFH after the last byte/word program operation to reset device to read array mode.		

FULL STATUS CHECK PROCEDURE



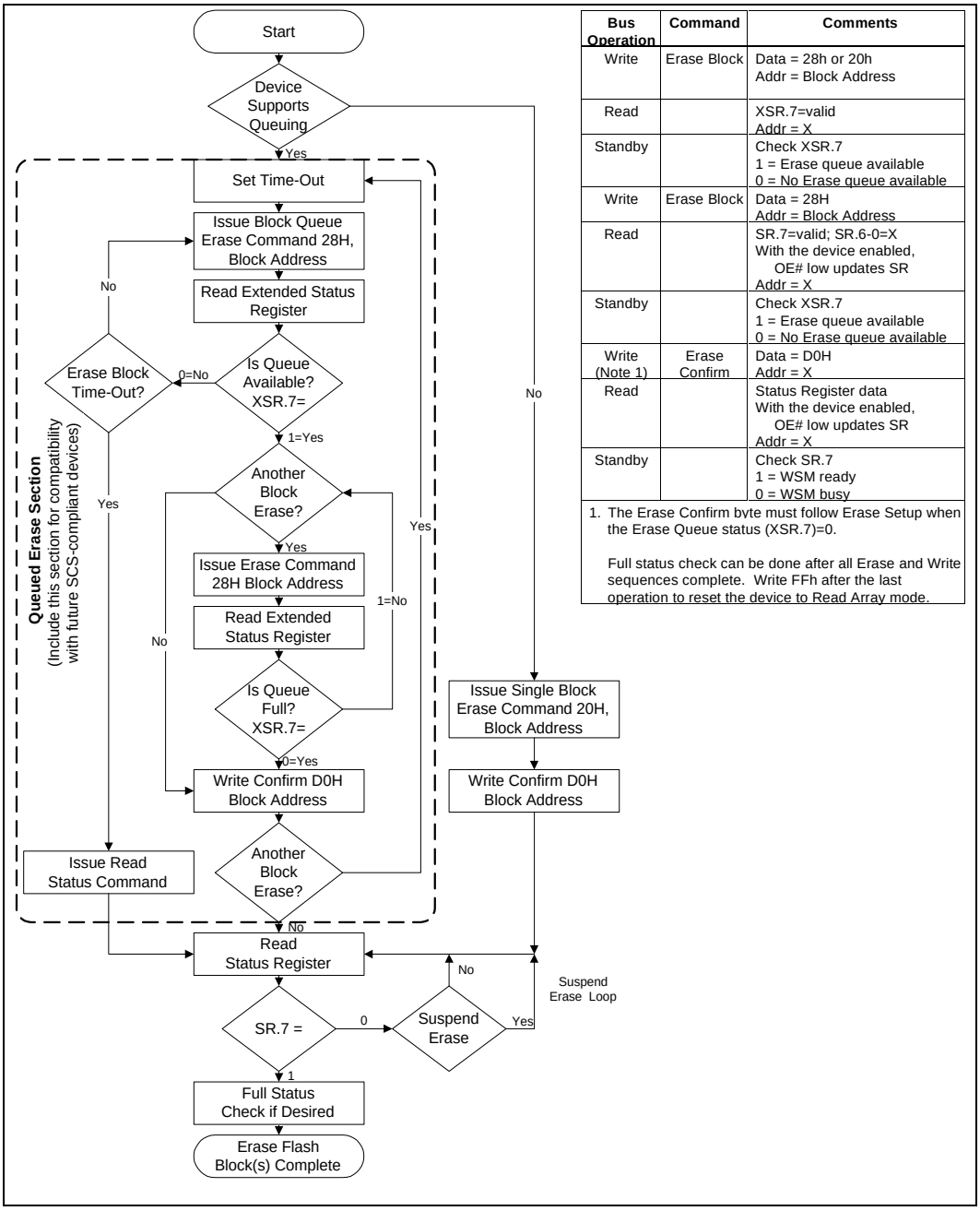
Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect RP# = V_{IH}, Block Lock-Bit Is Set Only required for systems implementing lock-bit configuration
Standby		Check SR.4 1 = Data Program Error
SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are programmed before full status is checked. If error is detected, clear the Status Register before attempting retry or other error recovery.		

Figure 8. Single Byte/Word Program Flowchart



Bus Operation	Command	Comments
Write	Program Suspend	Data = B0H Addr = X
Read		Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.2 1 = Programming Suspended 0 = Programming Completed
Write	Read Array	Data = FFH Addr = X
Read		Read array locations other than that being programmed.
Write	Program Resume	Data = D0H Addr = X

Figure 9. Program Suspend/Resume Flowchart

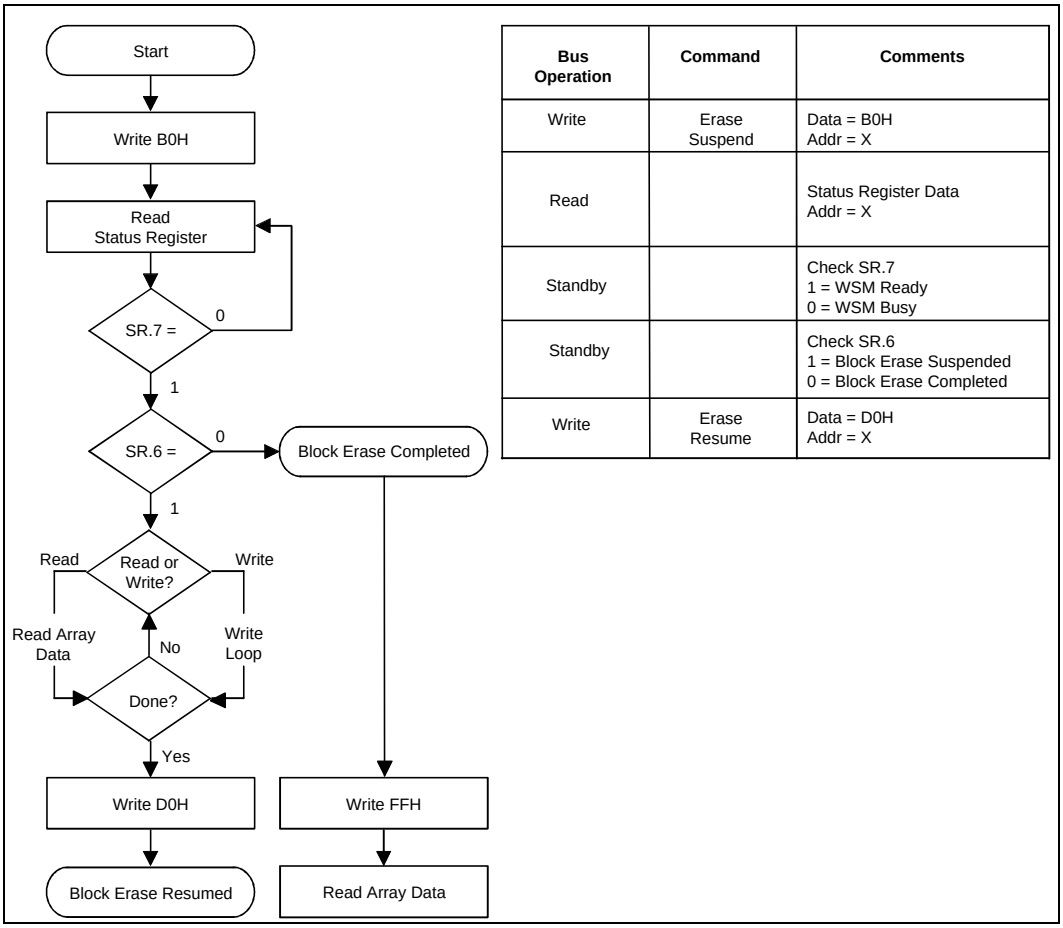


Bus Operation	Command	Comments
Write	Erase Block	Data = 28h or 20h Addr = Block Address
Read		XSR.7=valid Addr = X
Standby		Check XSR.7 1 = Erase queue available 0 = No Erase queue available
Write	Erase Block	Data = 28H Addr = Block Address
Read		SR.7=valid; SR.6-0=X With the device enabled, OE# low updates SR Addr = X
Standby		Check XSR.7 1 = Erase queue available 0 = No Erase queue available
Write (Note 1)	Erase Confirm	Data = D0H Addr = X
Read		Status Register data With the device enabled, OE# low updates SR Addr = X
Standby		Check SR.7 1 = WSM ready 0 = WSM busy

1. The Erase Confirm byte must follow Erase Setup when the Erase Queue status (XSR.7)=0.

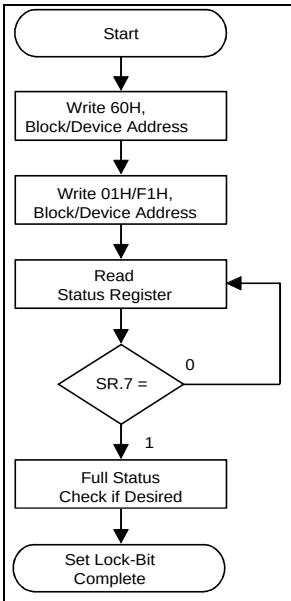
   Full status check can be done after all Erase and Write sequences complete. Write FFh after the last operation to reset the device to Read Array mode.

Figure 10. Block Erase Flowchart



Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0H Addr = X
Read		Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.6 1 = Block Erase Suspended 0 = Block Erase Completed
Write	Erase Resume	Data = D0H Addr = X

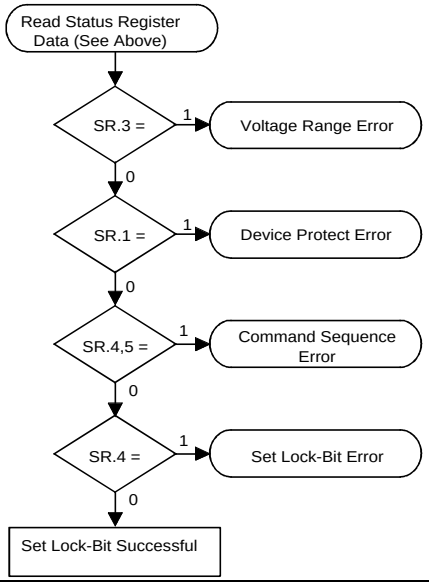
Figure 11. Block Erase Suspend/Resume Flowchart



Bus Operation	Command	Comments
Write	Set Block/Master Lock-Bit Setup	Data = 60H Addr = Block Address (Block), Device Address (Master)
Write	Set Block or Master Lock-Bit Confirm	Data = 01H (Block), F1H (Master) Addr = Block Address (Block), Device Address (Master)
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent lock-bit set operations.
Full status check can be done after each lock-bit set operation or after a sequence of lock-bit set operations.
Write FFH after the last lock-bit set operation to place device in read array mode.

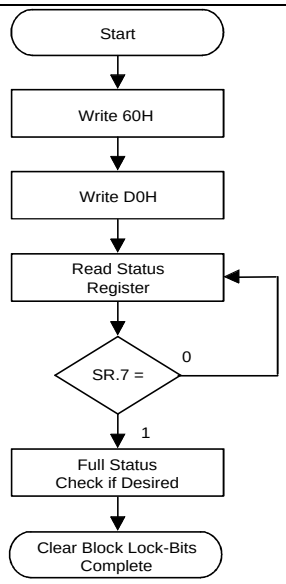
FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1 = Programming Voltage Error Detect
Standby		Check SR.1 1 = Device Protect Detect RST# = V_{IH} (Set Master Lock-Bit Operation) RST# = V_{IH}, Master Lock-Bit Is Set (Set Block Lock-Bit Operation)
Standby		Check SR.4,5 Both 1 = Command Sequence Error
Standby		Check SR.4 1 = Set Lock-Bit Error

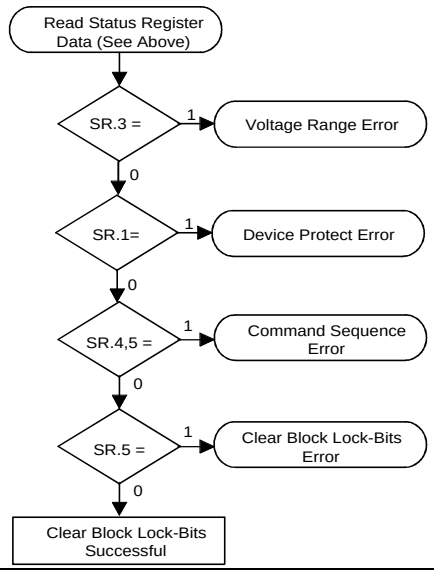
SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple lock-bits are set before full status is checked.
If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 12. Set Block Lock-Bit Flowchart



Bus Operation	Command	Comments
Write	Clear Block Lock-Bits Setup	Data = 60H Addr = X
Write	Clear Block Lock-Bits Confirm	Data = D0H Addr = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Write FFH after the Clear Block Lock-Bits operation to place device to read array mode.		

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1 = Programming Voltage Error Detect
Standby		Check SR.1 1 = Device Protect Detect RST# = V_{IH}, Master Lock-Bit Is Set
Standby		Check SR.4,5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Clear Block Lock-Bits Error
SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command. If error is detected, clear the Status Register before attempting retry or other error recovery.		

Figure 13. Clear Block Lock-Bits Flowchart

5.0 DESIGN CONSIDERATIONS

5.1 Three-Line Output Control

Intel provides three control inputs to accommodate multiple memory connections: CE_X# (CE_0#, CE_1#), OE#, and RP#. Three-line control provides for:

a. Lowest possible memory power dissipation;

b. Data bus contention avoidance.

To use these control inputs efficiently, an address decoder should enable CEx# while OE# should be connected to all memory devices and the system's READ# control line. This assures that only selected memory devices have active outputs, while de-selected memory devices are in standby mode. RP# should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should also toggle during system reset.

5.2 STS and WSM Polling

STS is an open drain output that should be connected to V_{CC} by a pull-up resistor to provide a hardware form of detecting block erase, program, and lock-bit configuration completion. In default mode, it transitions low during execution of these commands and returns to V_{OH} when the WSM has finished executing the internal algorithm. For alternate STS pin configurations, see Section 4.10. STS can be connected to an interrupt input of the system CPU or controller. It is active at all times. STS, in default mode, is also V_{OH} when the device is in block erase suspend (with programming inactive) or in reset/power-down mode.

5.3 Power Supply Decoupling

Flash memory power switching characteristics require careful device decoupling. Standby current levels, active current levels and transient peaks produced by falling and rising edges of CE_X# and OE# are areas of interest. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 µF ceramic capacitor connected between its V_{CC} and GND and V_{PP} and GND. These high-frequency, low-inductance capacitors should be placed as close as possible to package leads. Additionally, for every eight devices, a 4.7 µF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductance.

5.4 V_{PP} Trace on Printed Circuit Boards

Updating target-system resident flash memories requires that the printed circuit board designer pay attention to V_{PP} power supply traces. The V_{PP} pin supplies the memory cell current for programming and block erasing. Use similar trace widths and layout considerations given to the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

5.5 V_{CC}, V_{PP}, RP# Transitions

Block erase, program, and lock-bit configuration are not guaranteed if RP# ≠ V_{IH}, or if V_{PP} or V_{CC} fall outside of a valid voltage range ($V_{CC1/2}$ and $V_{PPH1/2}$). If V_{PP} error is detected, Status Register bit SR.3 and SR.4 or SR.5 are set to "1." If RP# transitions to V_{IL} during block erase, program, or lock-bit configuration, STS in level RY/BY# mode will remain low until the reset operation is complete. Then, the operation will abort and the device will enter deep power-down. Because the aborted operation may leave data partially altered, the command sequence must be repeated after normal operation is restored.

5.6 Power-Up/Down Protection

The device offers protection against accidental block erase, programming, or lock-bit configuration during power transitions.

A system designer must guard against spurious writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both WE# and CE_X# must be low for a command write, driving either input signal to V_{IH} will inhibit writes. The CUI's two-step command sequence architecture provides an added level of protection against data alteration.

In-system block lock and unlock renders additional protection during power-up by prohibiting block erase and program operations. RP# = V_{IL} disables the device regardless of its control inputs states.

6.0 ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings

NOTICE: This datasheet contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design

Temperature under Bias ..... –40°C to +85°C

Storage Temperature..... –65°C to +125°C

Voltage On Any Pin
(except V_{CC} and V_{PP})
..... –0.5V to + V_{CC} +0.5V(1)

V_{CC} Supply Voltage ..... –0.2V to + V_{CC}+0.5V(1)

V_{PP} Update Voltage during
Block Erase, Flash Write, and
Lock-Bit Configuration ..... –0.2V to +7.0V(2)

Output Short Circuit Current.....100 mA(3)

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:

1. All specified voltages are with respect to GND. Minimum DC voltage is –0.5V on input/output pins and –0.2V on V_{CC} and V_{PP} pins. During transitions, this level may undershoot to –2.0V for periods <20 ns. Maximum DC voltage on input/output pins and V_{CC} is V_{CC} +0.5V which, during transitions, may overshoot to V_{CC} +2.0V for periods <20 ns.
2. Maximum DC voltage on V_{PP} may overshoot to +7.0V for periods <20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.
4. Operating temperature is for extended product defined by this specification.

6.2 Operating Conditions

Table 17. Temperature and V_{CC} Operating Conditions(1)

Symbol	Parameter	Notes	Min	Max	Unit	Test Condition
T_A	Operating Temperature		-40	+85	℃	Ambient Temperature
V_{CC1}	V_{CC} Supply Voltage (2.7V to 3.6V)		2.7	3.6	V	
V_{CC2}	V_{CC} Supply Voltage (3.3V ± 0.3V)		3.0	3.6	V	

NOTES:

1. Device operations in the V_{CC} voltage ranges not covered in the table produce spurious results and should not be attempted.

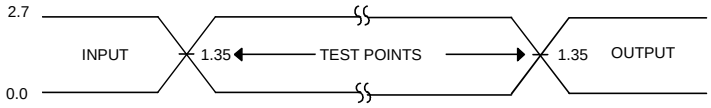
6.2.1 CAPACITANCE

Table 18. Capacitance(1), T_A = +25°C, f = 1 MHz

Symbol	Parameter	Typ	Max	Unit	Condition
C_{IN}	Input Capacitance	6	8	pF	V_{IN} = 0.0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0.0V

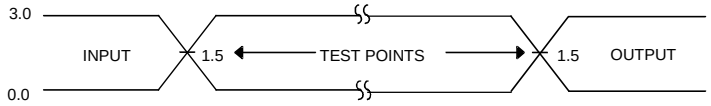
NOTE:
1. Sampled, not 100% tested.

6.2.2 AC INPUT/OUTPUT TEST CONDITIONS



AC test inputs are driven at 2.7V for a Logic "1" and 0.0V for a Logic "0." Input timing begins, and output timing ends, at 1.35V. Input rise and fall times (10% to 90%) <10 ns.

Figure 14. Transient Input/Output Reference Waveform for V_{CC} = 2.7V–3.6V



AC test inputs are driven at 3.0V for a Logic "1" and 0.0V for a Logic "0." Input timing begins, and output timing ends, at 1.5V. Input rise and fall times (10% to 90%) <10 ns.

Figure 15. Transient Input/Output Reference Waveform for V_{CC} = 3.3V ± 0.3V (High Speed Testing Configuration)

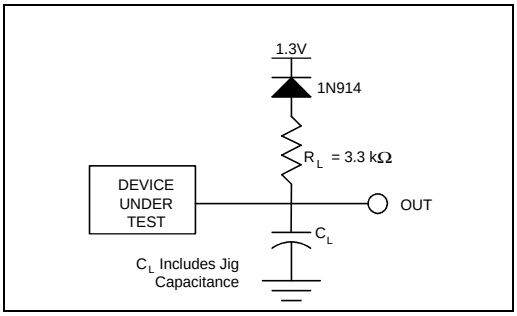


Figure 16. Transient Equivalent Testing Load Circuit

Test Configuration Capacitance Loading Value

Test Configuration	C_L (pF)
V_{CC} = 3.3V ± 0.3V, 2.7V to 3.6V	50

6.2.3 DC CHARACTERISTICS

Table 19. DC Characteristics, $T_A = -40^{\circ}C$ to $+85^{\circ}C$

Sym	Parameter	Notes	Typ	Max	Unit	Conditions
I_{LI}	Input Load Current	1		±0.5	µA	$V_{CC} = V_{CC1/2}$ Max $V_{IN} = V_{CC1/2}$ or GND
I_{LO}	Output Leakage Current	1		±0.5	µA	$V_{CC} = V_{CC1/2}$ Max $V_{out} = V_{CC1/2}$ or GND
I_{CCS}	V_{CC} Standby Current	1,3,6	20	100	µA	CMOS Inputs $V_{CC} = V_{CC1/2}$ Max $CE_X\# = RP\# = V_{CC} \pm 0.2V$
			0.2	2	mA	TTL Inputs $V_{CC} = V_{CC1/2}$ Max $CE_X\# = RP\# = V_{IH}$
I_{CCD}	V_{CC} Deep Power-Down Current	1		20	µA	RP# = GND ± 0.2V I_{OUT} (RY/BY#) = 0 mA
I_{CCR}	V_{CC} Read Current	1,5,6		25	mA	CMOS Inputs $V_{CC} = V_{CC1/2}$ Max $CE_X\#$ = GND f = 5 MHz, I_{OUT} = 0 mA
				30	mA	TTL Inputs $V_{CC} = V_{CC1/2}$ Max $CE_X\# = V_{IL}$ f = 5 MHz, I_{OUT} = 0 mA
I_{CCW}	V_{CC} Programming and Set Lock-Bit Current	1,7		17	mA	$V_{PP} = V_{PPH1/2}$
I_{CCE}	V_{CC} Block Erase or Clear Block Lock-Bits Current	1,7		17	mA	$V_{PP} = V_{PPH1/2}$
I_{CCWS} I_{CCES}	V_{CC} Program Suspend or Block Erase Suspend Current	1,2	1	6	mA	$CE_X\# = V_{IH}$
I_{PPS}	V_{PP} Standby or V_{PP} Read	1	± 2	± 15	µA	$V_{PP} \le V_{CC}$
I_{PPR}	Current		10	200	µA	$V_{PP} \ge V_{CC}$
I_{PPD}	V_{PP} Deep Power-Down Current	1	0.1	5	µA	RP# = GND ± 0.2V
I_{PPW}	V_{PP} Program or Set Lock-Bit Current	1,7		80	mA	$V_{PP} = V_{PPH1/2}$
I_{PPE}	V_{PP} Block Erase or Clear Block Lock-Bits Current	1,7		40	mA	$V_{PP} = V_{PPH1/2}$
I_{PPWS} I_{PPES}	V_{PP} Program Suspend or Block Erase Suspend Current	1	10	200	µA	$V_{PP} = V_{PPH1/2}$

Table 19. DC Characteristics (Continued)

Sym	Parameter	Notes	Min	Max	Unit	Conditions
V_{IL}	Input Low Voltage	7	-0.5	0.8	V	
V_{IH}	Input High Voltage	7	2.0	V_{CC} +0.5	V	
V_{OL}	Output Low Voltage	3,7		0.4	V	$V_{CC} = V_{CC1/2}$ Min I_{OL} = 5.8 mA
V_{OH1}	Output High Voltage (TTL)	3,7	2.4		V	$V_{CC} = V_{CC1/2}$ Min I_{OH} = –2.5 mA
V_{OH2}	Output High Voltage (CMOS)	3,7	0.85 × V_{CC}		V	$V_{CC} = V_{CC1/2}$ Min I_{OH} = –2.5 mA
			V_{CC} – 0.4		V	$V_{CC} = V_{CC1/2}$ Min I_{OH} = –100 µA
V_{PPLK}	V_{PP} Lockout Voltage	4,7		1.5	V	
V_{PPH1}	V_{PP} Voltage	4	2.7	3.6	V	
V_{PPH2}	V_{PP} Voltage	4	4.5	5.5	V	
V_{LKO}	V_{CC} Lockout Voltage	8	2.0		V	

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at nominal V_{CC} voltage and T_A = +25°C. These currents are valid for all product versions (packages and speeds).
2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or programmed while in erase suspend mode, the device's current is the sum of I_{CCWS} or I_{CCES} and I_{CCR} or I_{CCW}.
3. Includes STS in level RY/BY# mode.
4. Block erase, program, and lock-bit configurations are inhibited when $V_{PP} \le V_{PPLK}$, and not guaranteed in the ranges between V_{PPLK} (max) and V_{PPH1} (min), between V_{PPH1} (max) and V_{PPH2} (min), and above V_{PPH2} (max).
5. Automatic Power Savings (APS) reduces typical I_{CCR} to 3 mA at 2.7V and 3.3V V_{CC} static operation.
6. CMOS inputs are either V_{CC} ± 0.2V or GND ± 0.2V. TTL inputs are either V_{IL} or V_{IH}.
7. Sampled, not 100% tested.
8. With $V_{CC} \le V_{LKO}$ flash memory writes are inhibited.

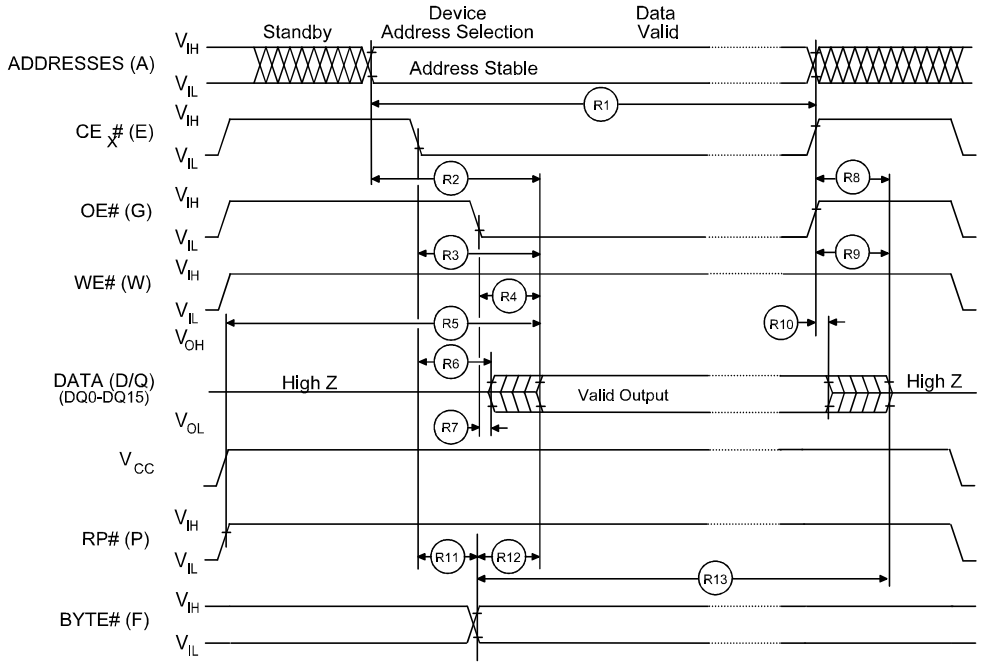
6.2.4 AC CHARACTERISTICS - READ-ONLY OPERATIONS

Table 20. AC Read Characteristics (1,5), T_A = –40°C to +85°C

Versions(4)				3.3V ± 0.3V V_{CC}		-100/-110			-130/-140		
(All units in ns unless otherwise noted)				2.7V - 3.6V V_{CC}			-120/-130			-150/-160	
#	Sym	Parameter		Notes	Min	Max	Min	Max	Min	Max	Min	Max
R1	t_{AVAV}	Read/Write Cycle Time	16 Mbit	1	100		120		130		150	
			32 Mbit	1	110		130		140		160	
R2	t_{AVQV}	Address to Output Delay	16 Mbit	1		100		120		130		150
			32 Mbit	1		110		130		140		160
R3	t_{ELQV}	CEx# to Output Delay	16 Mbit	2		100		120		130		150
			32 Mbit	2		110		130		140		160
R4	t_{GLQV}	OE# to Output Delay		2		45		50		50		55
R5	t_{PHQV}	RP# High to Output Delay				600		600		600		600
R6	t_{ELQX}	CEx# to Output in Low Z		3	0		0		0		0	
R7	t_{GLQX}	OE# to Output in Low Z		3	0		0		0		0	
R8	t_{EHQZ}	CEx# High to Output in High Z		3		50		50		55		55
R9	t_{GHQZ}	OE# High to Output in High Z		3		20		20		25		25
R10	t_{OH}	Output Hold from Address, CEx#, or OE# Change, Whichever Occurs First		3	0		0		0		0	
R11	t_{ELFL} t_{ELFH}	CEx# Low to BYTE# High or Low		3		5		5		5		5
R12	t_{FLOV} t_{FHQV}	BYTE# to Output Delay	16 Mbit	3		100		120		130		150
			32 Mbit	3		110		130		140		160
R13	t_{FLQZ}	BYTE# to Output in High Z		3		30		30		40		40

NOTES:

1. See AC Input/Output Reference Waveform for maximum allowable input slew rate.
2. OE# may be delayed up to t_{ELQV}-t_{GLQV} after the falling edge of CEx# without impact on t_{ELQV}.
3. Sampled, not 100% tested.
4. See Ordering Information for device speeds (valid operational combinations).
5. See Figures 14 through 16 for testing characteristics.



Note: CE_X# is the latter of CE_0# and CE_1# low or the first of CE_0# or CE_1# high.

Figure 17. AC Waveform for Read Operations

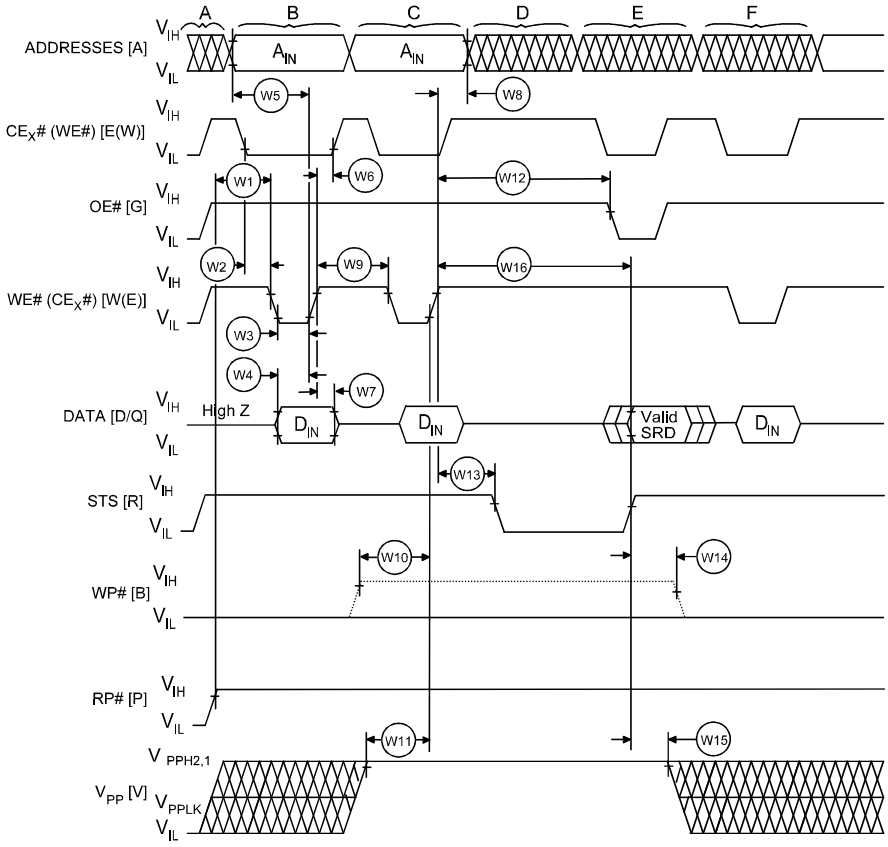
6.2.5 AC CHARACTERISTICS - WRITE OPERATIONS

Table 21. Write Operations[1,5,6], T_A = –40°C to +85°C

Versions[5]			3.3V ± 0.3V, 2.7V–3.6V V_{CC}	Valid for All Speeds		
#	Sym	Parameter	Notes	Min	Max	Unit
W1	t_{PHWL} (t_{PHEL})	RP# High Recovery to WE# (CE_X#) Going Low	2	1		µs
W2	t_{ELWL}	CE_X# Setup to WE# Going Low		10		ns
	(t_{WLEL})	(WE# Setup to CE_X# Going Low)		0		ns
W3	t_{WLWH}	WE# Pulse Width		50		ns
	(t_{ELEH})	(CE_X# Pulse Width)		70		ns
W4	t_{DVWH} (t_{DVEH})	Data Setup to WE# (CE_X#) Going High	3	50		ns
W5	t_{AVWH} (t_{AVEH})	Address Setup to WE# (CE_X#) Going High	3	50		ns
W6	t_{WHEH}	CE_X# Hold from WE# High		10		ns
	(t_{EHWH})	(WE# Hold from CE_X# High)		0		ns
W7	t_{WHDX} (t_{EHDX})	Data Hold from WE# (CE_X#) High		5		ns
W8	t_{WHAX} (t_{EHAX})	Address Hold from WE# (CE_X#) High		5		ns
W9	t_{WHWL}	WE# Pulse Width High		30		ns
	(t_{EHEL})	(CE_X# Pulse Width High)		25		ns
W10	t_{SHWH} (t_{SHEH})	WP# V_{IH} Setup to WE# (CE_X#) Going High		100		ns
W11	t_{VPWH} (t_{VPEH})	V_{PP} Setup to WE# (CE_X#) Going High	2	100		ns
W12	t_{WHGL} (t_{EHGL})	Write Recovery before Read		0		ns
W13	t_{WHRL} (t_{EHRL})	WE# High to STS in RY/BY# Low			100	ns
W14	t_{QVSL}	WP# V_{IH} Hold from Valid SRD	2,4	0		ns
W15	t_{QVVL}	V_{PP} Hold from Valid SRD, STS in RY/BY# High	2,4	0		ns

NOTES:

1. Read timing characteristics during block erase, program, and lock-bit configuration operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
2. Sampled, not 100% tested.
3. Refer to Table 3 for valid A_{IN} and D_{IN} for block erase, program, or lock-bit configuration.
4. V_{PP} should be at $V_{PPH1/2}$ until determination of block erase, program, or lock-bit configuration success (SR.1/3/4/5 = 0).
5. See Ordering Information for device speeds (valid operational combinations).
6. See Figures 14 through 16 for testing characteristics.



NOTES:

A. V_{CC} power-up and standby.
B. Write block erase or program setup.
C. Write block erase confirm or valid address and data..
D. Automated erase or program delay.
E. Read Status Register data.
F. Write Read Array command.

CE_X# is the latter of CE_0# and CE_1# low or the first of CE_0# or CE_1# high.

Figure 18. AC Waveform for Write Operations

6.2.6 RESET OPERATIONS

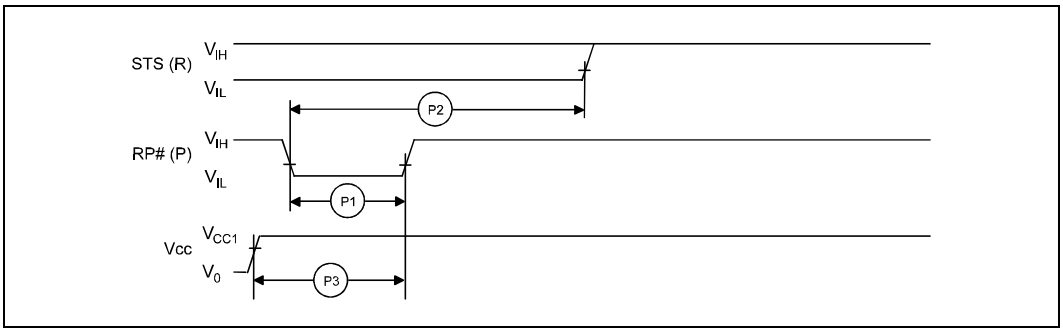


Figure 19. AC Waveform for Reset Operation

Table 22. Reset AC Specifications(1)

#	Sym	Parameter	Notes	V_{CC} = 2.7V		V_{CC} = 3.3V		Unit
				Min	Max	Min	Max	
P1	t_{PLPH}	RP# Pulse Low Time (If RP# is tied to V_{CC}, this specification is not applicable)		100		100		ns
P2	t_{PLRH}	RP# Low to Reset during Block Erase, Program, or Lock-Bit Configuration	2,3		20		20	µs
P3	t_{3VPH}	V_{CC} at 2.7V to RP# High V_{CC} at 3.0V to RP# High			50		50	µs

NOTES:

1. These specifications are valid for all product versions (packages and speeds).
2. If RP# is asserted while a block erase, program, or lock-bit configuration operation is not executing, the reset will complete within t_{PLPH}.
3. A reset time, t_{PHQV}, is required from the latter of STS in RY/BY# mode or RP# going high until outputs are valid.

6.2.7 ERASE, PROGRAM, AND LOCK-BIT CONFIGURATION PERFORMANCE

Table 23. Erase/Write/Lock Performance(3,4)

Version					2.7V–3.6V V_{CC}						
					2.7V V_{PP}		3.3V V_{PP}		5V V_{PP}		
#	Sym	Parameter		Notes	Typ(1)	Max	Typ(1)	Max	Typ(1)	Max	Units
W16		Byte/word program time (using write buffer)		5	5.76	TBD	5.76	TBD	2.76	TBD	µs
W16	t_{WHQV1} t_{EHQV1}	Per byte program time (without write buffer)		2	19.89	TBD	19.89	TBD	13.2	TBD	µs
W16	t_{WHQV1} t_{EHQV1}	Per word program time (without write buffer)		2	22.17	TBD	22.17	TBD	13.2	TBD	µs
W16		Block program time (byte mode)		2	1.63	TBD	1.63	TBD	0.87	TBD	sec
W16		Block program time (word mode)		2	0.91	TBD	0.91	TBD	0.44	TBD	sec
W16		Block program time (using write buffer)		2	0.37	TBD	0.37	TBD	0.16	TBD	sec
W16	t_{WHQV2} t_{EHQV2}	Block erase time		2	0.56	TBD	0.56	TBD	0.42	TBD	sec
W16		Full chip erase time	16 Mbit		17.9		17.9		13.3		sec
			32 Mbit		35.8		35.8		26.6		sec
W16	t_{WHQV3} t_{EHQV3}	Set Lock-Bit time		2	22.17	TBD	22.17	TBD	13.3	TBD	µs
W16	t_{WHQV4} t_{EHQV4}	Clear block lock-bits time		2	0.56	TBD	0.56	TBD	0.42	TBD	sec
W16	t_{WHRH1} t_{EHRH1}	Program suspend latency time to read			7.24	10.2	7.24	10.2	6.73	9.48	µs
W16	t_{WHRH2} t_{EHRH2}	Erase suspend latency time to read			15.5	21.5	15.5	21.5	12.54	17.54	µs

NOTES:

1. Typical values measured at T_A = +25°C and nominal voltages. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. Sampled but not 100% tested.
5. Uses whole buffer.

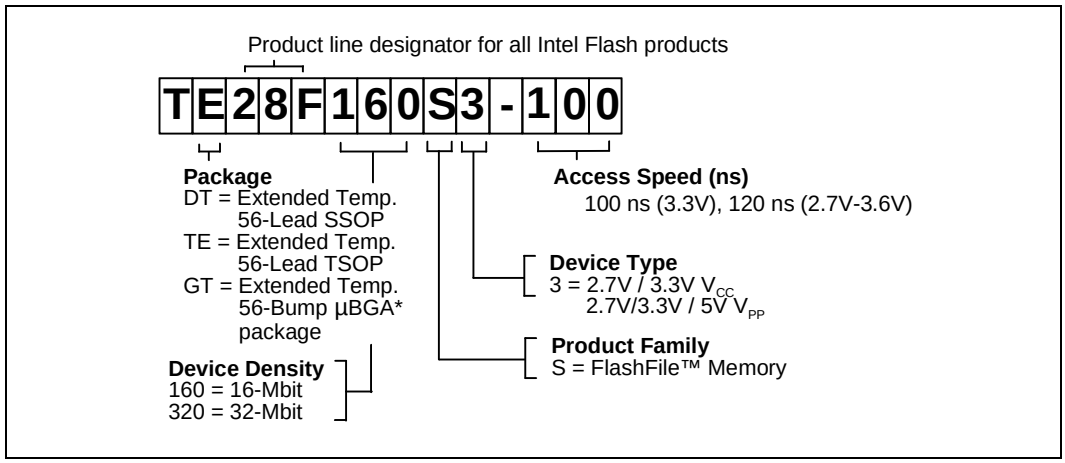
Table 24. Erase/Write/Lock Performance(3,4)

Version				3.3V ± 0.3V V_{CC}				
				3.3V V_{PP}		5V V_{PP}		
#	Sym	Parameter	Notes	Typ(1)	Max	Typ(1)	Max	Units
W16		Byte/word program time (using write buffer)	5	5.66	TBD	2.7	TBD	µs
W16	t_{WHQV1} t_{EHQV1}	Per byte program time (without write buffer)	2	19.51	TBD	12.95	TBD	µs
W16	t_{WHQV1} t_{EHQV1}	Per word program time (without write buffer)	2	21.75	TBD	12.95	TBD	µs
W16		Block program time (byte mode)	2	1.6	TBD	0.85	TBD	sec
W16		Block program time (word mode)	2	0.89	TBD	0.43	TBD	sec
W16		Block program time (using write buffer)	2	0.36	TBD	0.18	TBD	sec
W16	t_{WHQV2} t_{EHQV2}	Block erase time	2	0.55	TBD	0.41	TBD	sec
W16		Full chip erase time 16 Mbit		17.6	TBD	13.1	TBD	sec
		Full chip erase time 32 Mbit		35.2	TBD	26.2	TBD	sec
W16	t_{WHQV3} t_{EHQV3}	Set Lock-Bit time	2	22.75	TBD	12.95	TBD	µs
W16	t_{WHQV4} t_{EHQV4}	Clear block lock-bits time	2	0.55	TBD	0.41	TBD	sec
W16	t_{WHRH1} t_{EHRH1}	Program suspend latency time to read		7.1	10	6.6	9.3	µs
W16	t_{WHRH2} t_{EHRH2}	Erase suspend latency time to read		15.2	21.1	12.3	17.2	µs

NOTES:

1. Typical values measured at T_A = +25°C and nominal voltages. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. Sampled but not 100% tested.
5. Uses whole buffer.

APPENDIX A
DEVICE NOMENCLATURE AND ORDERING INFORMATION



Order Code by Density		Valid Operational Combinations	
16 Mb	**32 Mb**	**2.7V-3.6V V_{CC} 50 pF load** (16 Mb / 32 Mb)	**3.3V ± 0.3V V_{CC} 50 pF load** (16 Mb / 32 Mb)
56-lead TSOP S3-100	56-lead TSOP S3-110	-120 / -130	-100 / -110
56-lead TSOP S3-130	56-lead TSOP S3-140	-150 / -160	-130 / -140
56-lead SSOP S3-100	56-lead SSOP S3-110	-120 / -130	-100 / -110
56-lead SSOP S3-130	56-lead SSOP S3-140	-150 / -160	-130 / -140
56-bump µBGA S3-100	56-bump µBGA S3-110	-120 / -130	-100 / -110
56-bump µBGA S3-130	56-bump µBGA S3-140	-150 / -160	-130 / -140

ADVANCE INFORMATION

APPENDIX B
ADDITIONAL INFORMATION(1,2)

Order Number	Document/Tool
290609	*Word-Wide FlashFile Memory™ Family 28F160S5, 28F320S5* Datasheet
292203	*AP-645 28F160S3/S5 Compatibility with 28F016SA/SV*
292204	*AP-646 Common Flash Interface (CFI) and Command Sets*
www.mcif.com	*Common Flash Interface Specification*
290528	*28F016SV 16-Mb (1Mbit x 16, 2 Mbit x 8) FlashFile™ Memory* Datasheet
290489	*28F016SA 16-Mb (1Mbit x 16, 2 Mbit x 8) FlashFile™ Memory* Datasheet
297372	*16-Mbit Flash Product Family User's Manual*
292123	*AP-374 Flash Memory Write Protection Techniques*
292144	*AP-393 28F016SV Compatibility with 28F016SA*
292159	*AP-607 Multi-Site Layout Planning with Intel's FlashFile™ Components, Including ROM Capability*
292163	*AP-610 Flash Memory In-System Code and Data Update Techniques*
Contact Intel/Distribution Sales Office	*Mechanical Specification µBGA* Package Preliminary Guide*
Contact Intel/Distribution Sales Office	*Surface Mount and PCB Guidelines for µBGA* Packaging*
Contact Intel/Distribution Sales Office	*Multi-Site Layouts: 56-lead TSOP to 56-bump µBGA* package* *56-lead SSOP to 56-bump µBGA package*
Contact Intel/Distribution Sales Office	*CFI - Common Flash Interface Reference Code*

NOTES:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.intel.com for technical documentation and tools.