SMART 3 ADVANCED BOOT BLOCK WORD-WIDE 4-MBIT (256K X 16), 8-MBIT (512K X 16), 16-MBIT (1024K X 16) FLASH MEMORY FAMILY

28F400B3, 28F800B3, 28F160B3

- **Flexible SmartVoltage Technology**
  - **2.7V–3.6V Program/Erase**
  - **2.7V–3.6V Read Operation**
  - **12V V_{PP} Fast Production Programming**
- **2.7V or 1.8V I/O Option**
  - **Reduces Overall System Power**
- **Optimized Block Sizes**
  - **Eight 4-KW Blocks for Data, Top or Bottom Locations**
  - **Up to Thirty-One 32-KW Blocks for Code**
- **High Performance**
  - **2.7V–3.6V: 120 ns Max Access Time**
- **Block Locking**
  - **V_{CC}-Level Control through WP#**
- **Low Power Consumption**
  - **20 mA Maximum Read Current**
- **Absolute Hardware-Protection**
  - **V_{PP} = GND Option**
  - **V_{CC} Lockout Voltage**
- **Extended Temperature Operation**
  - **–40°C to +85°C**
- **Supports Code Plus Data Storage**
  - **Optimized for FDI, Flash Data Integrator Software**
  - **Fast Program Suspend Capability**
  - **Fast Erase Suspend Capability**
- **Extended Cycling Capability**
  - **10,000 Block Erase Cycles**
- **Automated Word Program and Block Erase**
  - **Command User Interface**
  - **Status Registers**
- **SRAM-Compatible Write Interface**
- **Automatic Power Savings Feature**
- **Reset/Deep Power-Down**
  - **1 µA I_{CC} Typical**
  - **Spurious Write Lockout**
- **Standard Surface Mount Packaging**
  - **48-Ball µBGA* Package**
  - **48-Lead TSOP Package**
- **Footprint Upgradeable**
  - **Upgradeable from 2-, 4- and 8-Mbit Boot Block**
- **ETOX™ V (0.4 µ) Flash Technology**

The new Smart 3 Advanced Boot Block, manufactured on Intel's latest 0.4µ technology, represents a feature-rich solution at overall lower system cost. Smart 3 flash memory devices incorporate low voltage capability (2.7V read, program and erase) with high-speed, low-power operation. Several new features have been added, including the ability to drive the I/O at 1.8V, which significantly reduces system active power and interfaces to 1.8V controllers. A new blocking scheme enables code and data storage within a single device. Add to this the Intel-developed Flash Data Integrator (FDI) software and you have the most cost-effective, monolithic code plus data storage solution on the market today. Smart 3 Advanced Boot Block Word-Wide products will be available in 48-lead TSOP and 48-ball µBGA* packages. Additional information on this product family can be obtained by accessing Intel's WWW page: http://www.intel.com/design/flcomp.

May 1997 Order Number: 290580-002

The 28F400B3, 28F800B3, 28F160B3 may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 7641
Mt. Prospect, IL 60056-7641

or call 1-800-879-4683
or visit Intel's website at http:\\www.intel.com

 CG-041493

*Third-party brands and names are the property of their respective owners

CONTENTS

REVISION HISTORY

Number	Description
-001	Original version
-002	Section 3.4, *V_{PP} Program and Erase Voltages*, added Updated Figure 9: Automated Block Erase Flowchart Updated Figure 10: Erase Suspend/Resume Flowchart (added program op. to table) Updated Figure 16: AC Waveform: Program and Erase Operations (updated notes) I_{PPR} maximum specification change from ±25 µA to ±50 µA Program and Erase Suspend Latency specification change Updated Appendix A: Ordering Information (included 8M and 4M information) Updated Figure, Appendix D: Architecture Block Diagram (Block info. in Words not bytes) Minor wording changes

1.0 INTRODUCTION

This preliminary datasheet contains the specifications for the Advanced Boot Block flash memory family, which is optimized for low power, portable systems. This family of products features 1.8V–2.2V or 2.7V–3.6V I/Os and a low V_{CC}/V_{PP} operating range of 2.7V–3.6V for read and program/erase operations. In addition this family is capable of fast programming at 12V. Throughout this document, the term "2.7V" refers to the full voltage range 2.7V–3.6V (except where noted otherwise) and "V_{PP} = 12V" refers to 12V ±5%. Section 1 and 2 provides an overview of the flash memory family including applications, pinouts and pin descriptions. Section 3 describes the memory organization and operation for these products. Finally, Sections 4, 5, 6 and 7 contain the operating specifications.

1.1 Smart 3 Advanced Boot Block Flash Memory Enhancements

The new 4-Mbit, 8-Mbit, and 16-Mbit Smart 3 Advanced Boot Block flash memory provides a convenient upgrade from and/or compatibility to previous 4-Mbit and 8-Mbit Boot Block products. The Smart 3 product functions are similar to lower density products in both command sets and operation, providing similar pinouts to ease density upgrades.

The Smart 3 Advanced Boot Block flash memory features

- Enhanced blocking for easy segmentation of code and data or additional design flexibility
- Program Suspend command which permits program suspend to read
- WP# pin to lock and unlock the upper two (or lower two, depending on location) 4-Kword blocks
- V_{CCQ} input for 1.8V–2.2V on all I/Os. See Figure 1-4 for pinout diagrams and V_{CCQ} location
- Maximum program time specification for improved data storage.

Table 1. Smart 3 Advanced Boot Block Feature Summary

Feature	28F160B3	Reference
V_{CC} Read Voltage	2.7V– 3.6V	Table 9, Table 12
V_{CCQ} I/O Voltage	1.8V–2.2V or 2.7V– 3.6V	Table 9, Table 12
V_{PP} Program/Erase Voltage	2.7V– 3.6V or 11.4V– 12.6V	Table 9, Table 12
Bus Width	16 bit	Table 2
Speed	120 ns	Table 15
Memory Arrangement	256-Kbit x 16 (4-Mbit), 512-Kbit x 16 (8-Mbit), 1024-Kbit x 16 (16-Mbit)	
Blocking (top or bottom)	Eight 4-Kword parameter blocks (4/8/16) & Seven 32-Kword blocks (4-Mbit) Fifteen 32-Kword blocks (8-Mbit) Thirty-one 32-Kword main blocks (16-Mbit)	Section 2.2 Figures 5 and 6
Locking	WP# locks/unlocks parameter blocks All other blocks protected using V_{PP} switch	Section 3.3 Table 8
Operating Temperature	Extended: –40°C to +85°C	Table 9, Table 12
Program/Erase Cycling	10,000 cycles	Table 9, Table 12
Packages	48-Lead TSOP, 48-Ball µBGA* CSP	Figures 1, 2, 3, and 4

1.2 Product Overview

Intel provides the most flexible voltage solution in the flash industry, providing three discrete voltage supply pins: V_{CC} for read operation, V_{CCQ} for output swing, and V_{PP} for program and erase operation. Discrete supply pins allow system designers to use the optimal voltage levels for their design. All Smart 3 Advanced Boot Block flash memory products provide program/erase capability at 2.7V or 12V and read with V_{CC} at 2.7V. Since many designs read from the flash memory a large percentage of the time, 2.7V V_{CC} operation can provide substantial power savings. The 12V V_{PP} option maximizes program and erase performance during production programming.

The Smart 3 Advanced Boot Block flash memory products are high-performance devices with low power operation. The available densities for word-wide devices (x16) are

a. 4-Mbit (4,194,304-bit) flash memory organized as 256-Kwords of 16 bits each

b. 8-Mbit (8,388,608-bit) flash memory organized as 512-Kwords of 16 bits each

c. 16-Mbit (16,777,216-bit) flash memory organized as 1024-Kwords of 16 bits each.

For byte-wide devices (x8) see the *Smart 3 Advanced Boot Block Byte-Wide Flash Memory Family* datasheet.

The parameter blocks are located at either the top (denoted by -T suffix) or the bottom (-B suffix) of the address map in order to accommodate different microprocessor protocols for kernel code location. The upper two (or lower two) parameter blocks can be locked to provide complete code security for system initialization code. Locking and unlocking is controlled by WP# (see Section 3.3 for details).

The Command User Interface (CUI) serves as the interface between the microprocessor or microcontroller and the internal operation of the flash memory. The internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for program and erase operations, including verification, thereby unburdening the microprocessor or microcontroller. The status register indicates the status of the WSM by signifying block erase or word program completion and status.

Program and erase automation allows program and erase operations to be executed using an industry-standard two-write command sequence to the CUI. Data writes are performed in word increments. Each word in the flash memory can be programmed independently of other memory locations; every erase operation erases all locations within a block simultaneously. Program suspend allows system software to suspend the program command in order to read from any other block. Erase suspend allows system software to suspend the block erase command in order to read from or program data to any other block.

The Smart 3 Advanced Boot Block flash memory is also designed with an Automatic Power Savings (APS) feature which minimizes system current drain, allowing for very low power designs. This mode is entered immediately following the completion of a read cycle.

When the CE# and RP# pins are at V_{CC}, the I_{CC} CMOS standby mode is enabled. A deep power-down mode is enabled when the RP# pin is at GND, minimizing power consumption and providing write protection. I_{CC} current in deep power-down is 1 µA typical (2.7V V_{CC}). A minimum reset time of t_{PHQV} is required from RP# switching high until outputs are valid to read attempts. With RP# at GND, the WSM is reset and Status Register is cleared. Section 3.5 contains additional information on using the deep power-down feature, along with other power consumption issues.

The RP# pin provides additional protection against unwanted command writes that may occur during system reset and power-up/down sequences due to invalid system bus conditions (see Section 3.6).

Refer to the DC Characteristics Table, Sections 5.1 and 6.1, for complete current and voltage specifications. Refer to the AC Characteristics Table, Section 7.0, for read, program and erase performance specifications.

2.0 PRODUCT DESCRIPTION

This section explains device pin description and package pinouts.

2.1 Package Pinouts

The Smart 3 Advanced Boot Block flash memory is available in 48-lead TSOP (see Figure 1) and 48-ball µBGA packages (see Figures 2-4). In Figure 1, pin changes from one density to the next are circled. Both packages, 48-lead TSOP and 48-ball µBGA* package, are 16-bits wide and fully upgradeable across product densities (from 4 Mb to 16 Mb).

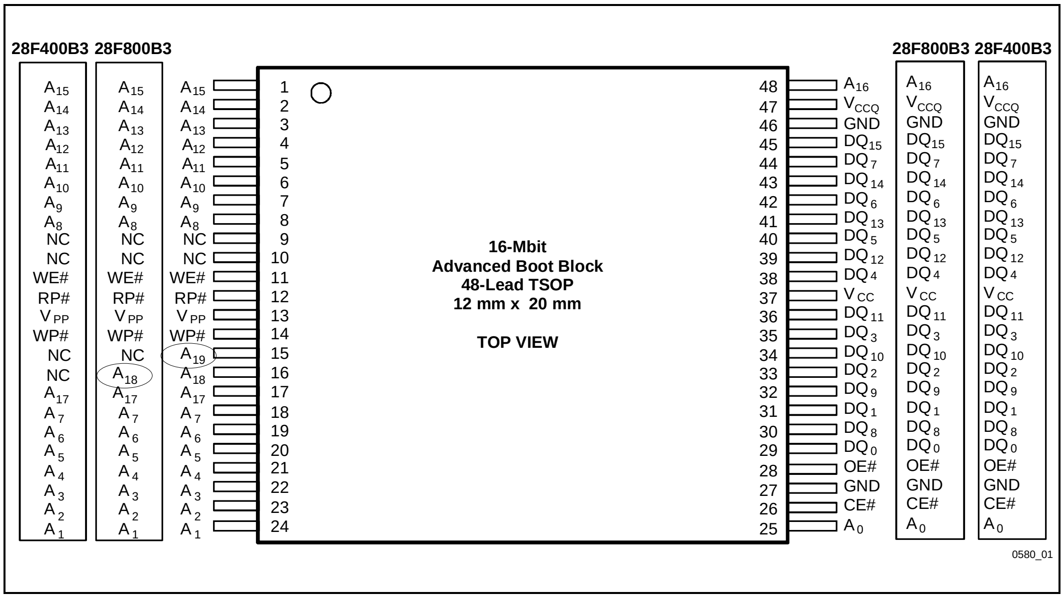
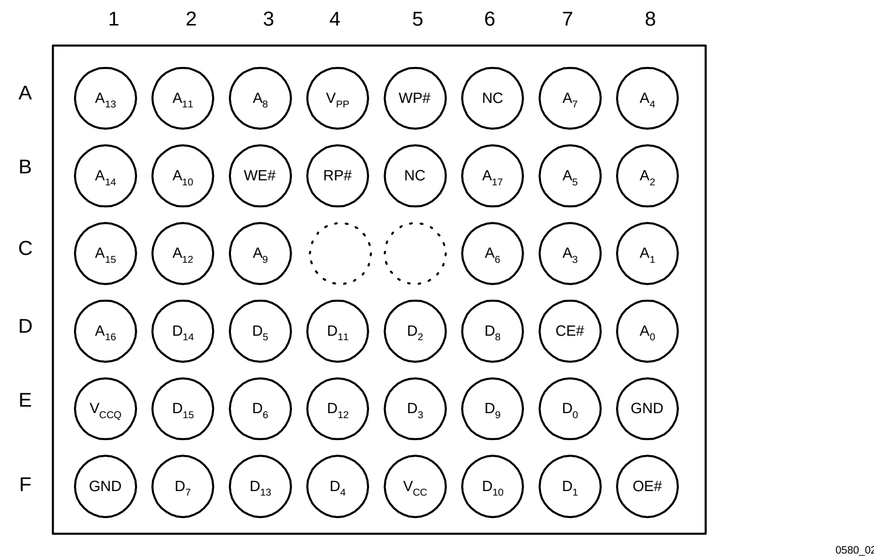


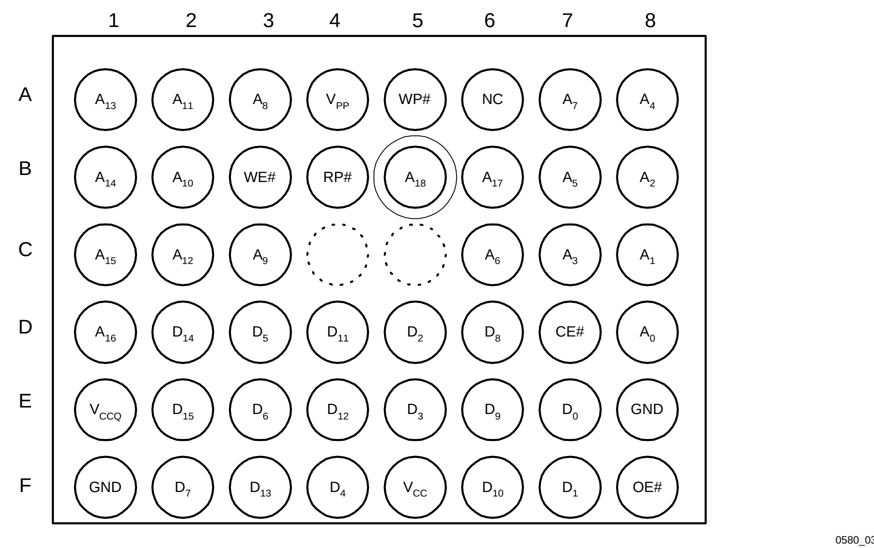
Figure 1. 48-Lead TSOP Package



NOTE:

Dotted connections indicate placeholders where there is no solder ball. These connections are reserved for future upgrades. Routing is not recommended in this area.

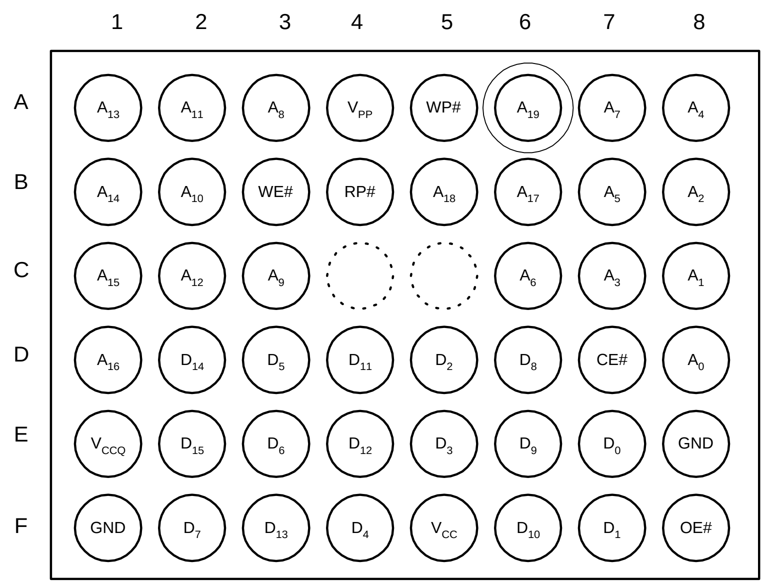
Figure 2. 4-Mbit 48-Ball μBGA* Chip Size Package



NOTE:

Dotted connections indicate placeholders where there is no solder ball. These connections are reserved for future upgrades. Routing is not recommended in this area.

Figure 3. 8-Mbit 48-Ball μBGA* Chip Size Package



NOTE:

Dotted connections indicate placeholders where there is no solder ball. These connections are reserved for future upgrades. Routing is not recommended in this area.

Figure 4. 16-Mbit 48-Ball µBGA* Chip Size Package (Top View, Ball Down)

The pin descriptions table details the usage of each device pin.

Table 2. 16-Mbit Smart 3 Advanced Boot Block Pin Descriptions

Symbol	Type	Name and Function
A_0–A_{19}	INPUT	**ADDRESS INPUTS** for memory addresses. Addresses are internally latched during a program or erase cycle. **28F400B3: A[0-17], 28F800B3: A[0-18], 28F160B3: A[0-19]**
DQ_0–DQ_7	INPUT/OUTPUT	**DATA INPUTS/OUTPUTS:** Inputs array data on the second CE# and WE# cycle during a Program command. Inputs commands to the Command User Interface when CE# and WE# are active. Data is internally latched. Outputs array, Intelligent Identifier and Status Register data. The data pins float to tri-state when the chip is de-selected or the outputs are disabled.
DQ_8–DQ_{15}	INPUT/OUTPUT	**DATA INPUTS/OUTPUTS:** Inputs array data on the second CE# and WE# cycle during a Program command. Data is internally latched. Outputs array and intelligent identifier data. The data pins float to tri-state when the chip is de-selected.
CE#	INPUT	**CHIP ENABLE:** Activates the internal control logic, input buffers, decoders and sense amplifiers. CE# is active low. CE# high de-selects the memory device and reduces power consumption to standby levels. If CE# and RP# are high, but not at a CMOS high level, the standby current will increase due to current flow through the CE# and RP# inputs.
OE#	INPUT	**OUTPUT ENABLE:** Enables the device’s outputs through the data buffers during an array or status register read. OE# is active low.
WE#	INPUT	**WRITE ENABLE:** Controls writes to the Command Register and memory array. WE# is active low. Addresses and data are latched on the rising edge of the second WE# pulse.
RP#	INPUT	**RESET/DEEP POWER-DOWN:** Uses two voltage levels (V_{IL}, V_{IH}) to control reset/deep power-down mode. **When RP# is at logic low, the device is in reset/deep power-down mode**, which drives the outputs to High-Z, resets the Write State Machine, and draws minimum current. **When RP# is at logic high, the device is in standard operation**. When RP# transitions from logic-low to logic-high, the device defaults to the read array mode.
WP#	INPUT	**WRITE PROTECT:** Provides a method for locking and unlocking the two lockable parameter blocks. **When WP# is at logic low, the lockable blocks are locked**, preventing program and erase operations to those blocks. If a program or erase operation is attempted on a locked block, SR.1 and either SR.4 [program] or SR.5 [erase] will be set to indicate the operation failed. **When WP# is at logic high, the lockable blocks are unlocked** and can be programmed or erased. See Section 3.3 for details on write protection.

Table 2. 16-Mbit Smart 3 Advanced Boot Block Pin Descriptions (Continued)

Symbol	Type	Name and Function
V_{CCQ}	INPUT	**OUTPUT V_{CC}:** Enables all outputs to be driven to 2.0V ±10% while the V_{CC} is at 2.7V. When this mode is used, the V_{CC} **should** be regulated to 2.7V–2.85V to achieve lowest power operation (see Section 6.1: DC Characteristics: V_{CCQ} = 1.8V–2.2V). This input may be tied directly to V_{CC} (2.7V–3.6V). See the DC Characteristics for further details.
V_{CC}		**DEVICE POWER SUPPLY:** 2.7V–3.6V
V_{PP}		**PROGRAM/ERASE POWER SUPPLY:** For erasing memory array blocks or programming data in each block, a voltage of either 2.7V–3.6V or 12V ± 5% must be applied to this pin. When $V_{PP} < V_{PPLK}$ all blocks are locked and protected against Program and Erase commands. Applying 11.4V-12.6V to V_{PP} can only be done for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. V_{PP} may be connected to 12V for a total of 80 hours maximum (see Section 3.4 for details).
GND		**GROUND:** For all internal circuitry. All ground inputs **must** be connected.
NC		**NO CONNECT:** Pin may be driven or left floating.

2.2 Block Organization

The Smart 3 Advanced Boot Block is an asymmetrically-blocked architecture that enables system integration of code and data within a single flash device. Each block can be erased independently of the others up to 10,000 times. For the address locations of each block, see the memory maps in Figure 5 (top boot blocking) and Figure 6 (bottom boot blocking).

2.2.1 PARAMETER BLOCKS

The Smart 3 Advanced Boot Block flash memory architecture includes parameter blocks to facilitate storage of frequently updated small parameters (e.g., data that would normally be stored in an EEPROM). By using software techniques, the word-rewrite functionality of EEPROMs can be emulated. Each 4-/8-/16-Mbit device contains eight parameter blocks of 4-Kwords (4,096-words) each.

2.2.2 MAIN BLOCKS

After the parameter blocks, the remainder of the array is divided into equal size main blocks for data or code storage. Each 16-Mbit device contains thirty-one 32-Kword (32,768-word) blocks. Each 8-Mbit device contains fifteen 32-Kword blocks. Each 4-Mbit device contains seven 32-Kword blocks.

16-Mbit Advanced Boot Block

FFFFF–FF000	4-Kword Block	38
FEFFF–FE000	4-Kword Block	37
FDFFF–FD000	4-Kword Block	36
FCFFF–FC000	4-Kword Block	35
FBFFF–FB000	4-Kword Block	34
FAFFF–FA000	4-Kword Block	33
F9FFF–F9000	4-Kword Block	32
F8FFF–F8000	4-Kword Block	31
F7FFF–F0000	32-Kword Block	30
EFFFF–E8000	32-Kword Block	29
E7FFF–E0000	32-Kword Block	28
DFFFF–D8000	32-Kword Block	27
D7FFF–D0000	32-Kword Block	26
CFFFF–C8000	32-Kword Block	25
C7FFF–C0000	32-Kword Block	24
BFFFF–B8000	32-Kword Block	23
B7000–B0000	32-Kword Block	22
AFFFF–A8000	32-Kword Block	21
A7FFF–A0000	32-Kword Block	20
9FFFF–98000	32-Kword Block	19
97FFF–90000	32-Kword Block	18
8FFFF–88000	32-Kword Block	17
87FFF–80000	32-Kword Block	16
7FFFF–78000	32-Kword Block	15
77FFF–70000	32-Kword Block	14
6FFFF–68000	32-Kword Block	13
67FFF–60000	32-Kword Block	12
5FFFF–58000	32-Kword Block	11
57FFF–50000	32-Kword Block	10
4FFFF–48000	32-Kword Block	9
47FFF–40000	32-Kword Block	8
3FFFF–38000	32-Kword Block	7
37FFF–30000	32-Kword Block	6
2FFFF–28000	32-Kword Block	5
27FFF–20000	32-Kword Block	4
1FFFF–18000	32-Kword Block	3
17FFF–10000	32-Kword Block	2
0FFFF–08000	32-Kword Block	1
07FFF–00000	32-Kword Block	0

8-Mbit Advanced Boot Block

7FFFF–7F000	4-Kword Block	22
7EFFF–7E000	4-Kword Block	21
7DFFF–7D000	4-Kword Block	20
7CFFF–7C000	4-Kword Block	19
7BFFF–7B000	4-Kword Block	18
7AFFF–7A000	4-Kword Block	17
79FFF–79000	4-Kword Block	16
78FFF–78000	4-Kword Block	15
77FFF–70000	32-Kword Block	14
6FFFF–68000	32-Kword Block	13
67FFF–60000	32-Kword Block	12
5FFFF–58000	32-Kword Block	11
57FFF–50000	32-Kword Block	10
4FFFF–48000	32-Kword Block	9
47FFF–40000	32-Kword Block	8
3FFFF–38000	32-Kword Block	7
37FFF–30000	32-Kword Block	6
2FFFF–28000	32-Kword Block	5
27FFF–20000	32-Kword Block	4
1FFFF–18000	32-Kword Block	3
17FFF–10000	32-Kword Block	2
0FFFF–08000	32-Kword Block	1
07FFF–00000	32-Kword Block	0

4-Mbit Advanced Boot Block

3FFFF–3F000	4-Kword Block	14
3EFFF–3E000	4-Kword Block	13
3DFFF–3D000	4-Kword Block	12
3CFFF–3C000	4-Kword Block	11
3BFFF–3B000	4-Kword Block	10
3AFFF–3A000	4-Kword Block	9
39FFF–39000	4-Kword Block	8
38FFF–38000	4-Kword Block	7
37FFF–30000	32-Kword Block	6
2FFFF–28000	32-Kword Block	5
27FFF–20000	32-Kword Block	4
1FFFF–18000	32-Kword Block	3
17FFF–10000	32-Kword Block	2
0FFFF–08000	32-Kword Block	1
07FFF–00000	32-Kword Block	0

0580_05

Figure 5. 4-/8-/16-Mbit Advanced Boot Block Word-Wide Top Boot Memory Maps

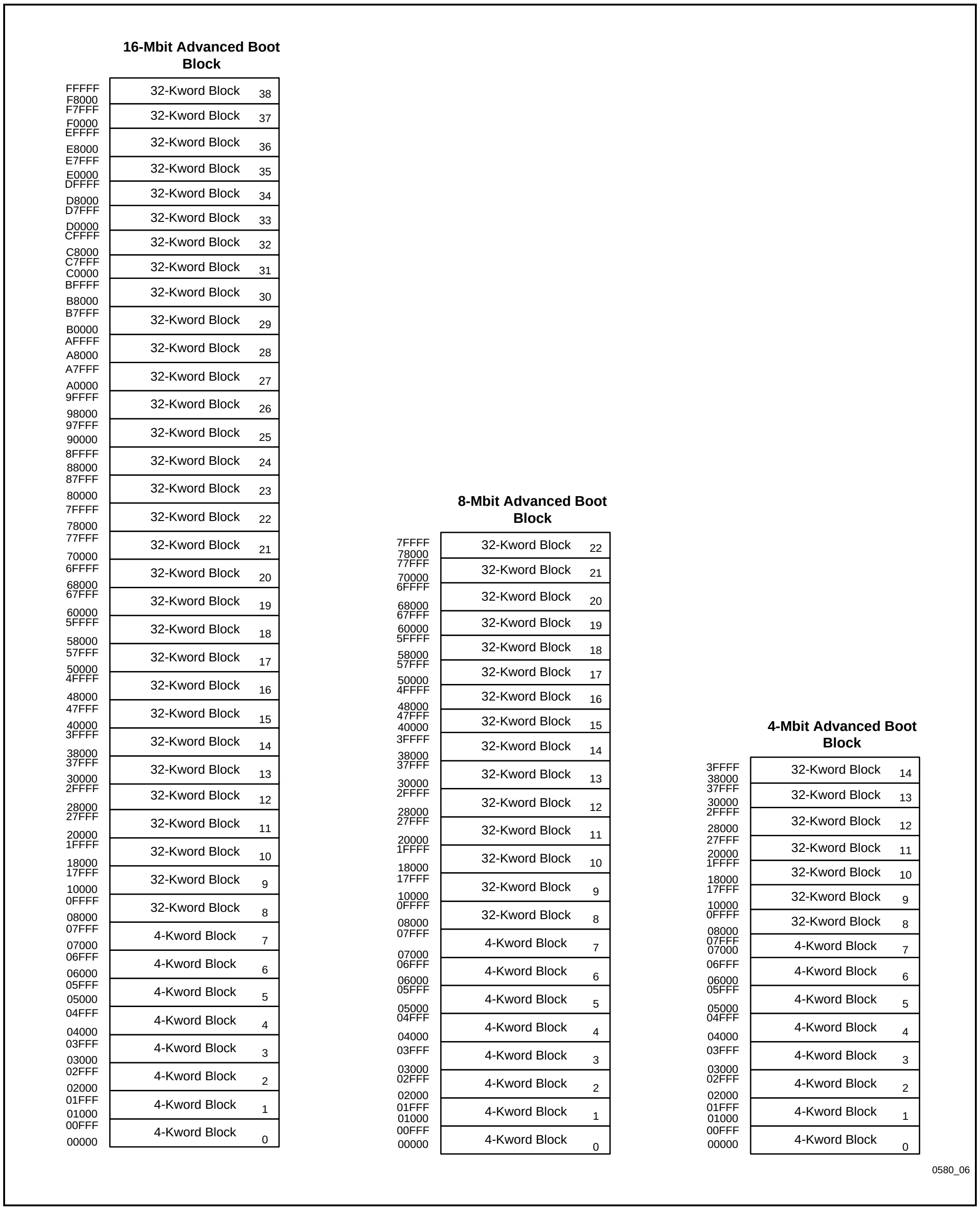


Figure 6. 4-/8-/16-Mbit Advanced Boot Block Word-Wide Top Boot Memory Maps

3.0 PRINCIPLES OF OPERATION

Flash memory combines EEPROM functionality with in-circuit electrical program and erase capability. The Smart 3 Advanced Boot Block flash memory family utilizes a Command User Interface (CUI) and automated algorithms to simplify program and erase operations. The CUI allows for 100% CMOS-level control inputs, fixed power supplies during erasure and programming, and maximum EEPROM compatibility.

When $V_{PP} < V_{PPLK}$, the device will only execute the following commands successfully: Read Array, Read Status Register, Clear Status Register and Read Intelligent Identifier. The device provides standard EEPROM read, standby and output disable operations. Manufacturer identification and device identification data can be accessed through the CUI. In addition, 2.7V or 12V on V_{PP} allows program and erase of the device. All functions associated with altering memory contents, namely program and erase, are accessible via the CUI.

The internal Write State Machine (WSM) completely automates program and erase operations while the CUI signals the start of an operation and the status register reports status. The CUI handles the WE# interface to the data and address latches, as well as system status requests during WSM operation.

3.1 Bus Operation

Smart 3 Advanced Boot Block flash memory devices read, program and erase in-system via the local CPU or microcontroller. All bus cycles to or from the flash memory conform to standard microcontroller bus cycles. Four control pins dictate the data flow in and out of the flash component: CE#, OE#, WE# and RP#. These bus operations are summarized in Table 3.

Table 3. Bus Operations for Word-Wide Mode

Mode	Notes	RP#	CE#	OE#	WE#	WP#	A_0	V_{PP}	$DQ_{0–15}$
Read	1,2,3	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	X	D_{OUT}
Output Disable	2	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	X	High Z
Standby	2	V_{IH}	V_{IH}	X	X	X	X	X	High Z
Deep Power-Down	2,9	V_{IL}	X	X	X	X	X	X	High Z
Intelligent Identifier (Mfr.)	2,4	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	V_{IL}	X	0089 H
Intelligent Identifier (Dvc.)	2,4,5	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	V_{IH}	X	See Table 5
Write	2,6,7, 8	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	V_{PPH}	D_{IN}

NOTES:

1. Refer to DC Characteristics.
2. X must be V_{IL}, V_{IH} for control pins and addresses, V_{PPLK} , V_{PPH1} or V_{PPH2} for V_{PP}.
3. See DC Characteristics for V_{PPLK}, V_{PPH1}, V_{PPH2} voltages.
4. Manufacturer and device codes may also be accessed via a CUI write sequence, A_1–A_{19} = X
5. See Table 5 for device IDs.
6. Refer to Table 6 for valid D_{IN} during a write operation.
7. Command writes for block erase or word program are only executed when $V_{PP} = V_{PPH1}$ or V_{PPH2}.
8. To program or erase the lockable blocks, hold WP# at V_{IH}. See Section 3.3.
9. RP# must be at GND ± 0.2V to meet the maximum deep power-down current specified.

3.1.1 READ

The flash memory has three read modes available: read array, read identifier, and read status. These modes are accessible independent of the V_{PP} voltage. The appropriate read mode command must be issued to the CUI to enter the corresponding mode. Upon initial device power-up or after exit from deep power-down mode, the device automatically defaults to read array mode.

CE# and OE# must be driven active to obtain data at the outputs. CE# is the device selection control; when active it enables the flash memory device. OE# is the data output (DQ_0–DQ_{15}) control and it drives the selected memory data onto the I/O bus. For all read modes, WE# and RP# must be at V_{IH}. Figure 15 illustrates a read cycle.

3.1.2 OUTPUT DISABLE

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. Output pins DQ_0–DQ_{15} are placed in a high-impedance state.

3.1.3 STANDBY

Deselecting the device by bringing CE# to a logic-high level (V_{IH}) places the device in standby mode, which substantially reduces device power consumption. In standby, outputs DQ_0–DQ_{15} are placed in a high-impedance state independent of OE#. If deselected during program or erase operation, the device continues to consume active power until the program or erase operation is complete.

3.1.4 DEEP POWER-DOWN / RESET

RP# at V_{IL} initiates the deep power-down mode, sometimes referred to as reset mode.

From read mode, RP# going low for time t_{PLPH} accomplishes the following:

1. deselects the memory
2. places output drivers in a high-impedance state

After return from power-down, a time t_{PHQV} is required until the initial memory access outputs are valid. A delay (t_{PHWL} or t_{PHEL}) is required after return from power-down before a write sequence can be initiated. After this wake-up interval, normal operation is restored. The CUI resets to read array mode, and the status register is set to 80H (ready).

If RP# is taken low for time t_{PLPH} during a program or erase operation, the operation will be aborted and the memory contents at the aborted location are no longer valid. After returning from an aborted operation, time t_{PHQV} or t_{PHWL}/t_{PHEL} must be met before a read or write operation is initiated respectively.

3.1.5 WRITE

A write is any command that alters the contents of the memory array. There are two write commands: Program (40H) and Erase (20H). Writing either of these commands to the internal Command User Interface (CUI) initiates a sequence of internally-timed functions that culminate in the completion of the requested task (unless that operation is aborted by either RP# being driven to V_{IL} for t_{PLRH} or an appropriate suspend command).

The Command User Interface does not occupy an addressable memory location. Instead, commands are written into the CUI using standard microprocessor write timings when WE# and CE# are low, OE# = V_{IH}, and the proper address and data (command) are presented. The command is latched on the rising edge of the first WE# or CE# pulse, whichever occurs first. Figure 16 illustrates a write operation.

Device operations are selected by writing specific commands into the CUI. Table 4 defines the available commands. Appendix B provides detailed information on moving between the different modes of operation.

3.2 Modes of Operation

The flash memory has three read modes and two write modes. The read modes are read array, read identifier, and read status. The write modes are program and block erase. Three additional modes (erase suspend to program, erase suspend to read and program suspend to read) are available only during suspended operations. These modes are reached using the commands summarized in Table 4. A comprehensive chart showing the state transitions is in Appendix B.

3.2.1 READ ARRAY

When RP# transitions from V_{IL} (reset) to V_{IH}, the device will be in the read array mode and will respond to the read control inputs (CE#, address inputs, and OE#) without any commands being written to the CUI.

When the device is in the read array mode, four control signals must be controlled to obtain data at the outputs.

- WE# must be logic high (V_{IH})
- CE# must be logic low (V_{IL})
- OE# must be logic low (V_{IL})
- RP# must be logic high (V_{IH})

In addition, the address of the desired location must be applied to the address pins.

If the device is not in read array mode, as would be the case after a program or erase operation, the Read Array command (FFH) must be written to the CUI before array reads can take place.

Table 4. Command Codes and Descriptions

Code	Device Mode	Description
00	Invalid/ Reserved	Unassigned commands that should not be used. Intel reserves the right to redefine these codes for future functions.
FF	Read Array	Places the device in read array mode, such that array data will be output on the data pins.
40	Program Set-Up	This is a two-cycle command. The first cycle prepares the CUI for a program operation. The second cycle latches addresses and data information and initiates the WSM to execute the Program algorithm. The flash outputs status register data when CE# or OE# is toggled. A Read Array command is required after programming to read array data. See Section 3.2.4.
10	Alternate Program Set-Up	(See 40H/Program Set-Up)
20	Erase Set-Up	Prepares the CUI for the Erase Confirm command. If the next command is not an Erase Confirm command, then the CUI will (a) set both SR.4 and SR.5 of the status register to a “1,” (b) place the device into the read status register mode, and (c) wait for another command. See Section 3.2.5.
D0	Program Resume Erase Resume/ Erase Confirm	If the previous command was an Erase Set-Up command, then the CUI will close the address and data latches, and begin erasing the block indicated on the address pins. If a program or erase operation was previously suspended, this command will resume that operation. During program/erase, the device will respond only to the Read Status Register, Program Suspend/Erase Suspend commands and will output status register data when CE# or OE# is toggled.

Table 4. Command Codes and Descriptions (Continued)

Code	Device Mode	Description
B0	Program Suspend Erase Suspend	Issuing this command will begin to suspend the currently executing program/erase operation. The status register will indicate when the operation has been successfully suspended by setting either the program suspend (SR.2) or erase suspend (SR.6) and the WSM Status bit (SR.7) to a "1" (ready). The WSM will continue to idle in the SUSPEND state, regardless of the state of all input control pins except RP#, which will immediately shut down the WSM and the remainder of the chip if it is driven to V_{IL}. See Sections 3.2.4.1 and 3.2.5.1.
70	Read Status Register	This command places the device into read status register mode. Reading the device will output the contents of the status register, regardless of the address presented to the device. The device automatically enters this mode after a program or erase operation has been initiated. See Section 3.2.3.
50	Clear Status Register	The WSM can set the Block Lock Status (SR.1) , V_{PP} Status (SR.3), Program Status (SR.4), and Erase Status (SR.5) bits in the status register to "1," but it cannot clear them to "0." Issuing this command clears those bits to "0."
90	Intelligent Identifier	Puts the device into the intelligent identifier read mode, so that reading the device will output the manufacturer and device codes (A_0 = 0 for manufacturer, A_0 = 1 for device, all other address inputs are ignored). See Section 3.2.2.

NOTE:
See Appendix B for mode transition information.

3.2.2 READ INTELLIGENT IDENTIFIER

To read the manufacturer and device codes, the device must be in read intelligent identifier mode, which can be reached by writing the Intelligent Identifier command (90H). Once in intelligent identifier mode, A_0 = 0 outputs the manufacturer's identification code and A_0 = 1 outputs the device code. See Table 5 for product signatures. To return to read array mode, write the Read Array command (FFH).

Table 5. Intelligent Identifier Table

Size	Mfr. ID	Device ID	
		-T (Top Boot)	-B (Bottom Boot)
4-Mbit	0089H	8894H	8895H
8-Mbit	0089H	8892H	8893H
16-Mbit	0089H	8890H	8891H

3.2.3 READ STATUS REGISTER

The device status register indicates when a program or erase operation is complete, and the success or failure of that operation. To read the status register issue the Read Status Register (70H) command to the CUI. This causes all subsequent read operations to output data from the status register until another command is written to the CUI. To return to reading from the array, issue the Read Array (FFH) command.

The status register bits are output on DQ_0–DQ_7. The upper byte, DQ_8–DQ_{15}, outputs 00H during a Read Status Register command.

The contents of the status register are latched on the falling edge of OE# or CE#. This prevents possible bus errors which might occur if status register contents change while being read. CE# or OE# must be toggled with each subsequent status read, or the status register will not indicate completion of a program or erase operation.

When the WSM is active, SR.7 will indicate the status of the WSM; the remaining bits in the status register indicate whether or not the WSM was successful in performing the desired operation (see Table 7).

3.2.3.1 Clearing the Status Register

The WSM sets status bits 1 through 7 to “1,” and clears bits 2, 6 and 7 to “0,” but cannot clear status bits 1 or 3 through 5 to “0.” Because bits 1, 3, 4 and 5 indicate various error conditions, these bits can only be cleared by the controlling CPU through the use of the Clear Status Register (50H) command. By allowing the system software to control the resetting of these bits, several operations may be performed (such as cumulatively programming several addresses or erasing multiple blocks in sequence) before reading the status register to determine if an error occurred during that series. Clear the Status Register before beginning another command or sequence. Note, again, that the Read Array command must be issued before data can be read from the memory array.

3.2.4 PROGRAM MODE

Programming is executed using a two-write sequence. The Program Setup command (40H) is written to the CUI followed by a second write which specifies the address and data to be programmed. The WSM will execute the following sequence of internally timed events:

1. Program the desired bits of the addressed memory.
2. Verify that the desired bits are sufficiently programmed.

Programming of the memory results in specific bits within an address location being changed to a “0.” If the user attempts to program “1”s, there will be no change of the memory cell contents and no error occurs.

The status register indicates programming status: while the program sequence is executing, bit 7 of the status register is a “0.” The status register can be polled by toggling either CE# or OE#. While programming, the only valid commands are Read Status Register, Program Suspend, and Program Resume.

When programming is complete, the Program Status bits should be checked. If the programming operation was unsuccessful, bit SR.4 of the status register is set to indicate a program failure. If SR.3 is set then V_{PP} was not within acceptable limits, and the WSM did not execute the program command. If SR.1 is set, a program operation was attempted to a locked block and the operation was aborted.

The status register should be cleared before attempting the next operation. Any CUI instruction can follow after programming is completed; however, to prevent inadvertent status register reads, be sure to reset the CUI to read array mode.

3.2.4.1 Suspending and Resuming Program

The Program Suspend command allows program suspension in order to read data in other locations of memory. Once the programming process starts, writing the Program Suspend command to the CUI requests that the WSM suspend the program sequence (at predetermined points in the program algorithm). The device continues to output status register data after the Program Suspend command is written. Polling status register bits SR.7 and SR.2 will determine when the program operation has been suspended (both will be set to “1”). t_{WHRH1}/t_{EHRH1} specify the program suspend latency.

A Read Array command can now be written to the CUI to read data from blocks other than that which is suspended. The only other valid commands, while program is suspended, are Read Status Register and Program Resume. After the Program Resume command is written to the flash memory, the WSM will continue with the program process and status register bits SR.2 and SR.7 will automatically be cleared. After the Program Resume command is written, the device automatically outputs status register data when read (see Figure 8, Program Suspend/Resume Flowchart). V_{PP} must remain at the same V_{PP} level used for program while in program suspend mode. RP# must also remain at $V_{IH.}$

3.2.4.2 V_{PP} Supply Voltage during Program

V_{PP} supply voltage considerations are outlined in Section 3.4

3.2.5 ERASE MODE

To erase a block, write the Erase Set-up and Erase Confirm commands to the CUI, along with an address identifying the block to be erased. This address is latched internally when the Erase Confirm command is issued. Block erasure results in all bits within the block being set to “1.” Only one block can be erased at a time.

The WSM will execute the following sequence of internally timed events to:

1. Program all bits within the block to “0.”
2. Verify that all bits within the block are sufficiently programmed to “0.”
3. Erase all bits within the block to “1.”
4. Verify that all bits within the block are sufficiently erased.

While the erase sequence is executing, bit 7 of the status register is a “0.”

When the status register indicates that erasure is complete, check the Erase Status bit to verify that the erase operation was successful. If the Erase operation was unsuccessful, SR.5 of the status register will be set to a “1,” indicating an erase failure. If V_{PP} was not within acceptable limits after the Erase Confirm command was issued, the WSM will not execute the erase sequence; instead, SR.5 of the status register is set to indicate an erase error, and SR.3 is set to a “1” to identify that V_{PP} supply voltage was not within acceptable limits.

After an erase operation, clear the Status Register (50H) before attempting the next operation. Any CUI instruction can follow after erasure is completed; however, to prevent inadvertent status register reads, it is advisable to reset the flash to read array after the erase is complete.

3.2.5.1 Suspending and Resuming Erase

Since an erase operation requires on the order of seconds to complete, an Erase Suspend command is provided to allow erase-sequence interruption in order to read data from or program data to another block in memory. Once the erase sequence is started, writing the Erase Suspend command to the CUI requests that the WSM pause the erase sequence at a predetermined point in the erase algorithm. The status register will indicate if/when the erase operation has been suspended.

A Read Array/Program command can now be written to the CUI in order to read/write data from/to blocks other than that which is suspended. The Program command can subsequently be suspended to read yet another array location. The only valid commands while erase is suspended are Erase Resume, Program, Program Resume, Read Array, or Read Status Register.

During erase suspend mode, the chip can be placed in a pseudo-standby mode by taking CE# to V_{IH}. This reduces active current consumption.

Erase Resume continues the erase sequence when CE# = V_{IL}. As with the end of a standard erase operation, the status register must be read and cleared before the next instruction is issued.

3.2.5.2 V_{PP} Supply Voltage during Erase

V_{PP} supply voltage considerations are outlined in Section 3.4.

Table 6. Command Bus Definitions

Command	Notes	First Bus Cycle			Second Bus Cycle		
		Oper	Addr	Data	Oper	Addr	Data
Read Array	5	Write	X	FFH			
Intelligent Identifier	2,3.5	Write	X	90H	Read	IA	ID
Read Status Register	5	Write	X	70H	Read	X	SRD
Clear Status Register	5	Write	X	50H			
Write (Program)	4,5	Write	X	40H	Write	PA	PD
Alternate Write (Program)	4,5	Write	X	10H	Write	PA	PD
Block Erase/Confirm	5	Write	X	20H	Write	BA	D0H
Program/Erase Suspend	5	Write	X	B0H			
Program/Erase Resume	5	Write	X	D0H			

ADDRESS
BA = Block Address
IA = Identifier Address
PA = Program Address
X = Don't Care

DATA
SRD = Status Register Data
ID = Identifier Data
PD = Program Data

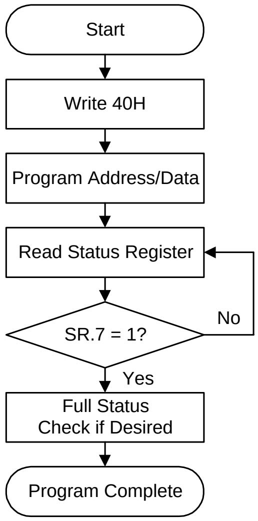
NOTES:

1. Bus operations are defined in Table 3.
2. A_0 = 0 for manufacturer code, A_0 = 1 for device code.
3. Following the Intelligent Identifier command, two read operations access manufacturer and device codes.
4. Either 40H or 10H command is valid.
5. When writing commands to the device, the upper data bus [DQ_8–DQ_{15}] should be either V_{IL} or V_{IH}, to minimize current draw.

Table 7. Status Register Bit Definition

WSMS	ESS	ES	PS	VPPS	PSS	BLS	R
7	6	5	4	3	2	1	0

	NOTES:
SR.7 WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	Check Write State Machine bit first to determine Word Program or Block Erase completion, before checking Program or Erase Status bits.
SR.6 = ERASE-SUSPEND STATUS (ESS) 1 = Erase Suspended 0 = Erase In Progress/Completed	When Erase Suspend is issued, WSM halts execution and sets both WSMS and ESS bits to “1.” ESS bit remains set to “1” until an Erase Resume command is issued.
SR.5 = ERASE STATUS (ES) 1 = Error In Block Erasure 0 = Successful Block Erase	When this bit is set to “1,” WSM has applied the max. number of erase pulses to the block and is still unable to verify successful block erasure.
SR.4 = PROGRAM STATUS (PS) 1 = Error in Word Program 0 = Successful Word Program	When this bit is set to “1,” WSM has attempted but failed to program a word.
SR.3 = V_{PP} STATUS (VPPS) 1 = V_{PP} Low Detect, Operation Abort 0 = V_{PP} OK	The V_{PP} Status bit does not provide continuous indication of V_{PP} level. The WSM interrogates V_{PP} level only after the Program or Erase command sequences have been entered, and informs the system if V_{PP} has not been switched on. The V_{PP} is also checked before the operation is verified by the WSM. The V_{PP} Status bit is not guaranteed to report accurate feedback between V_{PPLK} and V_{PPH}.
SR.2 = PROGRAM SUSPEND STATUS (PSS) 1 = Program Suspended 0 = Program in Progress/Completed	When Program Suspend is issued, WSM halts execution and sets both WSMS and PSS bits to “1.” PSS bit remains set to “1” until a Program Resume command is issued.
SR.1 = Block Lock Status 1 = Program/Erase attempted on locked block; Operation aborted 0 = No operation to locked blocks	If a program or erase operation is attempted to one of the locked blocks, this bit is set by the WSM. The operation specified is aborted and the device is returned to read status mode.
SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	These bits are reserved for future use and should be masked out when polling the Status Register.



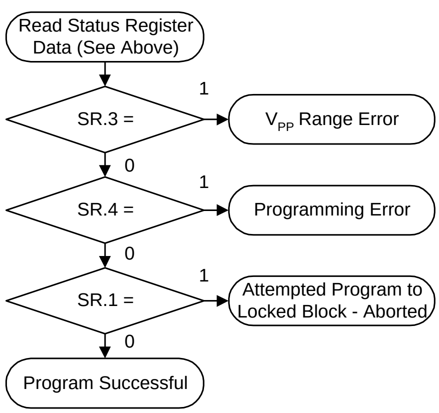
Bus Operation	Command	Comments
Write	Program Setup	Data = 40H
Write	Program	Data = Data to Program Addr = Location to Program
Read		Status Register Data Toggle CE# or OE# to Update Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent programming operations.

SR Full Status Check can be done after each program or after a sequence of program operations.

Write FFH after the last program operation to reset device to read array mode.

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4 1 = V_{PP} Program Error
Standby		Check SR.1 1 = Attempted Program to Locked Block - Program Aborted

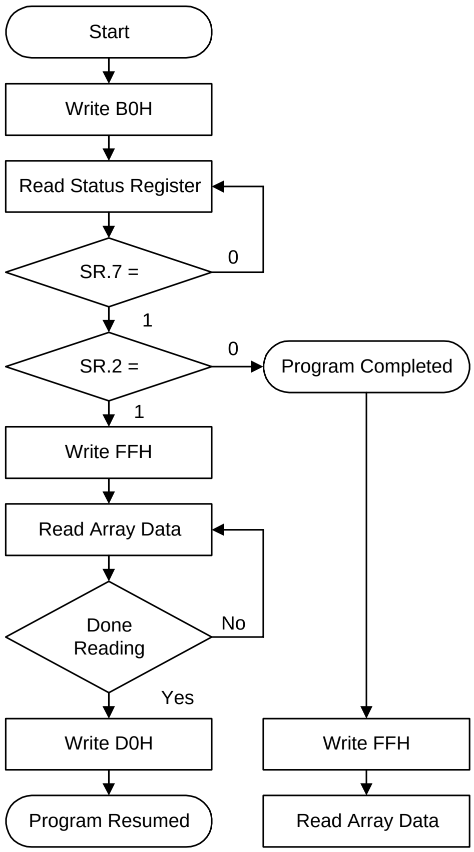
SR.3 MUST be cleared, if set during a program attempt, before further attempts are allowed by the Write State Machine.

SR.1, SR.3 and SR.4 are only cleared by the Clear Staus Register Command, in cases where multiple bytes are programmed before full status is checked.

If an error is detected, clear the status register before attempting retry or other error recovery.

0580_07

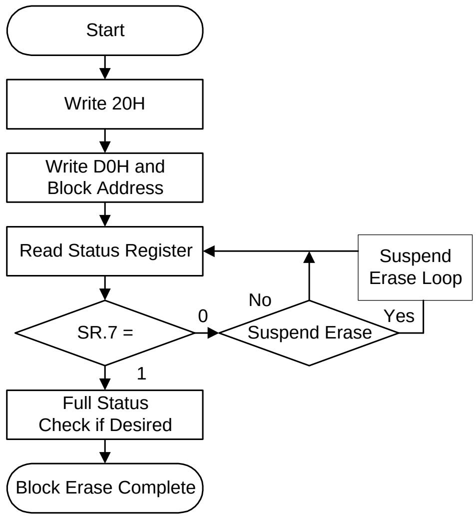
Figure 7. Automated Word Programming Flowchart



Bus Operation	Command	Comments
Write	Program Suspend	Data = B0H Addr = X
Read		Status Register Data Toggle CE# or OE# to Update Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.2 1 = Program Suspended 0 = Program Completed
Write	Read Array	Data = FFH Addr = X
Read		Read array data from block other than the one being programmed.
Write	Program Resume	Data = D0H Addr = X

0580_08

Figure 8. Program Suspend/Resume Flowchart



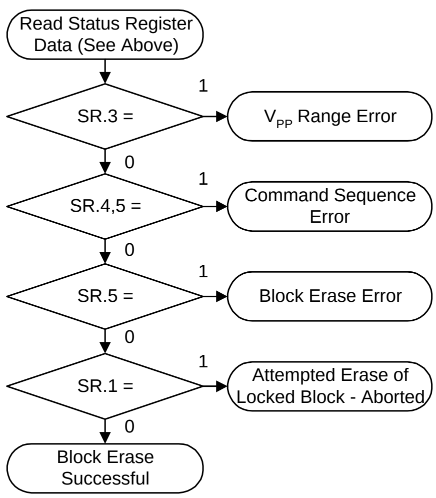
Bus Operation	Command	Comments
Write	Erase Setup	Data = 20H Addr = Within Block to Be Erased
Write	Erase Confirm	Data = D0H Addr = Within Block to Be Erased
Read		Status Register Data Toggle CE# or OE# to Update Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent block erasures.

Full Status Check can be done after each block erase or after a sequence of block erasures.

Write FFH after the last write operation to reset device to read array mode.

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4,5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error
Standby		Check SR.1 1 = Attempted Erase of Locked Block - Erase Aborted

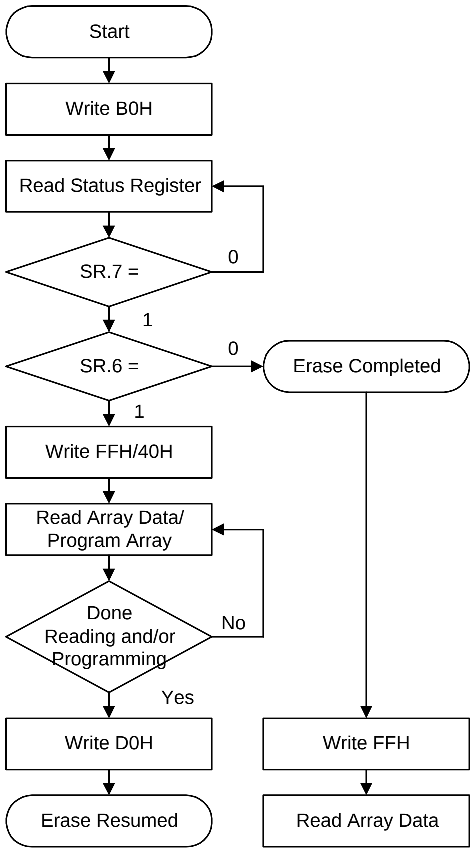
SR. 1 and 3 MUST be cleared, if set during an erase attempt, before further attempts are allowed by the Write State Machine.

SR.1, 3, 4, 5 are only cleared by the Clear Staus Register Command, in cases where multiple bytes are erased before full status is checked.

If an error is detected, clear the status register before attempting retry or other error recovery.

0580_09

Figure 9. Automated Block Erase Flowchart



Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0H Addr = X
Read		Status Register Data Toggle CE# or OE# to Update Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.6 1 = Erase Suspended 0 = Erase Completed
Write	Read Array	Data = FFH Addr = X
Read		Read array data from block other than the one being erased.
Program		Program data to block other than the one being erased.
Write	Erase Resume	Data = D0H Addr = X

0580_10

Figure 10. Erase Suspend/Resume Flowchart

3.3 Block Locking

The Smart 3 Advanced Boot Block flash memory architecture features two hardware-lockable parameter blocks so that the kernel code for the system can be kept secure while other parameter blocks are programmed or erased as necessary.

3.3.1 $V_{PP} = V_{IL}$ FOR COMPLETE PROTECTION

The V_{PP} programming voltage can be held low for complete write protection of all blocks in the flash device. When V_{PP} is below V_{PPLK}, any program or erase operation will result in a error, prompting the corresponding Status Register bit (SR.3) to be set.

3.3.2 WP# = V_{IL} FOR BLOCK LOCKING

The lockable blocks are locked when WP# = V_{IL}; any program or erase operation to a locked block will result in an error, which will be reflected in the status register. For top configuration, the top two parameter blocks (blocks #37 and #38 for the 16-Mbit, blocks #21 and #22 for the 8-Mbit, and blocks #13 and #14 for the 4-Mbit) are lockable. For the bottom configuration, the bottom two parameter blocks (blocks #0 and #1 for 4-/8-/16-Mbit) are lockable. Unlocked blocks can be programmed or erased normally (unless V_{PP} is below V_{PPLK}).

3.3.3 WP# = V_{IH} FOR BLOCK UNLOCKING

WP# = V_{IH} unlocks all lockable blocks.

These blocks can now be programmed or erased.

Note that RP# does not override WP# locking as in previous Boot Block devices. WP# controls all block locking and V_{PP} provides protection against spurious writes. Table 8 defines the write protection methods.

3.4 V_{PP} Program and Erase Voltages

Intel's Smart 3 products provide in-system programming and erase at 2.7V–3.6V V_{PP}. For customers requiring fast programming in their manufacturing environment, Smart 3 includes an additional low-cost, backward-compatible 12V programming feature.

The 12V V_{PP} mode enhances programming performance during the short period of time typically found in manufacturing processes; however, it is not intended for extended use. 12V may be applied to V_{PP} during program and erase operations for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. V_{PP} may be connected to 12V for a total of 80 hours maximum. Stressing the device beyond these limits may cause permanent damage.

Table 8. Write Protection Truth Table for Advanced Boot Block Flash Memory Family

V_{PP}	WP#	RP#	Write Protection Provided
X	X	V_{IL}	All Blocks Locked
V_{IL}	X	V_{IH}	All Blocks Locked
$\geq V_{PPLK}$	V_{IL}	V_{IH}	Lockable Blocks Locked
$\geq V_{PPLK}$	V_{IH}	V_{IH}	All Blocks Unlocked

3.5 Power Consumption

While in operation, the flash device consumes active power. However, Intel Flash devices have a three-tiered approach to power savings that can significantly reduce overall system power consumption. The Automatic Power Savings (APS) feature reduces power consumption when the device is idle. If the CE# is deasserted, the flash enters its standby mode, where current consumption is even lower. If RP# = V_{IL} the flash enters a deep power-down mode, where current is at a minimum. The combination of these features can minimize overall memory power consumption, and therefore, overall system power consumption.

3.5.1 ACTIVE POWER

With CE# at a logic-low level and RP# at a logic-high level, the device is in the active mode. Refer to the DC Characteristics tables for I_{CC} current values. Active power is the largest contributor to overall system power consumption. Minimizing the active current could have a profound effect on system power consumption, especially for battery-operated devices.

3.5.2 AUTOMATIC POWER SAVINGS (APS)

Automatic Power Savings provides low-power operation during active mode. Power Reduction Control (PRC) circuitry allows the flash to put itself into a low current state when not being accessed. After data is read from the memory array, PRC logic controls the device's power consumption by entering the APS mode where typical I_{CC} current is comparable to I_{CCS}. The flash stays in this static state with outputs valid until a new location is read.

APS reduces active current to standby current levels for 2.7V–3.6V CMOS input levels.

3.5.3 STANDBY POWER

With CE# at a logic-high level (V_{IH}) and the CUI in read mode, the flash memory is in standby mode, which disables much of the device's circuitry and substantially reduces power consumption. Outputs (DQ_0–DQ_{15}) are placed in a high-impedance state independent of the status of the OE# signal. If CE# transitions to a logic-high level during erase or program operations, the device will continue to perform the operation and consume corresponding active power until the operation is completed.

System engineers should analyze the breakdown of standby time versus active time and quantify the respective power consumption in each mode for their specific application. This will provide a more accurate measure of application-specific power and energy requirements.

3.5.4 DEEP POWER-DOWN MODE

The deep power-down mode of the Smart 3 Advanced Boot Block products switches the device into a low power savings mode, which is especially important for battery-based devices. This mode is activated when RP# = V_{IL} (GND $\pm$ 0.2V).

During read modes, RP# going low de-selects the memory and places the output drivers in a high impedance state. Recovery from the deep power-down state, requires a minimum time equal to t_{PHQV} (see AC Characteristics table).

During program or erase modes, RP# transitioning low will abort the operation, but the memory contents of the address being programmed or the block being erased are no longer valid as the data integrity has been compromised by the abort.

During deep power-down, all internal circuits are switched to a low power savings mode (RP# transitioning to V_{IL} or turning off power to the device clears the status register).

3.6 Power-Up/Down Operation

The device is protected against accidental block erasure or programming during power transitions. Power supply sequencing is not required, since the device is indifferent as to which power supply, V_{PP} or V_{CC}, powers-up first.

3.6.1 RP# CONNECTED TO SYSTEM RESET

The use of RP# during system reset is important with automated program/erase devices since the system expects to read from the flash memory when it comes out of reset. If a CPU reset occurs without a flash memory reset, proper CPU initialization will not occur because the flash memory may be providing status information instead of array data. Intel recommends connecting RP# to the system CPU RESET# signal to allow proper CPU/flash initialization following system reset.

System designers must guard against spurious writes when V_{CC} voltages are above V_{LKO} and V_{PP} is active. Since both WE# and CE# must be low for a command write, driving either signal to V_{IH} will inhibit writes to the device. The CUI architecture provides additional protection since alteration of memory contents can only occur after successful completion of the two-step command sequences. The device is also disabled until RP# is brought to V_{IH}, regardless of the state of its control inputs. By holding the device in reset (RP# connected to system PowerGood) during power-up/down, invalid bus conditions during power-up can be masked, providing yet another level of memory protection.

3.6.2 V_{CC}, V_{PP} AND RP# TRANSITIONS

The CUI latches commands as issued by system software and is not altered by V_{PP} or CE# transitions or WSM actions. Its default state upon power-up, after exit from deep power-down mode or after V_{CC} transitions above V_{LKO} (Lockout voltage), is read array mode.

After any program or block erase operation is complete (even after V_{PP} transitions down to V_{PPLK}), the CUI must be reset to read array mode via the Read Array command if access to the flash memory array is desired.

Refer to *AP-617 Additional Flash Data Protection Using V_{PP}, RP#, and WP#* for a circuit-level description of how to implement the protection schemes discussed in Section 3.5.

3.7 Power Supply Decoupling

Flash memory's power switching characteristics require careful device decoupling. System designers should consider three supply current issues:

1. Standby current levels (I_{CCS})
2. Active current levels (I_{CCR})
3. Transient peaks produced by falling and rising edges of CE#.

Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress these transient voltage peaks. Each flash device should have a 0.1 µF ceramic capacitor connected between each V_{CC} and GND, and between its V_{PP} and GND. These high-frequency, inherently low-inductance capacitors should be placed as close as possible to the package leads.

3.7.1 V_{PP} TRACE ON PRINTED CIRCUIT BOARDS

Designing for in-system writes to the flash memory requires special consideration of the V_{PP} power supply trace by the printed circuit board designer. The V_{PP} pin supplies the flash memory cells current for programming and erasing. V_{PP} trace widths and layout should be similar to that of V_{CC}. Adequate V_{PP} supply traces, and decoupling capacitors placed adjacent to the component, will decrease spikes and overshoots.

4.0 ABSOLUTE MAXIMUM RATINGS*

Extended Operating Temperature

During Read .... –40°C to +85°C

During Block Erase and Program............................ –40°C to +85°C

Temperature Under Bias .... –40°C to +85°C

Storage Temperature................... –65°C to +125°C

Voltage on Any Pin (except V_{CC}, V_{CCQ} and V_{PP}) with Respect to GND .... –0.5V to +5.0V[1]

V_{PP} Voltage (for Block Erase and Program) with Respect to GND ....–0.5V to +13.5V[1,2,4]

V_{CC} and V_{CCQ} Supply Voltage with Respect to GND .... –0.2V to +5.0V[1]

Output Short Circuit Current...................... 100 mA[3]

NOTICE: This datasheet contains preliminary information on new products in production. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

** WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may effect device reliability.*

NOTES:

1. Minimum DC voltage is –0.5V on input/output pins. During transitions, this level may undershoot to –2.0V for periods < 20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5V which, during transitions, may overshoot to V_{CC} + 2.0V for periods < 20 ns.
2. Maximum DC voltage on V_{PP} may overshoot to +14.0V for periods < 20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.
4. V_{PP} Program voltage is normally 2.7V–3.6V. Connection to supply of 11.4V–12.6V can only be done for 1000 cycles on the main blocks and 2500 cycles on the parameter blocks during program/erase. V_{PP} may be connected to 12V for a total of 80 hours maximum. See Section 3.4 for details.

5.0 OPERATING CONDITIONS (V_{CCQ} = 2.7V–3.6V)

Table 9. Temperature and Voltage Operating Conditions4

Symbol	Parameter	Notes	Min	Max	Units
T_A	Operating Temperature		–40	+85	°C
V_{CC}	2.7V–3.6V V_{CC} Supply Voltage	1,4	2.7	3.6	Volts
V_{CCQ}	2.7V–3.6V I/O Supply Voltage	1,2,4	2.7	3.6	Volts
V_{PP1}	Program and Erase Voltage	4	2.7	3.6	Volts
V_{PP2}		3	11.4	12.6	Volts
Cycling	Block Erase Cycling	5	10,000		Cycles

NOTES:

1. See DC Characteristics tables for voltage range-specific specifications.
2. The voltage swing on the inputs, V_{IN} is required to match V_{CCQ}.
3. Applying V_{PP} = 11.4V–12.6V during a program/erase can only be done for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. V_{PP} may be connected to 12V for a total of 80 hours maximum. See Section 3.4 for details.
4. V_{CC}, V_{CCQ} and V_{PP1} must share the same supply when all three are between 2.7V and 3.6V.
5. For operating temperatures of –25°C– +85°C the device is projected to have a minimum block erase cycling of 10,000 to 30,000 cycles.

5.1 DC Characteristics: V_{CCQ} = 2.7V–3.6V

Table 10. DC Characteristics

Sym	Parameter	Notes	V_{CC} = 2.7V–3.6V		Unit	Test Conditions
			Typ	Max		
I_{LI}	Input Load Current	1		± 1.0	µA	$V_{CC} = V_{CC}Max = V_{CCQ}Max$ $V_{IN} = V_{CCQ}$ or GND
I_{LO}	Output Leakage Current	1		± 10	µA	$V_{CC} = V_{CC}Max = V_{CCQ}Max$ $V_{IN} = V_{CCQ}$ or GND
I_{CCS}	V_{CC} Standby Current	1,7	20	50	µA	**CMOS INPUTS** $V_{CC} = V_{CC}Max = V_{CCQ}Max$ CE# = RP# = V_{CCQ}
I_{CCD}	V_{CC} Deep Power-Down Current	1,7	1	10	µA	**CMOS INPUTS** $V_{CC} = V_{CC}Max = V_{CCQ}Max$ $V_{IN} = V_{CCQ}$ or GND RP# = GND ± 0.2V
I_{CCR}	V_{CC} Read Current	1,5,7	10	20	mA	**CMOS INPUTS** $V_{CC} = V_{CC}Max = V_{CCQ}Max$ OE# = V_{IH} , CE# =V_{IL} f = 5 MHz, I_{OUT} = 0 mA Inputs = V_{IL} or V_{IH}
I_{CCW}	V_{CC} Program Current	1,4,7	8	20	mA	$V_{PP} = V_{PPH1}$ (3V) Program in Progress
			8	20	mA	$V_{PP} = V_{PPH2}$ (12V) Program in Progress
I_{CCE}	V_{CC} Erase Current	1,4,7	8	20	mA	$V_{PP} = V_{PPH1}$ (3V) Erase in Progress
			8	20	mA	$V_{PP} = V_{PPH2}$ (12V) Erase in Progress
I_{CCES}	V_{CC} Erase Suspend Current	1,2,4,7	20	50	µA	CE# = V_{IH} Erase Suspend in Progress
I_{CCWS}	V_{CC} Program Suspend Current	1,2,4,7	20	50	µA	CE# = V_{IH} Program Suspend in Progress
I_{PPD}	V_{PP} Deep Power-Down Current	1	0.2	5	µA	RP# = GND ± 0.2V
I_{PPR}	V_{PP} Read Current	1	2	±50	µA	$V_{PP} \leq V_{CC}$

Table 10. DC Characteristics (Continued)

Sym	Parameter	Notes	V_{CC} = 2.7V–3.6V		Unit	Test Conditions
			Typ	Max		
I_{PPW}	V_{PP} Program Current	1,4	15	40	mA	$V_{PP} = V_{PPH1}$ (3V) Program in Progress
			10	25	mA	$V_{PP} = V_{PPH2}$ (12V) Program in Progress
I_{PPE}	V_{PP} Erase Current	1,4	13	25	mA	$V_{PP} = V_{PPH1}$ (3V) Erase in Progress
			8	25	mA	$V_{PP} = V_{PPH2}$ (12V) Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current	1,4	50	200	µA	$V_{PP} = V_{PPH1}$ or V_{PPH2} Erase Suspend in Progress
I_{PPWS}	V_{PP} Program Suspend Current	1,4	50	200	µA	$V_{PP} = V_{PPH1}$ or V_{PPH2} Program Suspend in Progress

Table 10. DC Characteristics (Continued)

Sym	Parameter	Notes	V_{CC} = 2.7V–3.6V		Unit	Test Conditions
			Min	Max		
V_{IL}	Input Low Voltage		–0.4	0.4	V	
V_{IH}	Input High Voltage		V_{CCQ} – 0.4V		V	
V_{OL}	Output Low Voltage			0.10	V	V_{CC} = V_{CC}Min = V_{CCQ}Min I_{OL} = 100 μA
V_{OH}	Output High Voltage		V_{CCQ} – 0.1V		V	V_{CC} = V_{CC}Min = V_{CCQ}Min I_{OH} = –100 μA
V_{PPLK}	V_{PP} Lock-Out Voltage	3	1.5		V	Complete Write Protection
V_{PPH1}	V_{PP} during Prog/Erase Operations	3	2.7	3.6	V	
V_{PPH2}		3,6	11.4	12.6	V	
V_{LKO}	V_{CC} Program/Erase Lock Voltage		1.5		V	
V_{LKO2}	V_{CCQ} Program/Erase Lock Voltage		1.2		V	

NOTES:

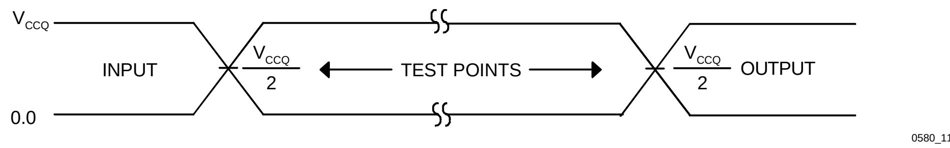
1. All currents are in RMS unless otherwise noted. Typical values at nominal V_{CC}, T_A = +25°C.
2. I_{CCES} and I_{CCWS} are specified with device de-selected. If device is read while in erase suspend, current draw is sum of I_{CCES} and I_{CCR}. If the device is read while in program suspend, current draw is the sum of I_{CCWA} and I_{CCR}.
3. Erase and Program are inhibited when V_{PP} < V_{PPLK} and not guaranteed outside the valid V_{PP} ranges of V_{PPH1} and V_{PPH2}.
4. Sampled, not 100% tested.
5. Automatic Power Savings (APS) reduces I_{CCR} to approximately standby levels in static operation (CMOS inputs).
6. Applying V_{PP} = 11.4V–12.6V during program/erase can only be done for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. V_{PP} may be connected to 12V for a total of 80 hours maximum. See Section 3.4 for details.
7. Includes the sum of V_{CC} and V_{CCQ} current.

Table 11. Capacitance (T_A = 25°C, f = 1 MHz)

Sym	Parameter	Notes	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	1	6	8	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	1	10	12	pF	V_{OUT} = 0V

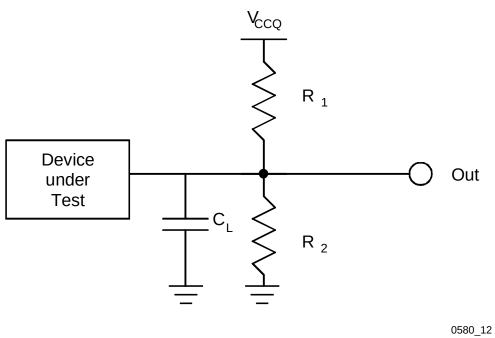
NOTE:

1. Sampled, not 100% tested.



NOTE:
AC test inputs are driven at V_{CCQ} for a logic “1” and 0.0V for a logic “0.” Input timing begins, and output timing ends, at $V_{CCQ}/2$. Input rise and fall times (10%–90%) <10 ns. Worst case speed conditions are when V_{CCQ} = 2.7V.

Figure 11. 2.7V–3.6V Input Range and Measurement Points



NOTE:
See table for component values.

Figure 12. Test Configuration

Test Configuration Component Values for Worst Case Speed Conditions

Test Configuration	C_L (pF)	R_1 (Ω)	R_2 (Ω)
2.7V Standard Test	50	25K	25K

NOTE:
C_L includes jig capacitance.

6.0 OPERATING CONDITIONS (V_{CCQ} = 1.8V–2.2V)

Table 12. Temperature and V_{CC} Operating Conditions

Symbol	Parameter	Notes	Min	Max	Units
T_A	Operating Temperature		–40	+85	°C
V_{CC1}	2.7V–2.85V V_{CC} Supply Voltage	1	2.7	2.85	Volts
V_{CC2}	2.7V–3.3V V_{CC} Supply Voltage	1	2.7	3.3	Volts
V_{CCQ}	1.8V–2.2V I/O Supply Voltage	1,4	1.8	2.2	Volts
V_{PP1}	Program and Erase Voltage	1	2.7	2.85	Volts
V_{PP2}		1	2.7	3.3	Volts
V_{PP3}		1,2	11.4	12.6	Volts
Cycling	Block Erase Cycling	3	10,000		Cycles

NOTES:

1. See DC Characteristics tables for voltage range-specific specifications.
2. Applying V_{PP} = 11.4V–12.6V during program/erase can only be done for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter. V_{PP} may be connected to 12V for a total of 80 hours maximum. See Section 3.4 for details.
3. For operating temperatures of –25°C– +85°C the device is projected to have a minimum block erase cycling of 10,000 to 30,000 cycles.
4. The voltage swing on the inputs, V_{IN} is required to match V_{CCQ}.

6.1 DC Characteristics: V_{CCQ} = 1.8V–2.2V

These tables are valid for the following power supply combinations only:

1. V_{CC1} and V_{CCQ} and (V_{PP1} or V_{PP3})
2. V_{CC2} and V_{CCQ} and (V_{PP2} or V_{PP3})

Wherever the input voltage V_{IN} is mentioned, it is required that V_{IN} matches the chosen V_{CCQ}.

Table 13. DC Characteristics: V_{CCQ} = 1.8V–2.2V

Sym	Parameter	Notes	V_{CC1}: 2.7V–2.85V V_{CC2}: 2.7V–3.3V		Unit	Test Conditions
			Typ	Max		
I_{LI}	Input Load Current	1		± 1.0	µA	$V_{CC} = V_{CC}$Max $V_{CCQ} = V_{CCQ}$Max $V_{IN} = V_{CCQ}$ or GND
I_{LO}	Output Leakage Current	1		± 10	µA	$V_{CC} = V_{CC}$ Max $V_{CCQ} = V_{CCQ}$Max $V_{IN} = V_{CCQ}$ or GND
I_{CCS}	V_{CC} Standby Current	1,7	20	50	µA	**CMOS INPUTS** $V_{CC} = V_{CC1}$ Max (2.7V–2.85V) $V_{CCQ} = V_{CCQ}$Max CE# = RP# = V_{CCQ}
			150	250	µA	**CMOS INPUTS** $V_{CC} = V_{CC2}$ Max (2.7V–3.3V) $V_{CCQ} = V_{CCQ}$Max CE# = RP# = V_{CCQ}
I_{CCD}	V_{CC} Deep Power-Down Current	1,7	1	10	µA	**CMOS INPUTS** $V_{CC} = V_{CC}$Max (V_{CC1} or V_{CC2}) $V_{CCQ} = V_{CCQ}$Max $V_{IN} = V_{CCQ}$ or GND RP# = GND ± 0.2V
I_{CCR}	V_{CC} Read Current	1,5,7	8	18	mA	**CMOS INPUTS** $V_{CC} = V_{CC1}$Max (2.7V–2.85V) $V_{CCQ} = V_{CCQ}$Max OE# = V_{IH}, CE# = V_{IL} f = 5 MHz, I_{OUT} = 0 mA Inputs = V_{IL} or V_{IH}
			12	23	mA	**CMOS INPUTS** $V_{CC} = V_{CC2}$Max (2.7V–3.3V) $V_{CCQ} = V_{CCQ}$Max OE# = V_{IH}, CE# = V_{IL} f = 5 MHz, I_{OUT} = 0 mA Inputs = GND ± 0.2V or V_{CCQ}

Table 13. DC Characteristics: V_{CCQ} = 1.8V–2.2V (Continued)

Sym	Parameter	Notes	V_{CC1}: 2.7V–2.85V V_{CC2}: 2.7V–3.3V Typ	Max	Unit	Test Conditions
I_{CCW}	V_{CC} Program Current	1,4,7	8	20	mA	$V_{PP} = V_{PPH1}$ or V_{PPH2} Program in Progress
			8	20	mA	$V_{PP} = V_{PPH3}$ (12V) Program in Progress
I_{CCE}	V_{CC} Erase Current	1,4,7	8	20	mA	$V_{PP} = V_{PPH1}$ or V_{PPH2} Erase in Progress
			8	20	mA	$V_{PP} = V_{PPH3}$ (12V) Erase in Progress
I_{CCES}	V_{CC} Erase Suspend Current	1,2,4,7	20	50	µA	CE# = V_{IH} Erase Suspend in Progress
I_{CCWS}	V_{CC} Program Suspend Current	1,2,4,7	20	50	µA	CE# = V_{IH} Program Suspend in Progress
I_{PPD}	V_{PP} Deep Power-Down Current	1	0.2	5	µA	RP# = GND ± 0.2V
I_{PPR}	V_{PP} Read and Standby Current	1	2	±50	µA	$V_{PP} \leq V_{CC}$
I_{PPW}	V_{PP} Program Current	1,4	15	40	mA	$V_{PP} = V_{PPH1}$ or V_{PPH2} Program in Progress
			10	25	mA	$V_{PP} = V_{PPH3}$ (12V) Program in Progress
I_{PPE}	V_{PP} Erase Current	1,4	13	25	mA	$V_{PP} = V_{PPH1}$ or V_{PPH2} Erase in Progress
			8	25	mA	$V_{PP} = V_{PPH3}$ (12V) Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current	1	50	200	µA	$V_{PP} = V_{PPH1}$, V_{PPH2} , or V_{PPH3} Erase Suspend in Progress
I_{PPWS}	V_{PP} Program Suspend Current	1	50	200	µA	$V_{PP} = V_{PPH1}$, V_{PPH2} , or V_{PPH3} Program Suspend in Progress

Table 13. DC Characteristics: V_{CCQ} = 1.8V–2.2V (Continued)

Sym	Parameter	Notes	V_{CC1}: 2.7V–2.85V V_{CC2}: 2.7V–3.3V Min	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage		–0.2	0.2	V	
V_{IH}	Input High Voltage		V_{CCQ} – 0.2V		V	
V_{OL}	Output Low Voltage		–0.10	0.10	V	V_{CC} = V_{CC}Min V_{CCQ} = V_{CCQ}Min I_{OL} = 100 µA
V_{OH}	Output High Voltage		V_{CCQ} – 0.1V		V	V_{CC} = V_{CC}Min V_{CCQ} = V_{CCQ}Min I_{OL} = –100 µA
V_{PPLK}	V_{PP} Lock-Out Voltage	3	1.5		V	Complete Write Protection
V_{PPH1}	V_{PP} during Program/ Erase Operations	3	2.7	2.85	V	
V_{PPH2}		3	2.7	3.3	V	
V_{PPH3}		3,6	11.4	12.6	V	
V_{LKO1}	V_{CC} Program/Erase Lock Voltage		1.5		V	
V_{LKO2}	V_{CCQ} Program/Erase Lock Voltage		1.2		V	

NOTES:

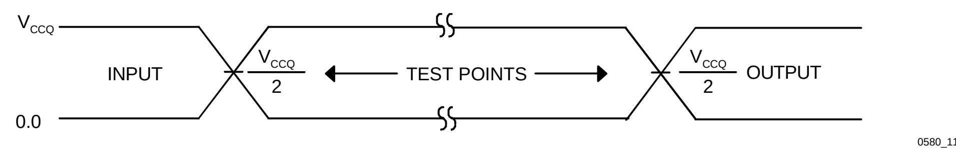
1. All currents are in RMS unless otherwise noted. Typical values at nominal V_{CC}, T_A = +25°C.
2. I_{CCES} and I_{CCWS} are specified with device de-selected. If device is read while in erase suspend, current draw is I_{CCR}. If the device is read while in program suspend , current draw is I_{CCR}.
3. Erases and Writes inhibited when $V_{PP} \leq V_{PPLK}$, and not guaranteed outside the valid V_{PP} ranges of V_{PPH1},V_{PPH2}. or V_{PPH3}.
4. Sampled, not 100% tested.
5. Automatic Power Savings (APS) reduces I_{CCR} to approximately standby levels in static operation (CMOS inputs).
6. Applying V_{PP} = 11.4V–12.6V during program/erase can only be done for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. V_{PP} may be connected to 12V for a total of 80 hours maximum. See Section 3.4 for details.
7. Includes the sum of V_{CC} and V_{CCQ} current

Table 14. Capacitance (T_A = 25°C, f = 1 MHz)

Sym	Parameter	Notes	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	1	6	8	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	1	10	12	pF	V_{OUT} = 0V

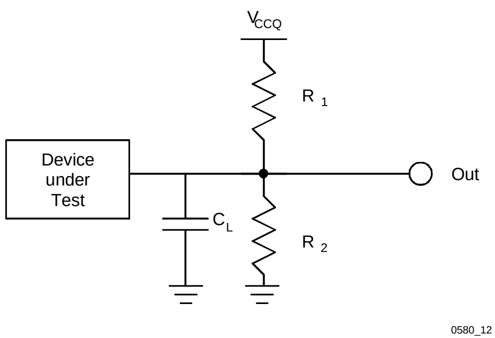
NOTE:

1. Sampled, not 100% tested.



NOTE:
AC test inputs are driven at V_{CCQ} for a logic "1" and 0.0V for a logic "0." Input timing begins, and output timing ends, at $V_{CCQ}/2$. Input rise and fall times (10%–90%) <10 ns. For worst case speed conditions V_{CCQ} = 1.8V.

Figure 13. 1.8V—2.2V Input Range and Measurement Points



NOTE:
See table for component values.

Figure 14. Test Configuration

Test Configuration Component Values for Worst Case Speed Conditions

Test Configuration	C_L (pF)	R_1 (Ω)	R_2 (Ω)
1.8V Standard Test	50	16.7K	16.7K

NOTE:
C_L includes jig capacitance.

7.0 AC CHARACTERISTICS

AC Characteristics are applicable to both V_{CCQ} ranges.

Table 15. AC Characteristics: Read Operations (Extended Temperature)

#	Symbol	Parameter	Load	C_L = 50 pF				Units
			V_{CC}	2.7V–3.6V[4]				
			Prod	120 ns		150 ns		
			Notes	Min	Max	Min	Max	
R1	t_{AVAV}	Read Cycle Time		120		150		ns
R2	t_{AVQV}	Address to Output Delay			120		150	ns
R3	t_{ELQV}	CE# to Output Delay	2		120		150	ns
R4	t_{GLQV}	OE# to Output Delay	2		65		65	ns
R5	t_{PHQV}	RP# to Output Delay			600		600	ns
R6	t_{ELQX}	CE# to Output in Low Z	3	0		0		ns
R7	t_{GLQX}	OE# to Output in Low Z	3	0		0		ns
R8	t_{EHQZ}	CE# to Output in High Z	3		40		40	ns
R9	t_{GHQZ}	OE# to Output in High Z	3		40		40	ns
R10	t_{OH}	Output Hold from Address, CE#, or OE# Change, Whichever Occurs First	3	0		0		ns

NOTES:

1. See AC Input/Output Reference Waveform for timing measurements.
2. OE# may be delayed up to t_{ELQV}–t_{GLQV} after the falling edge of CE# without impact on t_{ELQV}.
3. Sampled, but not 100% tested.
4. See Test Configuration (Figures 12 and 14), 2.7V–3.6V and 1.8V–2.2V Standard Test component values.

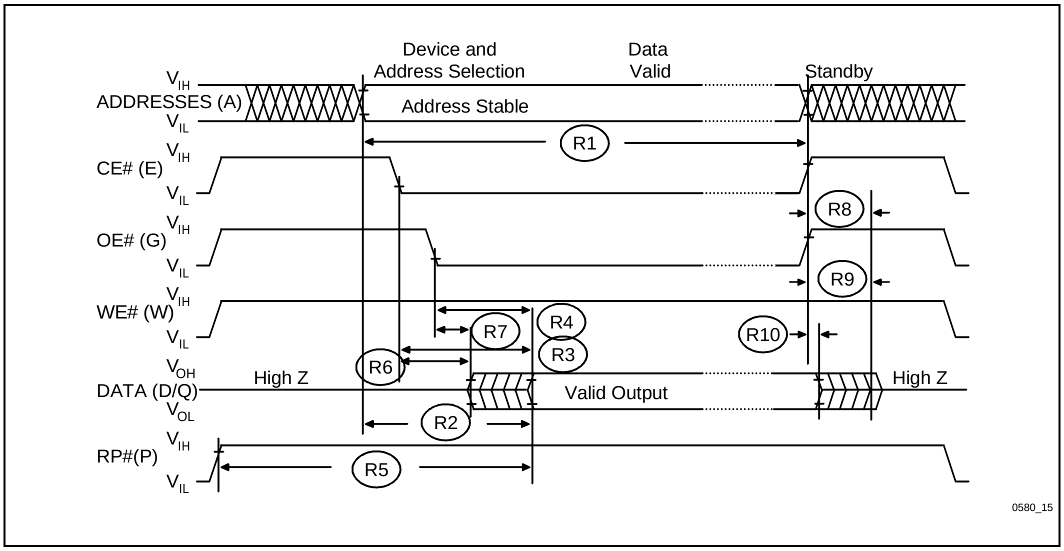


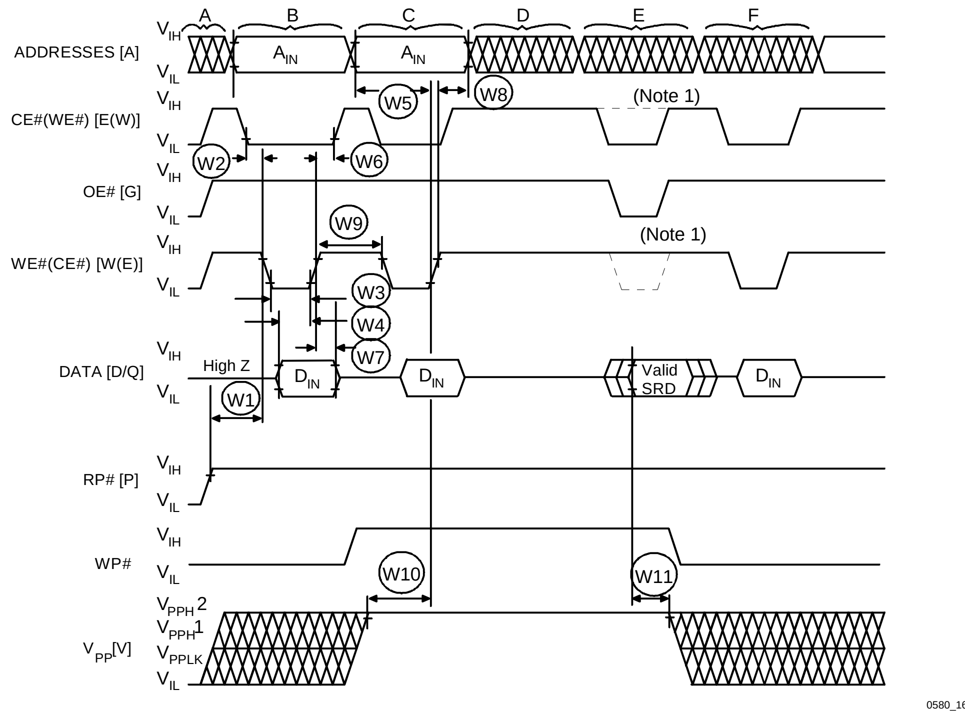
Figure 15. AC Waveform: Read Operations

Table 16. AC Characteristics: Write Operations (Extended Temperature)[1]

#	Symbol	Parameter	Load	50 pF				Units
			V_{CC}	2.7V–3.6V[5]		2.7V-3.6V[5]		
			Prod	120 ns		150 ns		
			Notes	Min	Max	Min	Max	
W1	t_{PHWL} t_{PHEL}	RP# High Recovery to WE# (CE#) Going Low		600		600		ns
W2	t_{ELWL} t_{WLEL}	CE# (WE#) Setup to WE# (CE#) Going Low		0		0		ns
W3	t_{WLWH} t_{ELEH}	WE# (CE#) Pulse Width		90		90		ns
W4	t_{DVWH} t_{DVEH}	Data Setup to WE# (CE#) Going High	3	70		70		ns
W5	t_{AVWH} t_{AVEH}	Address Setup to WE# (CE#) Going High	2	90		90		ns
W6	t_{WHEH} t_{EHWH}	CE# (WE#) Hold Time from WE# (CE#) High		0		0		ns
W7	t_{WHDX} t_{EHDX}	Data Hold Time from WE# (CE#) High	3	0		0		ns
W8	t_{WHAX} t_{EHAX}	Address Hold Time from WE# (CE#) High	2	0		0		ns
W9	t_{WHWL} t_{EHEL}	WE# (CE#) Pulse Width High		30		30		ns
W10	t_{VPWH} t_{VPEH}	V_{PP} Setup to WE# (CE#) Going High	4	200		200		ns
W11	t_{QVVL}	V_{PP} Hold from Valid SRD	4	0		0		ns
	t_{LOCK}	Block Unlock / Lock Delay	4, 6		200		200	ns

NOTES:

1. Read timing characteristics during program suspend and erase suspend are the same as during read-only operations. Refer to AC Characteristics during read mode.
2. Refer to command definition table for valid A_{IN} (Table 6).
3. Refer to command definition table for valid D_{IN} (Table 6).
4. Sampled, but not 100% tested.
5. See Test Configuration (Figures 12 and 14), 2.7V–3.6V and 1.8V–2.2V Standard Test component values.
6. Time t_{LOCK} is required for successful locking and unlocking of all lockable blocks.



NOTES:

1. CE# must be toggled low when reading Status Register Data. WE# must be inactive (high) when reading Status Register Data.

A. V_{CC} Power-Up and Standby.
B. Write Program or Erase Setup Command.
C. Write Valid Address and Data (for Program) or Erase Confirm Command.
D. Automated Program or Erase Delay.
E. Read Status Register Data (SRD): reflects completed program/erase operation.
F. Write Read Array Command.

Figure 16. AC Waveform: Program and Erase Operations

7.1 Reset Operations

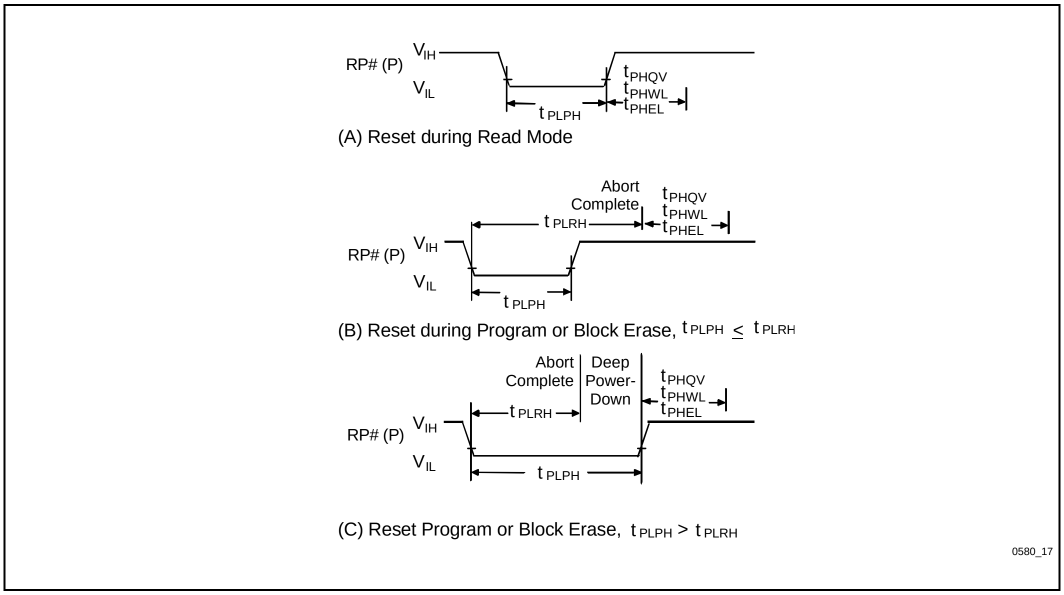


Figure 17. AC Waveform: Deep Power-Down/Reset Operation

Reset Specifications

Symbol	Parameter	Notes	V_{CC} = 2.7–3.6V Min	Max	Unit
t_{PLPH}	RP# Low to Reset during Read (If RP# is tied to V_{CC}, this specification is not applicable)	1,3	100		ns
t_{PLRH}	RP# Low to Reset during Block Erase or Program	2,3		22	µs

NOTES:

1. If t_{PLPH} is < 100 ns the device may still RESET but this is not guaranteed.
2. If RP# is asserted while a block erase or word program operation is not executing, the reset will complete within 100 ns.
3. Sampled, but not 100% tested.

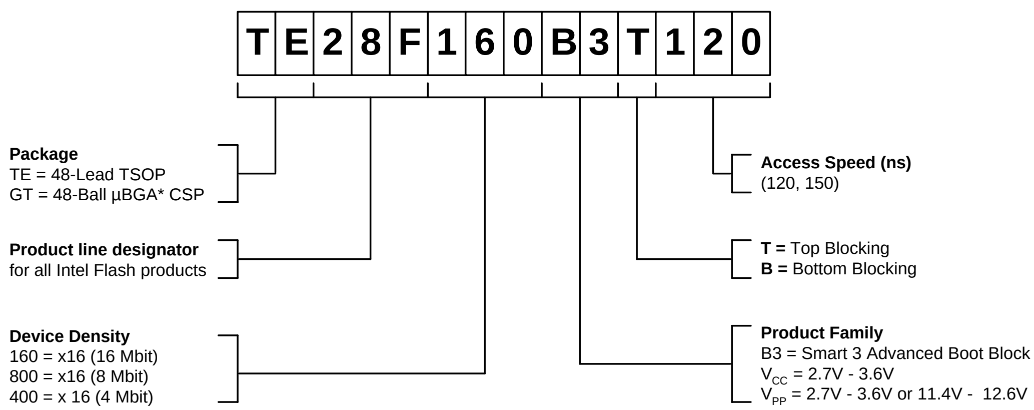
Table 17. Erase and Program Timings

Sym	Parameter	Notes	V_{PP} = 2.7V		V_{PP} = 12V		Unit
			Typ[1]	Max[3]	Typ[1]	Max[3]	
t_{BWPB}	Block Program Time (Parameter)	2	0.10	0.30	0.03	0.10	sec
t_{BWMB}	Block Program Time (Main)	2	0.80	2.40	0.24	0.80	sec
t_{WHQV1} t_{EHQV1}	Program Time	2	22	200	8	185	µs
t_{WHQV2} t_{EHQV2}	Block Erase Time (Parameter)	2	1	5.0	0.8	4.8	sec
t_{WHQV3} t_{EHQV3}	Block Erase Time (Main)	2	1.8	8.0	1.1	7.0	sec
t_{WHRH1} t_{EHRH1}	Program Suspend Latency	3	5	10	5	10	µs
t_{WHRH2} t_{EHRH2}	Erase Suspend Latency	3	5	20	6	12	µs

NOTES:

1. Typical values measured at T_A = +25°C and nominal voltages.
2. Excludes external system-level overhead.
3. Sampled, but not 100% tested.

APPENDIX A
ORDERING INFORMATION



VALID COMBINATIONS

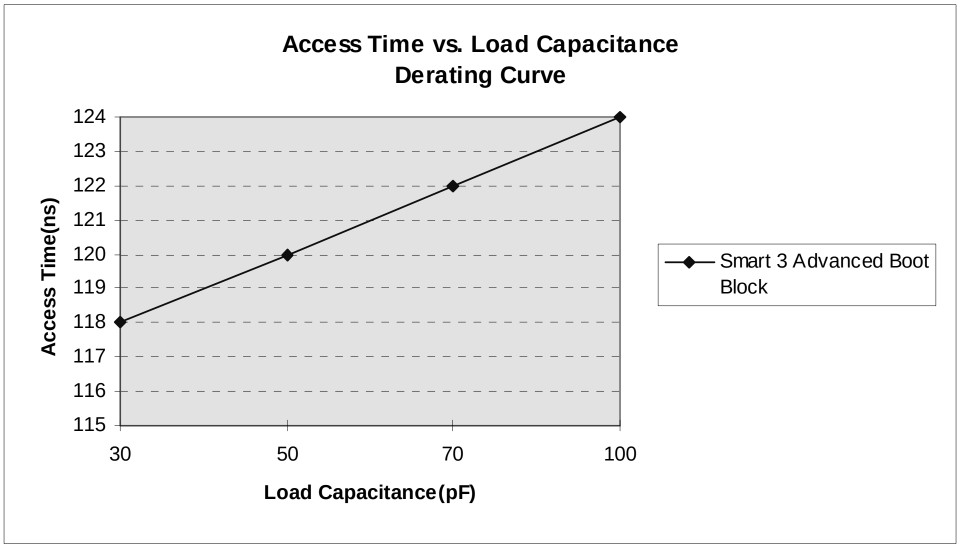
		48-Lead TSOP	48-Ball µBGA* CSP
Extended	**16M**	TE28F160B3T120	GT28F160B3T120
		TE28F160B3B120	GT28F160B3B120
		TE28F160B3T150	GT28F160B3T150
		TE28F160B3B150	GT28F160B3B150
Extended	**8M**	TE28F800B3T120	GT28F800B3T120
		TE28F800B3B120	GT28F800B3B120
		TE28F800B3T150	GT28F800B3T150
		TE28F800B3B150	GT28F800B3B150
Extended	**4M**	TE28F400B3T120	GT28F400B3T120
		TE28F400B3B120	GT28F400B3B120
		TE28F400B3T150	GT28F400B3T150
		TE28F400B3B150	GT28F400B3B150

APPENDIX B
WRITE STATE MACHINE CURRENT/NEXT STATES

			Command Input (and Next State)								
Current State	**SR.7**	**Data When Read**	**Read Array (FFH)**	**Program Setup (40/10H)**	**Erase Setup (20H)**	**Erase Confirm (D0H)**	**Program / Erase Susp. (B0H)**	**Program / Erase Resume (D0)**	**Read Status (70H)**	**Clear Status (50H)**	**Read ID (90H)**
Read Array	"1"	Array	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier
Program Setup	"1"	Status	Pgm.[1]	Program (Command input = Data to be programmed)							
Program (Not Comp.)	"0"	Status	Program				Pgm Susp. to Status	Program			
Program (Complete)	"1"	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier
Program Suspend to Status	"1"	Status	Prog. Susp. to Array	Program Suspend to Array		Program	Program Susp. to Array	Program	Prog. Susp. to Status	Program Suspend to Array	
Program Suspend to Array	"1"	Array	Prog. Susp. to Array	Program Suspend to Array		Program	Program Susp. to Array	Program	Prog. Susp. to Status	Prog. Susp. to Array	Prog. Susp. to Array
Erase Setup	"1"	Status	Erase Command Error			Erase	Erase Cmd. Err.	Erase	Erase Command Error		
Erase Cmd. Error	"1"	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier
Erase (Not Comp)	"0"	Status	Erase				Ers. Susp. to Status	Erase			
Erase (Complete)	"1"	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier
Erase Suspend to Status	"1"	Status	Erase Susp. to Array	Program Setup	Erase Susp. to Array	Erase	Erase Susp. to Array	Erase	Erase Susp. to Status	Erase Suspend to Array	
Erase. Susp. to Array	"1"	Array	Erase Susp. to Array	Program Setup	Erase Susp. to Array	Erase	Erase Susp. to Array	Erase	Erase Susp. to Status	Erase Suspend to Array	
Read Status	"1"	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier
Read Identifier	"1"	ID	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier

1. You cannot program "1"s to the flash. Writing FFH following the Program Setup will initiate the internal program algorithm of the WSM. Although the algorithm will execute, array data is not changed. The WSM returns to read status mode without reporting any error. Assuming $V_{PP} > V_{PPLK}$ writing a second FFH while in read status mode will return the flash to read array mode.

APPENDIX C
ACCESS TIME VS. CAPACITIVE LOAD
(t_{AVQV} vs. C_L)

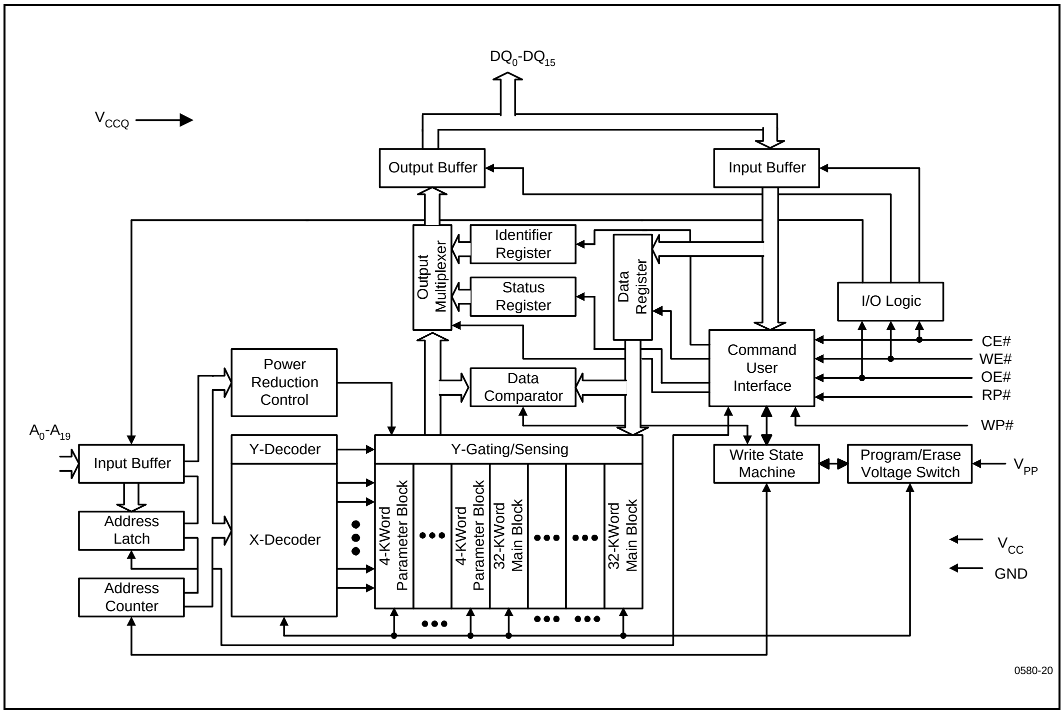


NOTE:
V_{CCQ} = 2.7V

This chart shows a derating curve for device access time with respect to capacitive load. The value in the DC characteristics section of the specification corresponds to C_L = 50 pF.

NOTE:
Sampled, but not 100% tested

APPENDIX D
ARCHITECTURE BLOCK DIAGRAM



APPENDIX E
ADDITIONAL INFORMATION[1,2]

Order Number	Document/Tool
210830	*1997 Flash Memory Databook*
290605	*Smart 3 Advanced Boot Block Byte-Wide 8-Mbit (1024K x8), 16-Mbit (2056K x 8) Flash Memory Family Datasheet*
292172	*AP-617 Additional Flash Data Protection Using V_{PP}, RP# and WP#*

NOTE:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.Intel.com for technical documentation and tools.