

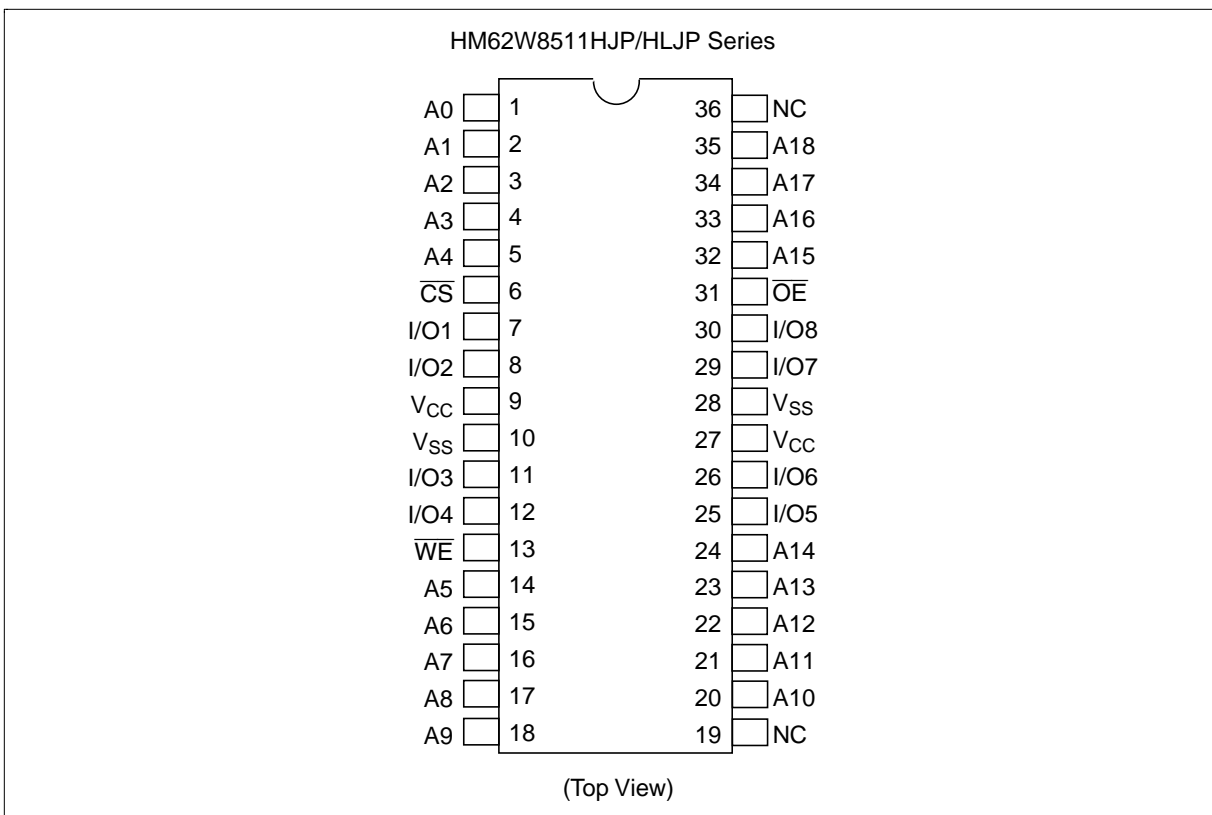


## HM62W8511H Series

### Ordering Information

Type No.	Access time	Package
HM62W8511HJP-12	12 ns	400-mil 36-pin plastic SOJ (CP-36D)
HM62W8511HJP-15	15 ns	
HM62W8511HLJP-12	12 ns	
HM62W8511HLJP-15	15 ns	

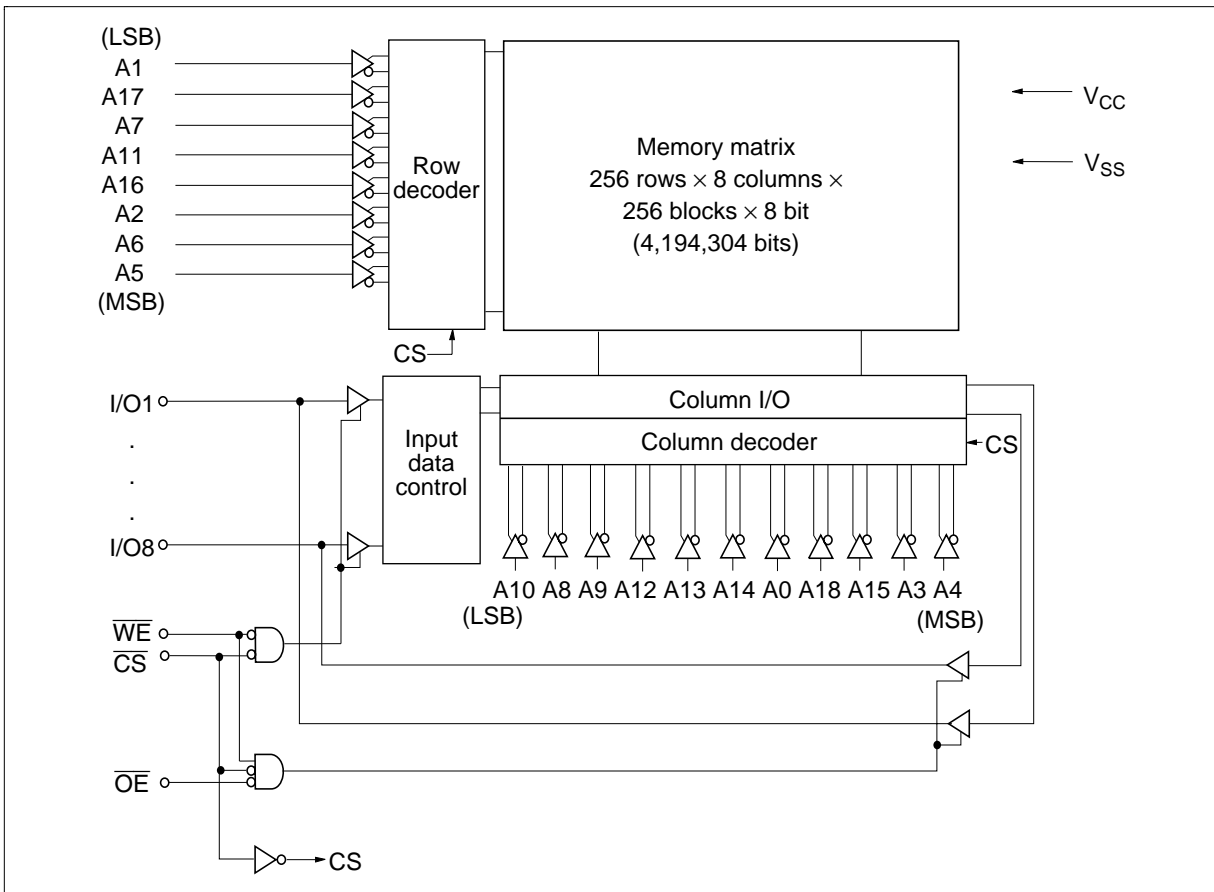
### Pin Arrangement



**Pin Description**

Pin name	Function
A0 to A18	Address input
I/O1 to I/O8	Data input/output
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
$V_{CC}$	Power supply
$V_{SS}$	Ground
NC	No connection

**Block Diagram**



## HM62W8511H Series

### Operation Table

$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	Mode	$V_{\text{CC}}$ current	I/O	Ref. cycle
H	×	×	Standby	$I_{\text{SB}}, I_{\text{SB1}}$	High-Z	—
L	H	H	Output disable	$I_{\text{CC}}$	High-Z	—
L	L	H	Read	$I_{\text{CC}}$	Dout	Read cycle (1) to (3)
L	H	L	Write	$I_{\text{CC}}$	Din	Write cycle (1)
L	L	L	Write	$I_{\text{CC}}$	Din	Write cycle (2)

Note: ×: H or L

### Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to $V_{\text{SS}}$	$V_{\text{CC}}$	-0.5 to +4.6	V
Voltage on any pin relative to $V_{\text{SS}}$	$V_{\text{T}}$	-0.5 <sup>*1</sup> to $V_{\text{CC}}+0.5$ <sup>*2</sup>	V
Power dissipation	$P_{\text{T}}$	1.0	W
Operating temperature	$T_{\text{opr}}$	0 to +70	°C
Storage temperature	$T_{\text{stg}}$	-55 to +125	°C
Storage temperature under bias	$T_{\text{bias}}$	-10 to +85	°C

- Notes: 1.  $V_{\text{T}}$  (min) = -2.0 V for pulse width (under shoot) ≤ 8 ns  
 2.  $V_{\text{T}}$  (max) =  $V_{\text{CC}}+2.0$  V for pulse width (over shoot) ≤ 8 ns

### Recommended DC Operating Conditions ( $T_{\text{a}} = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{\text{CC}}$ <sup>*3</sup>	3.0	3.3	3.6	V
	$V_{\text{SS}}$ <sup>*4</sup>	0	0	0	V
Input voltage	$V_{\text{IH}}$	2.2	—	$V_{\text{CC}} + 0.5$ <sup>*2</sup>	V
	$V_{\text{IL}}$	-0.5 <sup>*1</sup>	—	0.8	V

- Notes: 1.  $V_{\text{IL}}$  (min) = -2.0 V for pulse width (under shoot) ≤ 8 ns  
 2.  $V_{\text{IH}}$  (max) =  $V_{\text{CC}}+2.0$  V for pulse width (over shoot) ≤ 8 ns  
 3. The supply voltage with all  $V_{\text{CC}}$  pins must be on the same level.  
 4. The supply voltage with all  $V_{\text{SS}}$  pins must be on the same level.

## HM62W8511H Series

### DC Characteristics (Ta = 0 to +70°C, V<sub>CC</sub> = 3.3 V ± 0.3 V, V<sub>SS</sub> = 0V)

Parameter	Symbol	Min	Typ* <sup>1</sup>	Max	Unit	Test conditions
Input leakage current	I <sub>I<sub>L</sub></sub>	—	—	2	μA	V <sub>in</sub> = V <sub>SS</sub> to V <sub>CC</sub>
Output leakage current	I <sub>I<sub>O</sub></sub>	—	—	2	μA	V <sub>in</sub> = V <sub>SS</sub> to V <sub>CC</sub>
Operation power supply current	12 ns cycle I <sub>CC</sub>	—	—	150	mA	Min cycle CS = V <sub>IL</sub> , I <sub>out</sub> = 0 mA Other inputs = V <sub>IH</sub> /V <sub>IL</sub>
	15 ns cycle I <sub>CC</sub>	—	—	130		
Standby power supply current	12 ns cycle I <sub>SB</sub>	—	—	60	mA	Min cycle CS = V <sub>IH</sub> , Other inputs = V <sub>IH</sub> /V <sub>IL</sub>
	15 ns cycle I <sub>SB</sub>	—	—	50		
	I <sub>SB1</sub>	—	0.05	5	mA	f = 0 MHz V <sub>CC</sub> ≥ CS ≥ V <sub>CC</sub> - 0.2 V, (1) 0 V ≤ V <sub>in</sub> ≤ 0.2 V or (2) V <sub>CC</sub> ≥ V <sub>in</sub> ≥ V <sub>CC</sub> - 0.2 V
		—* <sup>2</sup>	0.05* <sup>2</sup>	1.0* <sup>2</sup>		
Output voltage	V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> = 8 mA
	V <sub>OH</sub>	2.4	—	—	V	I <sub>OH</sub> = -4 mA

- Notes: 1. Typical values are at V<sub>CC</sub> = 3.3 V, Ta = +25°C and not guaranteed.  
2. This characteristics is guaranteed only for L-version.

### Capacitance (Ta = +25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance* <sup>1</sup>	C <sub>in</sub>	—	—	6	pF	V <sub>in</sub> = 0 V
Input/output capacitance* <sup>1</sup>	C <sub>I/O</sub>	—	—	8	pF	V <sub>I/O</sub> = 0 V

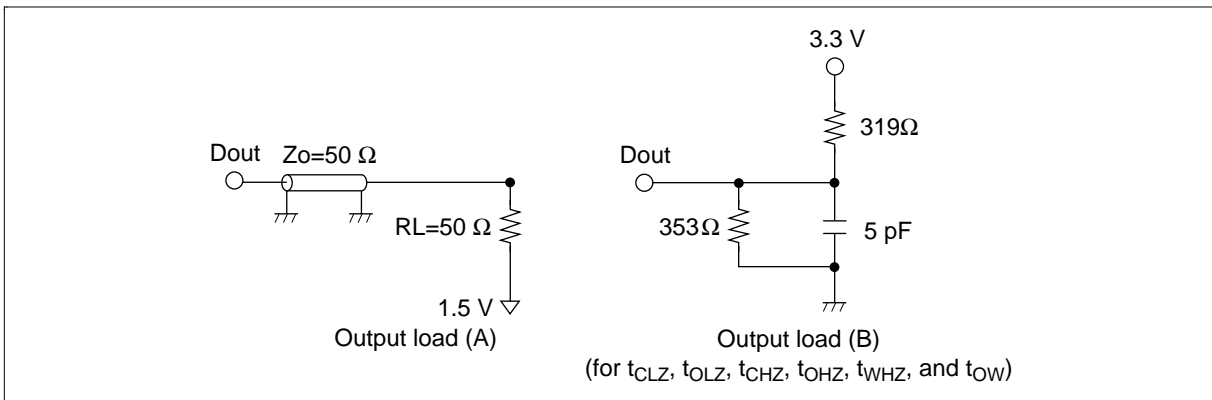
- Note: 1. This parameter is sampled and not 100% tested.

## HM62W8511H Series

**AC Characteristics** ( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ , unless otherwise noted.)

### Test Conditions

- Input pulse levels: 3.0 V/0.0 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures (Including scope and jig)



### Read Cycle

Parameter	Symbol	HM62W8511H				Unit	Notes
		-12		-15			
		Min	Max	Min	Max		
Read cycle time	$t_{RC}$	12	—	15	—	ns	
Address access time	$t_{AA}$	—	12	—	15	ns	
Chip select access time	$t_{ACS}$	—	12	—	15	ns	
Output enable to output valid	$t_{OE}$	—	6	—	7	ns	
Output hold from address change	$t_{OH}$	3	—	3	—	ns	
Chip select to output in low-Z	$t_{CLZ}$	3	—	3	—	ns	1
Output enable to output in low-Z	$t_{OLZ}$	0	—	0	—	ns	1
Chip deselect to output in high-Z	$t_{CHZ}$	—	6	—	7	ns	1
Output disable to output in high-Z	$t_{OHZ}$	—	6	—	7	ns	1

## Write Cycle

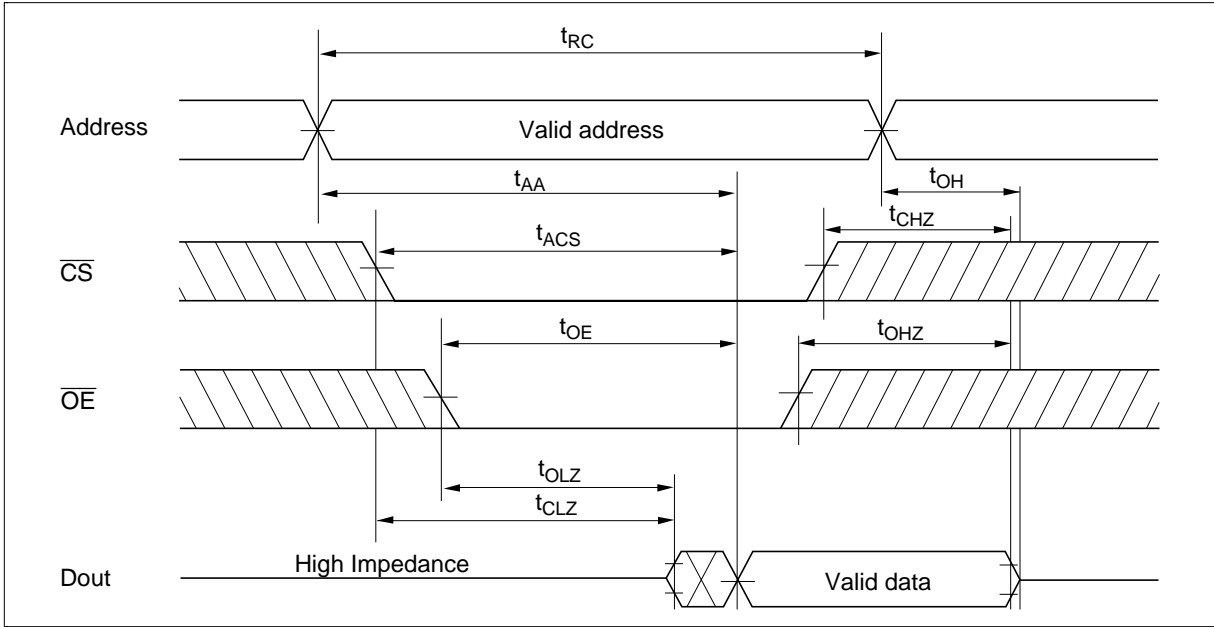
Parameter	Symbol	HM62W8511H				Unit	Notes
		-12		-15			
		Min	Max	Min	Max		
Write cycle time	$t_{WC}$	12	—	15	—	ns	
Address valid to end of write	$t_{AW}$	8	—	10	—	ns	
Chip select to end of write	$t_{CW}$	8	—	10	—	ns	9
Write pulse width	$t_{WP}$	8	—	10	—	ns	8
Address setup time	$t_{AS}$	0	—	0	—	ns	6
Write recovery time	$t_{WR}$	0	—	0	—	ns	7
Data to write time overlap	$t_{DW}$	6	—	7	—	ns	
Data hold from write time	$t_{DH}$	0	—	0	—	ns	
Write disable to output in low-Z	$t_{OW}$	3	—	3	—	ns	1
Output disable to output in high-Z	$t_{OHZ}$	—	6	—	7	ns	1
Write enable to output in high-Z	$t_{WHZ}$	—	6	—	7	ns	1

- Note:
1. Transition is measured  $\pm 200$  mV from steady voltage with Load (B). This parameter is sampled and not 100% tested.
  2. Address should be valid prior to or coincident with  $\overline{CS}$  transition low.
  3.  $\overline{WE}$  and/or  $\overline{CS}$  must be high during address transition time.
  4. if  $\overline{CS}$  and  $\overline{OE}$  are low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
  5. If the  $\overline{CS}$  low transition occurs simultaneously with the  $\overline{WE}$  low transition or after the  $\overline{WE}$  transition, output remains a high impedance state.
  6.  $t_{AS}$  is measured from the latest address transition to the later of  $\overline{CS}$  or  $\overline{WE}$  going low.
  7.  $t_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going high to the first address transition.
  8. A write occurs during the overlap of a low  $\overline{CS}$  and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS}$  going low and  $\overline{WE}$  going low. A write ends at the earliest transition among  $\overline{CS}$  going high and  $\overline{WE}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
  9.  $t_{CW}$  is measured from the later of  $\overline{CS}$  going low to the the end of write.

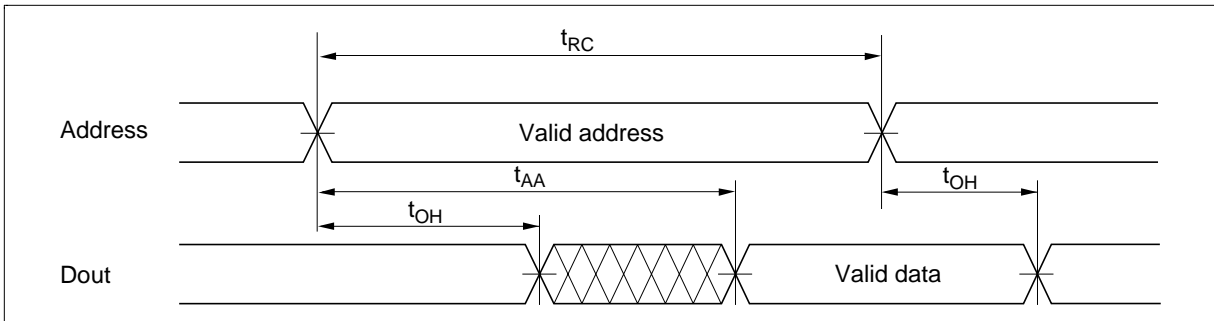
# HM62W8511H Series

## Timing Waveforms

Read Timing Waveform (1) ( $\overline{WE} = V_{IH}$ )

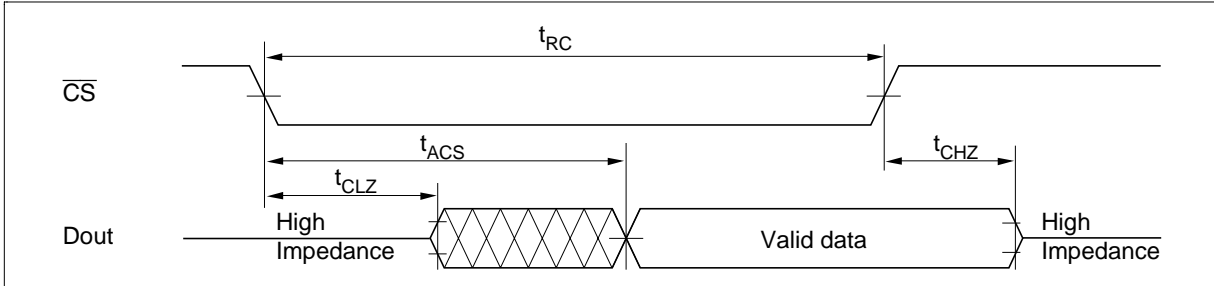


Read Timing Waveform (2) ( $\overline{WE} = V_{IH}$ ,  $\overline{CS} = V_{IL}$ ,  $\overline{OE} = V_{IL}$ )

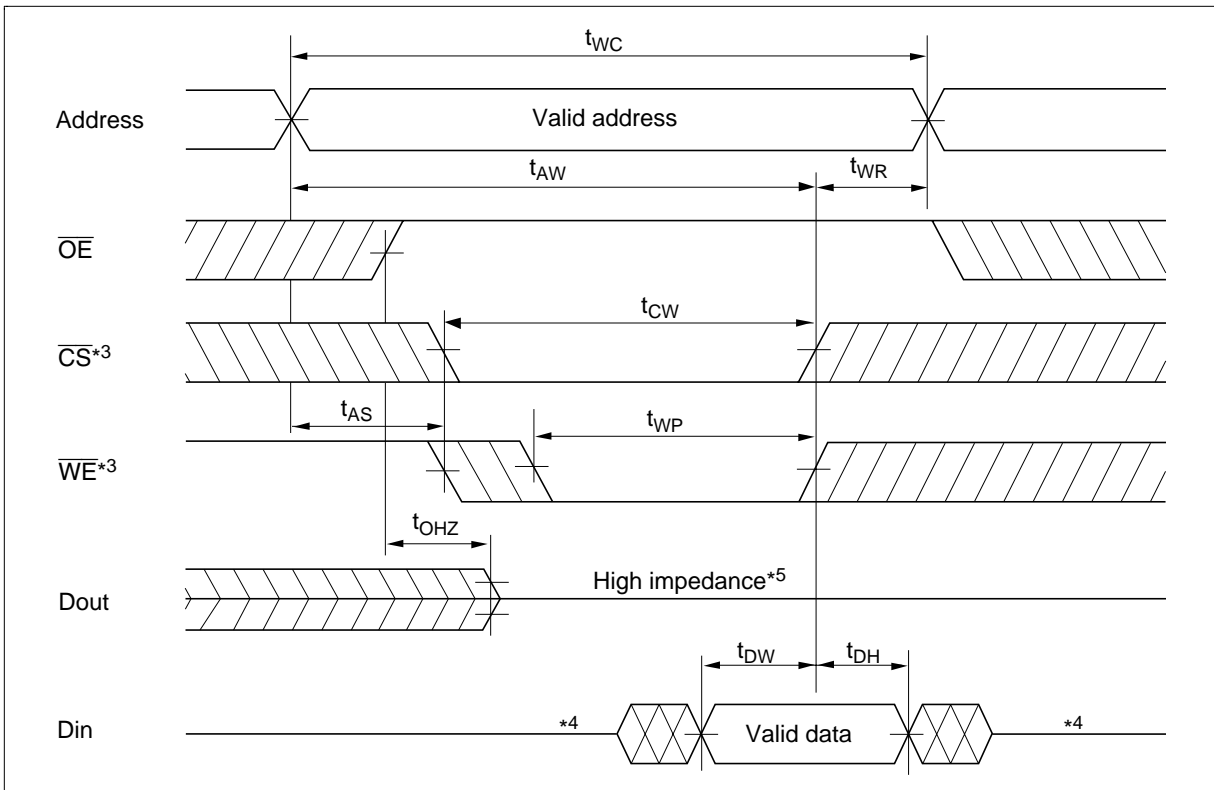




Read Timing Waveform (3) ( $\overline{WE} = V_{IH}, \overline{CS} = V_{IL}, \overline{OE} = V_{IL}$ )\*2

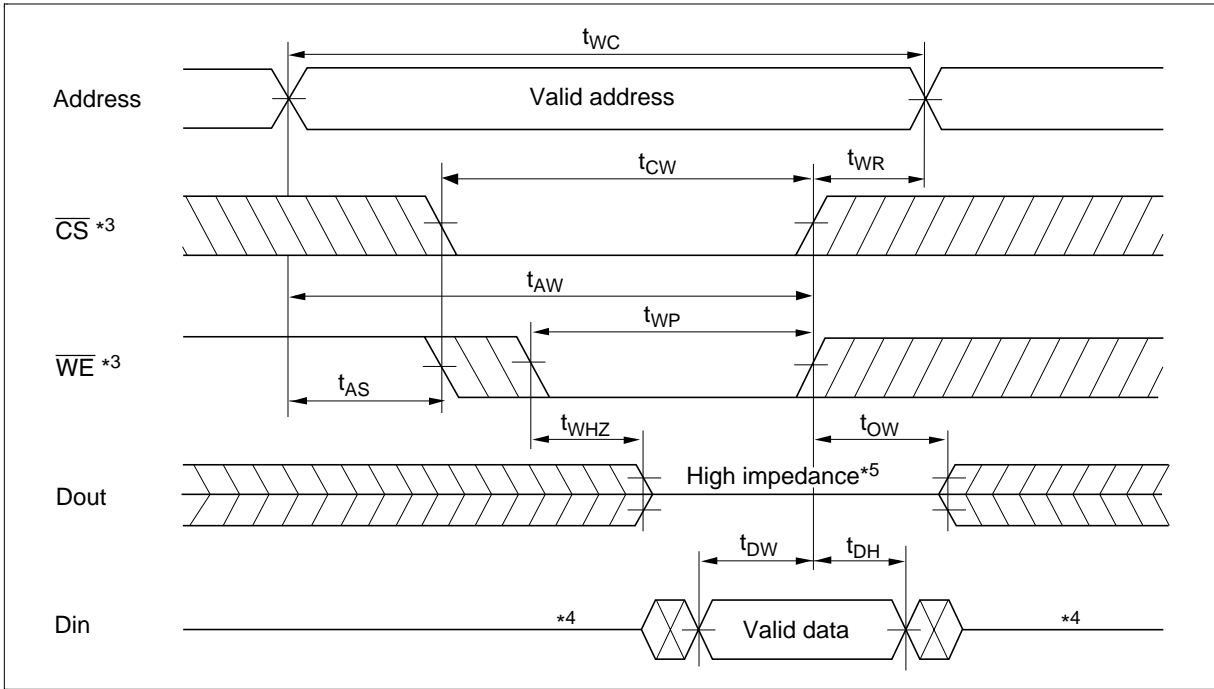


Write Timing Waveform (1) ( $\overline{WE}$  Controlled)



## HM62W8511H Series

### Write Timing Waveform (2) ( $\overline{CS}$ Controlled)



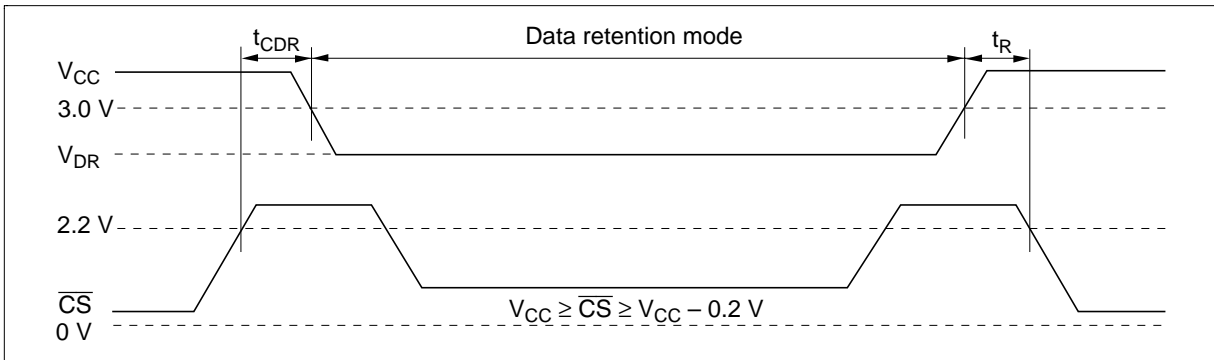
**Low  $V_{CC}$  Data Retention Characteristics** ( $T_a = 0$  to  $+70^\circ\text{C}$ )

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions
$V_{CC}$ for data retention	$V_{DR}$	2.0	—	—	V	$V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2$ V (1) $0 \text{ V} \leq V_{in} \leq 0.2 \text{ V}$ or (2) $V_{CC} \geq V_{in} \geq V_{CC} - 0.2 \text{ V}$
Data retention current	$I_{CCDR}$	—	40	600	$\mu\text{A}$	$V_{CC} = 3 \text{ V}$ , $V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2 \text{ V}$ (1) $0 \text{ V} \leq V_{in} \leq 0.2 \text{ V}$ or (2) $V_{CC} \geq V_{in} \geq V_{CC} - 0.2 \text{ V}$
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	See retention waveform
Operation recovery time	$t_R$	5	—	—	ms	

Note: 1. Typical values are at  $V_{CC} = 3.0 \text{ V}$ ,  $T_a = +25^\circ\text{C}$ , and not guaranteed.

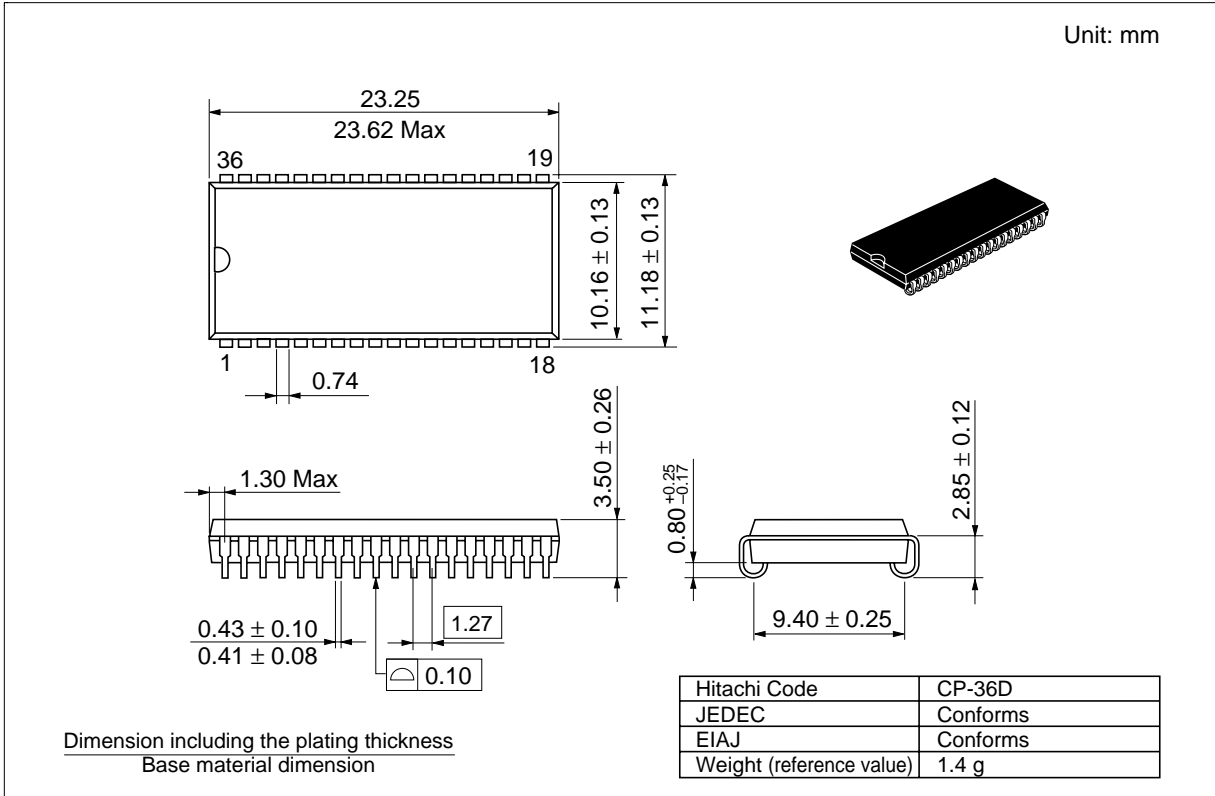
**Low  $V_{CC}$  Data Retention Timing Waveform**



# HM62W8511H Series

## Package Dimensions

### HM62W8511HJP/HLJP Series (CP-36D)



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