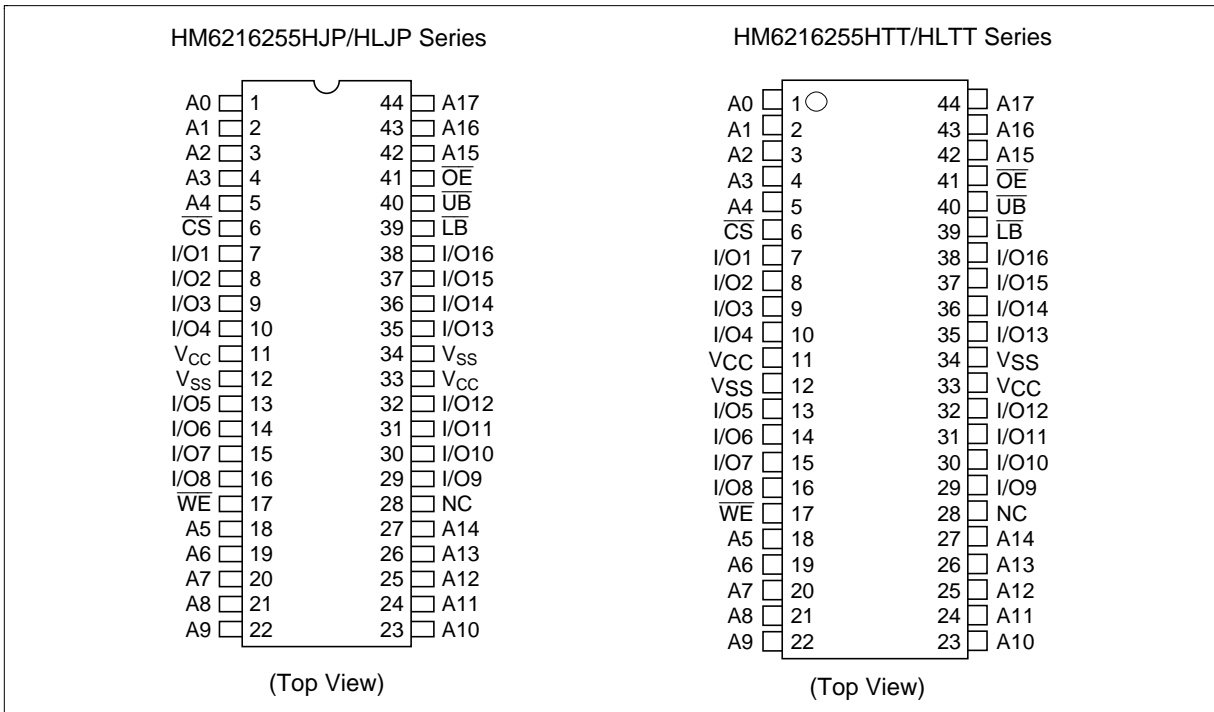


HM6216255H Series

Ordering Information

| Type No. | Access time | Package |
|------------------|-------------|--|
| HM6216255HJP-10 | 10 ns | 400-mil 44-pin plastic SOJ (CP-44D) |
| HM6216255HJP-12 | 12 ns | |
| HM6216255HJP-15 | 15 ns | |
| HM6216255HLJP-10 | 10 ns | 400-mil 44-pin plastic TSOPII (TTP-44DE) |
| HM6216255HLJP-12 | 12 ns | |
| HM6216255HLJP-15 | 15 ns | |
| HM6216255HTT-10 | 10 ns | 400-mil 44-pin plastic TSOPII (TTP-44DE) |
| HM6216255HTT-12 | 12 ns | |
| HM6216255HTT-15 | 15 ns | |
| HM6216255HLTT-10 | 10 ns | 400-mil 44-pin plastic TSOPII (TTP-44DE) |
| HM6216255HLTT-12 | 12 ns | |
| HM6216255HLTT-15 | 15 ns | |

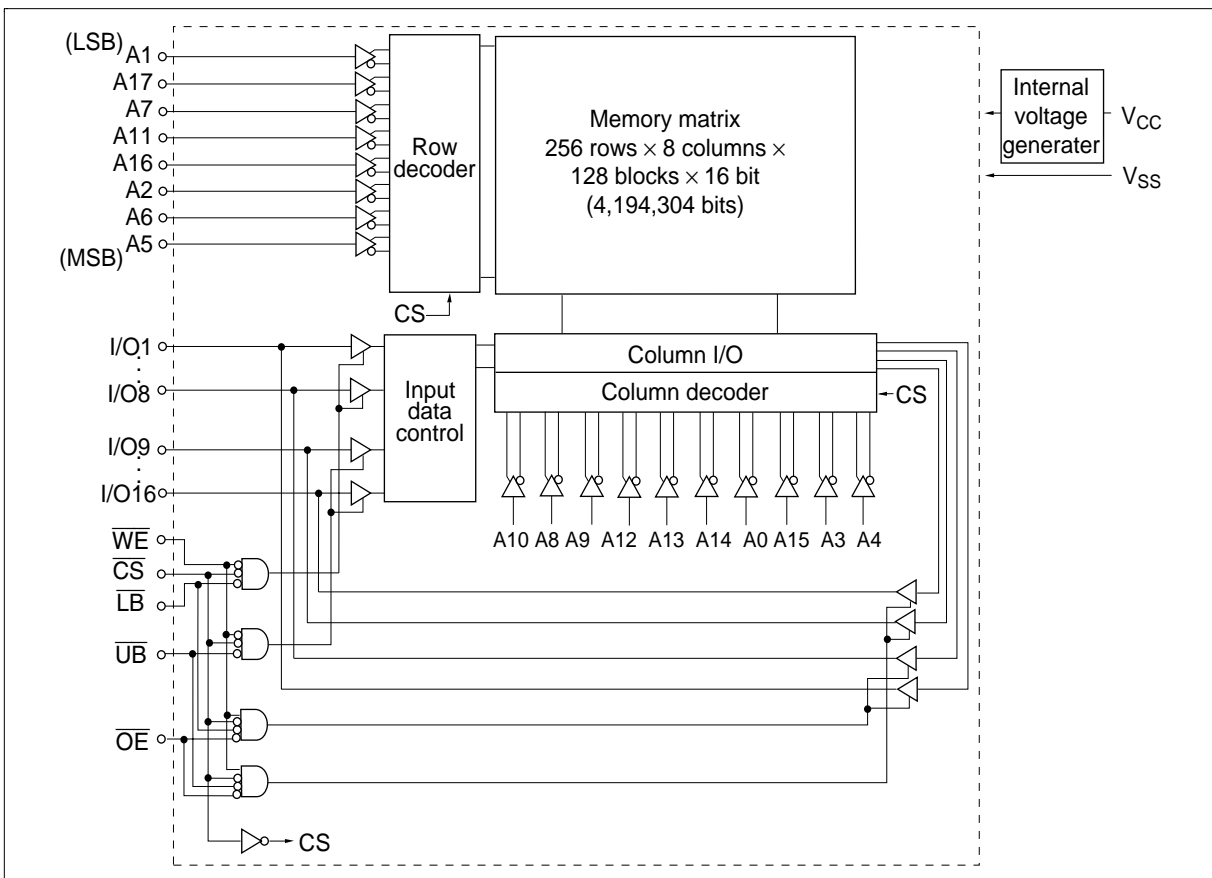
Pin Arrangement



Pin Description

| Pin name | Function | Pin name | Function |
|-----------------|-------------------|-----------------|-------------------|
| A0 to A17 | Address input | \overline{UB} | Upper byte select |
| I/O1 to I/O16 | Data input/output | \overline{LB} | Lower byte select |
| \overline{CS} | Chip select | V_{CC} | Power supply |
| \overline{OE} | Output enable | V_{SS} | Ground |
| \overline{WE} | Write enable | NC | No connection |

Block Diagram



HM6216255H Series

Operation Table

| $\overline{\text{CS}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | $\overline{\text{LB}}$ | $\overline{\text{UB}}$ | Mode | V_{CC} current | I/O1–I/O8 | I/O9–I/O16 | Ref. cycle |
|------------------------|------------------------|------------------------|------------------------|------------------------|------------------|---------------------------------|-----------|------------|-------------|
| H | × | × | × | × | Standby | $I_{\text{SB}}, I_{\text{SB1}}$ | High-Z | High-Z | — |
| L | H | H | × | × | Output disable | I_{CC} | High-Z | High-Z | — |
| L | L | H | L | L | Read | I_{CC} | Output | Output | Read cycle |
| L | L | H | L | H | Lower byte read | I_{CC} | Output | High-Z | Read cycle |
| L | L | H | H | L | Upper byte read | I_{CC} | High-Z | Output | Read cycle |
| L | L | H | H | H | — | I_{CC} | High-Z | High-Z | — |
| L | × | L | L | L | Write | I_{CC} | Input | Input | Write cycle |
| L | × | L | L | H | Lower byte write | I_{CC} | Input | High-Z | Write cycle |
| L | × | L | H | L | Upper byte write | I_{CC} | High-Z | Input | Write cycle |
| L | × | L | H | H | — | I_{CC} | High-Z | High-Z | — |

Note: ×: H or L

Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|--|-------------------|---|------|
| Supply voltage relative to V_{SS} | V_{CC} | –0.5 to +7.0 | V |
| Voltage on any pin relative to V_{SS} | V_{T} | –0.5 ^{*1} to $V_{\text{CC}} + 0.5$ ^{*2} | V |
| Power dissipation | P_{T} | 1.0 ^{*3} /1.3 ^{*4} | W |
| Operating temperature | T_{opr} | 0 to +70 | °C |
| Storage temperature | T_{stg} | –55 to +125 | °C |
| Storage temperature under bias | T_{bias} | –10 to +85 | °C |

- Notes: 1. V_{T} (min) = –2.0 V for pulse width (under shoot) ≤ 8 ns
 2. V_{T} (max) = $V_{\text{CC}} + 2.0$ V for pulse width (over shoot) ≤ 8 ns
 3. At still air condition
 4. At air flow ≥ 1.0 m/s

Recommended DC Operating Conditions (Ta = 0 to +70°C)

| Parameter | Symbol | Min | Typ | Max | Unit |
|----------------|---------------|-------------|-----|---------------------|------|
| Supply voltage | V_{CC}^{*2} | 4.5 | 5.0 | 5.5 | V |
| | V_{SS}^{*3} | 0 | 0 | 0 | V |
| Input voltage | V_{IH} | 2.2 | — | $V_{CC} + 0.5^{*2}$ | V |
| | V_{IL} | -0.5^{*1} | — | 0.8 | V |

- Notes: 1. V_{IL} (min) = -2.0 V for pulse width (under shoot) ≤ 8 ns
 2. V_{IH} (max) = $V_{CC} + 2.0$ V for pulse width (over shoot) ≤ 8 ns
 3. The supply voltage with all V_{CC} pins must be on the same level.
 4. The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics (Ta = 0 to +70°C, $V_{CC} = 5.0$ V ± 10 %, $V_{SS} = 0$ V)

| Parameter | Symbol | Min | Typ* ¹ | Max | Unit | Test conditions |
|--------------------------------------|----------------------|-----------------|-------------------|-------------------|---------|---|
| Input leakage current | $ I_{LI} $ | — | — | 2 | μ A | $V_{in} = V_{SS}$ to V_{CC} |
| Output leakage current* ¹ | $ I_{LO} $ | — | — | 2 | μ A | $V_{in} = V_{SS}$ to V_{CC} |
| Operating power supply current | 10 ns cycle I_{CC} | — | — | 200 | mA | $\overline{CS} = V_{IL}$, $I_{out} = 0$ mA Other inputs = V_{IH}/V_{IL} |
| | 12 ns cycle I_{CC} | — | — | 180 | | |
| | 15 ns cycle I_{CC} | — | — | 160 | | |
| Standby power supply current | 10 ns cycle I_{SB} | — | — | 70 | mA | $\overline{CS} = V_{IH}$, Other inputs = V_{IH}/V_{IL} |
| | 12 ns cycle I_{SB} | — | — | 60 | | |
| | 15 ns cycle I_{SB} | — | — | 50 | | |
| | I_{SB1} | — | 0.1 | 5 | mA | |
| | | —* ² | 0.1* ² | 1.2* ² | | |
| Output voltage | V_{OL} | — | — | 0.4 | V | $I_{OL} = 8$ mA |
| | V_{OH} | 2.4 | — | — | V | $I_{OH} = -4$ mA |

- Note: 1. Typical values are at $V_{CC} = 5.0$ V, $T_a = +25^\circ$ C and not guaranteed.
 2. This characteristics is guaranteed only for L-version.

HM6216255H Series

Capacitance (Ta = +25°C, f = 1.0 MHz)

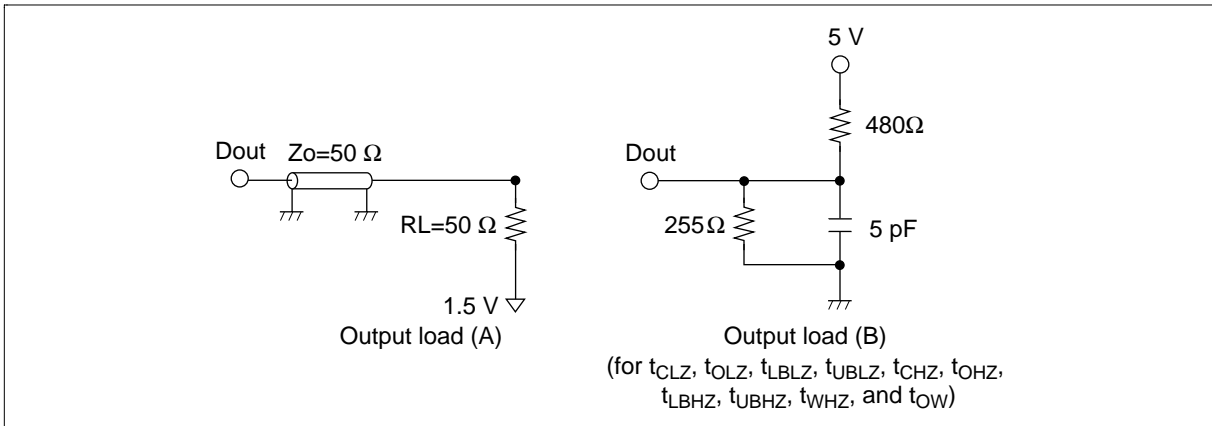
| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|----------------------------|------------------|-----|-----|-----|------|------------------------|
| Input capacitance*1 | C _{in} | — | — | 6 | pF | V _{in} = 0 V |
| Input/output capacitance*1 | C _{I/O} | — | — | 8 | pF | V _{I/O} = 0 V |

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, unless otherwise noted.)

Test Conditions

- Input pulse levels: 3.0 V/0.0 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures (Including scope and jig)



Read Cycle

| Parameter | Symbol | HM6216255H | | | | | | Unit | Notes |
|------------------------------------|-------------------------|------------|-----|-----|-----|-----|-----|------|-------|
| | | -10 | | -12 | | -15 | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| Read cycle time | t_{RC} | 10 | — | 12 | — | 15 | — | ns | |
| Address access time | t_{AA} | — | 10 | — | 12 | — | 15 | ns | |
| Chip select access time | t_{ACS} | — | 10 | — | 12 | — | 15 | ns | |
| Output enable to output valid | t_{OE} | — | 5 | — | 6 | — | 7 | ns | |
| Byte select to output valid | t_{LB} , t_{UB} | — | 5 | — | 6 | — | 7 | ns | |
| Output hold from address change | t_{OH} | 3 | — | 3 | — | 3 | — | ns | |
| Chip select to output in low-Z | t_{CLZ} | 3 | — | 3 | — | 3 | — | ns | 1 |
| Output enable to output in low-Z | t_{OLZ} | 0 | — | 0 | — | 0 | — | ns | 1 |
| Byte select to output in low-Z | t_{LBLZ} , t_{UBLZ} | 0 | — | 0 | — | 0 | — | ns | 1 |
| Chip deselect to output in high-Z | t_{CHZ} | — | 5 | — | 6 | — | 7 | ns | 1 |
| Output disable to output in high-Z | t_{OHZ} | — | 5 | — | 6 | — | 7 | ns | 1 |
| Byte deselect to output in high-Z | t_{LBHZ} , t_{UBHZ} | — | 5 | — | 6 | — | 7 | ns | 1 |

HM6216255H Series

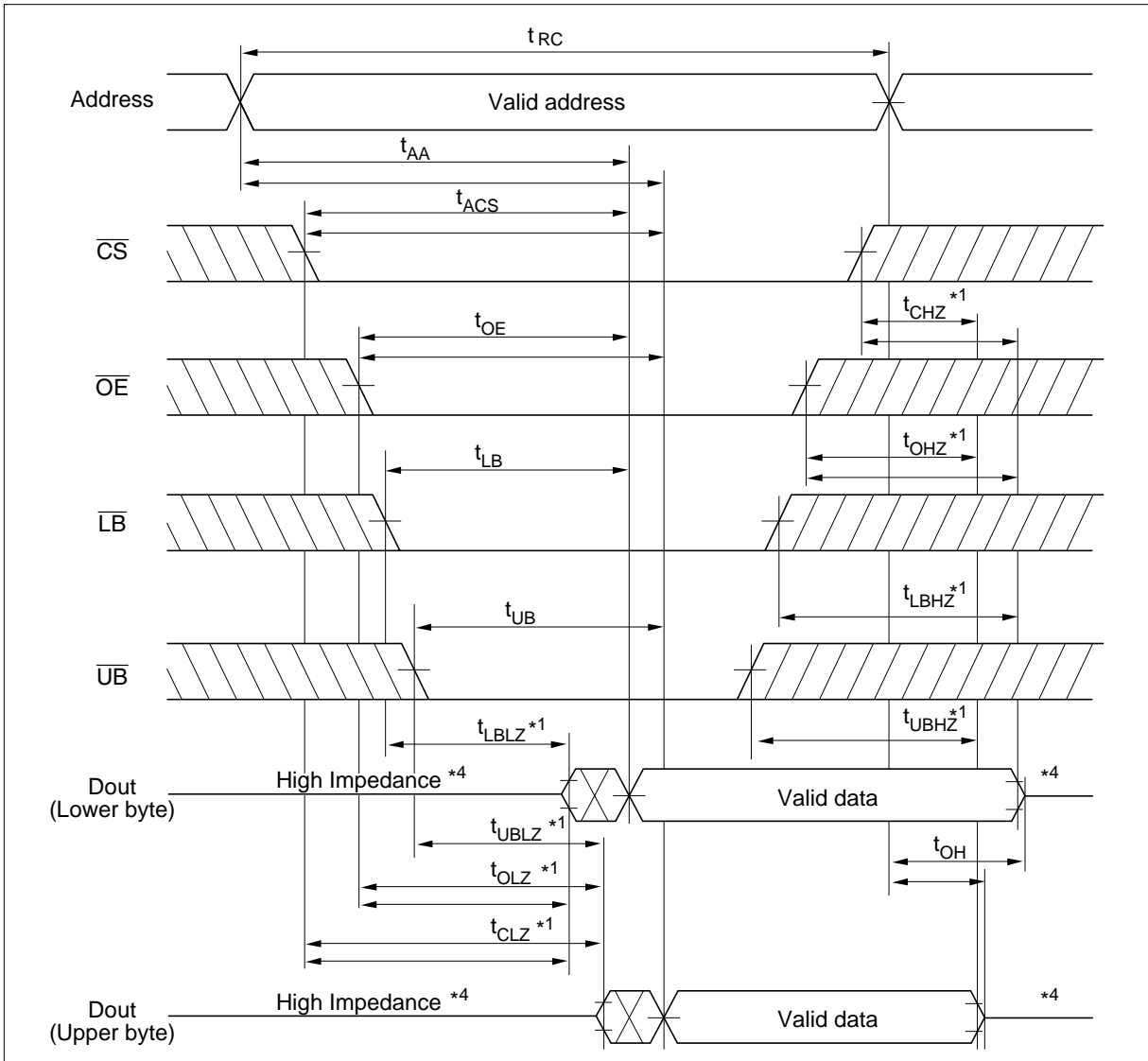
Write Cycle

| Parameter | Symbol | HM6216255H | | | | | | Unit | Notes |
|------------------------------------|--------------------|------------|-----|-----|-----|-----|-----|------|-------|
| | | -10 | | -12 | | -15 | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| Write cycle time | t_{WC} | 10 | — | 12 | — | 15 | — | ns | |
| Address valid to end of write | t_{AW} | 7 | — | 8 | — | 10 | — | ns | |
| Chip select to end of write | t_{CW} | 7 | — | 8 | — | 10 | — | ns | 8 |
| Write pulse width | t_{WP} | 7 | — | 8 | — | 10 | — | ns | 7 |
| Byte select to end of write | t_{LBW}, t_{UBW} | 7 | — | 8 | — | 10 | — | ns | 9, 10 |
| Address setup time | t_{AS} | 0 | — | 0 | — | 0 | — | ns | 5 |
| Write recovery time | t_{WR} | 0 | — | 0 | — | 0 | — | ns | 6 |
| Data to write time overlap | t_{DW} | 5 | — | 6 | — | 7 | — | ns | |
| Data hold from write time | t_{DH} | 0 | — | 0 | — | 0 | — | ns | |
| Write disable to output in low-Z | t_{OW} | 3 | — | 3 | — | 3 | — | ns | 1 |
| Output disable to output in high-Z | t_{OHZ} | — | 5 | — | 6 | — | 7 | ns | 1 |
| Write enable to output in high-Z | t_{WHZ} | — | 5 | — | 6 | — | 7 | ns | 1 |

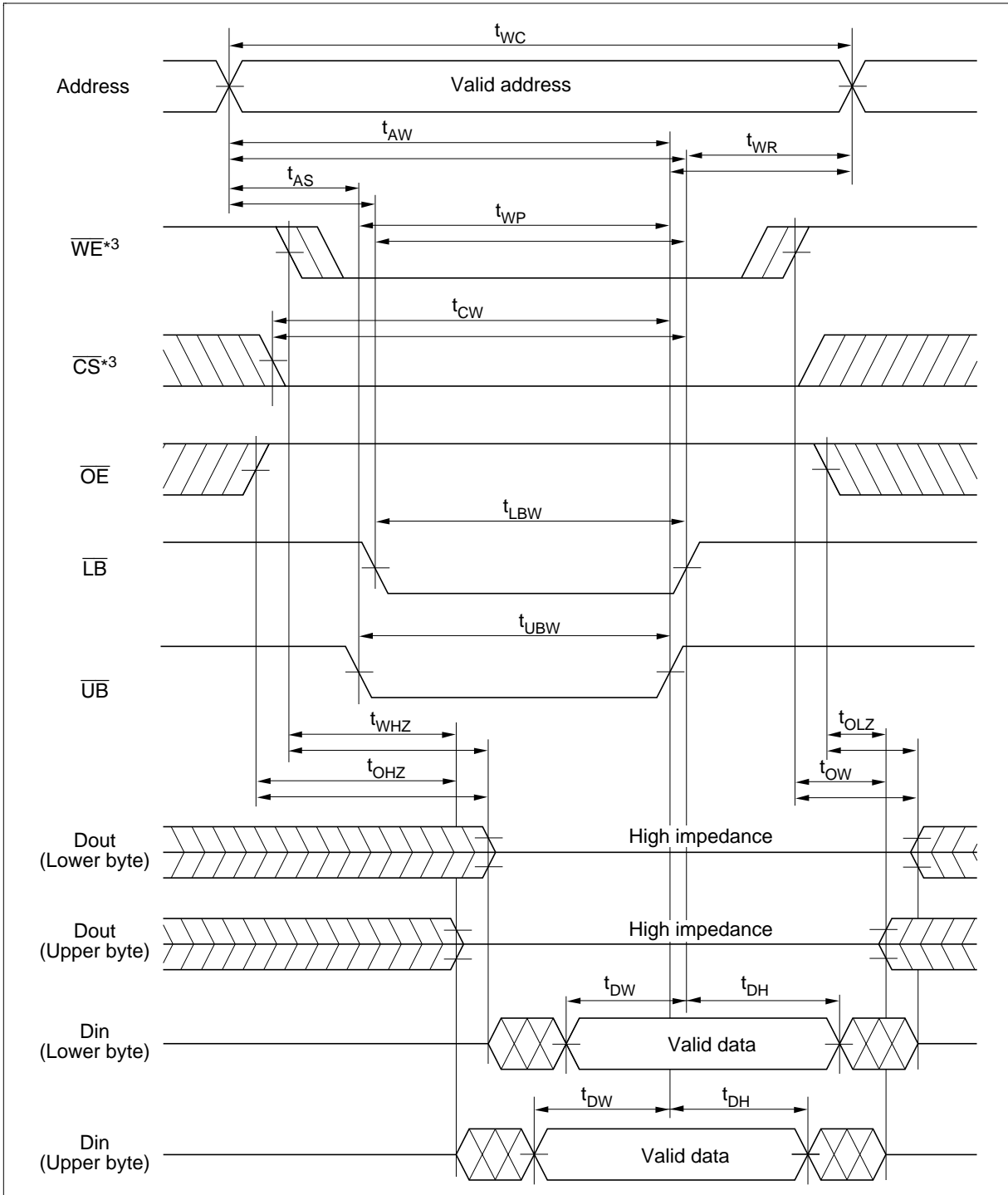
- Notes:
1. Transition is measured ± 200 mV from steady voltage with Load (B). This parameter is sampled and not 100% tested.
 2. If the \overline{CS} or \overline{LB} or \overline{UB} low transition occurs simultaneously with the \overline{WE} low transition or after the \overline{WE} transition, output remains a high impedance state.
 3. \overline{WE} and/or \overline{CS} must be high during address transition time.
 4. If \overline{CS} , \overline{OE} , \overline{LB} and \overline{UB} are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
 5. t_{AS} is measured from the latest address transition to the latest of \overline{CS} , \overline{WE} , \overline{LB} or \overline{UB} going low.
 6. t_{WR} is measured from the earliest of \overline{CS} , \overline{WE} , \overline{LB} or \overline{UB} going high to the first address transition.
 7. A write occurs during the overlap of low \overline{CS} , low \overline{WE} and low \overline{LB} or low \overline{UB} .
 8. t_{CW} is measured from the later of \overline{CS} going low to the end of write.
 9. t_{LBW} is measured from the later of \overline{LB} going low to the end of write.
 10. t_{UBW} is measured from the later of \overline{UB} going low to the end of write.

Timing Waveforms

Read Timing Waveform (1) ($\overline{WE} = V_{IH}$)

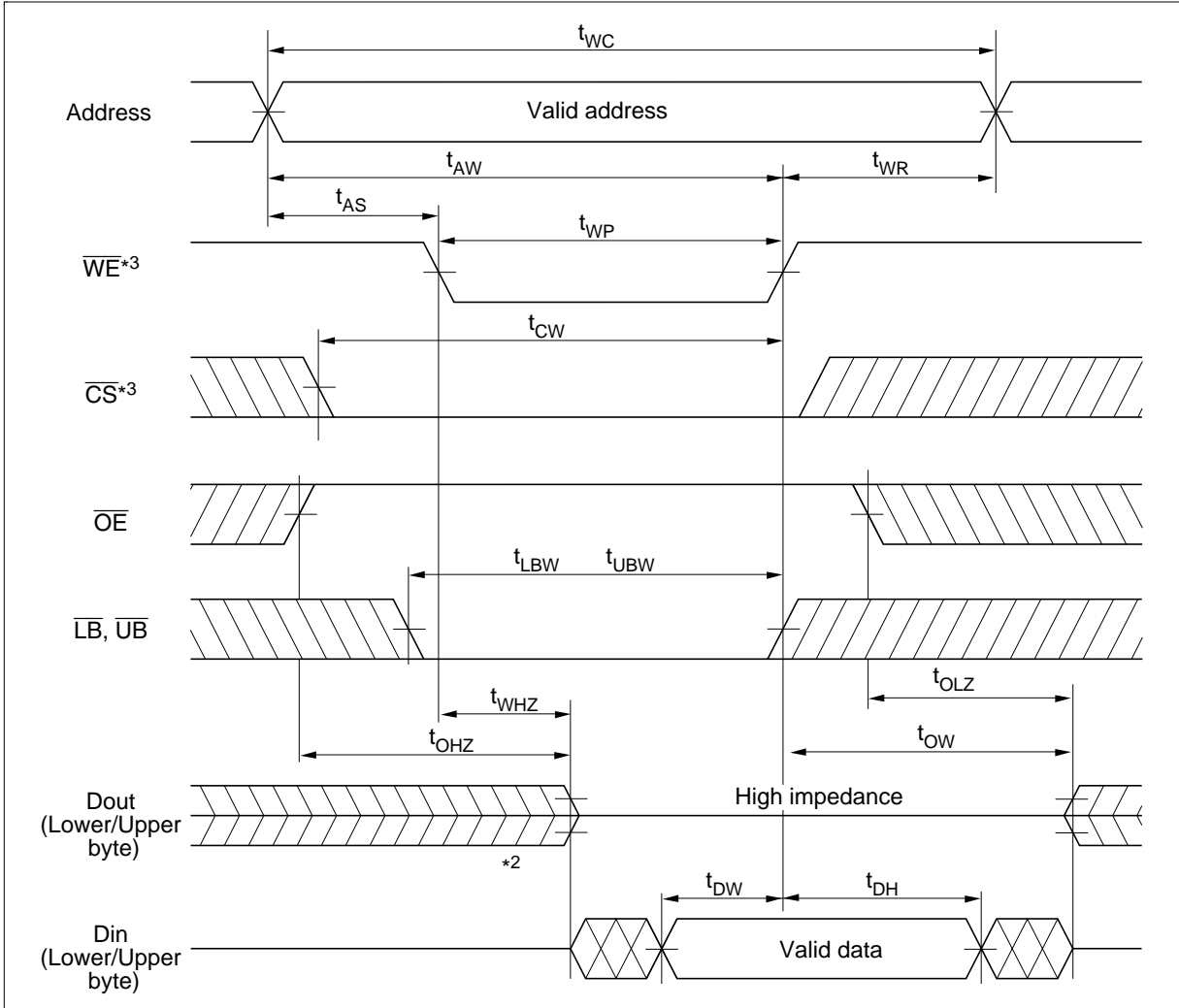


Write Timing Waveform (1) ($\overline{\text{LB}}$, $\overline{\text{UB}}$ Controlled)

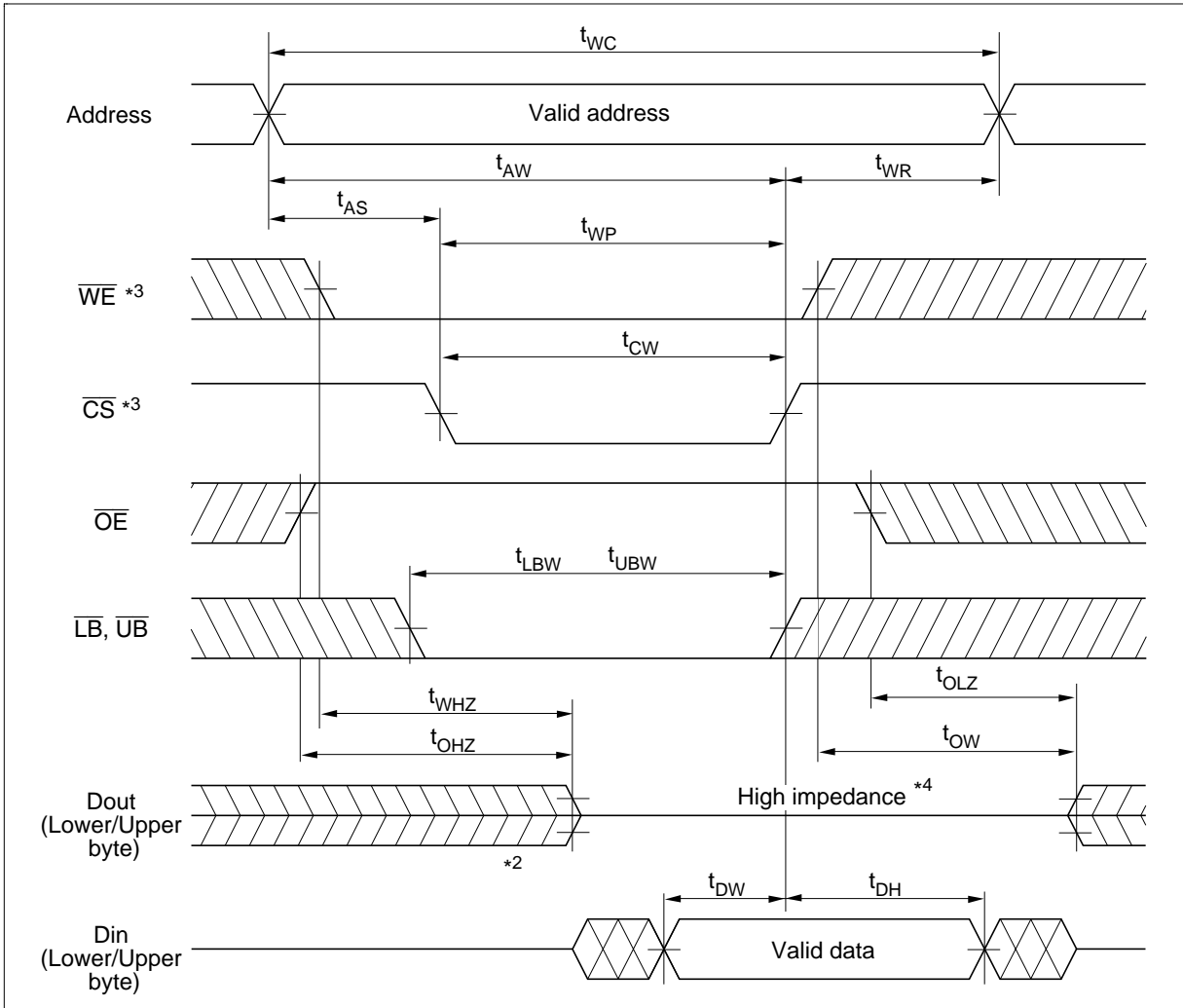


HM6216255H Series

Write Timing Waveform (2) (\overline{WE} Controlled)



Write Timing Waveform (3) (\overline{CS} Controlled)



HM6216255H Series

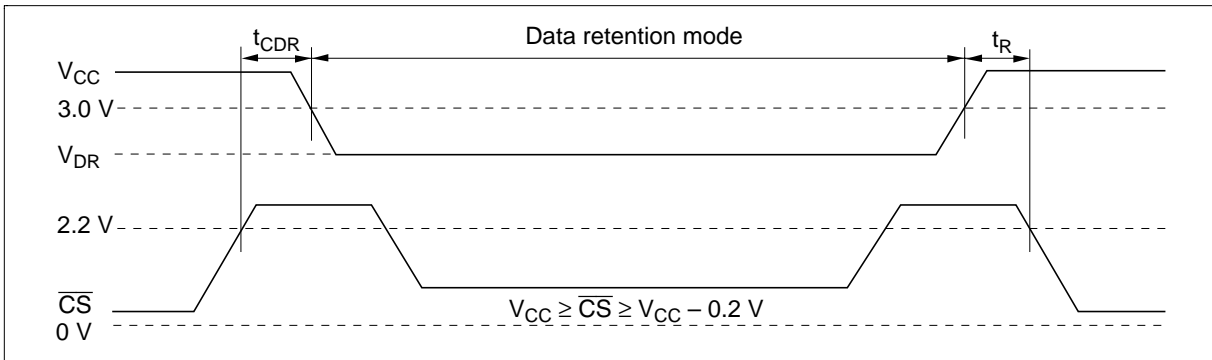
Low V_{CC} Data Retention Characteristics ($T_a = 0$ to $+70^\circ\text{C}$)

This characteristics is guaranteed only for L-version.

| Parameter | Symbol | Min | Typ* ¹ | Max | Unit | Test conditions |
|--------------------------------------|------------|-----|-------------------|-----|---------------|---|
| V_{CC} for data retention | V_{DR} | 2.0 | — | — | V | $V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2\text{ V}$, (1) $0\text{ V} \leq V_{in} \leq 0.2\text{ V}$ or (2) $V_{CC} \geq V_{in} \geq V_{CC} - 0.2\text{ V}$ |
| Data retention current | I_{CCDR} | — | 50 | 800 | μA | $V_{CC} = 3\text{ V}$ $V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2\text{ V}$, (1) $0\text{ V} \leq V_{in} \leq 0.2\text{ V}$ or (2) $V_{CC} \geq V_{in} \geq V_{CC} - 0.2\text{ V}$ |
| Chip deselect to data retention time | t_{CDR} | 0 | — | — | ns | See retention waveform |
| Operation recovery time | t_R | 5 | — | — | ms | |

Note: 1. Typical values are at $V_{CC} = 3.0\text{ V}$, $T_a = +25^\circ\text{C}$, and not guaranteed.

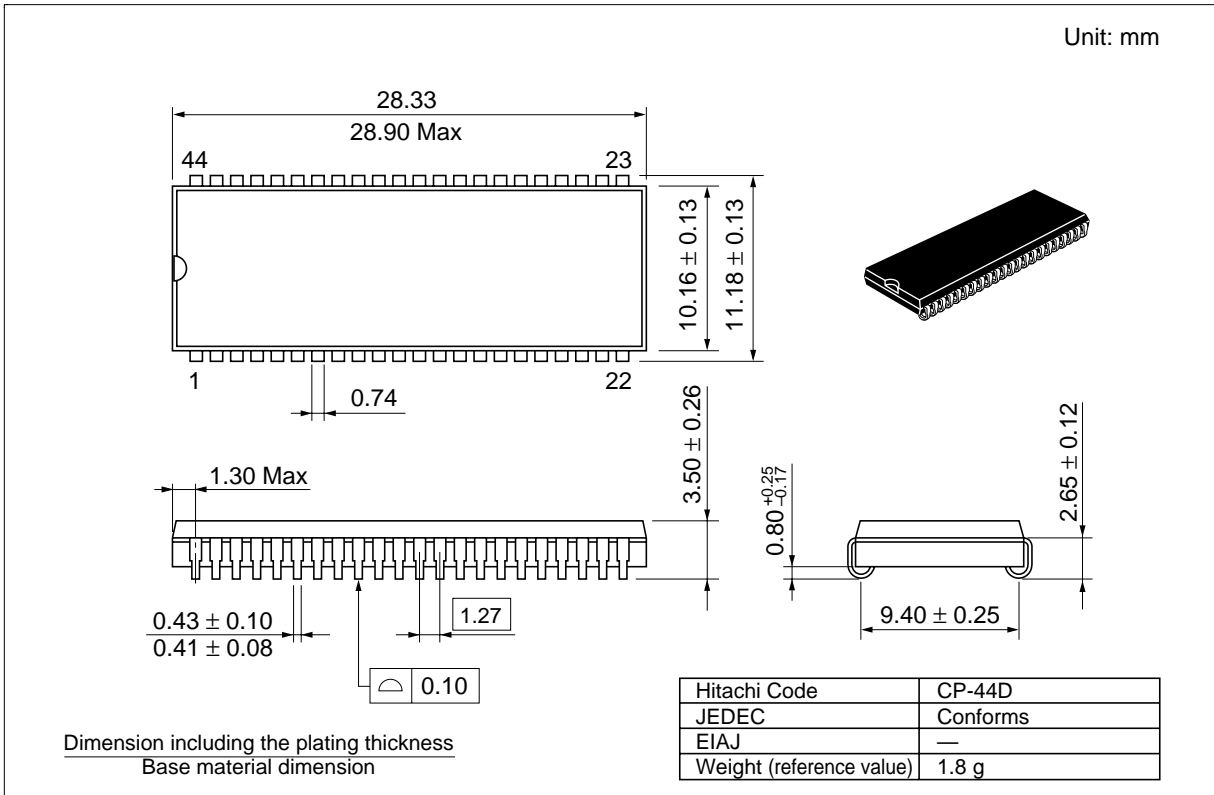
Low V_{CC} Data Retention Timing Waveform



HM6216255H Series

Package Dimensions

HM6216255HJP/HLJP Series (CP-44D)



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