82562EZ 10/100 Mbps Platform LAN Connect (PLC)

Networking Silicon

Datasheet

Product Features

- IEEE 802.3 10BASE-T/100BASE-TX compliant physical layer interface
- IEEE 802.3u Auto-Negotiation support
- Digital Adaptive Equalization control
- Link status interrupt capability
- XOR tree mode support
- 3-port LED support (speed, link and activity)
- 10BASE-T auto-polarity correction
- LAN Connect interface
- 82540EM layout compatible
- Diagnostic loopback mode
- 1:1 transmit transformer ratio support
- Low power (less than 300 mW in active transmit mode)
- Reduced power in “unplugged mode” (less than 50 mW)
- Automatic detection of “unplugged mode”
- 3.3 V device
- Thin BGA 15mm^2 package
- 82562EX with Alert on LAN support available
- Lead-free[a] 196-pin Ball Grid Array (BGA). (Devices that are lead-free are marked with a circled “e1” and have the product code: LUxxxxxx.)

a.This device is lead-free. That is, lead has not been intentionally added, but lead may still exist as an impurity at <1000 ppm. The Material Declaration Data Sheet, which includes lead impurity levels and the concentration of other Restriction on Hazardous Substances (RoHS)-banned materials, is available at:

`ftp://download.intel.com/design/packtech/material_content_IC_Package.pdf#pagemode=bookmark`

In addition, this device has been tested and conforms to the same parametric specifications as previous versions of the device.
For more information regarding lead-free products from Intel Corporation, contact your Intel Field Sales representative.

Revision 1.5
January 2005

Revision History

Revision	Revision Date	Description
0.5	Sep 2001	Initial release (Intel Secret)
0.6	Oct 2001	Update to Table 10 - Pin Assignments (Intel Secret)
1.0	Apr 2002	Added part number (Intel Confidential)
1.1	Jul 2002	Table 15- Pin assignments revised from Rev. 1.3 to Rev 2.0
1.2	Nov 2003	Removed confidential status
1.3	Nov 2004	Updated signal names to match design guides and reference schematics.
1.4	Nov 2004	• Added lead-free information. • Added Test Port Functionality section. • Added information about migrating from a 2-layer 0.36 mm wide-trace substrate to a 2-layer 0.32 mm wide-trace substrate. Refer to the section on Package and Pinout Information. • Added statement that no changes to existing soldering processes are needed for the 2-layer 0.32 mm wide-trace substrate change in the section describing “Package Information”.
1.5	January 2005	• Added a note for PHY signals RBIAS100 and RBIAS10 to Section 3.3.

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Contents

1.0 Introduction

1.1 Overview

The 82562EZ is a highly-integrated Platform LAN Connect device designed for 10 or 100 Mbps Ethernet systems. It is based on the IEEE 10BASE-T and 100BASE-TX standards. The IEEE 802.3u standard for 100BASE-TX defines networking over two pairs of Category 5 unshielded twisted pair cable or Type 1 shielded twisted pair cable.

The 82562EZ complies with the IEEE 802.3u Auto-Negotiation standard and the IEEE 802.3x Full Duplex Flow Control standard. The 82562EZ also includes a PHY interface compliant to the current platform LAN connect interface.

1.2 Scope

This document contains datasheet information for the 82562EZ Platform LAN Connect device, including signal descriptions, DC and AC specifications, packaging data, and pinout information.

1.3 Features

- IEEE 802.3 10BASE-T/100BASE-TX compliant physical layer interface
- IEEE 802.3u Auto-Negotiation support
- Digital Adaptive Equalization control
- Link status interrupt capability
- XOR Tree mode support for board testing
- 3-port LED support (speed, link and activity)
- 10BASE-T auto-polarity correction
- Platform LAN connect interface support
- 82540EM layout compatible
- Diagnostic loopback mode
- 1:1 transmit transformer ratio support
- Low power (less than 300 mW in active transmit mode)
- Reduced power in “unplugged mode” (less than 50 mW)
- Automatic detection of “unplugged mode”
- 3.3 V device
- Thin Ball Grid Array (BGA) 15mm^2 package
- 82562EX with Alert on LAN support available

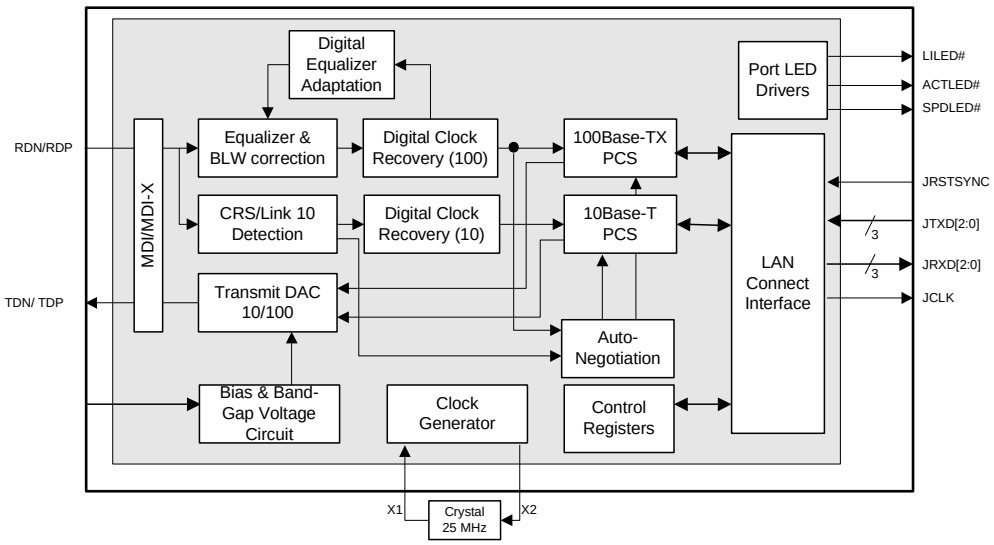
1.4 Reference Documents

- IEEE 802.3 Standard for Local and Metropolitan Area Networks, Institute of Electrical and Electronics Engineers
- 82555 10/100 Mbps LAN Physical Layer Interface Datasheet, Intel Corporation
- LAN Connect Interface Specification, Intel Corporation
- 82562EZ(EX)/82551QM & 82540EM Combined Footprint LOM Design Guide, AP-434, Intel Corporation
- 82562EZ(EX)/82547GI(EI) Dual Footprint Design Guide, AP-440, Intel Corporation
- 82540EP/82541(PI/GI/EI) & 82562EZ(EX) Dual Footprint Design Guide, AP-444, Intel Corporation
- 82562EZ(EX)/82551ER(IT) & 82541ER Combined Footprint LOM Design Guide, AP-456, Intel Corporation

2.0 82562EZ Architectural Overview

The 82562EZ is a highly integrated Platform LAN Connect device that combines a 10BASE-T and 100BASE-TX physical layer interfaces. The 82562EZ supports a single interface fully compliant with the IEEE 802.3 standard. Figure 1 provides a block diagram of the 82562EZ architecture.

Figure 1. 82562EZ Block Diagram



Four pins, test Enable (TESTEN), Test Clock (ISOL_TCK), Test Input (ISOL_TI), and Test Execute (ISOL_EXEC), define the general operation of the device. Table 1 shows the pin settings for the different modes of operation.

Table 1. 82562EZ Hardware Configuration

Mode of Operation	TESTEN	ISOL_TCK	ISOL_TI	ISOL_ EXEC	Comments
Normal operating mode	0	0	0	0	The ISOL_TCK, ISOL_TI, and ISOL_EXEC pins can remain floating.
Isolate mode (Tri-state and full power-down mode)	0	1	1	1	The device is in tri-state and power-down mode.
	1	1	1	1	The device is in tri-state and the fully powered down.
XOR Tree	1	0	0	0	The XOR Tree is used for board testing and tri-state mode.

NOTE: Combinations not shown in Table 1 are reserved and should not be used.

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3.0 82562EZ Signal Descriptions

3.1 Signal Type Definitions

Type	Name	Description
I	Input	Input pin to the 82562EZ.
O	Output	Output pin from the 82562EZ.
I/O	Input/Output	Multiplexed input and output pin to and from the 82562EZ.
MLT	Multi-level analog I/O	Multi-level analog pin used for input and output.
B	Bias	Bias pin used for ground connection through a resistor or an external voltage reference.
DPS	Digital Power Supply	Digital power or ground pin for the 82562EZ.
APS	Analog Power Supply	Analog power or ground pin for the 82562EZ.

3.2 Twisted Pair Ethernet (TPE) Pins

Pin Name	Type	Description
TDP TDN	MLT	**Transmit Differential Pair.** The transmit differential pair sends serial bit streams to the unshielded twisted pair (UTP) cable. The differential pair is a two-level signal in 10BASE-T (Manchester) mode and a three-level signal in 100BASE-TX mode (MLT-3). These signals directly interface with the isolation transformer.
RDP RDN	MLT	**Receive Differential Pair.** The receive differential pair receive the serial bit stream from an unshielded twisted pair (UTP) cable. The differential pair is a two-level signal in 10BASE-T mode (Manchester) or a three-level signal in 100BASE-TX mode (MLT-3). These signals directly interface with an isolation transformer.

3.3 External Bias Pins

Pin Name	Type	Description
RBIAS100	B	**Reference Bias Resistor (100 Mbps).** This pin should be connected to a pull-down resistor.[a]
RBIAS10	B	**Reference Bias Resistor (10 Mbps).** This pin should be connected to a pull-down resistor.[a]

a. Based on some board designs, RBIAS100 and RBIAS10 values may need to be increased/decreased to compensate for high/low MDI transmit amplitude. See the *82562EZ(EX)/82551ER(IT) & 82541ER Combined Footprint LOM Design Guide* for more information.

3.4 Clock Pins

Pin Name	Type	Description
X1	I	**Crystal Input Clock.** X1 and X2 can be driven by an external 25 MHz crystal of 30 PPM. Otherwise, X1 is driven by an external metal-oxide semiconductor (MOS) level 25 MHz oscillator when X2 is left floating.
X2	O	**Crystal Output Clock.** X1 and X2 can be driven by an external 25 MHz crystal of 30.

3.5 Platform LAN Connect Interface Pins

Pin Name	Type	Description
JCLK	O	**LAN Connect Clock.** The LAN Connect Clock is driven by the 82562EZ on two frequencies depending on operation speed. When the 82562EZ is in 100BASE-TX mode, JCLK drives a 50 MHz clock. Otherwise, JCLK drives a 5 MHz clock for 10BASE-T. The JCLK does not stop during normal operation.
JRSTSYNC	I	**Reset/Synchronize.** This is a multiplexed pin and is driven by the Media Access Control (MAC) layer device. Its functions are: • Reset. When this pin is asserted beyond one LAN Connect clock period, the 82562EZ uses this signal Reset. To ensure reset of the 82562EZ, the Reset signal should remain active for at least 500 µseconds. • Synchronize. When this pin is activated synchronously, for only one LAN Connect clock period, it is used to synchronize the MAC and PHY on LAN Connect word boundaries.
JTXD[2:0]	I	**LAN Connect Transmit Data.** The LAN Connect transmit pins are used to transfer data from the MAC device to the 82562EZ. These pins are used to move transmitted data and real time control and management data. They also transmit out of band control data from the MAC to the PHY. The pins should be fully synchronous to JCLK.
JRXD[2:0]	O	**LAN Connect Receive Data.** The LAN Connect receive pins are used to transfer data from the 82562EZ to the MAC device. These pins are used to move received data and real time control and management data. They also move out of band control data from the PHY to the MAC. These pins are synchronous to JCLK.

3.6 LED Pins

Pin Name	Type	Description
LILED#	O	**Link Integrity LED.** The LED is active low and the Link Integrity LED pin indicates link status in either 10BASE-T or 100BASE-TX mode. If a link is present in either mode, the LILED is asserted.
ACTLED#	O	**Activity LED.** The LED is active low and the Activity LED signal indicates either receive or transmit activity. When no activity is present, the LED is off. The Activity LED will flicker when activity is present. The flicker rate depends on the activity load. The individual address LED control bit (Word A hexadecimal, bit 4) in the ICH4 EEPROM can select the ACTLED# behavior. It controls the Activity LED (ACTLED#) functionality in Wake on LAN (WOL) mode. 0 = In WOL mode, the ACTLED# is activated by the transmission and reception of broadcast and individual address match packets. 1 = In WOL mode, the ACTLED# is activated by the transmission and reception of individual address match packets only. This bit is configured by the OEM and is activated by a transmission and reception of individual address match packets.
SPDLED#	O	**Speed LED.** The LED is active low and the Speed LED signal indicates the speed of operation, either 10 Mbps or 100 Mbps. The Speed LED is on during 100BASE-TX operation and off in 10BASE-T mode.

3.7 Miscellaneous Control Pins

Pin Name	Type	Description
ADV10	I	**Advertise 10 Mbps Only.** The Advertise 10 Mbps Only signal is asserted high, and the 82562EZ advertises only 10BASE-T technology during Auto-Negotiation processes in this state. Otherwise, the 82562EZ advertises all of its technologies. Note: ADV10 has an internal pull-down resistor.
ISOL_TCK	I	**Test Clock.** The Test Clock signal sets the device into asynchronous test mode in conjunction with the Test Input, Test Execute and Test Enable pins (refer to Table 1, “82562EZ Hardware Configuration”). In the manufacturing test mode, it acts as the test clock. Note: ISOL_TCK has an internal pull-down resistor.
ISOL_TI	I	**Test Input.** The Test Input signal sets the device into asynchronous test mode in conjunction with the Test Clock, Test Execute and Test Enable pins (refer to Table 1, “82562EZ Hardware Configuration”). In the manufacturing test mode, it acts as the test data input pin. Note: ISOL_TI has an internal pull-down resistor.
ISOL_EXEC	I	**Test Execute.** The Test Execute signal sets the device into asynchronous test mode in conjunction with the Test Clock, Test Input, and Test Enable pins (refer to Table 1, “82562EZ Hardware Configuration”). In the manufacturing test mode, it places the command that was entered through the TI pin in the instruction register. Note: ISOL_EXEC has an internal pull-down resistor.
TOUT	O	**Test Output.** The Test Output pin is used for Boundary XOR scan output. In the manufacturing test mode, it acts as the test output port.
TESTEN	I	**Test Enable.** The Test Enable pin is used to enable test mode and should be pulled down to V_{SS} to allow XOR Tree test mode.

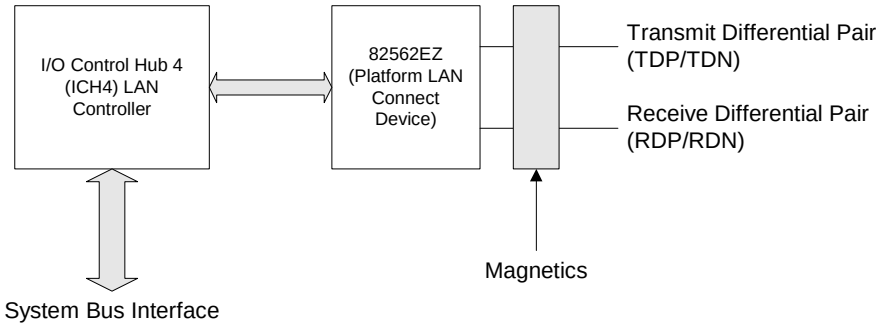
3.8 Power and Ground Connections

Pin Name	Type	Description
VCC	DPS	**Digital 3.3 V Power.** These pins should be connected to the main digital power supply.
VSS	DPS	**Digital Ground.** These pins should be connected to the main digital ground.

4.0 Physical Layer Interface Functionality

The 82562EZ is designed to work in Data Terminating Equipment (DTE) mode only. It supports a direct glueless interface to all components that comply with the LAN Connect specification. The following figure shows how the 82562EZ PLC can be used in a 10/100 Mbps Ethernet switch design.

Figure 2. 82562EZ 10/100 Mbps Ethernet Solution



4.1 100BASE-TX Mode

4.1.1 100BASE-TX Transmit Blocks

The transmit subsection of the 82562EZ accepts 3 bit wide data from the LAN Connect unit. Another subsection passes data unconditionally to the 4B/5B encoder.

The 4B/5B encoder accepts nibble-wide data (4 bits) from the CSMA unit and compiles it into 5-bit-wide parallel symbols. These symbols are scrambled and serialized into a 125 Mbps bit stream, converted by the analog transmit driver into a MLT-3 waveform format, and transmitted onto the Unshielded Twisted Pair (UTP) or Shielded Twisted Pair (STP) wire.

4.1.1.1 100BASE-TX 4B/5B Encoder

The 4B/5B encoder complies with the IEEE 802.3u 100BASE-TX standard. Four bits are encoded according to the transmit 4B/5B lookup table. The lookup table matches a 5-bit code to each 4-bit code. Table 2 lists the 4B/5B encoding scheme associated with the given symbol.

Table 2. 4B/5B Encoder

Symbol	5B Symbol Code	4B Nibble Code
0	11110	0000
1	01001	0001
2	10100	0010
3	10101	0011
4	01010	0100
5	01011	0101

Symbol	5B Symbol Code	4B Nibble Code
6	01110	0110
7	01111	0111
8	10010	1000
9	10011	1001
A	10110	1010
B	10111	1011
C	11010	1100
D	11011	1101
E	11100	1110
F	11101	1111
I	11111	Inter Packet Idle Symbol (No 4B)
J	11000	1st Start of Packet Symbol 0101
K	10001	2nd Start of Packet Symbol 0101
T	01101	1st End of Packet Symbol
R	00111	2nd End of Packet Symbol and Flow Control
V	00000	INVALID
V	00001	INVALID
V	00010	INVALID
V	00011	INVALID
H	00100	INVALID
V	00101	INVALID
V	00110	INVALID
V	01000	INVALID
V	01100	INVALID
V	10000	Flow Control S
V	11001	INVALID

4.1.1.2 100BASE-TX Scrambler and MLT-3 Encoder

Data is scrambled in 100BASE-TX in order to reduce electromagnetic emissions during long transmissions of high-frequency data codes. The scrambler logic accepts 5 bits from the 4B/5B encoder block and presents the scrambled data to the MLT-3 encoder. The 82562EZ implements the 11-bit stream cipher scrambler as adopted by the ANSI XT3T9.5 committee for UTP operation. The cipher equation used is:

$X[n] = X[n-11] + X[n-9] \pmod 2$

The MLT-3 encoder receives the scrambled Non-Return to Zero (NRZ) data stream from the scrambler and encodes the stream into MLT-3 for presentation to the driver. MLT-3 is similar to NRZ1 coding, but three levels are output instead of two. The three output levels are positive, negative and zero. When an NRZ “0” arrives at the input of the encoder, the last output level is maintained (either positive, negative or zero). When an NRZ “1” arrives at the input of the encoder, the output steps to the next level. The order of steps is negative-zero-positive-zero which continues periodically. Refer to IEEE 802.3 Specification for further details.

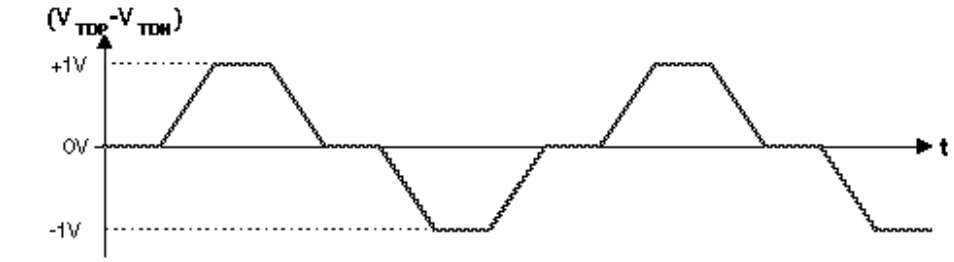
4.1.1.3 100BASE-TX Transmit Framing

The 82562EZ does not differentiate between the fields of the MAC frame containing preamble, start of frame delimiter, data and Cyclic Redundancy Check (CRC). The 82562 encodes the first byte of the preamble as the “JK” symbol, encodes all other pieces of data according to the 4B/5B lookup table, and adds the “TR” code after the end of the packet. The 82562 scrambles and serializes the data into a 125 Mbps stream, encodes it as MLT-3, and drives it onto the wire.

4.1.1.4 Transmit Driver

The transmit differential lines are implemented with a digital slope controlled current driver that meets Twisted Pair Physical Media Device (TP-PMD) specifications. Current is sunk from the isolation transformer by the transmit differential pins. The conceptual transmit differential waveform for 100 Mbps is illustrated in the following figure.

Figure 3. Conceptual Transmit Differential Waveform



The magnetics module external to the 82562EZ converts I_{TDP} and I_{TDN} to 2.0 V_{PP}, as required by the TP-PMD specification. The same magnetics used for 100BASE-TX mode can also work in 10BASE-T mode.

4.1.2 100BASE-TX Receive Blocks

The receive subsection of the 82562EZ accepts 100BASE-TX MLT-3 data on the receive differential pair. Due to the advanced digital signal processing design techniques employed, the 82562EZ will accurately receive valid data from Category 5 (CAT5) UTP and Type 1 STP cable of length well in excess of 100 meters.

4.1.2.1 Adaptive Equalizer

The distorted MLT-3 signal at the end of the wire is restored by the equalizer. The equalizer performs adaptation based on the shape of the received signal, equalizing the signal to meet superior data dependent jitter performance.

4.1.2.2 Receive Clock and Data Recovery

The clock recovery circuit uses advanced digital signal processing technology to compensate for various signal jitter causes. The circuit recovers the 125 MHz clock and data and presents the data to the MLT-3 decoder.

4.1.2.3 MLT-3 Decoder, Descrambler, and Receive Digital Section

The 82562EZ first decodes the MLT-3 data, and then the descrambler reproduces the 5B symbols originated in the transmitter. The descrambling is based on synchronization to the transmission of the 11-bit Linear Feedback Shift Register (LFSR) during an idle phase. The data is decoded at the 4B/5B decoder. After the 4B symbols are obtained, the 82562EZ outputs the receive data to the CSMA unit.

In 100BASE-TX mode, the 82562EZ can detect errors in receive data in a number of ways. Any of the following conditions is considered an error:

- Link integrity fails in the middle of frame reception.
- The start of stream delimiter “JK” symbol is not fully detected after idle.
- An invalid symbol is detected at the 4B/5B decoder.
- Idle is detected in the middle of a frame (before “TR” is detected).

4.2 10BASE-T Mode

4.2.1 10BASE-T Transmit Blocks

4.2.1.1 10BASE-T Manchester Encoder

After the 2.5 MHz clocked data is serialized in a 10 Mbps serial stream, the 20 MHz clock performs the Manchester encoding. The Manchester code always has a mid-bit transition. The boundary transition occurs only when the data is the same from bit to bit. For example, if the value is 11b, then the change is from low to high within the boundary.

4.2.1.2 10BASE-T Driver and Filter

Since 10BASE-T and 100BASE-TX have different filtration needs, both filters are implemented inside the chip. The 82562EZ supports both technologies through one pair of transmit differential pins and by externally sharing the same magnetics.

In 10 Mbps mode the line drivers use a pre-distortion algorithm to improve jitter tolerance. The line drivers reduce their drive level during the second half of “wide” (100 ns) Manchester pulses and maintain a full drive level during all narrow (50 ns) pulses and the first half of the wide pulses. This reduces line overcharging during wide pulses, a major source of jitter.

4.2.2 10BASE-T Receive Blocks

4.2.2.1 10BASE-T Manchester Decoder

The 82562EZ performs Manchester decoding and timing recovery in 10BASE-T mode. The Manchester encoded data stream is decoded from the receive differential pair. This data is transferred to the controller at 2.5 MHz/nibble. The high-performance circuitry of the 82562EZ exceeds the IEEE 802.3 jitter requirements.

4.2.2.2 10BASE-T Twisted Pair Ethernet (TPE) Receive Buffer and Filter

In 10 Mbps mode, data is expected to be received on the receive differential pair after passing through isolation transformers. The filter is implemented inside the 82562EZ for supporting single magnetics that are shared with the 100BASE-TX side. The input differential voltage range for the Twisted Pair Ethernet (TPE) receiver is greater than 585 mV and less than 3.1 V. The TPE receive buffer distinguishes valid receive data, link test pulses, and the idle condition, according to the requirements of the 10BASE-T standard.

The following line activity is determined to be inactive and is rejected as invalid data:

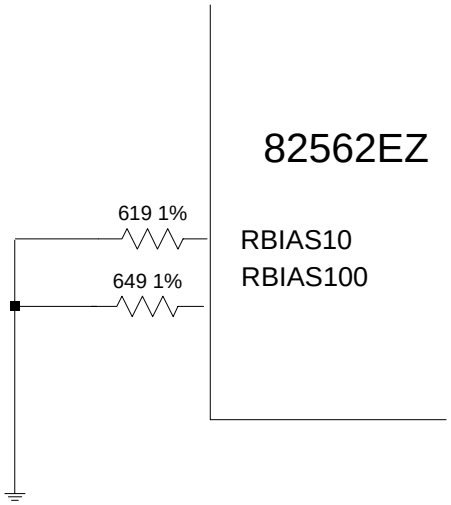
- Differential pulses of peak magnitude less than 300 mV.
- Continuous sinusoids with a differential amplitude less than 6.2 V_{pp} and frequency less than 2 MHz.
- Sine waves of a single cycle duration starting with 0° or 180° phase that have a differential amplitude less than 6.2 V_{pp} and a frequency of at least 2 MHz and not more than 16 MHz. These single-cycle sine waves are discarded only if they are preceded by 4 bit times (400 ns) of silence.

All other activity is determined to be either data, link test pulses, Auto-Negotiation fast link pulses, or the idle condition.

4.3 Analog References

The 82562EZ has two inputs, RBIAS100 and RBIAS10, that require external resistor connections to set biases for its internal analog section. The input pins are sensitive to the resistor value and experimentation is required to determine the correct values for any given layout. Resistors of 1% tolerance should be used.

Figure 4. Analog References



4.4 Dynamic Reduced Power & Auto Plugging Detection

The 82562EZ can be configured to support a dynamic reduced power mode. This mode reduces power consumption of the 82562EZ when LAN activity is not present. The reduced power mode decreases power consumption from 300 mW to about 50 mW and is based on automatic detection of cable plugging. If the 82562EZ is configured to support dynamic power reduction, it enters the reduced power mode whenever a cable is not connected to the device. In reduced power mode, the 82562EZ shuts off the link circuits, except the circuit used for the automatic plugging detection. On the LAN Connect side, the entire interface remains active, including full access to all MII Management Interface (MMI) registers. In this mode, the 82562EZ switches to the 10 Mbps speed interface
(5 MHz for LAN Connect). Thus, the reduced power mode is fully transparent to driver.

4.4.1 Auto Plugging Detection

The 82562EZ senses the link all the time. If it detects loss of any link activity for more than 6.6 seconds, it indicates to the Media Access Controller (MAC) an “unplugged state” by resetting the SQL LAN Connect control bit. If the 82562EZ is in reduced power mode and link activity is detected, the 82562EZ notifies the MAC (in less than 1 second) that it is in a “plugged state” by setting the SQL LAN Connect control bit. Link activity detection is based on energy detection.

4.4.2 Dynamic Reduced Power

The 82562EZ can be configured to support dynamic reduced power. In the dynamic reduced power mode, the 82562EZ transitions to reduced power mode when an unplugged state is detected. The 82562EZ will only return to full power if the reduced power bit on the LAN Connect is reset and a plugged state is detected. However, if the 82562EZ is not configured to support dynamic reduced power, the 82562EZ operates according to the LAN Connect power-down bit (in other words, the 82562EZ will operate in reduced power mode only if the LAN Connect power-down bit is set).

4.4.3 Configuration

The dynamic reduced power mode is configured through bit 13 of register 16. The default value is disabled (0). The status of the 82562EZ can be read through bits 10:9 of register 16. When the 82562EZ is in reduced power mode, these two bits are set to 1b.

Table 3. Register 16 (10 Hexadecimal): PLC Status, Control and Address Data

Bit	Name	Description	Read/Write
13	Dynamic Reduced Power Down	0 = Automatic reduced power down enabled 1 = Automatic reduced power down disabled (default)	Read/Write
10	100BASE-TX Power Down	The 100BASE-TX Power Down bit indicates the power state. 0 = Normal operation (default) 1 = Power down	Read Only
9	10BASE-T Power Down	The 10BASE-T Power Down bit indicates the power state. 0 = Normal operation (default) 1 = Power down	Read Only

The 82562EZ can enter a reduced power state manually through bit 11 of register 0. This bit is ORed with the LAN Connect power down bit, which allows the 82562EZ to enter a reduced power state.

Table 4. Register 0: Control Data

Bit	Name	Description	Read/Write
11	Reduced Power Down	0 = Reduced power down disabled (normal operation; default) 1 = Reduced power down enabled	Read/Write

4.5 Reset

When 82562EZ's Reset signal (RSTSYNC) is asserted for at least 500 µseconds, all internal circuits are reset. The 82562EZ can also be reset through the MII management register reset bit (register 0, bit 15).

4.6 LAN Connect Interface

The 82562EZ supports the LAN connect interface as specified in the LAN Connect Interface Specification. The LAN Connect is the I/O Control Hub 4(ICH4) interface to the 82562EZ. The 8-pin interface incorporates all MII and MII management functionality and includes the reset functionality as well.

4.6.1 LAN Connect Clock

The 82562EZ drives a 50 MHz or 5 MHz clock to the MAC depending on the selected technology (100BASE-TX or 10BASE-T, respectively). The 82562EZ does not stop the LAN Connect clock for any reason. During reduced power mode, the 82562EZ drives a 5 MHz clock.

4.6.2 LAN Connect Reset

To determine the type of signal on the PLC Reset/Synchronization pin, the 82562EZ filters out pulses that are less than 200 nanoseconds. To reset the 82562EZ, the pulse should be longer than 500 µseconds.

4.7 LED Functionality

Table 5. LED Functionality

LED Driver	Function	Description
ACTLED#	Activity	The driver blinks at a rate related to the utilization. The blinking occurs during transmission or reception of a frame.
SPDLED#	Speed	The driver is low for 100BASE-TX operation and high for 10BASE-T mode.
LILED#	Link valid	The driver is low when a valid link is present.

Note: This page is intentionally left blank.

5.0 Platform LAN Connect Registers

The following subsections describe PHY registers that are accessible through the LAN Connect management frame protocol.

Acronyms mentioned in the registers are defined as follows:

- SC: Self cleared.
- RO: Read only.
- RW: Read/Write.
- E: EEPROM setting affects content.
- LL: Latch low.
- LH: Latch high.

5.1 Medium Dependent Interface Registers 0 through 7

5.1.1 Register 0: Control Register Bit Definitions

Bit(s)	Name	Description	Default	R/W
15	Reset	This bit sets the status and control register of the PHY to their default states and is self-clearing. The PHY returns a value of one until the reset process has completed and accepts a read or write transaction. 0 = Normal operation 1 = PHY Reset	0	RW SC
14	Loopback	This bit enables loopback of transmit data nibbles to the receive data path. The PHY receive circuitry is isolated from the network. Note that this may cause the descrambler to lose synchronization and produce 560 nanoseconds of “dead time.” Note also that the loopback configuration bit takes priority over the Loopback MDI bit. 0 = Loopback disabled (normal operation) 1 = Loopback enabled	0	RW
13	Speed Selection	This bit is valid on read and controls speed when Auto-Negotiation is disabled. 0 = 10 Mbps 1 = 100 Mbps	1	RW
12	Auto-Negotiation Enable	This bit enables Auto-Negotiation. Bits 13 and 8, Speed Selection and Duplex Mode, respectively, are ignored when Auto-Negotiation is enabled. 0 = Auto-Negotiation disabled 1 = Auto-Negotiation enabled	1	RW
11	Reduced Power Down	This bit sets the PHY into a low power mode. 0 = Power down disabled (normal operation) 1 = Power down enabled	0	RW

Bit(s)	Name	Description	Default	R/W
10	Isolate	This bit allows the PHY to isolate the medium independent interface. The PHY is disconnected from the LAN Connect block on both the transmit and receive side. 0 = Normal operation 1 = Isolates internal medium independent interface	0	RW
9	Restart Auto-Negotiation	This bit restarts the Auto-Negotiation process and is self-clearing. 0 = Normal operation 1 = Restart Auto-Negotiation process	0	RW SC
8	Duplex Mode	This bit controls the duplex mode when Auto-Negotiation is disabled. When Auto-Negotiation is enabled this bit is read only and always equals 1b. When the PHY is placed in Loopback mode, the behavior of the PHY shall not be affected by the status of this bit. 0 = Half Duplex 1 = Full Duplex	0	RW/ RO
7	Collision Test	This bit is not used in the 82562EZ and has a default value of 1b. (If it is used in other devices, it forces a collision in response to the assertion of the transmit enable signal.)	1	RW
6:0	Reserved	These bits are reserved and should be set to 0000000b.	0	RW

5.1.2 Register 1: Status Register Bit Definitions

Bit(s)	Name	Description	Default	R/W
15	Reserved	This bit is reserved and should be set to 0b.	0	RO
14	100BASE-TX Full-duplex	This bit enables 100BASE-TX full-duplex operation and is dependent on ADV10. If ADV10 is active, the default value is 0. 0 = PHY unable to perform full-duplex 100BASE-TX 1 = PHY able to perform full-duplex 100BASE-TX	1	RO
13	100 Mbps Half-duplex	This bit enables 100BASE-TX half-duplex operation and is dependent on ADV10. If ADV10 is active, the default value is 0. 0 = PHY unable to perform half-duplex 100BASE-TX 1 = PHY able to perform half-duplex 100BASE-TX	1	RO
12	10 Mbps Full-duplex	This bit enables 10BASE-T full duplex operation. 0 = PHY unable to perform full-duplex 10BASE-T 1 = PHY able to perform full-duplex 10BASE-T	1	RO
11	10 Mbps Half-duplex	This bit enables 10BASE-T half-duplex operation. 0 = PHY unable to perform half-duplex 10BASE-T 1 = PHY able to perform half-duplex 10BASE-T	1	RO
10:7	Reserved	These bits are reserved and should be set to 0000b.	0	RO
6	Management Frames Preamble Suppression	This bit allows the 82562EZ to receive management frames with suppressed preamble. 0 = PHY will not accept management frames with preamble suppressed 1 = PHY will accept management frames with preamble suppressed	0	RO

Bit(s)	Name	Description	Default	R/W
5	Auto-Negotiation Complete	This bit reflects status of the Auto-Negotiation process. 0 = Auto-Negotiation process has not completed 1 = Auto-Negotiation process completed	0	RO
4	Remote Fault	0 = No remote fault condition detected 1 = Remote fault condition detected	0	RO
3	Auto-Negotiation Ability	This bit reflects the PHY's Auto-Negotiation ability status. 0 = PHY is unable to perform Auto-Negotiation 1 = PHY is able to perform Auto-Negotiation	1	RO
2	Link Status	This bit reflects link status. 0 = Invalid link detected 1 = Valid link established	0	RO LL
1	Jabber Detect	This bit is used only in 10BASE-T mode. 0 = No jabber condition detected 1 = Jabber condition detected	0	RO LH
0	Extended Capability	This bit enables the extended register capabilities. 0 = Extended register capabilities disabled 1 = Extended register capabilities enabled	1	RO

5.1.3 Register 2: PHY Identifier Register Bit Definitions

Bit(s)	Name	Description	Default	R/W
15:0	PHY ID (high byte)	Value: 02A8 hexadecimal	--	RO

5.1.4 Register 3: PHY Identifier Register Bit Definitions

Bit(s)	Name	Description	Default	R/W
15:0	PHY ID (low byte)	Value: 0320 hexadecimal	--	RO

5.1.5 Register 4: Auto-Negotiation Advertisement Register Bit Definitions

Bit(s)	Name	Description	Default	R/W
15	Next Page	This bit is a constant 0, transmit primary capability data page.	0	RO
14	Reserved	This bit is reserved and should be set to 0b.	0	RO
13	Remote Fault	0 = No remote fault 1 = Indicate link partner's remote fault	0	RW
12:5	Technology Ability Field	Technology Ability Field is an 8-bit field containing information indicating supported technologies specific to the selector field value.	00101111	RW

Bit(s)	Name	Description	Default	R/W
4:0	Selector Field	The Selector Field is a 5-bit field identifying the type of message to be sent by Auto-Negotiation. This field is read only and contains a value of 00001b, IEEE Standard 802.3.	00001	RO

5.1.6 Register 5: Auto-Negotiation Link Partner Ability Register Bit Definitions

Bit(s)	Name	Description	Default	R/W
15	Next Page	This bit reflects the PHY's link partner's Next Page ability.	--	RO
14	Acknowledge	This bit is used to indicate that the 82562EZ has successfully received its link partner's Auto-Negotiation advertising ability.	--	RO
13	Remote Fault	This bit reflects the PHY's link partner's Remote Fault condition.	--	RO
12:5	Technology Ability Field	This bit reflects the PHY's link partner's Technology Ability Field.	--	RO
4:0	Selector Field	This bit reflects the PHY's link partner's Selector Field.	--	RO

5.1.7 Register 6: Auto-Negotiation Expansion Register Bit Definitions

Bit(s)	Name	Description	Default	R/W
15:5	Reserved	These bits are reserved and should be set to 0.	0	RO
4	Parallel Detection Fault	This bit clears itself on read. 0 = No fault detected via parallel detection 1 = Fault detected via parallel detection (multiple link fault occurred)	0	RO SC LH
3	Link Partner Next Page Able	0 = Link Partner is not Next Page able 1 = Link Partner is Next Page able	0	RO
2	Next Page Able	0 = Local drive is not Next Page able 1 = Local drive is Next Page able	0	RO
1	Page Received	This bit clears itself on read. 0 = New Page not received 1 = New Page received	0	RO SC LH
0	Link Partner Auto-Negotiation Able	0 = Link Partner is not Auto-Negotiation able 1 = Link Partner is Auto-Negotiation able	0	RO

5.2 Medium Dependent Interface Registers 8 through 15

Registers 8 through 15 are reserved for IEEE.

5.3 Medium Dependent Interface Registers 16 through 31

5.3.1 Register 16: PHY Status and Control Register Bit Definitions

Bit(s)	Name	Description	Default	R/W
15:14	Reserved	These bits are reserved and should be set to 00b.	00	RW
13	Reduced Power Down Disable	This bit disables the automatic reduced power down. 0 = Enable automatic reduced power down 1 = Disable automatic reduced power down	1	RW
12	Reserved	This bit is reserved and should be set to 0b.	0	RW
11	Receive De-Serializer In-Sync Indication	This bit indicates status of the 100BASE-TX Receive De-Serializer In-Sync.	--	RO
10	100BASE-TX Power-Down	This bit indicates the power state of 100BASE-TX PHY unit. 0 = Normal operation 1 = Power-down	1	RO
9	10BASE-T Power-Down	This bit indicates the power state of 10BASE-T PHY unit. 0 = Normal operation 1 = Power-Down	1	RO
8	Polarity	This bit indicates 10BASE-T polarity. 0 = Normal polarity 1 = Reverse polarity	--	RO
7	Reserved	This bit is reserved and should be set to 0b.	0	RO
6:2	PHY Address	These bits contain the sampled PHY address.	--	RO
1	Speed	This bit indicates the Auto-Negotiation result. 0 = 10 Mbps 1 = 100 Mbps	--	RO
0	Duplex Mode	This bit indicates the Auto-Negotiation result. 0 = Half-duplex 1 = Full-duplex	--	RO

5.3.2 Register 17: PHY Unit Special Control Bit Definitions

Bit(s)	Name	Description	Default	R/W
15	Scrambler By-pass	0 = Normal operations 1 = By-pass scrambler	0	RW
14	By-pass 4B/5B	0 = Normal operation 1 = 4 bit to 5 bit by-pass	0	RW
13	Force Transmit H-Pattern	0 = Normal operation 1 = Force transmit H-pattern	0	RW
12	Force 34 Transmit Pattern	0 = Normal operation 1 = Force 34 transmit pattern	0	RW

Bit(s)	Name	Description	Default	R/W
11	Valid Link	0 = Normal operation 1 = 100BASE-TX valid link	0	RW
10	Symbol Error Enable	0 = Normal operation 1 = Symbol error output is enabled	0	RW
9	Carrier Sense Disable	This bit controls the receive 100 carrier sense disable function. 0 = Carrier sense enabled 1 = Carrier sense disabled	0	RW
8	Disable Dynamic Power-Down	0 = Dynamic Power-Down enabled 1 = Dynamic Power-Down disabled	0	RW
7	Auto-Negotiation Loopback	0 = Auto-Negotiation normal mode 1 = Auto-Negotiation loopback	0	RW
6	MDI Tri-State	0 = Normal operation 1 = MDI Tri-state (transmit driver tri-states)	0	RW
5	Force Polarity	0 = Normal polarity 1 = Reversed polarity	0	RW
4	Auto Polarity Disable	0 = Normal polarity operation 1 = Auto Polarity disabled	0	RW
3	Squelch Disable	0 = Normal squelch operation 1 = 10BASE-T squelch test disable	0	RW
2	Extended Squelch	1 = 10BASE-T Extended Squelch control enabled 0 = 10BASE-T Extended Squelch control disabled	0	RW
1	Link Integrity Disable	0 = Normal Link Integrity operation 1 = Link disabled	0	RW
0	Jabber Function Disable	0 = Normal Jabber operation 1 = Jabber disabled	0	RW

5.3.3 Register 18: PHY Address Register

Bit(s)	Name	Description	Default	R/W
15:5	Reserved	These bits are reserved and should be set to a constant 0.	0	RO
4:0	PHY Address	These bits are set to the PHY's address.	00001	RO

5.3.4 Register 19: 100BASE-TX Receive False Carrier Counter Bit Definitions

Bit(s)	Name	Description	Default	R/W
15:0	Receive False Carrier	These bits are used for the false carrier counter.	--	RO SC

5.3.5 Register 20: 100BASE-TX Receive Disconnect Counter Bit Definitions

Bit(s)	Name	Description	Default	R/W
15:0	Disconnect Event	This field contains a 16-bit counter that increments for each disconnect event. The counter stops when it is full and self-clears on read	--	RO SC

5.3.6 Register 21: 100BASE-TX Receive Error Frame Counter Bit Definitions

Bit(s)	Name	Description	Default	R/W
15:0	Receive Error Frame	This field contains a 16-bit counter that increments once per frame for any receive error condition (such as a symbol error or premature end of frame) in that frame. The counter stops when it is full and self-clears on read.	--	RO SC

5.3.7 Register 22: Receive Symbol Error Counter Bit Definitions

Bit(s)	Name	Description	Default	R/W
15:0	Symbol Error Counter	This field contains a 16-bit counter that increments for each symbol error. The counter stops when it is full and self-clears on read. In a frame with a bad symbol, each sequential six bad symbols count as one.	--	RO SC

5.3.8 Register 23: 100BASE-TX Receive Premature End of Frame Error Counter Bit Definitions

Bit(s)	Name	Description	Default	R/W
15:0	Premature End of Frame	This field contains a 16-bit counter that increments for each premature end of frame event. The counter stops when it is full and self-clears on read.	--	RO SC

5.3.9 Register 24: 10BASE-T Receive End of Frame Error Counter Bit Definitions

Bit(s)	Name	Description	Default	R/W
15:0	End of Frame Counter	This is a 16-bit counter that increments for each end of frame event. The counter stops when it is full and self-clears on read.	--	RO SC

5.3.10 Register 25: 10BASE-T Transmit Jabber Detect Counter Bit Definitions

Bit(s)	Name	Description	Default	R/W
15:0	Jabber Detect Counter	This is a 16-bit counter that increments for each jabber detection event. The counter stops when it is full and self-clears on read.	--	RO SC

5.3.11 Register 27: PHY Unit Special Control Bit Definitions

Bit(s)	Name	Description	Default	R/W
15:6	Reserved	These bits are reserved and should be set to a constant 0.	0	RO
5	Switch Probe Mapping	This bit switches the mapping on the LEDs. The LED mapping is described below in bits 2:0, LED Switch Control. This bit should always be set to 0b.	0	RW
4	Reserved	This bit is reserved and should be set to 0.	0	RO
3	100BASE-TX Receive Jabber Disable	This bit enables the carrier sense disconnection while the PHY is in jabber mode at 100 Mbps speed.	0	RW
2:0	LED Switch Control	Value / ACTLED# / LILED# 000 Activity Link 001 Speed Collision 010 Speed Link 011 Activity Collision 100 Off Off 101 Off On 110 On Off 111 On On	000	RW

6.0 Voltage and Temperature Specifications

6.1 Absolute Maximum Ratings

Maximum ratings are listed below:

Case Temperature under Bias . . . . . 0° C to 135° C
Storage Temperature . . . . . -65° C to 150° C
Supply Voltage with respect to V_{SS} . . . . . -0.5 V to 3.45 V
Output Voltages . . . . . -0.50 V to 3.45 V
Input Voltages . . . . . V_{CC} to 3.45 V

Stresses above the listed absolute maximum ratings may cause permanent damage to the 82562EZ device. This is a stress rating only and functional operations of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6.2 DC Characteristics

Table 6. General DC Specifications

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
V_{CC}	Supply Voltage		3.0	3.3	3.45	V	
T	Temperature	Minimum/Maximum Case Temperature	0		85	C	
P	Power Consumption	10/100Mbps (transmitter on)		300		mW	
		Reduce Power		50		mW	
		Auto-Negotiation*		200		mW	

6.2.1 X1 Clock DC Specifications

Table 7. X1 Clock DC Specifications

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
V_{IL}	Input Low Voltage				0.8	V	
V_{IH}	Input High Voltage		2.0			V	
I_{ILIH}	Input Leakage Currents	$0 < V_{IN} < V_{CC}$			±10	µA	
C_I	Input Capacitance				8	pF	1

NOTES:
1. This characteristic is only characterized, not tested. It is valid for digital pins only.

6.2.2 LAN Connect Interface DC Specifications

Table 8. LAN Connect Interface DC Specifications

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
V_{CCJ}	Input/Output Supply Voltage		3.0		3.45	V	
V_{IL}	Input Low Voltage		-0.5		$0.3V_{CCJ}$	V	
V_{IH}	Input High Voltage		$0.6V_{CCJ}$		V_{CCJ} + 0.5	V	
I_{IL}	Input Leakage Current	$0 < V_{IN} < V_{CCJ}$			±10	µA	
V_{OL}	Output Low Voltage	I_{OUT} = 1500 µA			$0.1V_{CCJ}$	V	
V_{OH}	Output High Voltage	I_{OUT} = -500 µA	$0.9V_{CCJ}$			V	
C_{IN}	Input Pin Capacitance				8	pF	1

NOTES:
1. This characteristic is only characterized, not tested. It is valid for digital pins only.

6.2.3 LED DC Specifications

Table 9. LED DC Specifications

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
V_{OLLED}	Output Low Voltage	I_{OUT} = 10 mA			0.7	V	
V_{OHLED}	Output High Voltage	I_{OUT} = -10 mA	2.4			V	

6.2.4 10BASE-T Voltage and Current DC Specifications

Table 10. 10BASE-T Transmitter

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
V_{OD10}	Output Differential Peak Voltage	R_L = 100 Ω	2.2		2.8	V	1

NOTES: Current is measured between the transmit differential pins (TDP and TDN) at 3.3 V.
1. R_L is the resistive load measured across the transmit differential pins, TDP and TDN.

Table 11. 10BASE-T Receiver

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
R_{ID10}	Input Differential Resistance	DC	10			KΩ	1
V_{IDA10}	Input Differential Accept Peak Voltage	5 MHz ≤ f ≤ 10 MHz	585		3100	mV	
V_{IDR10}	Input Differential Reject Peak Voltage	5 MHz ≤ f ≤ 10 MHz			300	mV	
V_{ICM10}	Input Common Mode Voltage			$V_{CC/2}$		V	

NOTES:
1. The input differential resistance is measured across the receive differential pins, RDP and RDN.

6.2.5 100BASE-TX Voltage and Current DC Specifications

Table 12. 100BASE-TX Transmitter

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
V_{OD100}	Output Differential Peak Voltage	R_L = 100 Ω	0.95	1.0	1.05	V	1

NOTES: Current is measured between the transmit differential pins (TDP and TDN) at 3.3 V.
1. R_L is the resistive load measured across the transmit differential pins, TDP and TDN.

Table 13. 100BASE-TX Receiver

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
R_{ID100}	Input Differential Resistance	DC	10			K Ω	1
V_{IDA100}	Input Differential Accept Peak Voltage		500		1200	mV	
V_{IDR100}	Input Differential Reject Peak Voltage				100	mV	
V_{ICM100}	Input Common Mode Voltage			$V_{CC/2}$		V	

NOTES:
1. The input differential resistance is measured across the receive differential pins, RDP and RDN.

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7.0 82562EZ Test Port Functionality

The 82562EZ's XOR Tree Test Access Port (TAP) is the access point for test data to and from the device. The port provides the ability to perform basic production level testing.

7.1 Asynchronous Test Mode

An asynchronous test mode is supported for system level design use. The modes are selected through the use of the Test Port input pins (TESTEN, ISOL_TCK, ISOL_TI and ISOL_EXEC) in static combinations. During normal operation the test pins must be pulled down through a resistor (pulling Test high enables the test mode). All other port inputs may have a pull-down at the designers discretion.

7.2 Test Function Description

The 82562EZ TAP mode supports several tests that can be used in board level design. These tests can help verify basic functionality and test the integrity of solder connections on the board. The tests are described in the following sections.

The XOR Tree test mode is the most useful of the asynchronous test modes. It enables the placement of the 82562EZ to be validated at board test. The XOR Tree was chosen for its speed advantages. Modern Automated Test Equipment (ATE) can perform a complete peripheral scan without support at the board level. This command connects all output signals of the input buffers in the device periphery into an XOR Tree scheme. All output drivers of the output-buffers, except the test output (TOUT) pin, are put into high-Z mode. These pins are driven to affect the tree's output. Any hard strapped pins will prevent the tester from scanning correctly. The XOR Tree test mode is obtained by placing the test pins in the following configuration (refer to Table 14):

TESTEN = 1

ISOL_TCK = 0

ISOL_TI = 0

ISOL_EXEC = 0.

Table 14. XOR Tree Chain Order

Chain Order	Chain
1	JTXD2
2	JTXD1
3	JTXD0
4	JRSTSYNC
5	ADV10 (LAN_DISABLE#)
6	JCLK
7	JRXD2
8	JRXD1
9	JRXD0
10	ACTLED#

Table 14. XOR Tree Chain Order

Chain Order	Chain
11	SPDLED#
12	LILED#
XOR Tree Output	TOUT

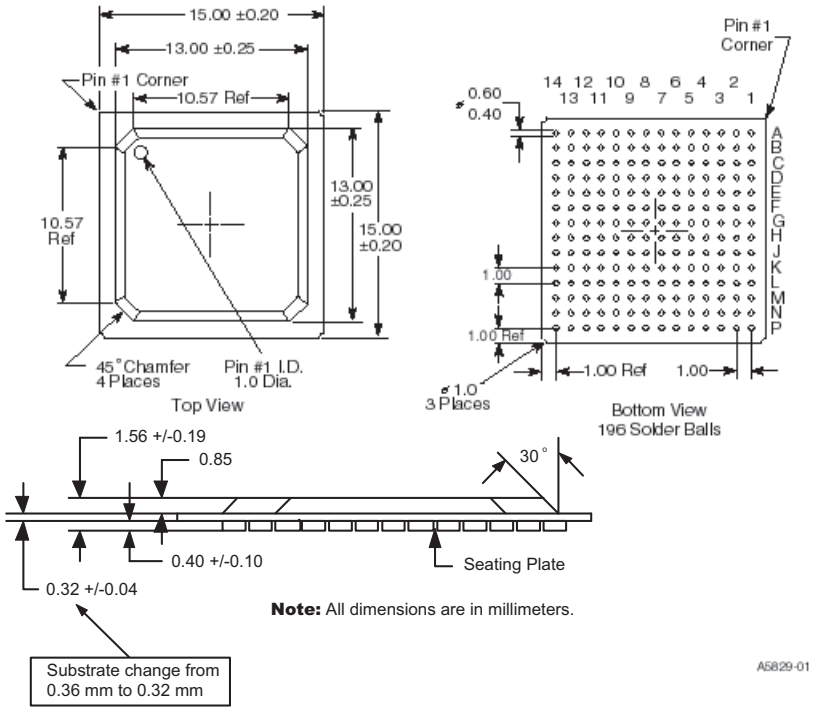
The following pins are not included in the XOR Tree chain: X1, ISOL_TCK, ISOL_EXEC, ISOL_TI and TESTEN.

8.0 Package and Pinout Information

8.1 Package Information

The 82562EZ is a 196 Ball Grid Array (BGA) package. The package dimensions are shown in Figure 5. More information on Intel device packaging is available in the Intel Packaging Handbook, which is available from the Intel Developer website..

Figure 5. Dimension Diagram for the 196-pin BGA



Note: No changes to existing soldering processes are needed for the 0.32 mm substrate change.

8.2 Pinout Information

Note: The power (VCC) and ground (VSS) pins have not been finalized and are subject to change. Do not finalize a design with this information. Revised information will be published when the product is available.

Table 15. 82562EZ Pin Assignments

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
A1	NC	E1	VCC	J1	NC	N1	VSS
A2	NC	E2	VSS	J2	NC	N2	NC
A3	VCC	E3	NC	J3	NC	N3	NC
A4	NC	E4	VSS	J4	NC	N4	NC
A5	NC	E5	VSS	J5	VCCR	N5	NC
A6	NC	E6	VSS	J6	VCC	N6	VCC
A7	VCC	E7	VSS	J7	VCC	N7	NC
A8	NC	E8	VSS	J8	VCC	N8	VCC
A9	NC	E9	VSS	J9	VCC	N9	NC
A10	NC	E10	VSS	J10	VCC	N10	NC
A11	VCCT	E11	VCCT	J11	VCC	N11	NC
A12	LILED#	E12	VCCT	J12	NC	N12	VSSP
A13	TESTEN	E13	RDP	J13	NC	N13	JRXD[1]
A14	NC	E14	RDN	J14	X2	N14	JCLK
B1	NC	F1	NC	K1	NC	P1	NC
B2	NC	F2	NC	K2	VSS	P2	VCC
B3	VSS	F3	NC	K3	VCC	P3	NC
B4	NC	F4	VSS	K4	VCC	P4	NC
B5	NC	F5	VSS	K5	VCC	P5	NC
B6	NC	F6	VSS	K6	VCC	P6	NC
B7	VSS	F7	VSS	K7	VCC	P7	NC
B8	NC	F8	VSS	K8	VCC	P8	VSS
B9	NC	F9	VSS	K9	VCC	P9	NC
B10	NC	F10	VSS	K10	VCC	P10	NC
B11	SPDLED#	F11	VSS	K11	VCC	P11	NC
B12	TOUT	F12	NC	K12	VSS	P12	VCC
B13	RBIAS100	F13	NC	K13	VCC	P13	JRXD[0]
B14	RBIAS10	F14	NC	K14	X1	P14	NC
C1	NC	G1	NC	L1	NC		
C2	NC	G2	NC	L2	NC		
C3	NC	G3	NC	L3	NC		
C4	NC	G4	NC	L4	VCC		

Table 15. 82562EZ Pin Assignments

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
C5	NC	G5	VCCR	L5	VCC		
C6	NC	G6	VCC	L6	VSS		
C7	NC	G7	VSS	L7	ADV10		
C8	NC	G8	VSS	L8	NC		
C9	NC	G9	VSS	L9	VCC		
C10	VSS	G10	VSS	L10	VCC		
C11	ACTLED#	G11	VSS	L11	VSS		
C12	VSSA	G12	NC	L12	NC		
C13	TDP	G13	VCC	L13	JTXD[1]		
C14	TDN	G14	VSS	L14	JTXD[2]		
D1	NC	H1	NC	M1	NC		
D2	NC	H2	NC	M2	NC		
D3	NC	H3	NC	M3	NC		
D4	VSS	H4	NC	M4	NC		
D5	VSS	H5	VCCR	M5	NC		
D6	VSS	H6	VCC	M6	VSS		
D7	VSS	H7	VCC	M7	NC		
D8	VSS	H8	VCC	M8	NC		
D9	NC	H9	VSS	M9	NC		
D10	ISOL_EXEC	H10	VSS	M10	NC		
D11	NC	H11	VCC	M11	NC		
D12	ISOL_TI	H12	NC	M12	JRXD[2]		
D13	VSSA	H13	NC	M13	JRSTSYNC		
D14	ISOL_TCK	H14	NC	M14	JTXD[0]		

Figure 6. 82562EZ Pin Out Diagram (Thru-the-Top View)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P
1	NC	NC	NC	NC	VCC	NC	NC	NC	NC	NC	NC	NC	VSS	NC
2	NC	NC	NC	NC	VSS	NC	NC	NC	NC	VSS	NC	NC	NC	VCC
3	VCC	VSS	NC	NC	NC	NC	NC	NC	NC	VCC	NC	NC	NC	NC
4	NC	NC	NC	VSS	VSS	VSS	NC	NC	NC	VCC	VCC	NC	NC	NC
5	NC	NC	NC	VSS	VSS	VSS	VCCR	VCCR	VCCR	VCC	VCC	NC	NC	NC
6	NC	NC	NC	VSS	VSS	VSS	VCC	VCC	VCC	VCC	VSS	VSS	VCC	NC
7	VCC	VSS	NC	VSS	VSS	VSS	VSS	VCC	VCC	VCC	ADV10	NC	NC	NC
8	NC	NC	NC	VSS	VSS	VSS	VSS	VCC	VCC	VCC	NC	NC	VCC	VSS
9	NC	NC	NC	NC	VSS	VSS	VSS	VSS	VCC	VCC	VCC	NC	NC	NC
10	NC	NC	VSS	ISOL_EXEC	VSS	VSS	VSS	VSS	VCC	VCC	VCC	NC	NC	NC
11	VCCT	SPDLED#	ACTLED#	NC	VCCT	VSS	VSS	VCC	VCC	VCC	VSS	NC	NC	NC
12	LILED#	TOUT	VSSA	ISOL_TI	VCCT	NC	NC	NC	NC	VSS	NC	JRXD[2]	VSSP	VCC
13	TESTEN	RBIAS100	TDP	VSSA	RDP	NC	NC	NC	NC	VCC	JTXD[1]	JRSTSYNC	JRXD[1]	JRXD[0]
14	NC	RBIAS10	TDN	ISOL_TCK	RDN	NC	NC	NC	X2	X1	JTXD[2]	JTXD[0]	JCLK	NC