ZiLOG

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Z90231/233/234/239

Z8 DIGITAL TELEVISION CONTROLLERS

FEATURES

Device	ROM (KB)	RAM (Bytes)	I/O Lines[1]	Voltage Range
Z90231	32(OTP)	236	27	4.5V to 5.5V
Z90233	16	236	27	4.5V to 5.5V
Z90234	24	236	27	4.5V to 5.5V
Z90239	32(ext.)	236	27	4.5V to 5.5V

Note: 1) It counts all muxed I/O port.

Z8-Based CMOS Microcontroller for Consumer Television, Cable Box, and Satellite Receiver Applications.

- 42-Pin SDIP Package except Z90239 (124 PGA)
- Z8® MCU Core at 6 MHz
- Mask ROM sizes Available in 16 and 24KB
- Ten 6-bit Pulse Width Modulators
- One 14-bit Pulse Width Modulator
- On-Chip Infrared (IR) Capture Registers
- Four Channel 4-bit Analog-to-Digital Converter
- Twenty Seven General Purpose I/O Pins
- I^2C Master Serial Communication Port

On Screen Display (OSD) Section

- Supports Displays up to 10 rows by 24 Columns with 256 Characters
- Character Cell Resolution of 14 Pixels by 18 Scan lines
- Variable Inter-row Spacing from 0–15 Horizontal Scan Lines
- Foreground and Background Colors Fully Programmable by Character

GENERAL DESCRIPTION

The Z9023X Digital Television Controller (DTC) family is Zilog's latest and most powerful Z8-based DTC product offering. These parts feature larger system RAM and ROM options, together with a host of new features including a new color palette system, flexible inter-row spacing, higher character cell resolution, background mesh effect, dedicated I.R. capture registers, on-chip Analog-to-Digital conversion, and a hardware Master mode I^2C interface. The familiar Z8 core in combination with these advanced features makes the Z9023X family an ideal choice for low to mid-range televisions in both PAL and NTSC markets.

The Z9023X family consists of three basic device types; ICE Chip(Z90239), ROM Mask Parts(Z90233/Z90234), and OTP Part(Z90231). The OTP(Z90231) supports field programmable 32KB system ROM. ICE Chip(Z90239) is used in Z90239 Emulator and ProtoPak. As described above, Z90233 supports 16KB system ROM and Z90234 supports 24KB system ROM for mask.

The Z9021X family takes full advantage of the Z8's expanded register file space to offer greater flexibility in On Screen Display creation.

Note: All signals with an overline, "‾", are active Low. For example, B/$\overline{W}$ (WORD is active Low, only); $\overline{B}$/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}, AV_{SS}

GENERAL DESCRIPTION (Continued)

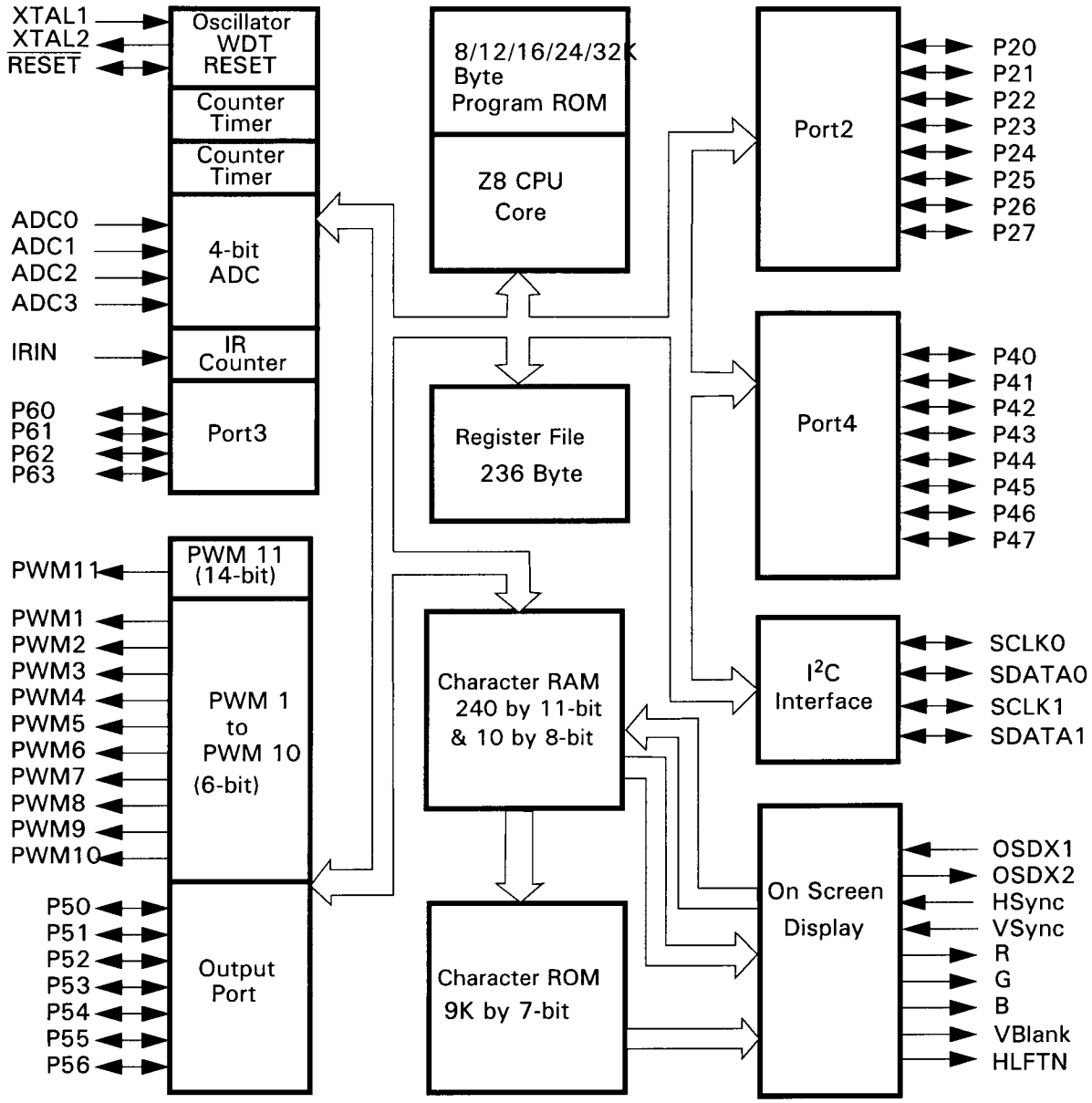

Figure 1. Functional Block Diagram

PIN IDENTIFICATION

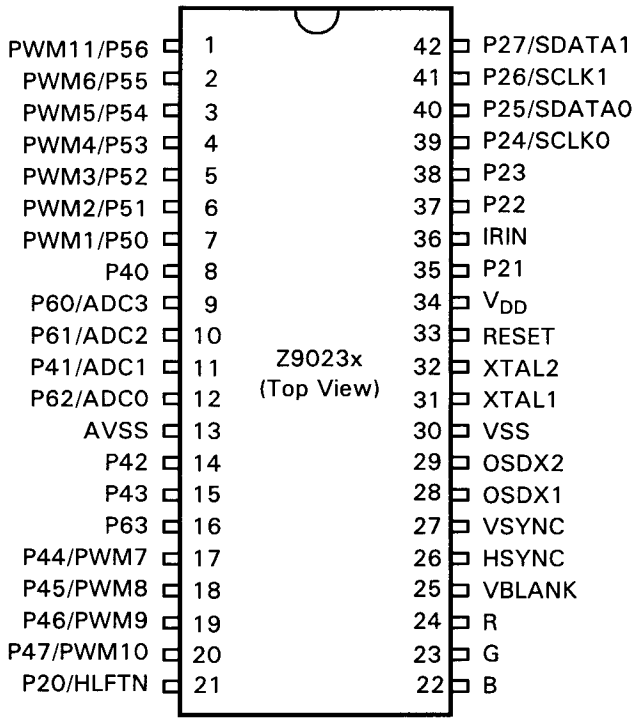

Figure 2. 42-Pin SIDP Pin Identification

PIN IDENTIFICATION (Continued)

Table 1. Z90231/233/234 42-Pin SDIP Package

Pin Number	Pin Function	I/O/PWR	Reset State	Name	Note
34	+5 Volts	PWR	PWR	V_{DD}	
30,13	0 Volts	PWR	PWR	V_{SS}, AV_{SS}	
36	Infra Red remote capture input	I	I	IRIN	
1	14-bit Pulse Width Modulator output	O	I	PWM11	1
20,19,18,17,2,3,4,5,6,7	6-bit Pulse Width Modulator output	O	I	PWM[10:1]	1
7,6,5,4,3,2,1	Bit Programmable Input/Output ports	I/O	I	P5[6:0]	
42,41,40,39,38,37,35,21	Bit programmable Input/Output ports	I/O	I	P2[7:0]	
21	Half tone output	O	I	HLFTN	
40,42	I²C Data	I/O	I	SDATA0,1	
39,41	I²C Clock	I/O	I	SCLK0,1	
16,12,10,9	Bit programmable Input/Output ports	I/O	I	P6[3:0]	
20,19,18,17,15,14,11,8	Bit programmable Input/Output ports	I/O	I	P4[7:0]	
31	Crystal oscillator input	I	I	XTAL1	
32	Crystal oscillator output	O	O	XTAL2	
28	Dot clock oscillator input	I	I	OSDX1	
29	Dot clock oscillator output	O	O	OSDX2	
26	Horizontal Sync	I	I	HSYNC	
27	Vertical Sync	I	I	VSYNC	
25	Video blank	O	O	VBLANK	
24,23,22	Video R,G,B	O	O	R,G,B	
9,10,11,12	4-bit Analog to Digital converter input	AI	I	ADC[3:0]	
33	Device reset	I	I	/RESET	

Note:
1. It is Input on POR. It must be configured to be output ports for PWM applications

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This rating is a stress rating only. Operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Symbol	Parameters	Min	Max	Units	Notes
V_{DD}	Power Supply Voltage	-0.3	+7	V	
V_I	Input Voltage	-0.3	V_{DD} +0.3	V	
V_O	Output Voltage	-0.3	V_{DD} +0.3	V	
I_{OH}	Output Current High		-10	mA	per pin
I_{OH}	Output Current High		-100	mA	per device
I_{OL}	Output Current Low		20	mA	per pin
I_{OL}	Output Current Low		200	mA	per device
T_A	Operating Temperature	0	70	°C	
T_{STG}	Storage Temperature	-55	150	°C	

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 3).

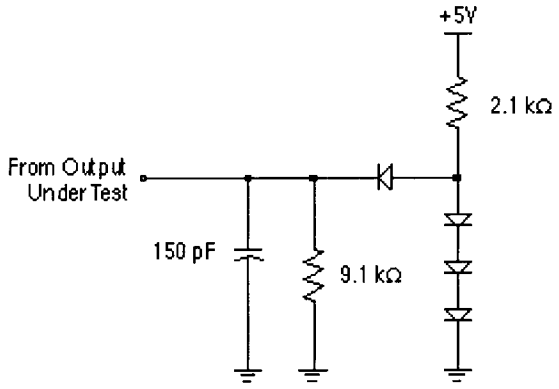

Figure 3. Test Load Diagram

DC CHARACTERISTICS

$T_A = 0^oC$ to $+ 70^oC$; $V_{DD} = +4.5V$ to $+5.5V$; $F_{OSC} = 6$ MHz

Symbol	Parameter	Min	Typical	Max	Units	Conditions
V_{DD}	Power Supply Voltage	4.5	5.00	5.5	V	
V_{IH}	Input Voltage High	$0.7V_{DD}$		V_{DD}	V	
V_{IL}	Input Voltage Low	0		$0.2V_{DD}$	V	
V_{IHC}	Input XTAL/Osc in High	$0.7V_{DD}$		V_{CC}	V	
V_{ILC}	Input XTAL/Osc In Low	0		$0.07V_{DD}$	V	
V_{OH_ST}	Output Voltage High	$V_{DD}-0.4$	4.75		V	$I_{OH} = -2$mA for standard drive
V_{OL_ST}	Output Voltage Low		0.16	0.4	V	$I_{OL} = 2.00$mA for standard drive
V_{OH_LE}	Output Voltage High			$V_{DD}-0.4$	V	$I_{OH} = -0.98$mA for low EMI drive
V_{OL_LE}	Output Voltage Low	0.4			V	$I_{OL} = 0.66$mA for low EMI drive
V_{HY}	Schmitt Hysteresis	$0.1V_{DD}$	0.8		V	
I_{IR}	Reset Input Current		–46	–80	uA	$V_{RL} = 0V$
I_{IL}	Input Leakage	–3.0	0.01	3.0	uA	$0V, V_{DD}$
I_{OL}	Tri-State Leakage	–3.0	0.02	3.0	uA	$0V, V_{DD}$
I_{CC}	Supply Current		25	40	mA	All inputs at rail;outputs floating
I_{CC1}	HALT Mode Current		3.2	6	mA	All inputs at rail;outputs floating
I_{CC2}	STOP Mode Current		0.1	10	uA	All inputs at rail;outputs floating

Note: Typical values measured at 25^oC. Minimum and Maximum values indicated from 0^oC to 70^oC.

AC CHARACTERISTICS

No	Symbol	Parameter	Min	Max	Unit
1	T_pC	Input clock period	166	1000	ns
2	T_rC, T_fC	Clock input raise and fall		25	ns
3	T_wC	Input clock width	35		ns
4	$T_wH_{SYNC}L$	Timer input low width	70		ns
5	$T_wH_{SYNC}H$	Timer input high width	$3T_pC$		
6	T_pH_{SYNC}	Timer input period	$8T_pC$		
7	T_rH_{SYNC}, T_rH_{SYNC}	Timer input raise and fall		100	ns
8	T_wIL	Int request input low	70		ns
9	T_wIH	Int request input high	$3T_pC$		
10	T_dPOR	Power-On reset delay	25	100	ms
11	$T_dLVIRES$	Low voltage detect to internal RESET condition	200		ns
12	T_wRES	Reset minimum width	$5T_pC$		
13	T_dH_sOI	H_{sync} start to V_{osc} stop	$2T_pV$	$3T_pV$	
14	T_dH_sOh	H_{sync} start to V_{osc} start		$1T_pV$	

AC TIMING DIAGRAMS

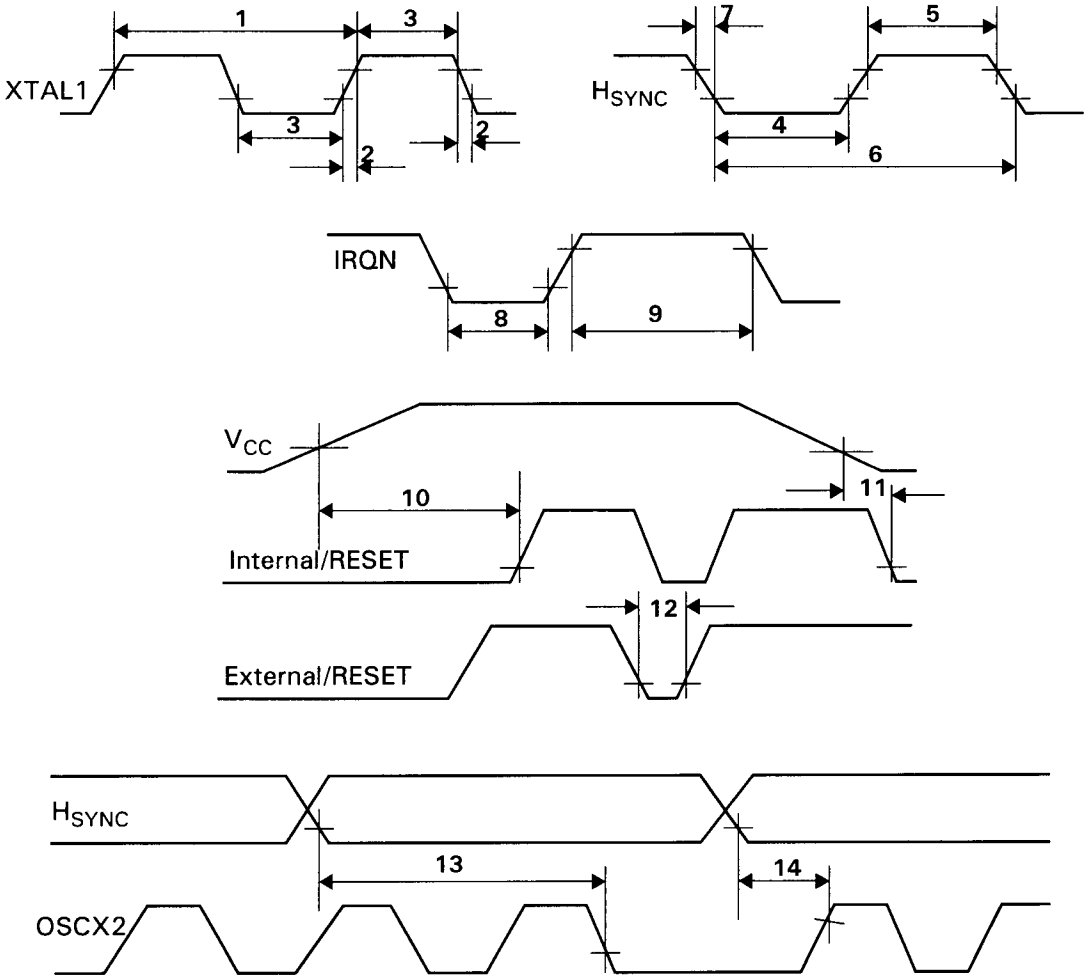

Figure 4. Timing Diagram

Pre-Characterization Product:

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

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