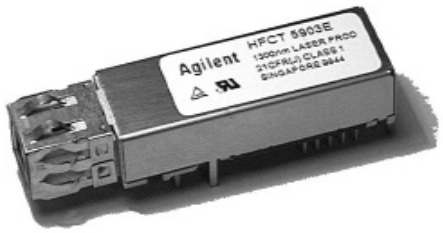
HFCT-5903E
MT-RJ Duplex Single Mode Transceiver

Data Sheet



Description

The HFCT-5903E transceiver is a high performance, cost effective module for serial optical data communications applications specified for a signal rate of 125 MBd. It is designed to provide an FDDI SMF-PMD1 link for FDDI or Fast Ethernet applications and is also compatible with ATM/SONET/SDH transceivers. The HFCT-5903 does not include a nose shield and is not recommended due to the potential degradation of EMI performance in a complete system. The HFCT-5903 is available on the rare occasion that a system mechanical design may not allow for a nose shield.

This module is designed for single mode fiber and operates at a nominal wavelength of 1300 nm. It incorporates Avago's high performance, reliable, long wavelength optical devices and proven circuit technology to give long life and consistent service.

The transmitter section uses an advanced SMQW Fabry Perot laser with full IEC 825 and CDRH Class I eye safety.

The receiver section uses a MOVPE grown planar PIN photodetector for low dark current and excellent responsivity.

A pseudo-ECL logic interface simplifies interface to external circuitry.

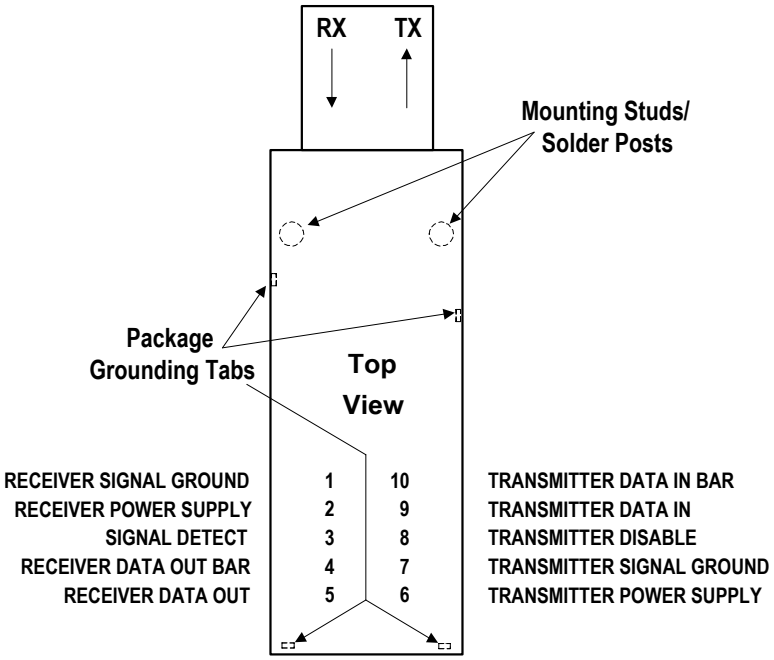
Features

- MT-RJ duplex single mode transceiver
- Power compliant to ANSI X3.184- 1993 standard for FDDI SMF-PMD category 1 optoelectronic performance
- Single +3.3 V power supply
- Multisourced 2 x 5 pin configuration
- Interchangeable with LED multisourced 2 x 5 transceivers
- Unconditionally eye safe laser IEC 825/CDRH Class 1 compliant
- Temperature range: 0°C to +70°C

Applications

- FDDI SMF-PMD1
- Fast ethernet
- ATM compatible

Connection Diagram



Pin Descriptions:

Pin 1 Receiver Signal Ground V_{EE} RX:[1]

Directly connect this pin to the receiver ground plane.

Pin 2 Receiver Power Supply V_{CC} RX:

Provide +3.3 V dc via the recommended receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CC} RX pin.

Pin 3 Signal Detect SD:

Normal optical input levels to the receiver result in a logic "1" output.

Low optical input levels to the receiver result in a fault condition indicated by a logic "0" output.

This Signal Detect output can be used to drive a PECL input on an upstream circuit, such as Signal Detect input or Loss of Signal-bar.

Pin 4 Receiver Data Out Bar RD-:

No internal terminations are provided. See recommended circuit schematic.

Pin 5 Receiver Data Out RD+:

No internal terminations are provided. See recommended circuit schematic.

Pin 6 Transmitter Power Supply V_{CC} TX:

Provide +3.3 V dc via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CC} TX pin.

Pin 7 Transmitter Signal Ground V_{EE} TX:

Directly connect this pin to the transmitter ground plane.

Pin 8 Transmitter Disable T_{DIS}:

Optional feature for laser based products only. For laser based products connect this pin to +3.3 V TTL logic high "1" to disable module. To enable module connect to TTL logic low "0".

Pin 9 Transmitter Data In TD+:

No internal terminations are provided. See recommended circuit schematic.

Pin 10 Transmitter Data In Bar TD-:

No internal terminations are provided. See recommended circuit schematic.

Mounting Studs/Solder Posts

The two mounting studs are provided for transceiver mechanical attachment to the circuit board. It is recommended that the holes in the circuit board be connected to chassis ground.

Package Grounding Tabs

Connect four package grounding tabs to signal ground.

Note: 1. The Transmitter and Receiver V_{EE} connections are commoned within the module.

Functional Description

Receiver Section

Design

The receiver section contains an InGaAs/InP photo detector and a preamplifier mounted in an optical subassembly. This optical subassembly is coupled to a postamp/decision circuit on a separate circuit board.

The postamplifier is ac coupled to the preamplifier as illustrated in Figure 1. The coupling capacitor is large enough to pass the FDDI test pattern at 125 MBd and the SONET/SDH test pattern at 155 MBd without significant distortion or performance penalty If a lower signal rate, or a code which has significantly more low frequency content is used, sensitivity, jitter and pulse distortion could be degraded.

Figure 1 also shows a filter network which limits the bandwidth of the preamp output signal. The filter is designed to bandlimit the preamp output noise and thus improve the receiver sensitivity.

These components will also reduce the sensitivity of the receiver as the signal bit rate is increased above 155 MBd.

Noise Immunity

The receiver includes internal circuit components to filter power supply noise. Under some conditions of EMI and power supply noise, external power supply filtering may be necessary. If receiver sensitivity is found to be degraded by power supply noise, the filter network illustrated in Figure 3 may be used to improve performance. The values of the filter components are general recommendations and may be changed to suit a particular system environment. Shielded inductors are recommended.

Terminating the Outputs

The PECL Data outputs of the receiver may be terminated with the standard Thevenin-equivalent 50 ohm to V_{CC} - 2 V termination. Other standard PECL terminating techniques may be used.

The two outputs of the receiver should be terminated with identical load circuits to avoid unnecessarily large ac current in V_{CC}. If the outputs are loaded identically the ac current is largely nulled. The SD output of the receiver is PECL logic and must be loaded if it is to be used. The signal detect circuit is much slower that the data path, so the ac noise generated by an asymmetrical load is negligible. Power consumption may be reduced by using a higher than normal load impedance for the SD output. Transmission line effects are not generally a problem as the switching rate is slow.

The Signal Detect Circuit

The signal detect circuit works by sensing the peak level of the received signal and comparing this level to a reference.

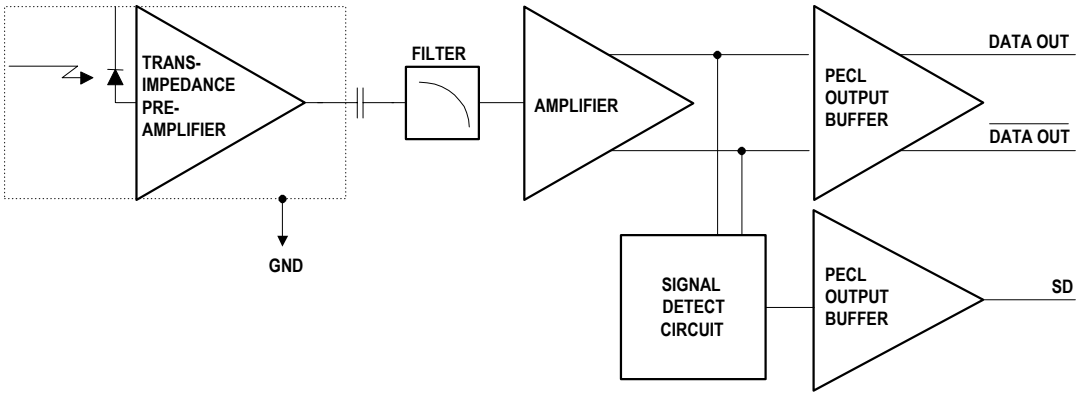


Figure 1. Receiver Block Diagram

Functional Description

Transmitter Section

Design

The transmitter section uses a buried heterostructure Fabry Perot laser as its optical source. The package of this laser is designed to allow repeatable coupling into single mode fiber. In addition, this package has been designed to be compliant with IEC 825 Class 1 and CDRH Class I eye safety requirements. The optical output is controlled by a custom IC which detects the laser output via the monitor photodiode. This IC provides both dc and ac current drive to the laser to ensure correct modulation, eye diagram and extinction ratio over temperature, supply voltage and life.

Solder and Wash Process Compatibility

The transceivers are delivered with protective process plugs inserted into the MT-RJ connector receptacle. This process plug protects the optical subassemblies during wave solder and aqueous wash processing and acts as a dust cover during shipping.

These transceivers are compatible with either industry standard wave or hand solder processes. Each process plug can only be used once during processing, although with subsequent use, it can be used as a dust cover.

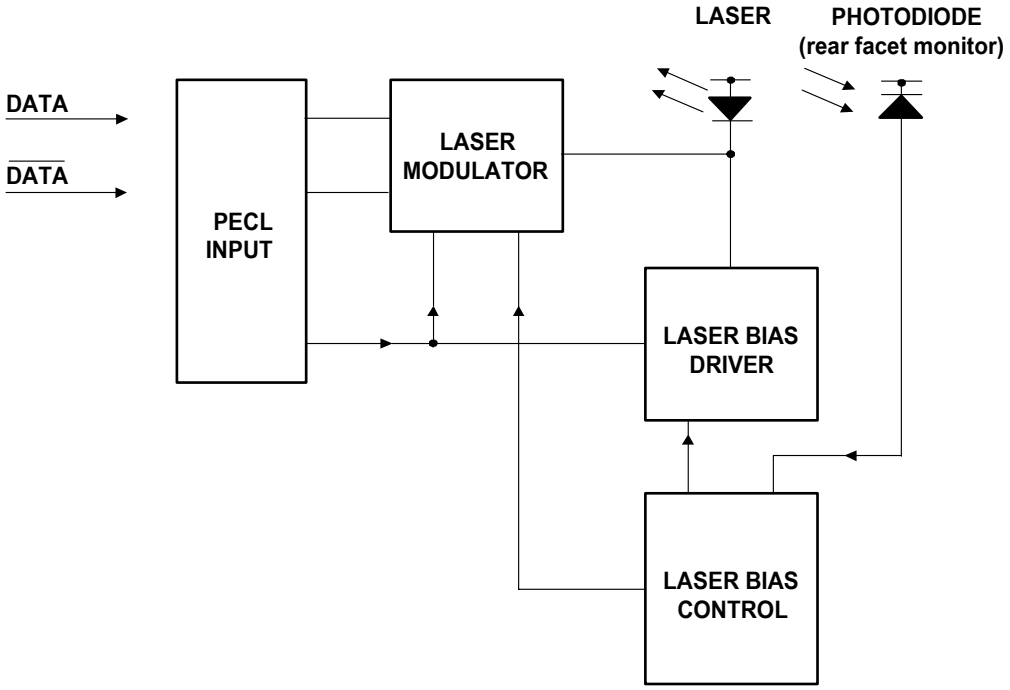


Figure 2. Simplified Transmitter Schematic

Interface and Termination Recommendations

Figure 3 shows a +3.3 V coupling scheme. Also present are power supply filtering arrangements which comply with the recommendations of the small form factor multisource agreement. Such a compliance ensures noise rejection compatibility between transceivers from various vendors.

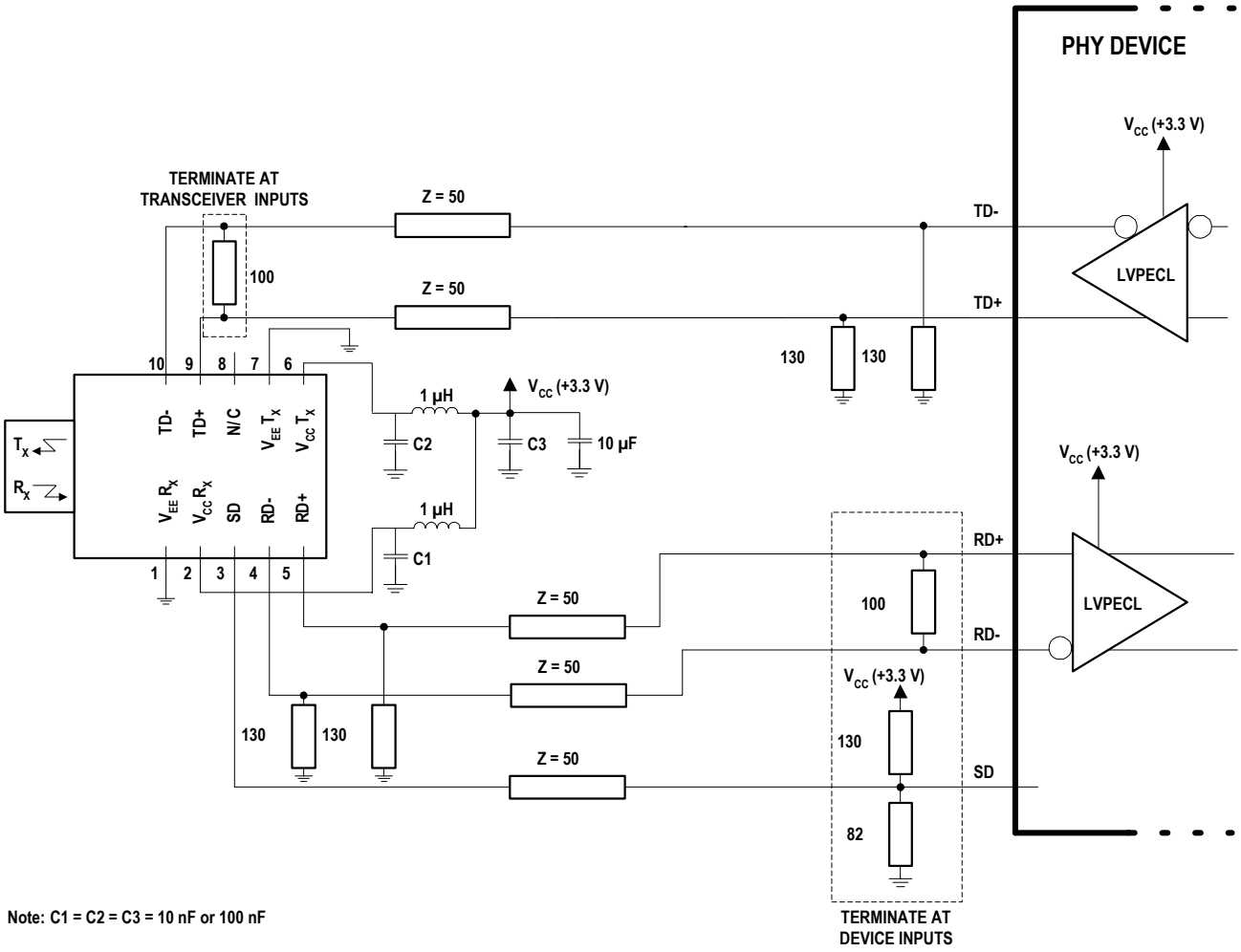


Figure 3. +3.3 V Transceiver Interface with +3.3 V LVPECL Device

Regulatory Compliance

Feature	Test Method	Targeted Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883C Method 3015.4	Meets Class 1 (2000 Volts).
Electrostatic Discharge (ESD) to the Duplex MT-RJ Receptacle	Variation of IEC 801-2	Products of this type, typically, withstand at least 25 kV without damage when the Duplex MT-RJ Connector Receptacle is contacted by a Human Body Model probe.
Electromagnetic Interference (EMI)	FCC Class B CENELEC EN55022 Class B (CISPR 22A) VCCI Class 1	Transceivers typically provide 12 dB margin to the noted standard limits when tested at a certified test range with the transceiver mounted to a circuit card without a chassis enclosure. Three transceivers typically provide 20 dB of margin in a 'perfect' closed box with the recommended port openings.
Immunity	Variation of IEC 801-3	Typically show no measurable effect from a 10 V/m field swept from 10 to 450 MHz applied to the transceiver when mounted to a circuit card without a chassis enclosure.
Eye Safety	FDA CDRH 21-CFR 1040 Class 1	Compliant per Avago testing under normal operating conditions. Accession Number: 9521220-20.
	IEC 825 Issue 1 1993:11 Class 1 CENELEC EN60825 Class 1	Compliant per Avago testing under single fault conditions. TUV Certification: 933/510817/05.

Performance Specifications

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device. Limits apply to each parameter in isolation, all other parameters having values within the recommended operating conditions. It should not be assumed that limiting values of more than one parameter can be applied to the product at the same time. Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Storage Temperature	T_S	-40		+85	°C	
Lead Soldering Temperature/Time	T_{SOLD} /t_{SOLD}			+260/10	°C/s	
Output Current	I_O	0		30	mA	
Data Input Voltage	V_I	GND		V_{CC}	V	
Power Supply Voltage	V_{CC}	0		3.6	V	

Operating Environment

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Ambient Operating Temperature	T_A	0		+70	°C	1
Power Supply Voltage	V_{CC}	3.1		3.5	V	
Data Input Voltage - Low	V_{IL} - V_{CC}	-1.810		-1.475	V	
Data Input Voltage - High	V_{IH} - V_{CC}	-1.165		-0.880	V	
Data and Signal Detect Output Load	R_L		50		Ω	2

Transmitter Section

(Ambient Operating Temperature V_{CC} = 3.1 V to 3.5 V)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Supply Current	I_{CC}		50	120	mA	3
Power Dissipation	P_{DISS}		0.175	0.42	W	
Optical Output Power	P_O	-20		-14	dBm avg.	4
Center Wavelength	λ_C	1261		1360	nm	
Spectral Width	$\Delta\lambda$			7.7	nm	
Extinction Ratio	E_R	8.2			dB	
Output Optical Eye	Compliant with Eye Mask Bellcore TR-NWT-000253 and ITU recommendation G.957					
Optical Rise Time	t_R			2	ns	5
Optical Fall Time	t_F			2	ns	5
Data Input Current - Low	I_{IL}	-200			µA	
Data Input Current - High	I_{IH}			200	µA	
Data Input Voltage - Low	V_{IL} - V_{CC}	-1.810		-1.475	V	6
Data Input Voltage - High	V_{IH} - V_{CC}	-1.165		-0.880	V	6

Notes:

1. 2 ms^{-1} air flow required.
2. Outputs terminated with 50 Ω to V_{CC} – 2V are the Thevenin equivalent.
3. The power supply current varies with temperature. Maximum current is specified at V_{CC} = Maximum @ maximum temperature (not including terminations) and end of life.
4. Output power is power coupled into a single mode fiber.
5. 10% - 90% Values
6. These inputs are compatible with 10 K, 10 KH, and 100 K ECL and LVPECL inputs.

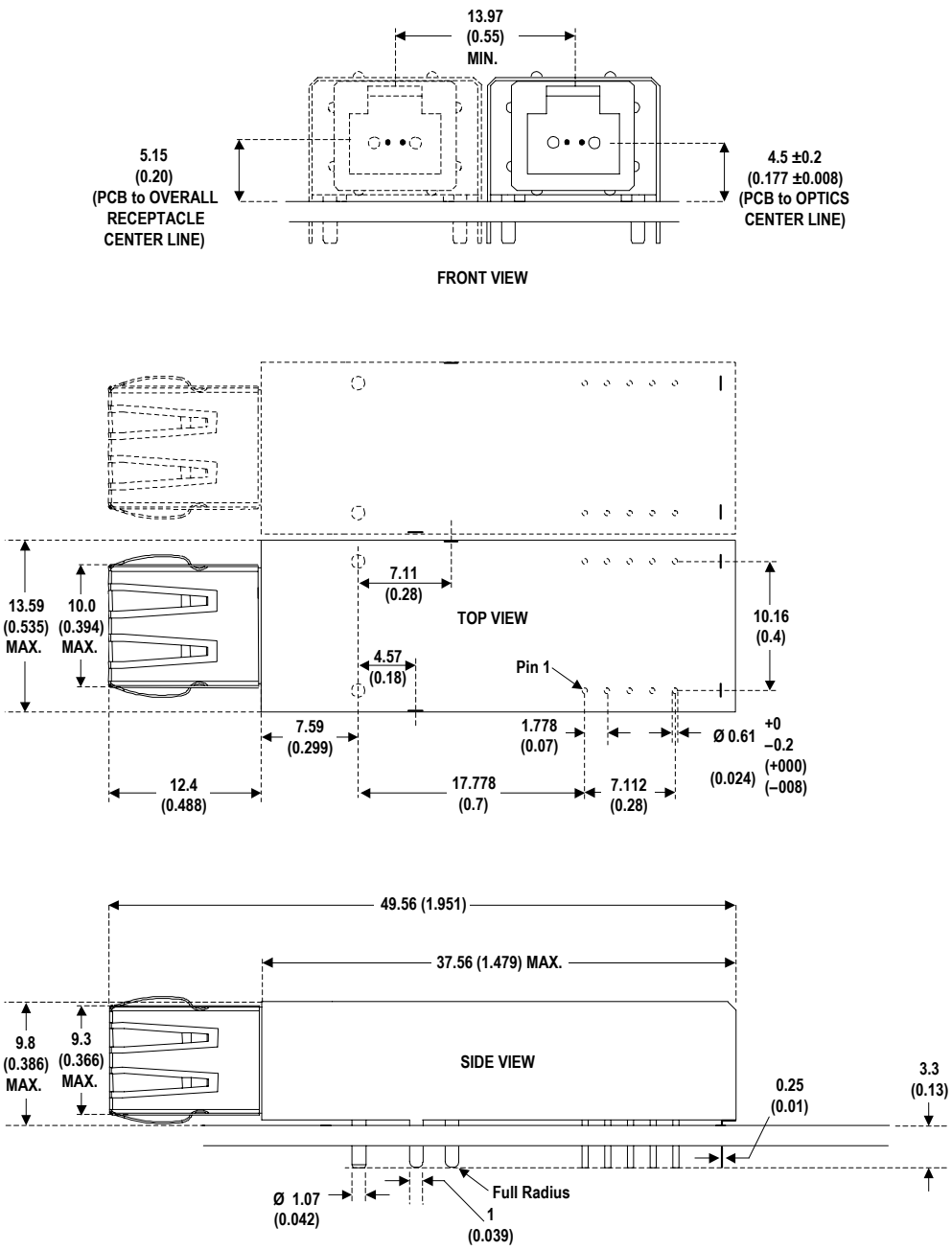
Receiver Section

(Ambient Operating Temperature V_{CC} = 3.1 V to 3.5 V)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Supply Current	I_{CC}		75	100	mA	7
Power Dissipation	P_{DISS}		0.263	0.35	W	8
Receiver Sensitivity at Eye Center	$P_{IN\ Min.}$ (C)			-31.8	dBm avg.	9
Receiver Sensitivity at Window Edge	$P_{IN\ Min.}$ (W)			-31	dBm avg.	9
Maximum Input Optical Power	$P_{IN\ Max.}$	-8.0			dBm avg.	9
Operating Wavelength		1261		1360	nm	
Data Output Voltage - Low	V_{OL} - V_{CC}	-1.840		-1.620	V	10
Data Output Voltage - High	V_{OH} - V_{CC}	-1.045		-0.880	V	10
Signal Detect Output Voltage - Low	V_{OL} - V_{CC}	-1.840		-1.620	V	10
Signal Detect Output Voltage - High	V_{OH} - V_{CC}	-1.045		-0.880	V	10
Signal Detect - Asserted	P_A	P_D + 1.5 dB		-34	dBm avg.	
Signal Detect - Deasserted	P_D	-45			dBm avg.	
Signal Detect - Hysteresis	P_A - P_D	0.5		4.0	dB	
Signal Detect Assert time (off to on)	AS_Max	0		100	µs	
Signal Detect Deassert time (on to off)	ANS_Max	0		350	µs	
Power Supply Noise Rejection	PSNR			50	mV p-p	11

Notes:

7. This does not include the output load current.
8. This does not include the output load power.
9. Minimum sensitivity and saturation levels for a 2^{23}-1 PRBS with 72 ones and 72 zeros inserted. (CCITT recommendation G.958)
10. These outputs are compatible with 10 K, 10 KH and 100 K ECL and PECL outputs.
11. Between 20 Hz and 2000 KHz with the recommended power supply filter. No degradation above the maximum 'receiver sensitivity at eye center'specification of –31.8 dBm.



DIMENSIONS IN MILLIMETERS (INCHES)

NOTES:
1. THIS PAGE DESCRIBES THE MAXIMUM PACKAGE OUTLINE, MOUNTING STUDS, PINS AND THEIR RELATIONSHIPS TO EACH OTHER.
2. TOLERANCED TO ACCOMMODATE ROUND OR RECTANGULAR LEADS.
3. THE 10 I/O PINS, 2 SOLDER POSTS AND 4 PACKAGE GROUNDING TABS ARE TO BE TREATED AS A SINGLE PATTERN. (SEE FIGURE 6 PCB LAYOUT).
4. THE MT-RJ HAS A 750 µm FIBER SPACING.
5. THE MT-RJ ALIGNMENT PINS ARE IN THE MODULE.
6. SEE MT-RJ TRANSCEIVER PIN OUT DIAGRAM FOR DETAILS.

Figure 4. HFCT-5903E Package Outline Drawing

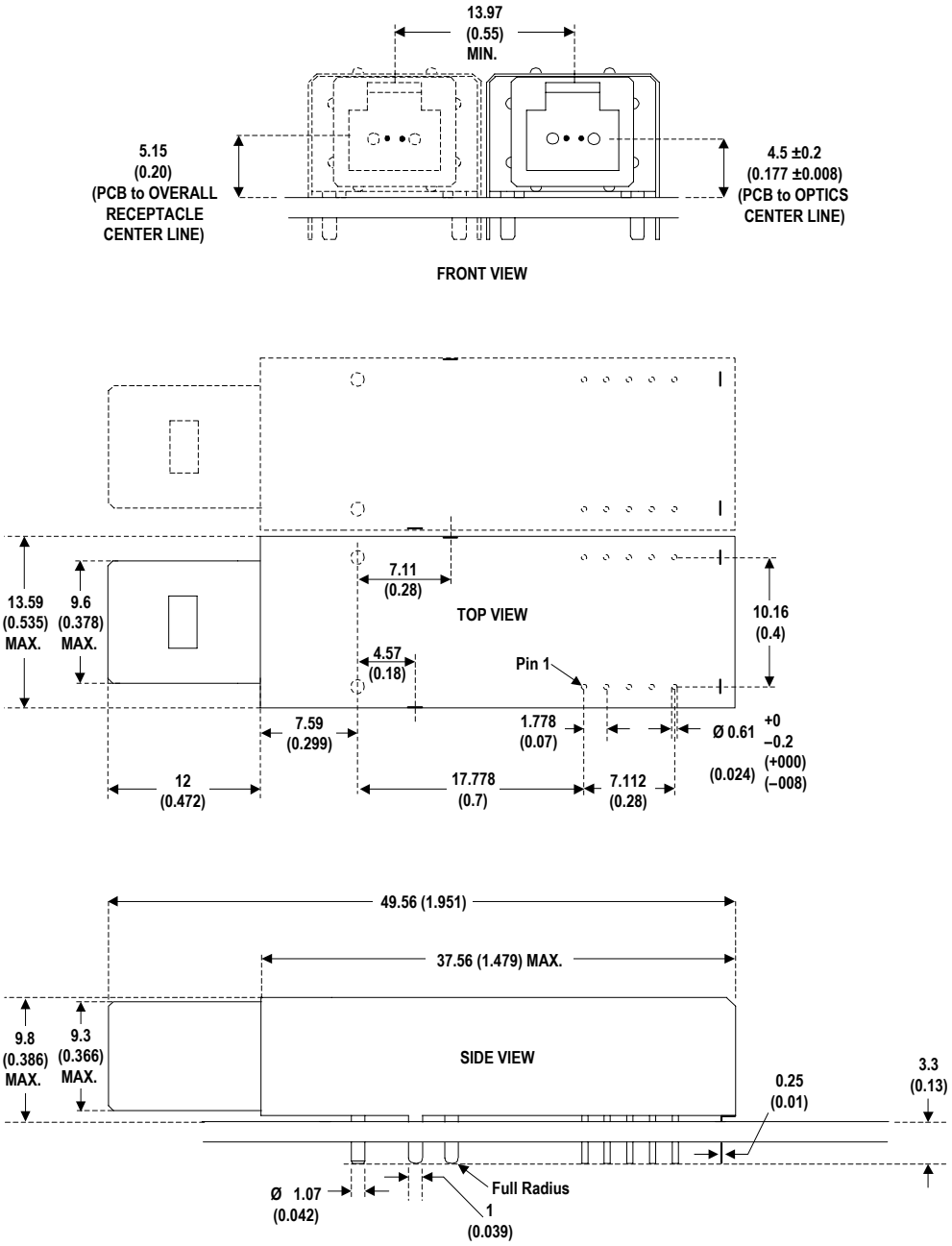


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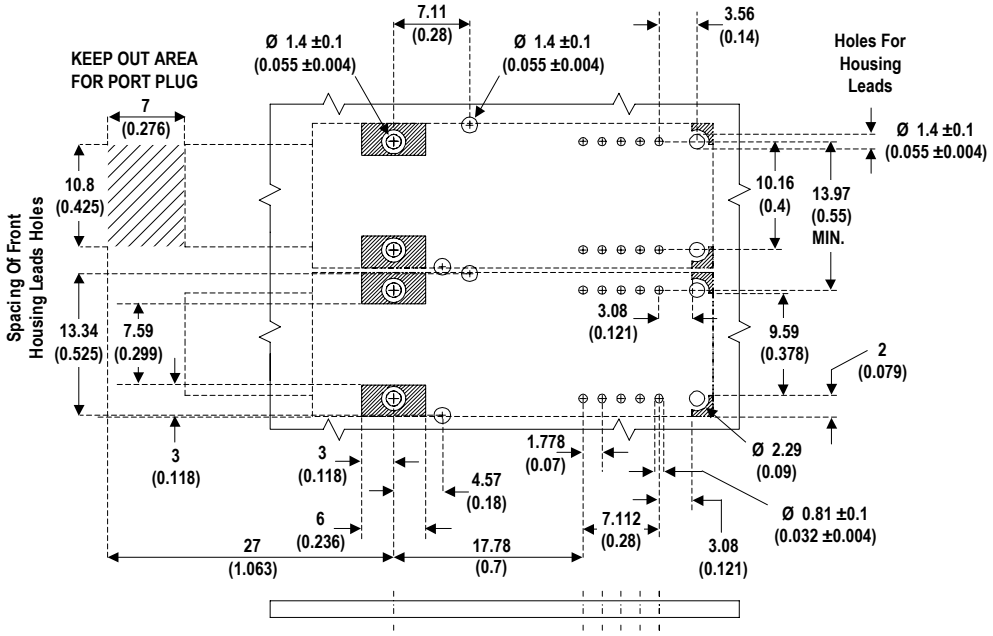
Figure 5. HFCT-5903 Package Outline Drawing

Board Layout - Decoupling Circuit and Ground Planes

It is important to take care in the layout of your circuit board to achieve optimum performance from these transceivers. Figure 3 provides a good example of a schematic for a power supply decoupling circuit that works well with these parts. It is further recommended that a continuous ground plane be provided in the circuit board directly under the transceiver to provide a low inductance ground for signal return current. This recommendation is in keeping with good high frequency board layout practices.

Board Layout - Hole Pattern

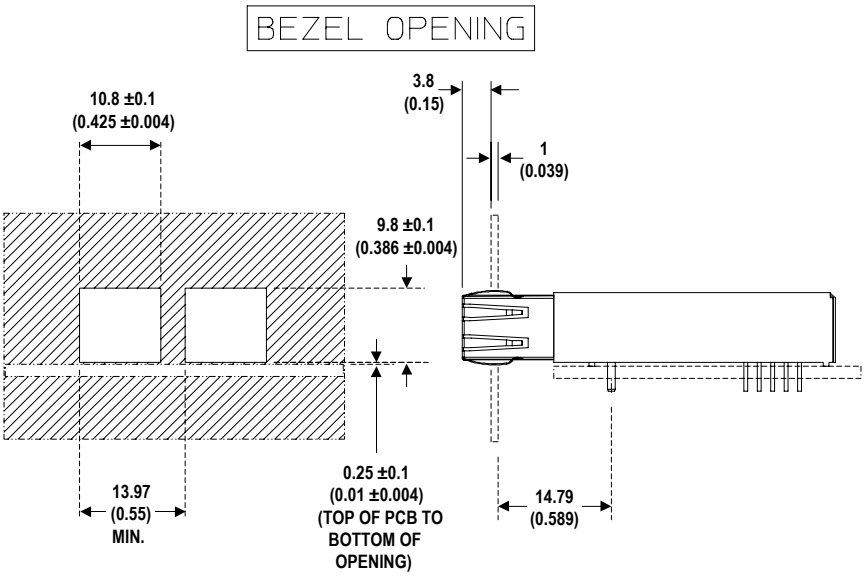
The Avago transceiver complies with the circuit board "Common Transceiver Footprint" hole pattern defined in the original multisource announcement which defined the 2 x 5 package style. This drawing is reproduced in Figure 6 with the addition of ANSI Y14.5M compliant dimensioning to be used as a guide in the mechanical layout of your circuit board. Figure 7 shows the front panel dimensions associated with such a layout.



DIMENSIONS IN MILLIMETERS (INCHES)

NOTES:
1. THIS FIGURE DESCRIBES THE RECOMMENDED CIRCUIT BOARD LAYOUT FOR THE MT-RJ TRANSCEIVER PLACED AT .550 SPACING.
2. THE HATCHED AREAS ARE KEEP-OUT AREAS RESERVED FOR HOUSING STANDOFFS. NO METAL TRACES OR GROUND CONNECTION IN KEEP-OUT AREAS.
3. 2 x 5 TRANSCEIVER MODULE REQUIRES 16 PCB HOLES (10 I/O PINS, 2 SOLDER POSTS AND 4 PACKAGE GROUNDING TABS).
   PACKAGE GROUNDING TABS SHOULD BE CONNECTED TO SIGNAL GROUND.
4. THE SOLDER POSTS SHOULD BE SOLDERED TO CHASSIS GROUND FOR MECHANICAL INTEGRITY AND TO ENSURE FOOTPRINT COMPATIBILITY WITH OTHER SFF TRANSCEIVERS.

Figure 6. Recommended Board Layout Hole Pattern



DIMENSIONS IN MILLIMETERS (INCHES)

NOTE: NOSE SHIELD SHOULD BE CONNECTED TO CHASSIS GROUND.

Figure 7. Recommended Panel Mounting

Design Support Materials

Further technical details and supporting information regarding small form factor transceivers are contained in an application note aimed at providing useful information to the fiber-optic system designer. This document describes PC board layout techniques, power supply filtering, EMI considerations and interfacing options. Avago has created a number of reference designs with major PHY IC vendors in order to establish full functionality and interoperability. Such design information and results can be made available to the designer as a technical aid. Please contact your Avago representative for further information if required.

Ordering Information

HFCT-5903E

Model Name:
HFCT-5903E - Preferred option with nose shield fitted
HFCT-5903 - Non-preferred option without nose shield

Class 1 Laser Product: This product conforms to the applicable requirements of 21 CFR 1040 at the date of manufacture
Date of Manufacture: _____
Avago Technolgies Ltd., Depot Road, Singapore

Handling Precautions

1. The HFCT-5903E can be damaged by current surges or overvoltage. Power supply transient precautions should be taken.
2. Normal handling precautions for electrostatic sensitive devices should be taken.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

5988-0698EN - May 24, 2007