

CDP1872C, CDP1875C

March 1997

High-Speed 8-Bit Input and Output Ports

Features

- Parallel 8-Bit Input/Output Register with Buffered Outputs
- High-Speed Data-In to Data-Out 85ns (Max) at V_{DD} = 5V
- Flexible Applications In Microprocessor Systems as Buffers and Latches
- High Order Address-Latch Capability in CDP1800-Series Microprocessor Systems
- Output Sink Current = 5mA (Min) at V_{DD} = 5V
- Three-State Output CDP1872C and CDP1874C

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
CDP1872CE	-40°C to +85°C	PDIP	E22.4
CDP1874CE	-40°C to +85°C	PDIP	E22.4
CDP1875CE	-40°C to +85°C	PDIP	E22.4

Description

The CDP1872C, CDP1874C and CDP1875C devices are high-speed 8-bit parallel input and output ports designed for use in the CDP1800 microprocessor system and for general use in other microprocessor systems. The CDP1872C and CDP1874C are 8-bit input ports; the CDP1875C is an 8-bit output port.

These devices have flexible capabilities as buffers and data latches and are reset by $\overline{\text{CLR}}$ input when the data strobe is not active.

The CDP1872C and CDP1874C are functionally identical except for device selects. The CDP1872C has one active low and one active high select; the CDP1874C has two active high device selects. These devices also feature Three-state outputs when deselected. Data is strobed into the register on the leading edge of the CLOCK and latched on the trailing edge of the CLOCK.

The CDP1875C is an output port with data latched into the registers when the device selects are active. There are two active high and one active low selects. The output buffers are enabled at all times.

Pinouts CDP1874C INPUT PORT CDP1875C OUTPUT PORT CDP1872C INPUT PORT (PDIP) (PDIP) (PDIP) TOP VIEW TOP VIEW TOP VIEW 22 1 22 V_{DD} CS1 CS1 V_{DD} CS1 V_{DD} 21 21 2 DI7 DI7 DI7 DIO DI0 DIO 20 3 20 D07 D07 20 DO0 DO0 D07 DO₀ 4 19 DI6 DI1 19 DI6 DI1 19 DI6 DI1 5 18 18 18 D01 D06 D01 D06 D01 D06 17 17 6 17 6 DI2 DI5 DI2 DI5 DI2 DI5 D02 7 16 D05 D02 16 D05 D02 16 D05 15 8 DI4 15 8 DI4 DI4 DI3 DI3 DI3 14 14 D03 D04 D04 D04 D03 D03 13 13 CLOCK CLR CLOCK CLR CS3 10 CLR CS2 CS2 V_{SS} V_{SS} CS₂ ٧ss

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD}).....-0.5V to +7V (Voltage referenced to V_{SS} Terminal) Input Voltage Range, All Inputs-0.5V to V_{DD} +0.5V DC Input Current, Any One Input.....±10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)
PDIP Package	75
Device Dissipation Per Output Transistor	
T _A = Full Package Temperature Range	
(All Package Types)	100mW
Operating Temperature Range (T _A)	
Package Type E40	
Storage Temperature Range (T _{STG})65°	C to +150°C
Lead Temperature (During Soldering)	
At distance $1/16 \pm 1/32$ In. $(1.59 \pm 0.79$ mm)	
from case for 10s max	+265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions At $T_A = -40$ to $+85^{\circ}$ C. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	LIMITS ALL TYPES	UNITS
DC Operating-Voltage Range	4 to 6.5	V
Input Voltage Range	V _{SS} to V _{DD}	V

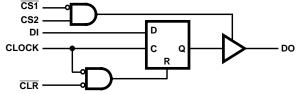
Static Electrical Specifications At T_A = -40 to +85°C, V_{DD} ±5%, Unless Otherwise Specified.

		TEST CONDITIONS		LIMITS ALL TYPES				
PARAMETER		V _O (V)	V _{IN} (V)	V _{DD} (V)	MIN	(NOTE 1) TYP	MAX	UNITS
Quiescent Device Current	I _{DD}	-	0, 5	5	-	25	50	μΑ
Output Low Drive (Sink) Current	I _{OL}	0.4	0, 5	5	5	10	-	mA
Output High Drive (Source) Current	I _{OH}	4.6	0, 5	5	-4	-7	-	mA
Output Voltage Low-Level (Note 2)	V _{OL}	-	0, 5	5	-	0	0.1	V
Output Voltage High-Level (Note 2)	V _{OH}	-	0, 5	5	4.9	5	-	V
Input Low Voltage	V _{IL}	0.5, 4.5	-	5	-	-	1.5	V
Input High Voltage	V _{IH}	0.5, 4.5	-	5	3.5	-	-	V
Input Leakage Current	I _{IN}	-	0, 5	5	-	-	±1	μΑ
Three-State Output Leakage Current (Note 3)	I _{OUT}	0, 5	0, 5	5	-	-	±5	μΑ
Input Capacitance	C _{IN}	-	-	-	-	15	-	pF
Output Capacitance (Note 3)	C _{OUT}	-	-	-	-	15	-	pF

NOTES:

- 1. Typical values are for $T_A = +25^{\circ}C$ and nominal $V_{DD} \pm 5\%$.
- 2. $I_{OL} = I_{OH} = 1 \mu A$
- 3. For CDP1872C and CDP1874C only.

Logic Diagrams



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FIGURE 1. EQUIVALENT LOGIC DIAGRAM (1 OF 8 LATCHES SHOWN) FOR CDP1872C

FIGURE 2. EQUIVALENT LOGIC DIAGRAM (1 OF 8 LATCHES SHOWN) for CDP1874C

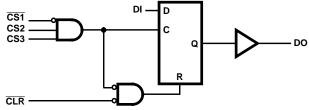


FIGURE 3. EQUIVALENT LOGIC DIAGRAM (1 OF 8 LATCHES SHOWN) FOR CDP1875C

$\textbf{Dynamic Electrical Specifications} \ \, \text{At T}_{A} = 25^{o}\text{C}, \, \text{V}_{DD} \, \, 5\text{V}, \, \text{t}_{R}, \, \text{t}_{F} = 10 \text{ns}, \, \text{V}_{IH} = 0.7 \text{V}_{DD}, \, \text{V}_{IL} = 0.3 \text{V}_{DD}, \, \text{C}_{L} = 150 \text{pF}$

			CDP1872C, CDP1874C			
PARAMETER		MIN	(NOTE 1) TYP	(NOTE 2) MAX	UNITS	
INPUT PORT (FIGURE 4)		-		-		
Output Enable	t _{EN}	-	45	90	ns	
Output Disable	t _{DIS}	-	45	90	ns	
Clock to Data Out	t _{CLO}	-	45	90	ns	
Clear to Output	t _{CRO}	-	80	160	ns	
Data In to Data Out	t _{DIO}	-	50	85	ns	
Minimum Data Setup Time	t _{DSU}	-	10	30	ns	
Data Hold Time	t _{DH}	-	10	30	ns	
Minimum Clock Pulse Width	t _{CL}	-	30	60	ns	
Minimum Clear Pulse Width	t _{CR}	-	30	60	ns	

NOTES:

- 1. Typical values are for T_A = +25°C and V_{DD} ±5%. 2. Maximum values are for T_A = +85°C and V_{DD} ±5%

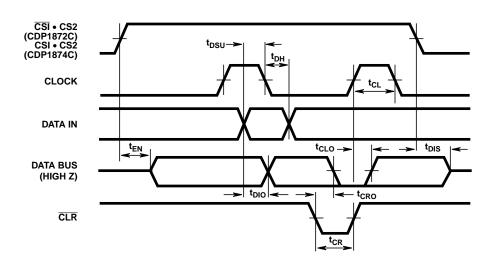


FIGURE 4. TIMING WAVEFORMS FOR CDP1872C AND CDP1874C (INPUT-PORT TYPES)

 $\textbf{Dynamic Electrical Specifications} \ \, \text{At T}_{A} = 25^{o}\text{C}, \, \text{V}_{DD} \, \, \text{5V}, \, \text{t}_{R}, \, \text{t}_{F} = 10 \text{ns}, \, \text{V}_{IH} = 0.7 \text{V}_{DD}, \, \text{V}_{IL} = 0.3 \text{V}_{DD}, \, \text{C}_{L} = 150 \text{pF}$

			LIMITS			
			CDP1875C			
PARAMETER		MIN	(NOTE 1) TYP	(NOTE 2) MAX	UNITS	
OUTPUT PORT (FIGURE 5)						
Clock to Data Out	t _{CLO}	-	50	100	ns	
Clear to Output	t _{CRO}	-	80	160	ns	
Data In to Data Out	t _{DIO}	-	50	85	ns	
Minimum Data Setup Time	t _{DS}	-	10	30	ns	
Data Hold Time	t _{DH}	-	10	30	ns	
Minimum Clear Pulse Width	t _{CR}	-	30	60	ns	

NOTES:

- 1. Typical values are for T_A = +25°C and V_{DD} ±5%.
- 2. Maximum values are for T_A = +85°C and V_{DD} ±5%

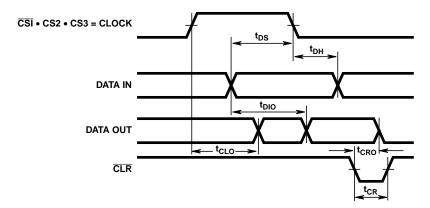


FIGURE 5. TIMING WAVEFORMS FOR CDP1875C (OUTPUT PORT)

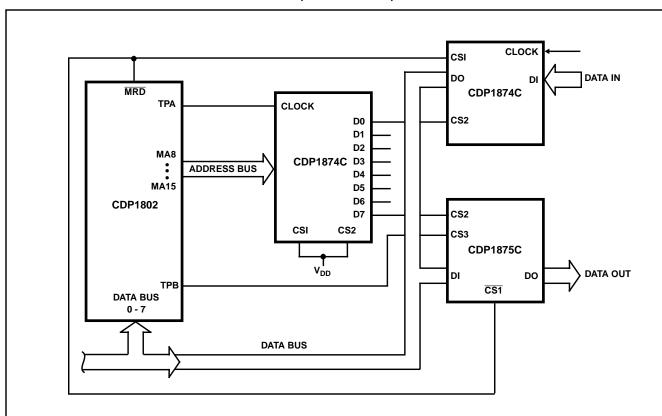


FIGURE 6. CDP1874C USED AS AN INPUT PORT AND ADDRESS LATCH WITH CDP1875C USED AS AN OUTPUT PORT

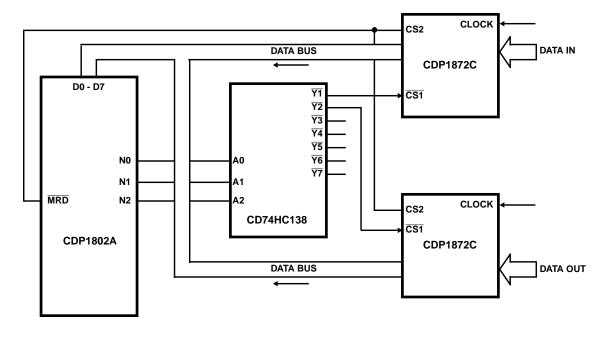


FIGURE 7. CDP1872C USED AS AN INPUT PORT AND SELECTED BY CD74HC138

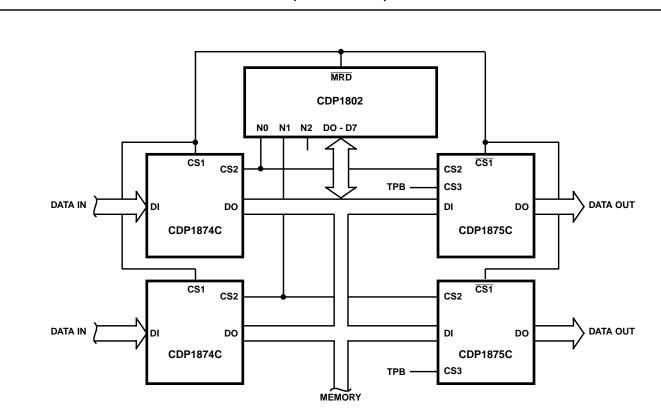


FIGURE 8. CDP1874C AND CDP1875C USED AS INPUT/OUTPUT BUFFERS

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