# RENESAS

HD74LS374

Octal D-type Edge-triggered Flip-Flops (with three-state outputs)

REJ03D0483–0200 Rev.2.00 Feb.18.2005

The HD74LS374, 8-bit register features totem-pole three-state outputs designed specifically for driving highlycapacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide this register with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The eight flip-flops are edge-triggered D-type flipflops. On the positive transition the clock, the Q outputs will be set to the logic states that ware setup at the D inputs.

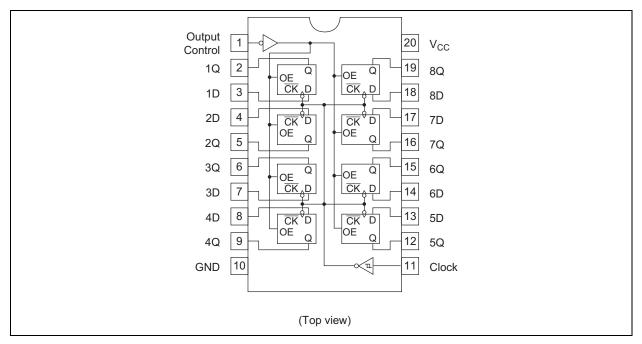
# Features

• Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)	
HD74LS374P	DILP-20 pin	PRDP0020AC-B (DP-20NEV)	Ρ	—	
HD74LS374FPEL	SOP-20 pin (JEITA)	PRSP0020DD-B (FP-20DAV)	FP	EL (2,000 pcs/reel)	
HD74LS374RPEL	SOP-20 pin (JEDEC)	PRSP0020DC-A (FP-20DBV)	RP	EL (1,000 pcs/reel)	

Note: Please consult the sales office for the above package availability.

# Pin Arrangement





### **Function Table**

	Inputs					
Output control	Output control Clock D					
L	$\uparrow$	Н	Н			
L	$\uparrow$	L	L			
L	L	X	Q <sub>0</sub>			
н	Х	Х	Z			

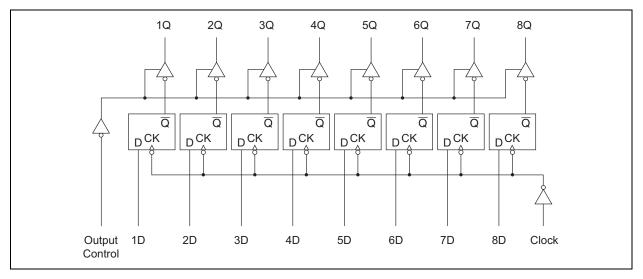
Notes: H; high level, L; low level, X; irrelevant

 $\uparrow;$  transition from low to high level

 $\mathsf{Q}_{0}\!;$  level of  $\mathsf{Q}$  before the indicated steady state input conditions were established

Z; off (high-impedance) state of a three state output

# **Block Diagram**



# **Absolute Maximum Ratings**

Item	Symbol	Ratings	Unit	
Supply voltage	V <sub>CC</sub>	7	V	
Input voltage	V <sub>IN</sub>	7	V	
Power dissipation	P <sub>T</sub>	400	mW	
Storage temperature	Tstg	-65 to +150	٥C	

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

### **Recommended Operating Conditions**

Item		Symbol	Min	Тур	Max	Unit
Supply voltage		V <sub>CC</sub>	4.75	5.00	5.25	V
Output voltage		V <sub>OH</sub>	—	—	5.5	V
Output current		I <sub>ОН</sub>	—	—	-2.6	mA
		I <sub>OL</sub>	—	—	24	mA
Operating temperature		Topr	-20	25	75	°C
Clock pulse width	"H" Level	+	15	—	—	ns
	"L" Level	t <sub>w</sub>	15	—	—	ns
Data setup time		t <sub>su</sub>	t <sub>su</sub> 20↑		—	ns
Data hold time		t <sub>h</sub>	0↑	—	—	ns

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### **Electrical Characteristics**

 $(Ta = -20 \text{ to } +75 \text{ }^{\circ}\text{C})$ 

Item	Symbol	min.	typ.*	max.	Unit	Condition	
Input voltage	V <sub>IH</sub>	2.0	_	—	V		
input voltage	V <sub>IL</sub>	-	_	0.8	V		
Output veltage	V <sub>OH</sub>	2.4		—	V	$\label{eq:V_CC} \begin{split} V_{CC} &= 4.75 \ \text{V}, \ V_{\text{IH}} = 2 \ \text{V}, \ V_{\text{IL}} = 0.8 \ \text{V}, \\ I_{OH} &= -2.6 \ \text{mA} \end{split}$	
Output voltage	V			0.4	V	$I_{OL} = 12 \text{ mA}$ $V_{CC} = 4.75 \text{ V},$	
	V <sub>OL</sub>	_	_	0.5	v	$I_{OL} = 24 \text{ mA}$ $V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}$	
	I <sub>OZH</sub>	_	—	20	۸	$V_0 = 2.7 V$ $V_{CC} = 5.25 V$ ,	
Output current	I <sub>OZL</sub>	_	—	-20	μA	$V_{O} = 0.4 V$ $V_{IH} = 2 V, V_{IL} = 0.8 V$	
	IIH	_	—	20	μΑ	$V_{CC} = 5.25 \text{ V}, \text{ V}_{I} = 2.7 \text{ V}$	
Input current	IL	—	—	-0.4	mA	$V_{CC} = 5.25 \text{ V}, \text{ V}_{I} = 0.4 \text{ V}$	
	l <sub>l</sub>	—	—	0.1	mA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 7 V	
Short-circuit output current	I <sub>OS</sub>	-30	—	-130	mA	V <sub>CC</sub> = 5.25 V	
Supply current	I <sub>CC</sub>	_	27	40	mA	$V_{CC} = 5.25 \text{ V},$ $V_{I} = 4.5 \text{ V}$ (Output control)	
Input clamp voltage	VIK	_	_	-1.5	V	$V_{CC} = 4.75 \text{ V}, \text{ I}_{IN} = -18 \text{ mA}$	

Note:  $V_{CC} = 5 \text{ V}, \text{ Ta} = 25^{\circ}\text{C}$ 

# **Switching Characteristics**

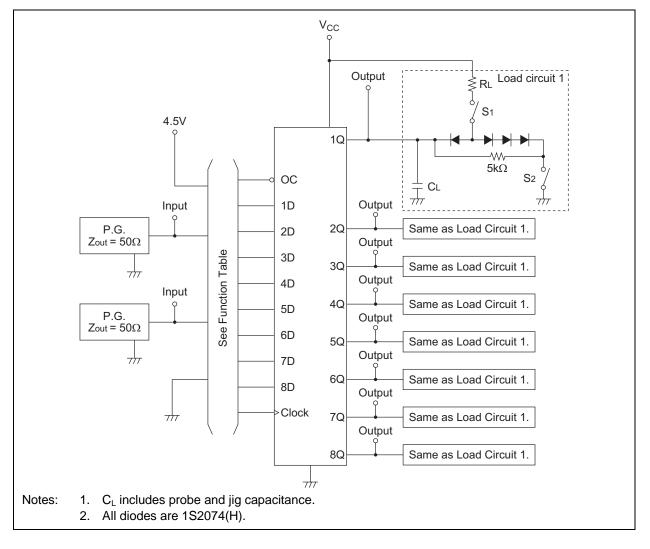
 $(V_{CC} = 5 V, Ta = 25^{\circ}C)$ 

ltem	Symbol	Inputs	Output	min.	typ.	max.	Unit	Condition
Maximum clock frequency	$f_{\sf max}$	Clock	Q	35	50	_	MHz	
Dranagatian dalay time	t <sub>PLH</sub>	Clock	Q	—	15	28	ns	$C_L = 45 \text{ pF},$ $R_L = 667 \Omega$
Propagation delay time	t <sub>PHL</sub>			—	19	28		
Output onable time	t <sub>ZH</sub>	OC	Q	_	20	28		
Output enable time	t <sub>ZL</sub>			_	21	28		
Output disable time	t <sub>HZ</sub>	ос	Q	_	12	20		$C_L = 5 \text{ pF},$
Output disable time	t <sub>LZ</sub>		Q	—	14	25	]	$R_L = 667 \ \Omega$



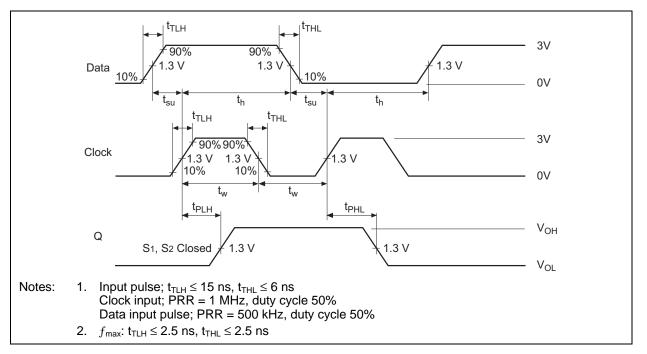
### **Testing Method**

### Test Circuit

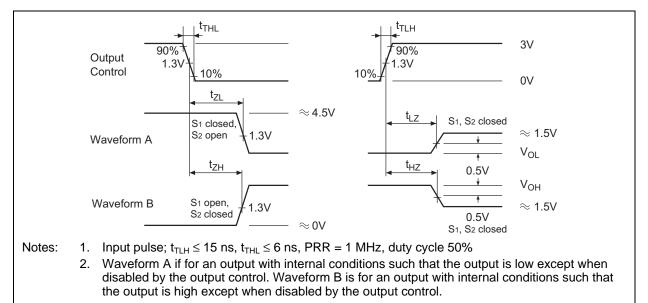




#### Waveforms 1

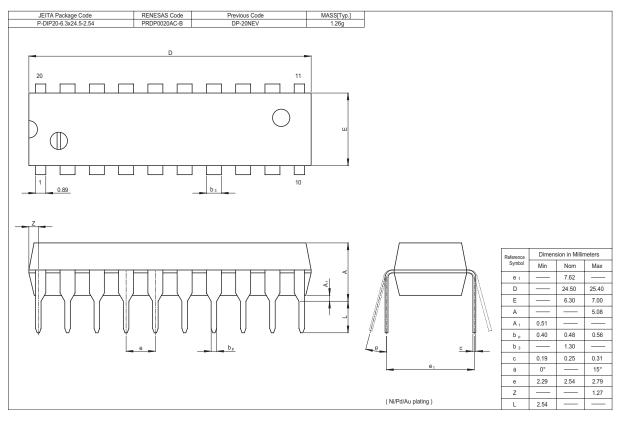


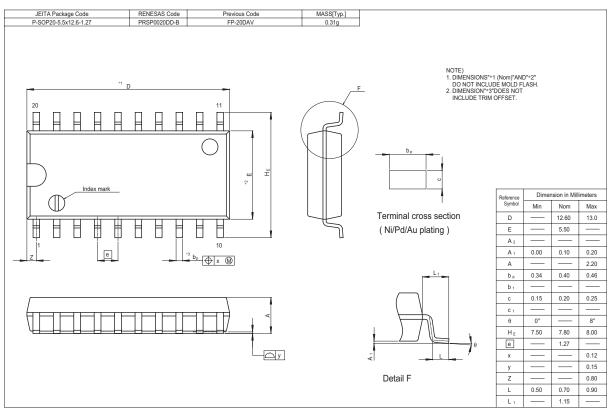
#### Waveforms 2





### **Package Dimensions**

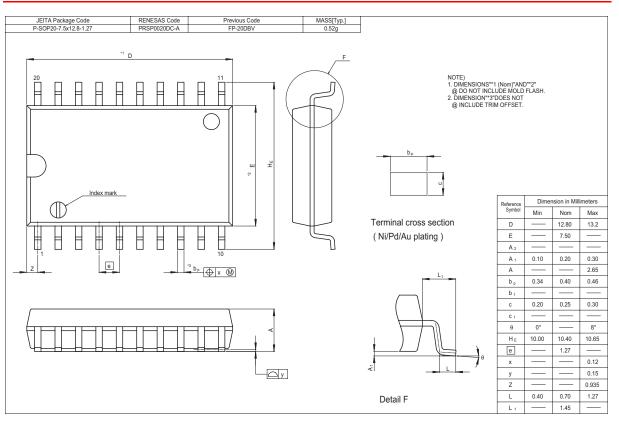




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