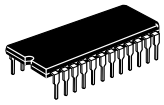
4-Bit Arithmetic Logic Unit/ Function Generator

MC10181

The MC10181 is a high–speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic operations on two four–bit words. Full internal carry is incorporated for ripple through operation.

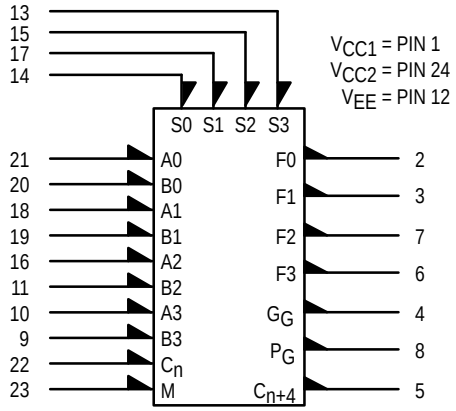
Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S0 through S3) as indicated in the tables of arithmetic/logic functions. Group carry propagate (P_G) and carry generate (G_G) are provided to allow fast operations on very long words using a second order look ahead. The internal carry is enabled by applying a low level voltage to the mode control input (M).

P_D = 600 mW typ/pkg (No Load)
t_{pd} (typ): A1 to F = 6.5 ns
C_n to C_{n+4} = 3.1 ns
A1 to P_G = 5.0 ns
A1 to G_G = 4.5 ns
A1 to C_{n+4} = 5.0

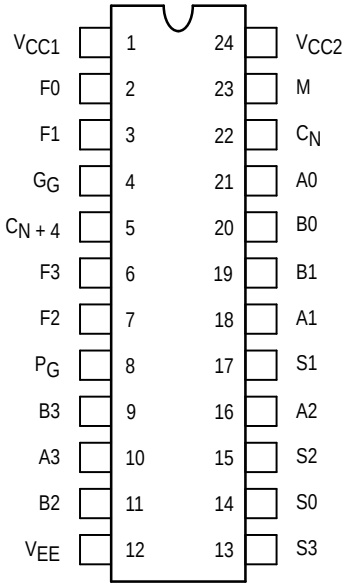


L SUFFIX
CERAMIC PACKAGE
CASE 623–05

LOGIC DIAGRAM

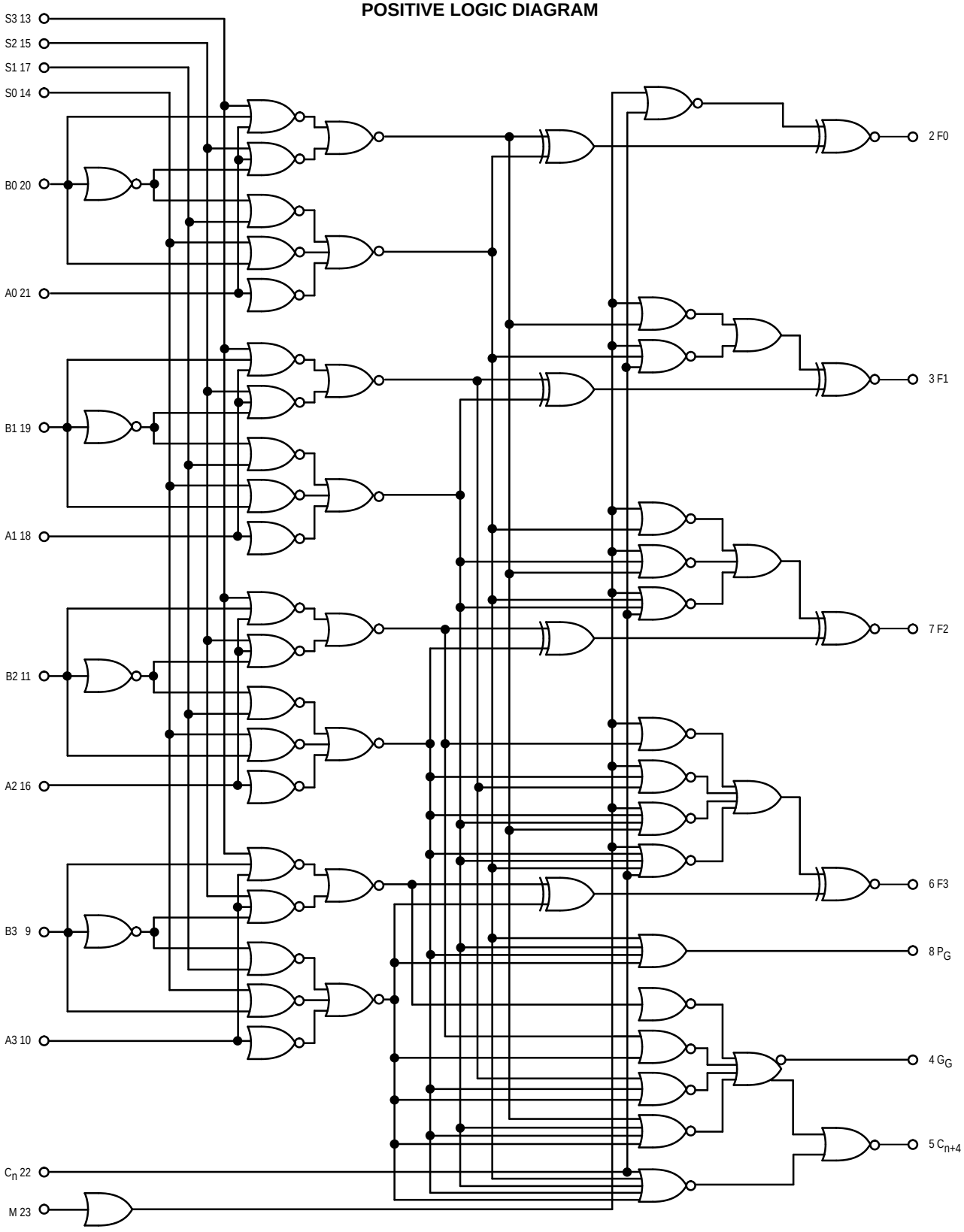


PIN ASSIGNMENT



Function Select S3	S2	S1	S0	Logic Functions M is High C = D.C. F	Arithmetic Operation M is Low C_n is low F
L	L	L	L	$F = \overline{A}$	F = A
L	L	L	H	F = $\overline{A}$ + B	F = A plus (A • B)
L	L	H	L	F = A + B	F = A plus (A • $\overline{B}$)
L	L	H	H	F = Logical "1"	F = A times 2
L	H	L	L	F = A • B	F = (A + B) plus 0
L	H	L	H	F = B	F = (A + B) plus (A • $\overline{B}$)
L	H	H	L	F = A ⊙ B	F = A plus B
L	H	H	H	F = $\overline{A}$ + B	F = A plus (A + B)
H	L	L	L	F = A • B	F = (A + B) plus 0
H	L	L	H	F = A ⊕ B	F = A minus B minus 1
H	L	H	L	F = B	F = (A + B) plus (A • $\overline{B}$)
H	L	H	H	F = A + B	F = A plus (A + B)
H	H	L	L	F = Logical "0"	F = minus 1 (two's complement)
H	H	L	H	F = A • B	F = (A • B) minus 1
H	H	H	L	F = A • B	F = (A • B) minus 1
H	H	H	H	F = A	F = A minus 1

POSITIVE LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	Pin Under Test	Test Limits							Unit
				–30°C		+25°C			+85°C		
				Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current		I_E	12		159			145		159	mAdc
Input Current		I_{inH}	9		390			245		245	µAdc
			10		350			220		220	
			11		390			245		245	
			13		320			200		200	
			14		425			265		265	
			15		425			265		265	
			16		350			220		220	
			17		425			265		265	
			18		350			220		220	
			19		390			245		245	
			20		390			245		245	
			21		350			220		220	
			22		460			290		290	
			23		320			200		200	
Input Leakage Current		I_{inL}	9	0.5		0.5			0.3		µAdc
			10	0.5		0.5			0.3		
			11	0.5		0.5			0.3		
			13	0.5		0.5			0.3		
			14	0.5		0.5			0.3		
			15	0.5		0.5			0.3		
			16	0.5		0.5			0.3		
			17	0.5		0.5			0.3		
			18	0.5		0.5			0.3		
			19	0.5		0.5			0.3		
			20	0.5		0.5			0.3		
			21	0.5		0.5			0.3		
			22	0.5		0.5			0.3		
			23	0.5		0.5			0.3		
Output Voltage	Logic 1	V_{OH}	*	–1.060	–0.890	–0.960		–0.810	–0.890	–0.700	Vdc
Output Voltage	Logic 0	V_{OL}	*	–2.000	–1.675	–1.990		–1.650	–1.920	–1.615	Vdc
Threshold Voltage	Logic 1	V_{OHA}	*	–1.080		–0.980			–0.910		Vdc
Threshold Voltage	Logic 0	V_{OLA}	*		–1.655			–1.630		–1.595	Vdc

* Test all input–output combinations according to Function Table.

** For threshold level test, apply threshold input level to only one input pin at a time.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)					
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C			–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C			–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C			–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic		**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**				**(V_{CC}) Gnd**
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	12					12	1, 24
Input Current		I_{inH}	9	9				12	1, 24
			10	10				12	1, 24
			11	11				12	1, 24
			13	13				12	1, 24
			14	14				12	1, 24
			15	15				12	1, 24
			16	16				12	1, 24
			17	17				12	1, 24
			18	18				12	1, 24
			19	19				12	1, 24
			20	20				12	1, 24
			21	21				12	1, 24
			22	22				12	1, 24
			23	23				12	1, 24
Input Leakage Current		I_{inL}	9		9			12	1, 24
			10		10			12	1, 24
			11		11			12	1, 24
			13		13			12	1, 24
			14		14			12	1, 24
			15		15			12	1, 24
			16		16			12	1, 24
			17		17			12	1, 24
			18		18			12	1, 24
			19		19			12	1, 24
			20		20			12	1, 24
			21		21			12	1, 24
			22		22			12	1, 24
			23		23			12	1, 24
Output Voltage	Logic 1	V_{OH}	*	*	*			12	1, 24
Output Voltage	Logic 0	V_{OL}	*	*	*			12	1, 24
Threshold Voltage	Logic 1	V_{OHA}	*			**	**	12	1, 24
Threshold Voltage	Logic 0	V_{OLA}	*			**	**	12	1, 24

* Test all input–output combinations according to Function Table.

** For threshold level test, apply threshold input level to only one input pin at a time.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

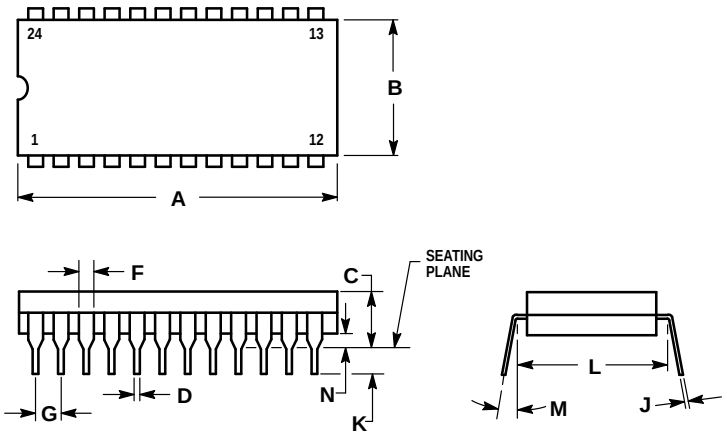
Characteristic	Symbol	Input	Output	Conditions†	AC Switching Characteristics							
					–30°C *		+25°C			+85°C *		
					Min	Max	Min	Typ	Max	Min	Max	Unit
Propagation Delay	t++,t– –	C_n	C_{n+4}	A0,A1,A2,A3	1.0	5.1	1.1	3.1	5.0	1.1	5.4	ns
Rise Time, Fall Time	t+,t–	C_n	C_{n+4}	A0,A1,A2,A3	1.0	3.2	1.0	2.0	3.0	1.0	3.2	ns
Propagation Delay	t++,t+–	C_n	F1	A0	1.7	7.2	2.0	4.5	7.0	2.0	7.5	ns
	t–+,t– –	C_n	F1	A0	1.7	7.2	2.0	4.5	7.0	2.0	7.5	ns
Rise Time, Fall Time	t+,t–	C_n	F1	A0	1.3	5.3	1.5	3.0	5.0	1.5	5.3	ns
Propagation Delay	t++,t+–	A1	F1	—	2.6	10.4	3.0	6.5	10	3.0	10.8	ns
	t–+,t– –	A1	F1	—	2.6	10.4	3.0	6.5	10	3.0	10.8	ns
Rise Time, Fall Time	t+,t–	A1	F1	—	1.3	5.4	1.5	3.0	5.0	1.5	5.3	ns
Propagation Delay	t++,t– –	A1	P_G	S0,S3	1.6	7.0	2.0	5.0	6.5	2.0	7.0	ns
Rise Time, Fall Time	t+,t–	A1	P_G	S0,S3	0.8	3.7	1.1	2.0	3.5	1.1	3.8	ns
Propagation Delay	t++,t– –	A1	G_G	A0,A2,A3,C_n	1.1	7.4	2.0	4.5	7.0	1.3	7.7	ns
Rise Time, Fall Time	t+,t–	A1	G_G	A0,A2,A3,C_n	1.2	5.1	1.5	4.0	5.0	1.2	5.3	ns
Propagation Delay	t+–,t–+	A1	C_{n+4}	A0,A2,A3,C_n	1.7	7.3	2.0	5.0	7.0	2.0	7.8	ns
Rise Time, Fall Time	t+,t–	A1	C_{n+4}	A0,A2,A3,C_n	1.0	3.1	1.0	2.0	3.0	1.0	3.2	ns
Propagation Delay	t++,t–+	B1	F1	S3,C_n	2.7	11.3	3.0	8.0	11	3.0	11.9	ns
Rise Time, Fall Time	t+,t–	B1	F1	S3,C_n	1.2	5.3	1.5	3.5	5.0	1.5	5.3	ns
Propagation Delay	t++,t– –	B1	P_G	S0,A1	1.6	7.7	2.0	6.0	7.5	2.0	8.0	ns
Rise Time, Fall Time	t+,t–	B1	P_G	S0,A1	1.0	3.6	1.1	2.0	3.5	1.1	3.9	ns
Propagation Delay	t++,t– –	B1	G_G	S3,C_n	1.7	8.2	2.0	6.0	8.0	2.0	8.6	ns
Rise Time, Fall Time	t+,t–	B1	G_G	S3,C_n	1.4	5.2	1.5	3.0	5.0	1.2	5.4	ns
Propagation Delay	t+–,t–+	B1	C_{n+4}	S3,C_n	1.8	8.2	2.0	6.0	8.0	2.0	8.7	ns
Rise Time, Fall Time	t+,t–	B1	C_{n+4}	S3,C_n	0.9	3.1	1.0	2.0	3.0	1.0	3.2	ns
Propagation Delay	t++,t+–	M	F1	—	2.4	10.3	3.0	6.5	10	3.0	10.8	ns
Rise Time, Fall Time	t+,t–	M	F1	—	1.1	5.1	1.5	4.0	5.0	1.5	5.3	ns
Propagation Delay	t+–,t–+	S1	F1	A1,B1	2.5	10.7	3.0	6.5	10	3.0	10.8	ns
Rise Time, Fall Time	t+,t–	S1	F1	A1,B1	1.0	5.4	1.5	3.0	5.0	1.5	5.4	ns
Propagation Delay	t–+,t+–	S1	P_G	A3,B3	1.7	8.3	2.0	6.0	8.0	2.0	8.4	ns
Rise Time, Fall Time	t+,t–	S1	P_G	A3,B3	0.8	5.1	1.1	3.0	5.0	1.1	5.2	ns
Propagation Delay	t+–,t–+	S1	C_{n+4}	A3,B3	1.6	9.3	2.0	6.0	9.0	2.0	9.9	ns
Rise Time, Fall Time	t+,t–	S1	C_{n+4}	A3,B3	0.9	5.3	1.1	3.0	5.0	1.0	5.2	ns
Propagation Delay	t+–,t–+	S1	G_G	A3,B3	1.5	9.6	2.0	6.0	9.0	1.9	9.7	ns
Rise Time, Fall Time	t+,t–	S1	G_G	A3,B3	0.8	6.2	0.8	3.0	6.0	0.8	6.5	ns

† Logic high level (+1.11 Vdc) applied to pins listed. All other input pins are left floating or tied to +0.31 Vdc.
$V_{CC1} = V_{CC2} = +2.0$ Vdc, $V_{EE} = -3.2$ Vdc

* L Suffix Only

OUTLINE DIMENSIONS

L SUFFIX
CERAMIC PACKAGE
CASE 623–05
ISSUE M



NOTES:
1. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (WHEN FORMED PARALLEL).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0 °	15 °	0 °	15 °
N	0.51	1.27	0.020	0.050

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