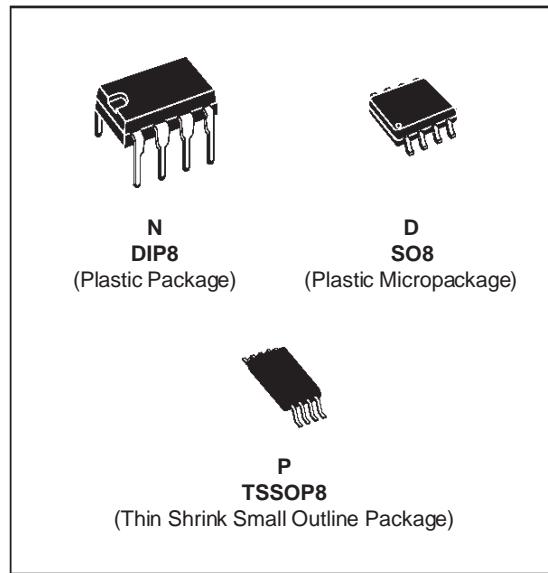


LOW POWER DUAL OPERATIONAL AMPLIFIERS

- INTERNALLY FREQUENCY COMPENSATED
- LARGE DC VOLTAGE GAIN : 100dB
- WIDE BANDWIDTH (unity gain) : 1.1MHz
(temperature compensated)
- VERY LOW SUPPLY CURRENT/OP (500 μ A) -
ESSENTIALLY INDEPENDENT OF SUPPLY
VOLTAGE
- LOW INPUT BIAS CURRENT : 20nA
(temperature compensated)
- LOW INPUT OFFSET CURRENT : 2nA
- INPUT COMMON-MODE VOLTAGE RANGE
INCLUDES GROUND
- DIFFERENTIAL INPUT VOLTAGE RANGE
EQUAL TO THE POWER SUPPLY VOLTAGE
- LARGE OUTPUT VOLTAGE SWING 0V TO
(Vcc – 1.5V)



ORDER CODES

Part Number	Temperature Range	Package		
		N	D	P
LM2904	-40°C, +125°C	•	•	•
Example : LM2904D				

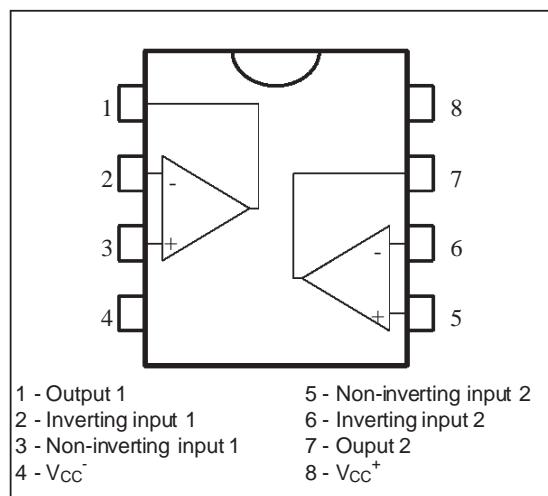
DESCRIPTION

This circuit consists of two independent, high gain, internally frequency compensated which were designed specifically for automotive and industrial control system. It operates from a single power supply over a wide range of voltages. The low power supply drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op-amp circuits which now can be more easily implemented in single power supply systems. For example, these circuits can be directly supplied with off the standard +5V which is used in logic systems and will easily provide the required interface electronics without requiring any additional power supply.

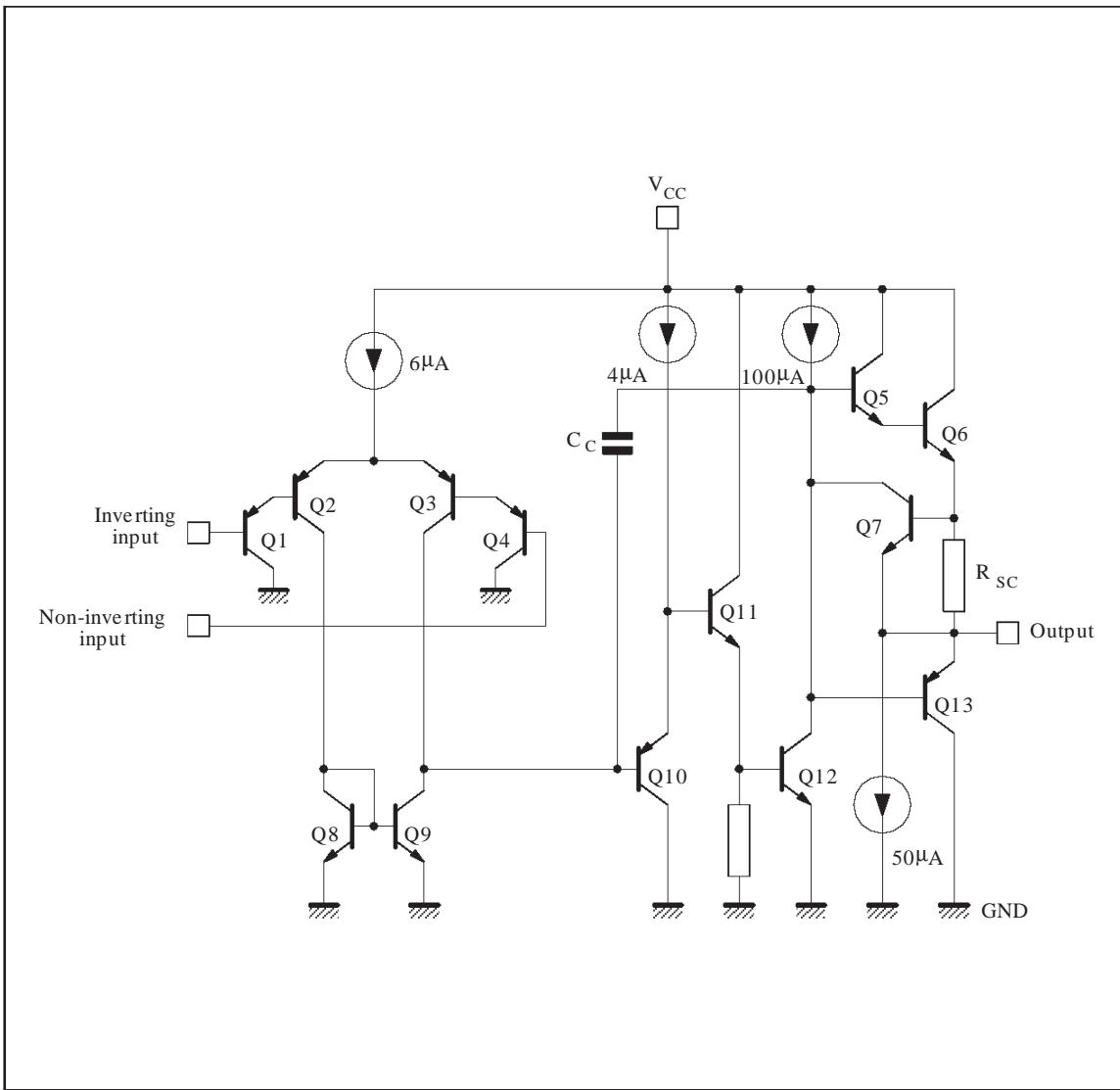
In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

PIN CONNECTIONS (top view)



LM2904

SCHEMATIC DIAGRAM (1/2 LM2904)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LM2904	Unit
V_{CC}	Supply Voltage	+32	V
V_i	Input Voltage	-0.3 to +32	V
V_{id}	Differential Input Voltage	+32	V
Output Short-circuit Duration - (note 2)			
P_{tot}	Power Dissipation	500	mW
I_{in}	Input Current - (note 1)	50	mA
T_{oper}	Operating Free-air Temperature Range	-40 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

$V_{CC^+} = +5V$, V_{CC^-} = Ground, $V_O = 1.4V$, $T_{amb} = 25^\circ C$ (unless otherwise specified)

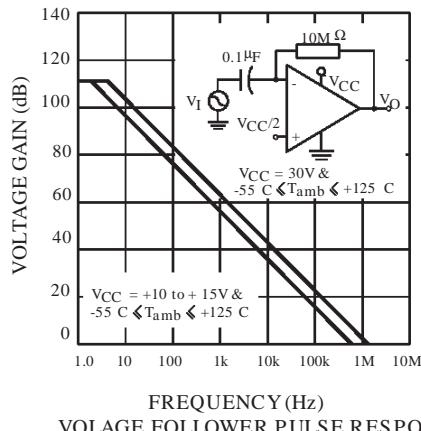
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage - (note 3) $T_{amb} = 25^\circ C$ $T_{min.} \leq T_{amb} \leq T_{max.}$		2	7 9	mV
I_{io}	Input Offset Current $T_{amb} = 25^\circ C$ $T_{min.} \leq T_{amb} \leq T_{max.}$		2	30 40	nA
I_{ib}	Input Bias Current - (note 4) $T_{amb} = 25^\circ C$ $T_{min.} \leq T_{amb} \leq T_{max.}$		20	150 200	nA
A_{vd}	Large Signal Voltage Gain ($V_{CC^+} = +15V$, $R_L = 2k\Omega$, $V_O = 1.4V$ to $11.4V$) $T_{amb} = 25^\circ C$ $T_{min.} \leq T_{amb} \leq T_{max.}$	50 25	100		V/mV
SVR	Supply Voltage Rejection Ratio ($R_S = 10k\Omega$) ($V_{CC^+} = 5$ to $30V$) $T_{amb} = 25^\circ C$ $T_{min.} \leq T_{amb} \leq T_{max.}$	65 65	100		dB
I_{cc}	Supply Current, all Amp, no Load $V_{CC^+} = +5V$, $T_{min.} \leq T_{amb} \leq T_{max.}$ $V_{CC^+} = +30V$, $T_{min.} \leq T_{amb} \leq T_{max.}$		0.7	1.2 2	mA
V_{icm}	Input Common Mode Voltage Range ($V_{CC^+} = +30V$) - (note 6) $T_{amb} = 25^\circ C$ $T_{min.} \leq T_{amb} \leq T_{max.}$	0 0		$V_{CC^+}-1.5$ $V_{CC^+}-2$	V
CMR	Common-mode Rejection Ratio ($R_S = 10k\Omega$) $T_{amb} = 25^\circ C$ $T_{min.} \leq T_{amb} \leq T_{max.}$	70 60	85		dB
I_{source}	Output Source Current ($V_{CC^+} = +15V$, $V_O = 2V$, $V_{id} = +1V$)	20	40	60	mA
I_{sink}	Output Current Sink ($V_{id} = -1V$) $V_{CC^+} = +15V$, $V_O = 2V$ $V_{CC^+} = +15V$, $V_O = +0.2V$	10 12	20 50		mA μA
V_{OPP}	Output Voltage Swing ($R_L = 2k\Omega$) $T_{amb} = 25^\circ C$ $T_{min.} \leq T_{amb} \leq T_{max.}$	0 0		$V_{CC^+}-1.5$ $V_{CC^+}-2$	V
V_{OH}	High Level Output Voltage ($V_{CC^+} = 30V$) $T_{amb} = 25^\circ C$ $T_{min.} \leq T_{amb} \leq T_{max.}$ $T_{amb} = 25^\circ C$ $T_{min.} \leq T_{amb} \leq T_{max.}$ $R_L = 2k\Omega$ $R_L = 10k\Omega$	26 26 27 27	27 28		V
V_{OL}	Low Level Output Voltage ($R_L = 10k\Omega$) $T_{amb} = 25^\circ C$ $T_{min.} \leq T_{amb} \leq T_{max.}$		5	20 20	mV
SR	Slew Rate ($V_{CC^+} = 15V$, $V_I = 0.5$ to $3V$, $R_L = 2k\Omega$, $C_L = 100pF$, unity gain)	0.3	0.6		V/ μs
GBP	Gain Bandwidth Product ($V_{CC^+} = 30V$, $f = 100kHz$, $V_{in} = 10mV$, $R_L = 2k\Omega$, $C_L = 100pF$)	0.7	1.1		MHz
THD	Total Harmonic Distortion ($f = 1kHz$, $A_v = 20dB$, $R_L = 2k\Omega$, $V_{CC^+} = 30V$, $C_L = 100pF$, $V_O = 2PP$)		0.02		%

ELECTRICAL CHARACTERISTICS (continued)

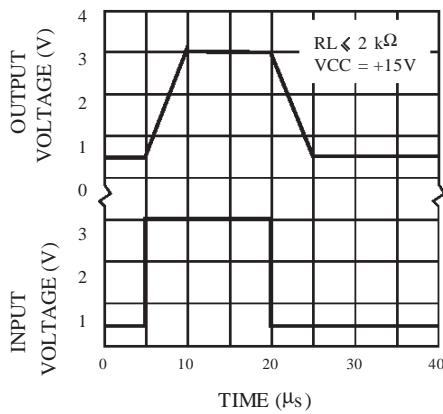
Symbol	Parameter	Min.	Typ.	Max	Unit
DV _{io}	Input Offset Voltage Drift		7	30	µA/°C
DI _{io}	Input Offset Current Drift		10	300	pA/°C
V _{O1} /V _{O2}	Channel Separation (note 5) 1kHz ≤ f ≤ 20kHz		120		dB

- Notes :
1. This input current only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the Op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output will set up again for input voltage higher than -0.3V.
 2. Short-circuits from the output to V_{CC} can cause excessive heating if V_{CC} > 15V. The maximum output current is approximatively 40mA independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.
 3. V_O = 1.4V, R_S = 0Ω, 5V < V_{CC} < 30V, 0 < V_{ic} < V_{CC} - 1.5V.
 4. The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
 5. Due to the proximity of external components insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.
 6. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC} - 1.5V. But either or both inputs can go to +32V without damage.

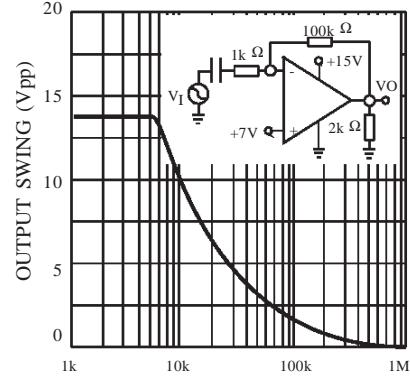
OPEN LOOP FREQUENCY RESPONSE (NOTE 3)



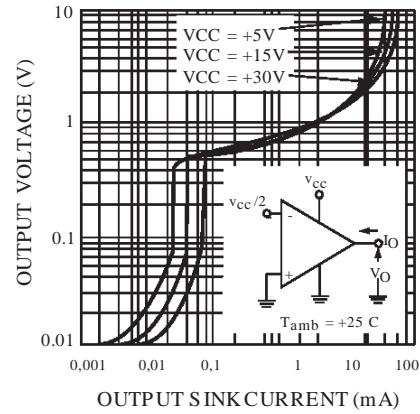
VOLAGE FOLLOWER PULSE RESPONSE

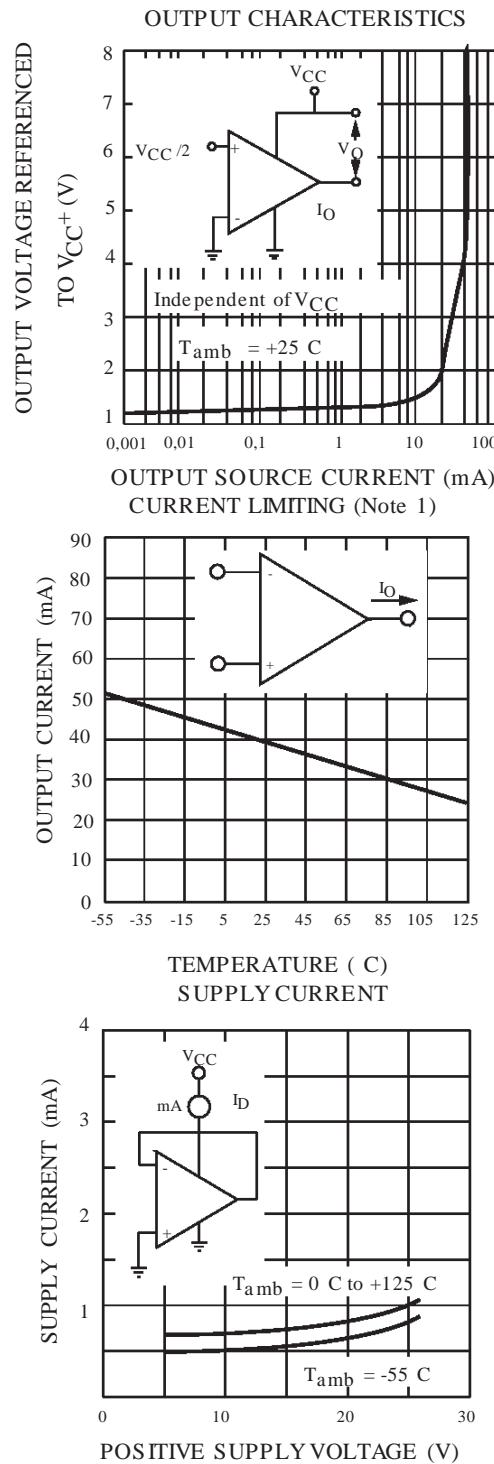
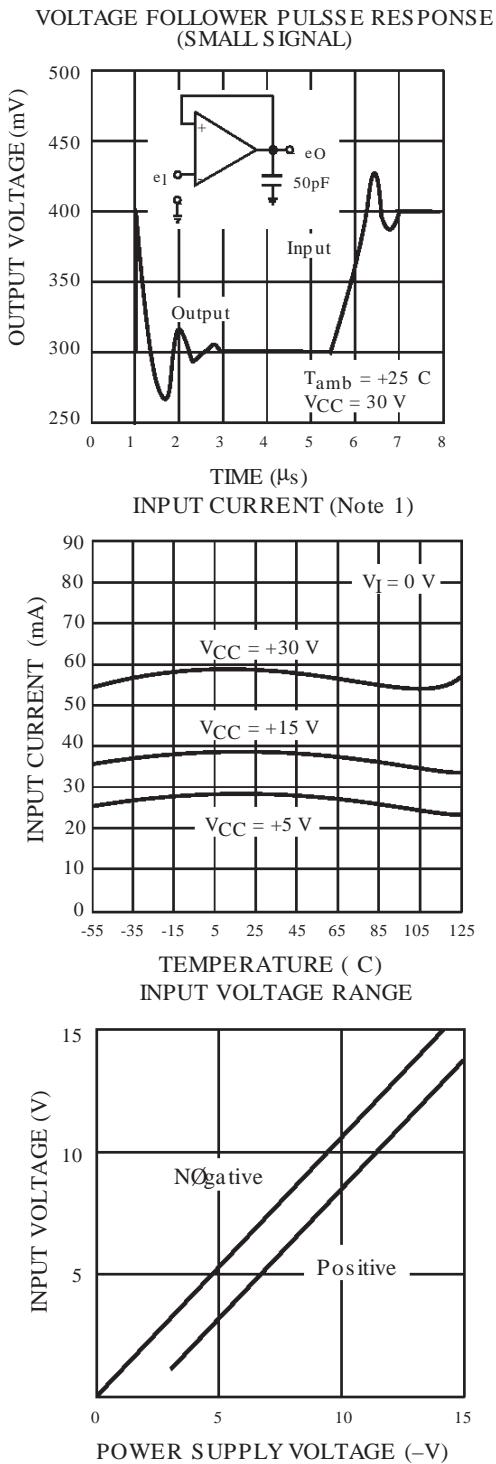


LARGE SIGNAL FREQUENCY RESPONSE

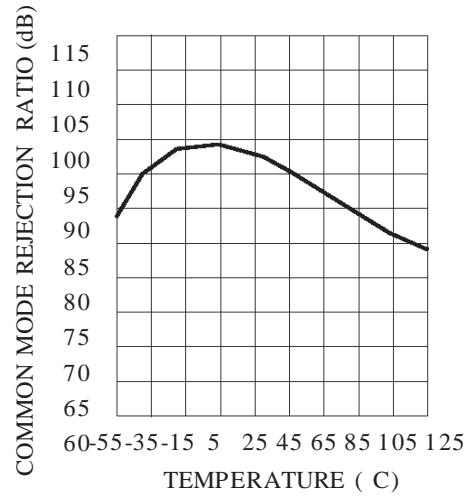
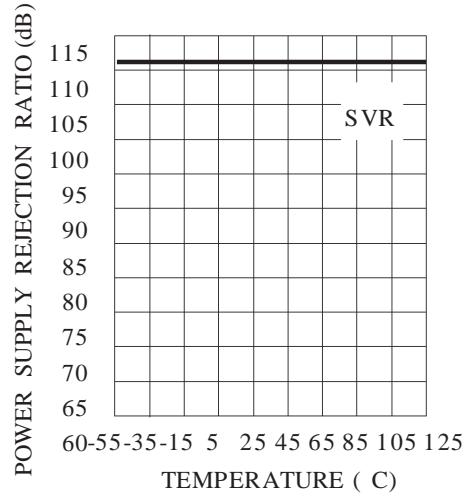
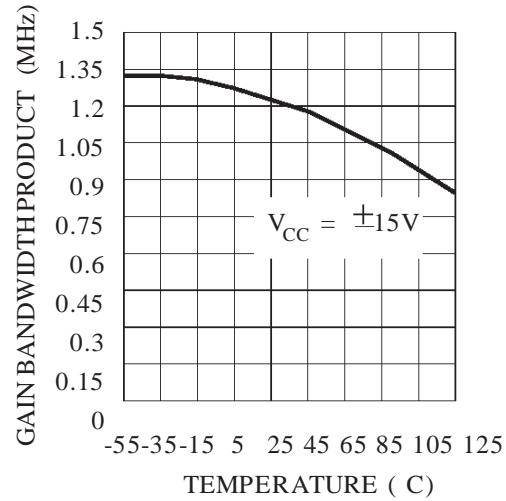
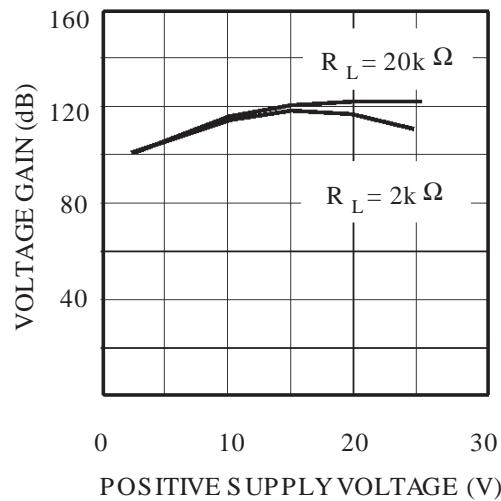
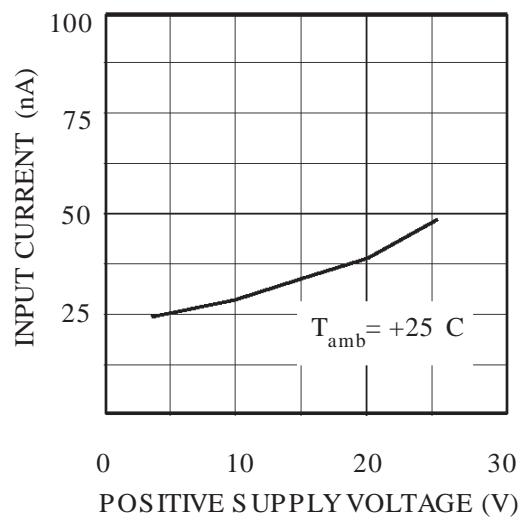
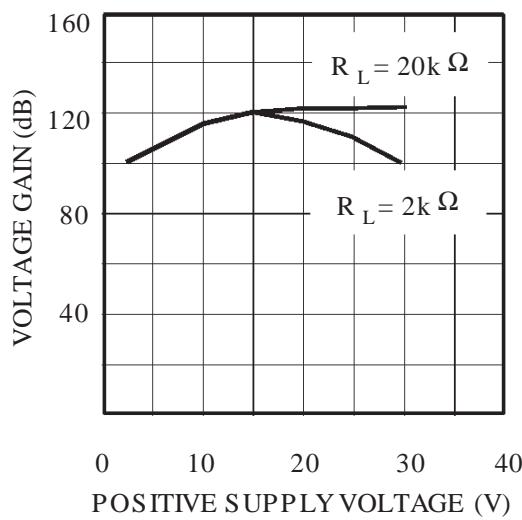


OUTPUT CHARACTERISTICS



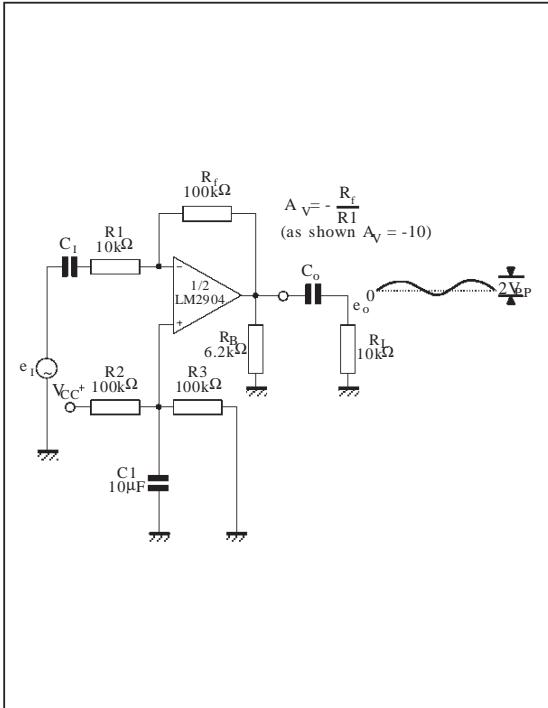


LM2904

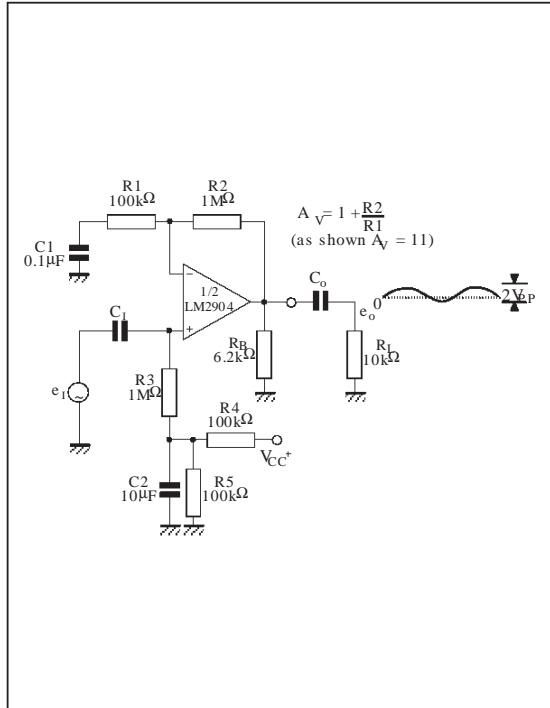


TYPICAL APPLICATIONS (single supply voltage) $V_{CC} = +5V_{DC}$

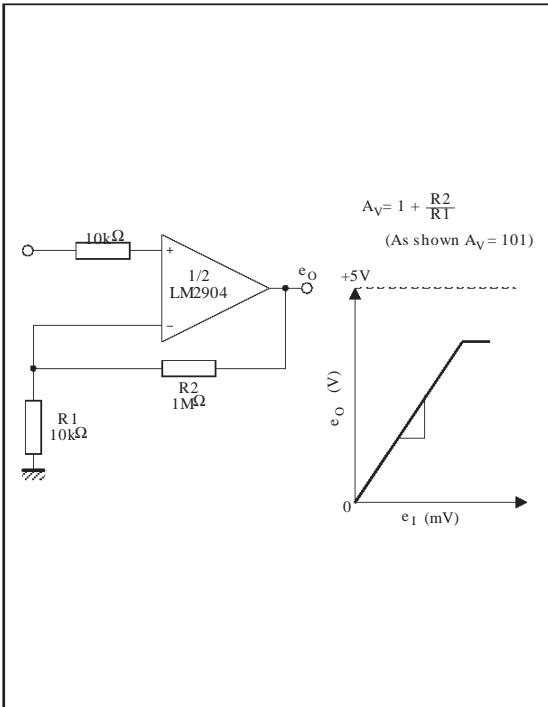
AC COUPLED INVERTING AMPLIFIER



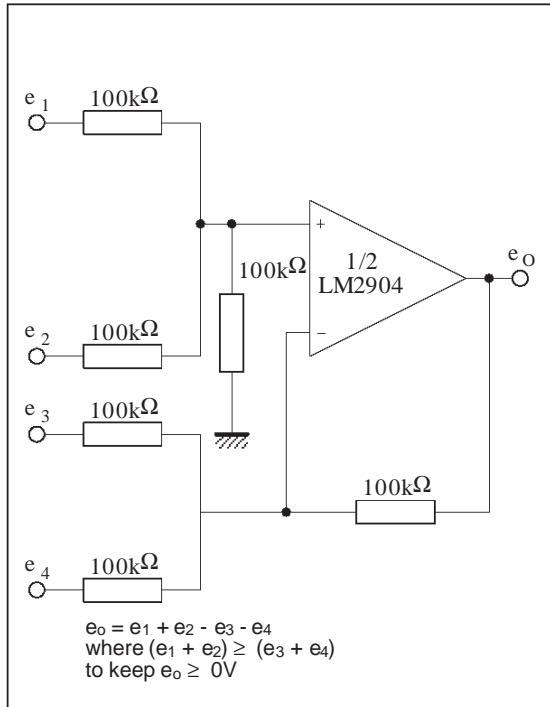
AC COUPLED NON-INVERTING AMPLIFIER



NON-INVERTING DC AMPLIFIER

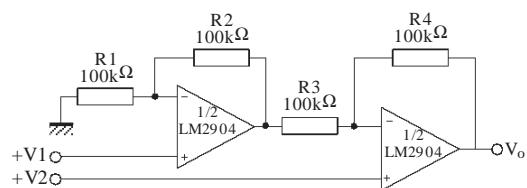


DC SUMMING AMPLIFIER



LM2904

HIGH INPUT Z, DC DIFFERENTIAL AMPLIFIER

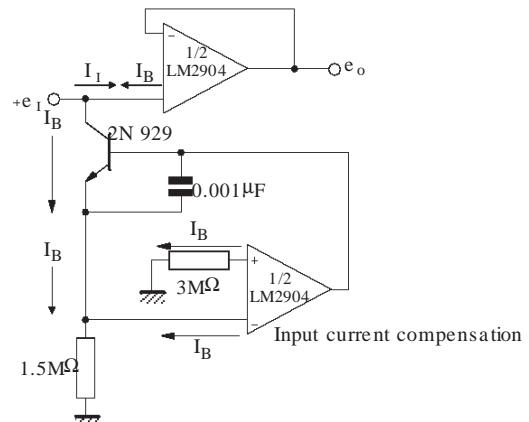


if $R_1 = R_5$ and $R_3 = R_4 = R_6 = R_7$

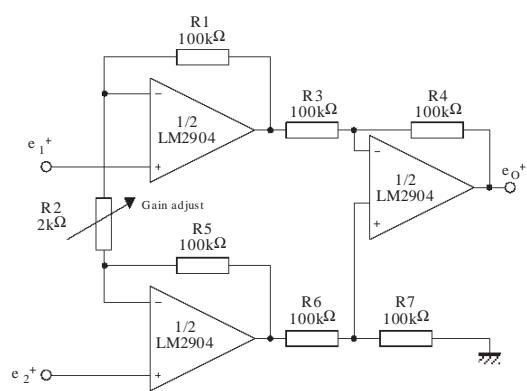
$$e_o = \left[1 + \frac{2R_1}{R_2} \right] (e_2 - e_1)$$

As shown $e_o = 101 (e_2 - e_1)$.

USING SYMMETRICAL AMPLIFIERS TO REDUCE INPUT CURRENT



HIGH INPUT Z ADJUSTABLE GAIN DC INSTRUMENTATION AMPLIFIER

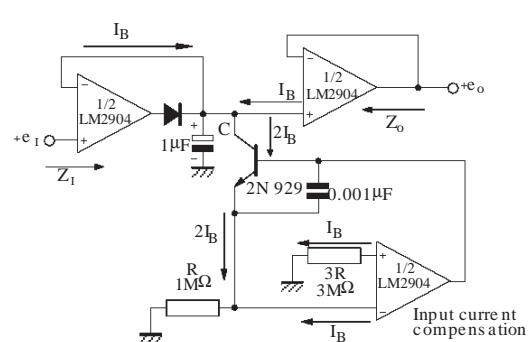


if $R_1 = R_5$ and $R_3 = R_4 = R_6 = R_7$

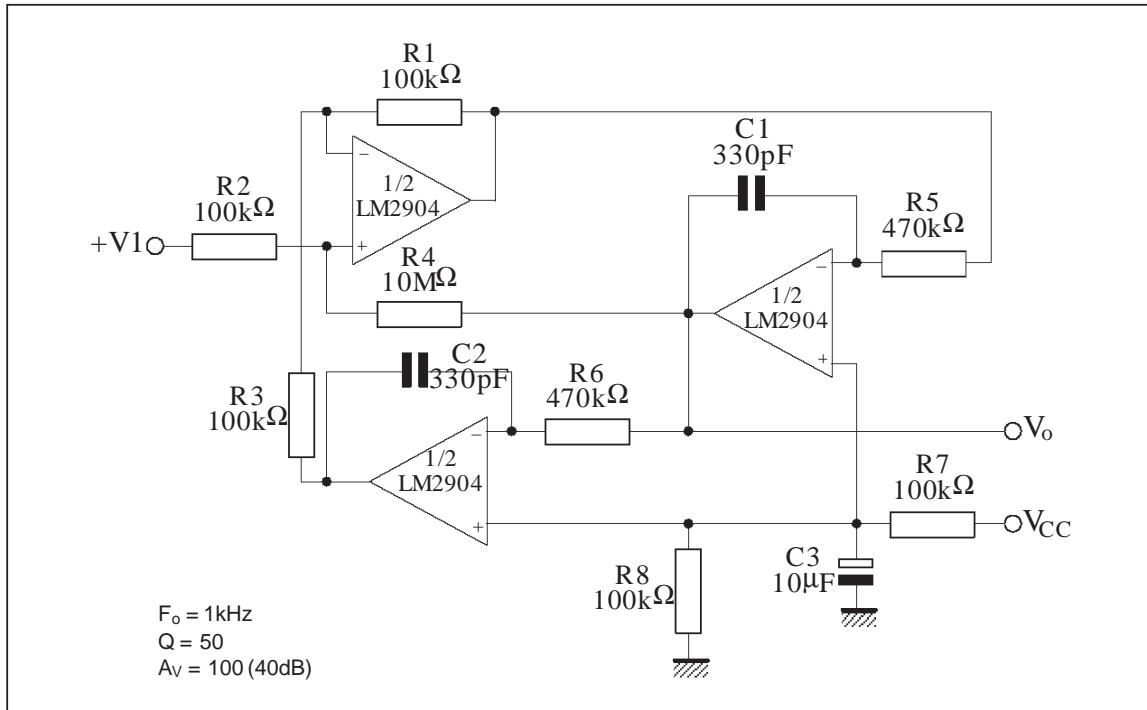
$$e_o = \left[1 + \frac{2R_1}{R_2} \right] (e_2 - e_1)$$

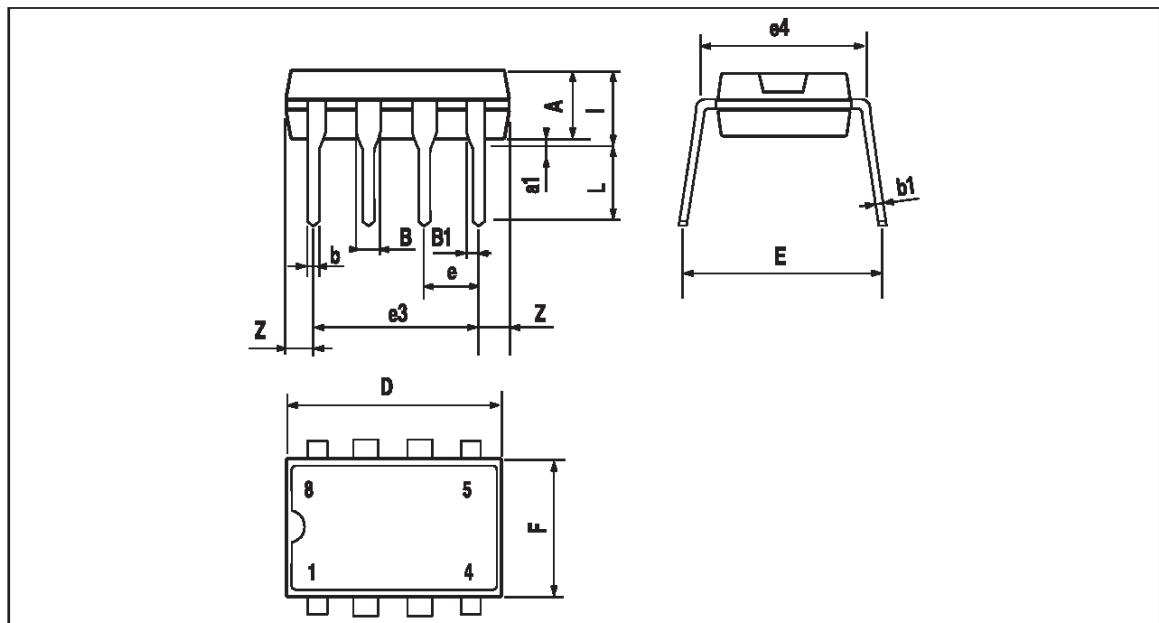
As shown $e_o = 101 (e_2 - e_1)$

LOW DRIFT PEAK DETECTOR



ACTIVE BAND-PASS FILTER



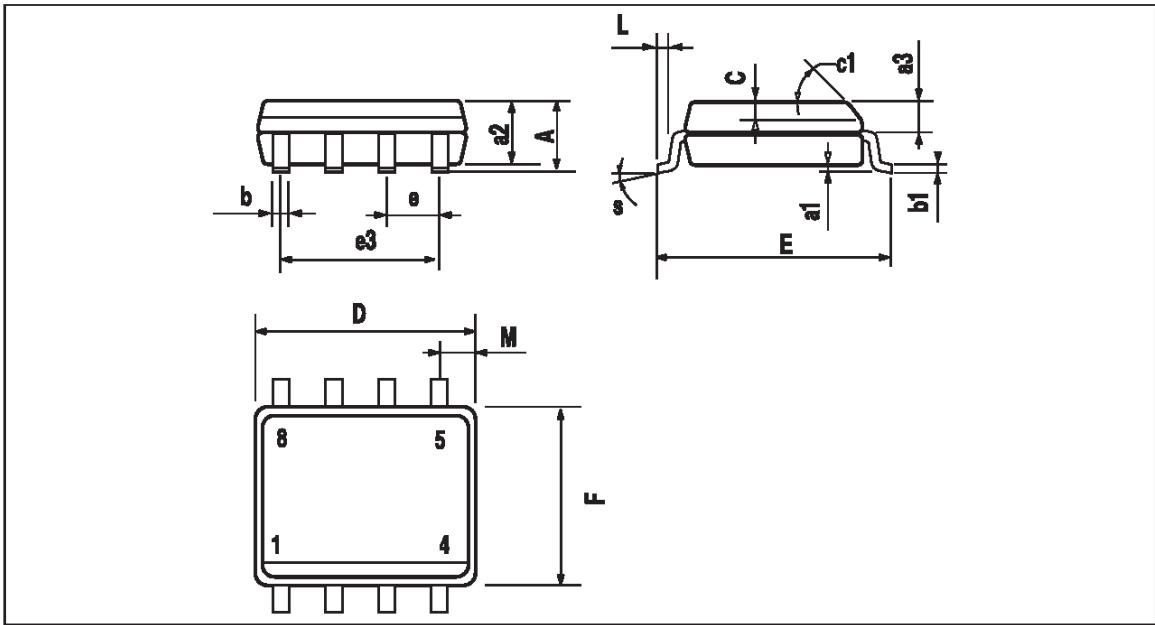
PACKAGE MECHANICAL DATA
 8 PINS - PLASTIC DIP


PMDIP8.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
i			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

DIP8.TBL

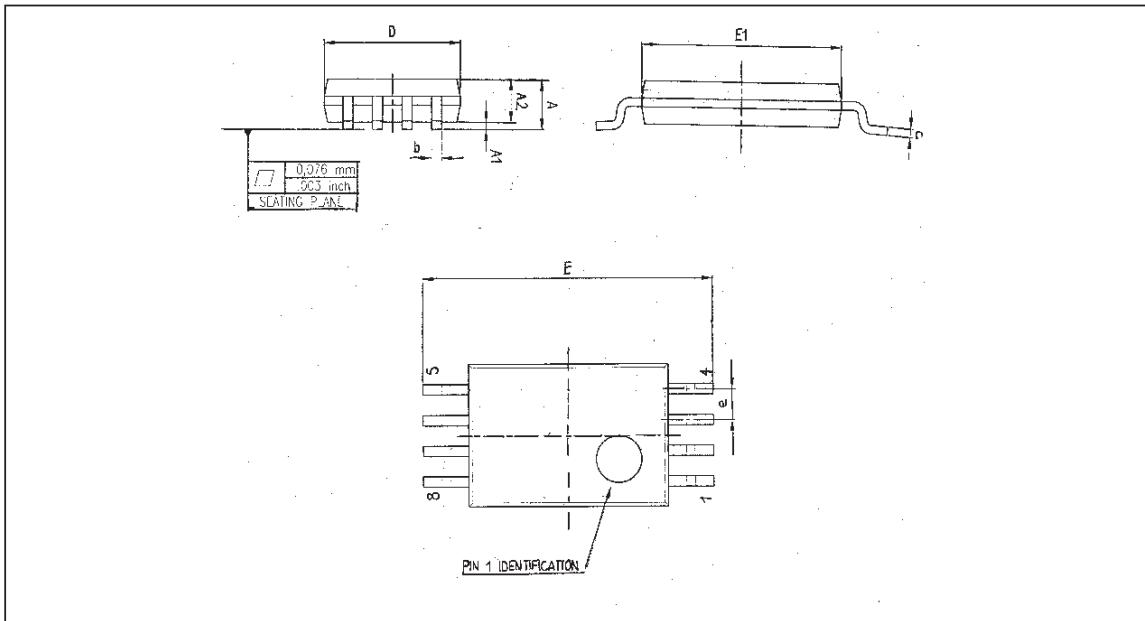
PACKAGE MECHANICAL DATA
8 PINS - PLASTIC MICROPACKAGE (SO)



PMSO8.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

SO8.TBL

PACKAGE MECHANICAL DATA
8 PINS - THIN SHRINK SMALL OUTLINE PACKAGE
PREVIEW

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.05
A1	0.05		0.15	0.01		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.15
c	0.09		0.20	0.003		0.012
D	2.90	3.00	3.10	0.114	0.118	0.122
E		6.40			0.252	
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.025	
k	0°		8°	0°		8°
I	0.50	0.60	0.75	0.09	0.0236	0.030

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a trademark of STMicroelectronics

© 1999 STMicroelectronics – Printed in Italy – All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - France - Germany - Italy - Japan - Korea - Malaysia - Malta - Mexico - Morocco
The Netherlands - Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A.

ORDER CODE: