PRELIMINARY

AMD

Am79C981

Integrated Multiport Repeater Plus™ (IMR+™)

DISTINCTIVE CHARACTERISTICS

- **Enhanced version of AMD's Am79C980 Integrated Multiport Repeater™ (IMR™) chip with the following enhancements:**
  - — Additional management port features
  - — **Minimum** mode provides support for an extra four LED outputs per port for additional status in non-intelligent repeater designs
  - — Pin/socket-compatible with the Am79C980 IMR chip
  - — Fully backward-compatible with existing IMR device designs
- **Interfaces directly with the Am79C987 HIMIB™ device to build a fully managed multiport repeater**
- **CMOS device features high integration and low power with a single +5 V supply**
- **Repeater functions comply with IEEE 802.3 Repeater Unit specifications**
- **Eight integral 10BASE-T transceivers utilize the required predistortion transmission technique**
- **Attachment unit interface (AUI) port allows connectivity with 10BASE-5 (Ethernet) and 10BASE-2 (Cheapernet) networks, as well as 10BASE-F and/or Fiber Optic Inter-Repeater Link (FOIRL) segments**
- **On-board PLL, Manchester encoder/decoder, and FIFO**
- **Expandable to increase number of repeater ports**
- **All ports can be separately isolated (partitioned) in response to excessive collision conditions or fault conditions**
- **Network management and optional features are accessible through a dedicated serial management port**
- **Twisted-pair Link Test capability conforming to the 10BASE-T standard. The receive Link Test function can be optionally disabled through the management port to facilitate interoperability with devices that do not implement the Link Test function**
- **Programmable option of Automatic Polarity Detection and Correction permits automatic recovery due to wiring errors**
- **Full amplitude and timing regeneration for retransmitted waveforms**
- **Preamble loss effects eliminated by deep FIFO**

GENERAL DESCRIPTION

The Integrated Multiport Repeater Plus (IMR+) chip is a VLSI circuit that provides a system-level solution to designing a compliant 802.3 repeater incorporating 10BASE-T transceivers. The device integrates the Repeater functions specified by Section 9 of the IEEE 802.3 standard and Twisted-Pair Transceiver functions complying with the 10BASE-T standard. The Am79C981 provides eight integral twisted-pair medium attachment units (MAUs) and an attachment unit interface (AUI) port in an 84-pin plastic leaded chip carrier (PLCC).

A network based on the 10BASE-T standard uses unshielded twisted-pair cables, thereby providing an economical solution to networking by allowing the use of low-cost unshielded twisted-pair (UTP) cable or existing telephone wiring.

The total number of ports per repeater unit can be increased by connecting multiple IMR+ devices through their expansion ports, minimizing the total cost per repeater port. Furthermore, a general-purpose attachment unit interface (AUI) provides connection capability to 10BASE-5 (Ethernet) and 10BASE-2 (Cheapernet) coaxial networks, as well as 10BASE-F and/or Fiber Optic Inter-Repeater Link (FOIRL) fiber segments. Network management and test functions are provided through TTL-compatible I/O pins.

The IMR+ device interfaces directly with AMD's Am79C987 Hardware Implemented Management Information Base™ (HIMIB) chip to build a fully managed multiport repeater as specified by the IEEE 802.3 (Layer Management for 10 Mb/s Baseband Repeaters) standard. When the IMR+ and HIMIB devices are interconnected, complete repeater and per-port statistics are maintained and can be accessed on demand using a simple 8-bit parallel interface.

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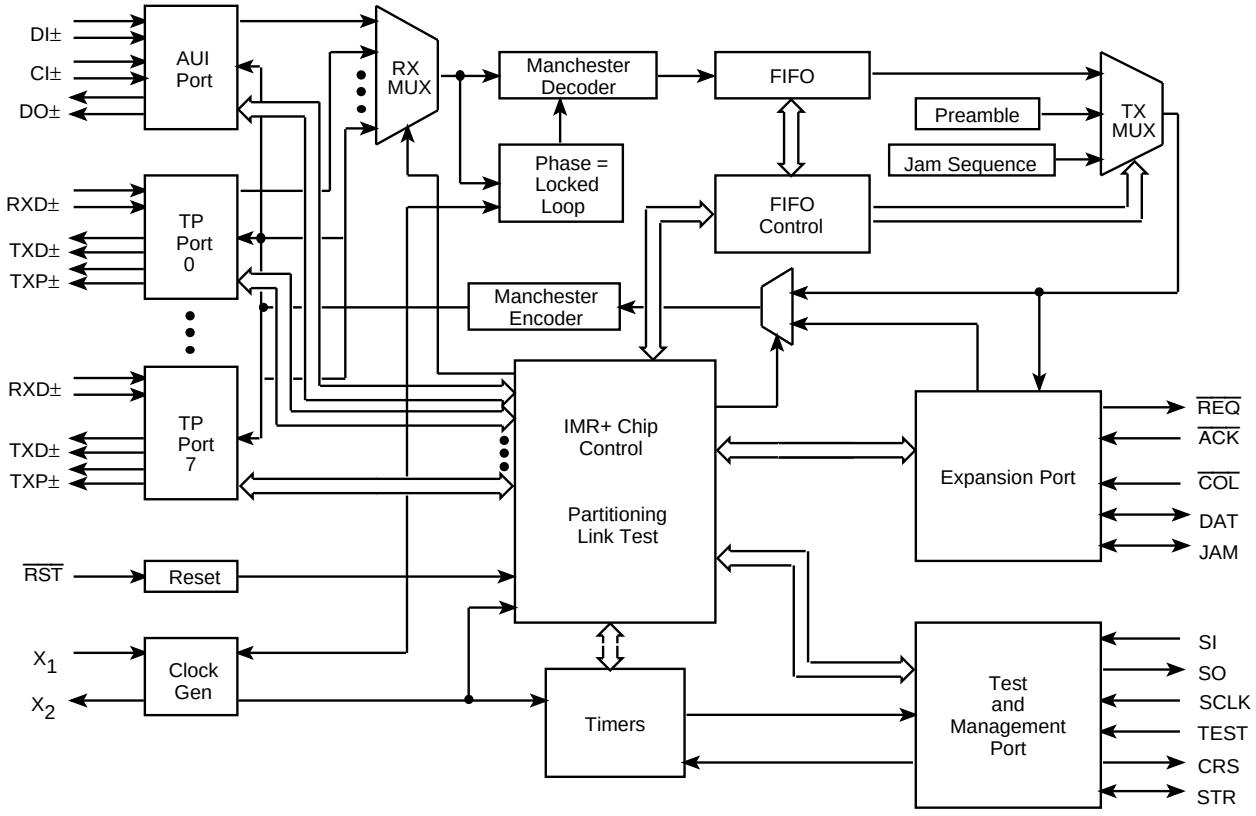
For application examples on building a fully managed repeater using the IMR+ and HIMIB devices, refer to AMD's IEEE 802.3 Repeater Technical Manual (PID#17314A) and the ISA-HUB™ User Manual (PID # 17642A).

The device is fabricated in CMOS technology and requires a single +5 V supply.

BLOCK DIAGRAM



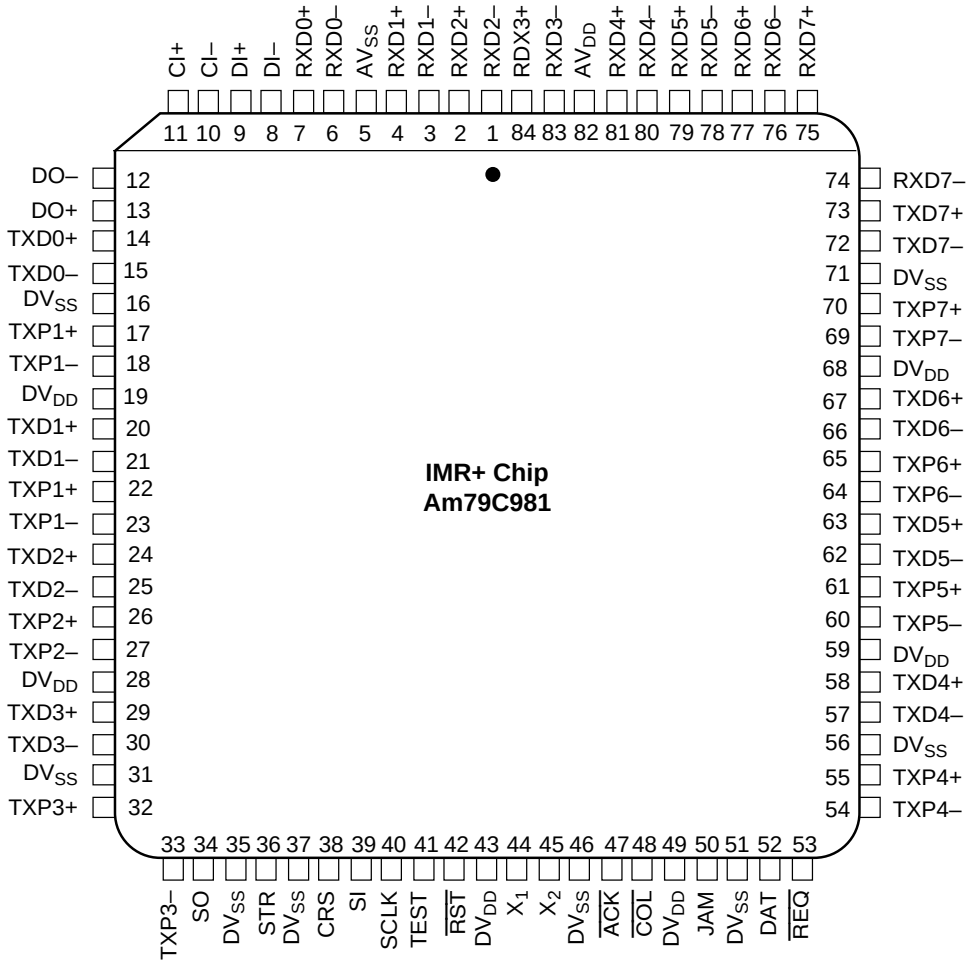
17306B-1

RELATED AMD PRODUCTS

Part No.	Description
Am79C98	Twisted Pair Ethernet Transceiver (TPEX)
Am79C100	Twisted Pair Ethernet Transceiver Plus (TPEX+)
Am7996	IEEE 802.3/Ethernet/Cheapernet Transceiver
Am79C987	Hardware Implemented Management Information Base™ (HIMIB™)
Am79C940	Media Access Controller for Ethernet (MACE™)
Am7990	Local Area Network Controller for Ethernet (LANCE)
Am79C90	CMOS Local Area Network Controller for Ethernet (C-LANCE)
Am79C900	Integrated Local Area Communications Controller™ (ILACC™)
Am79C960	PCnet-ISA Single-Chip Ethernet Controller (for ISA bus)
Am79C961	PCnet-ISA+ Single-Chip Ethernet Controller for ISA (with Microsoft® Plug n' Play® Support)
Am79C965	PCnet-32 Single-Chip 32-Bit Ethernet Controller
Am79C970	PCnet-PCI Single-Chip Ethernet Controller (for PCI bus)
Am79C974	PCnet-SCSI Combination Ethernet and SCSI Controller for PCI Systems

CONNECTION DIAGRAM

PLCC



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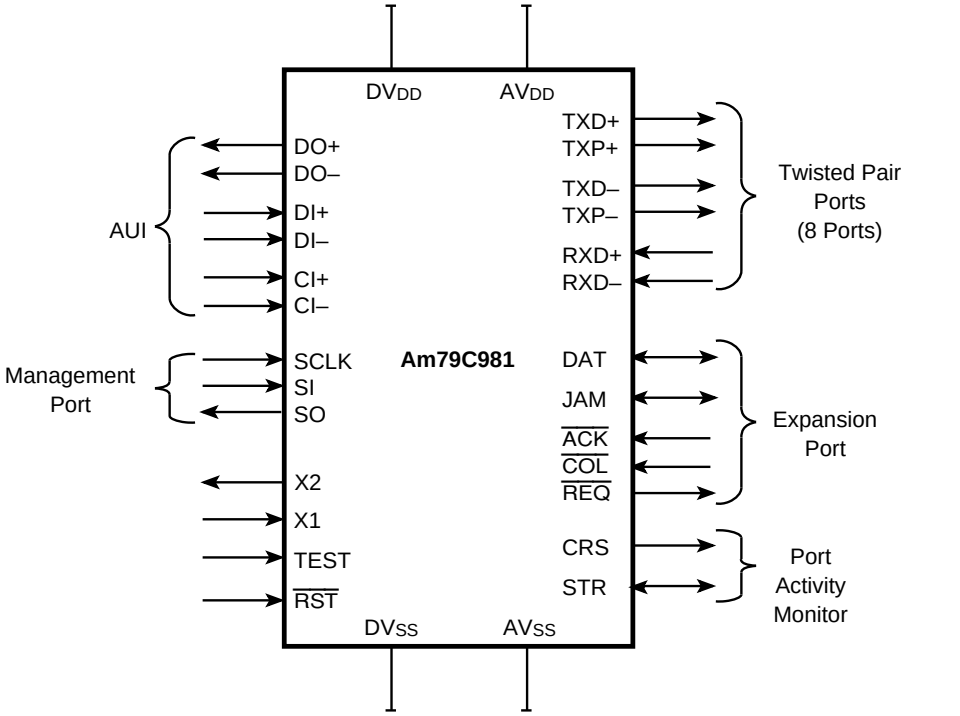
LOGIC SYMBOL



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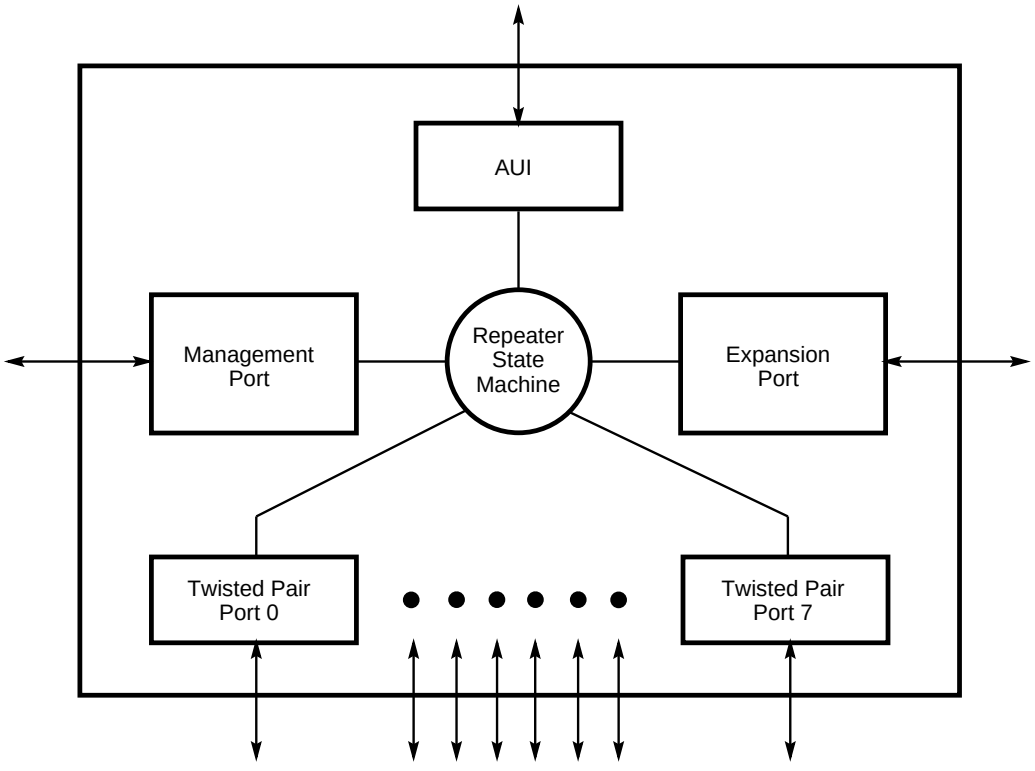
LOGIC DIAGRAM



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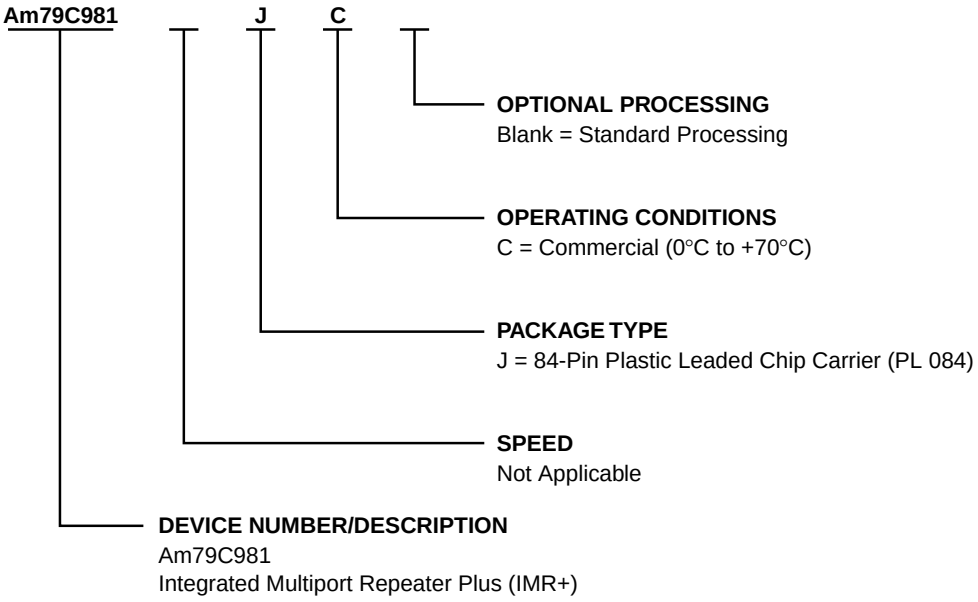
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (valid combination) is formed by a combination of the elements below.



Valid Combinations	
Am79C981	JC

Valid Combinations

Valid combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PIN DESCRIPTION

$\overline{ACK}$

Acknowledge
Input, Active LOW

When this input is asserted, it signals to the requesting IMR+ device that it may control the DAT and JAM pins. If the IMR+ chip is not requesting control of the DAT line ($\overline{REQ}$ pin HIGH), then the assertion of the $\overline{ACK}$ signal indicates the presence of valid collision status on the JAM or valid data on the DAT line.

AV_{DD}

Analog Power
Power Pin

These pins supply the +5 V to the RXD+/– receivers, the DI+/– and CI+/– receivers, the DO+/– drivers, the internal PLL, and the internal voltage reference of the IMR+ device. These power pins should be decoupled and kept separate from other power and ground planes.

AV_{SS}

Analog Ground
Ground Pin

These pins are the 0 V reference for AV_{DD}.

$\overline{COL}$

Expansion Collision
Input, Active LOW

When this input is asserted by an external arbiter, it signifies that more than one IMR+ device is active and that each IMR+ device should generate the Collision Jam sequence independently.

CI+, CI–

Control In
Input

AUI port differential receiver. Signals comply with IEEE 802.3, Section 7.

CRS

Carrier Sense
Output

The states of the internal carrier sense signals for the AUI port and the eight twisted-pair ports are serially output on this pin continuously. The output serial bit stream is synchronized to the X_1 clock.

DAT

Data
Input/Output/3-State

In non-collision conditions, the active IMR+ device will drive DAT with NRZ data, including regenerated preamble. During collision, when JAM = HIGH, DAT is used to signal a multiport (DAT = 0) or single-port (DAT = 1) condition.

When $\overline{ACK}$ is not asserted, DAT is in high impedance. If $\overline{REQ}$ and $\overline{ACK}$ are both asserted, then DAT is an output. If $\overline{ACK}$ is asserted and $\overline{REQ}$ not asserted, then DAT is an input.

This pin needs to be either pulled up or pulled down through a high-value resistor.

DI+, DI–

Data In
Input

AUI port differential receiver. Signals comply with IEEE 802.3, Section 7.

DO+, DO–

Data Out
Output

AUI port differential driver. Signals comply with IEEE 802.3, Section 7.

DV_{DD}

Digital Power
Power Pin

These pins supply +5 V to the logic portions of the IMR+ chip and the TXP+/–, TXD+/–, and DO+/– line drivers.

DV_{SS}

Digital Ground
Ground Pin

These pins are the 0 V reference for DV_{DD}.

DV_{DD} Pin #	DV_{SS} Pin #	Function
19	16	TP ports 0 & 1 drivers
28	31	TP ports 2 & 3 drivers
43, 49	35, 37, 46, 51	Core logic and expansion and control pins
59	56	TP ports 4 & 5 drivers
68	71	TP ports 6 & 7 drivers

JAM

Jam
Input/Output/3-State

When JAM is asserted, the state of DAT will indicate either a multiport (DAT = 0) or single-port (DAT = 1) collision condition.

When $\overline{ACK}$ is not asserted, JAM is in high impedance. If $\overline{REQ}$ and $\overline{ACK}$ are both asserted, then JAM is an output. If $\overline{ACK}$ is asserted and $\overline{REQ}$ not asserted, then JAM is an input.

This pin needs to be either pulled up or pulled down through a high-value resistor.

$\overline{REQ}$

Request
Output, Active LOW

This pin is driven LOW when the IMR+ chip is active. An IMR+ chip is active when it has one or more ports receiving or colliding or is in the state where it is still transmitting data from the internal FIFO. The assertion of this signal signifies that the IMR+ device is requesting the use of the DAT and JAM lines for the transfer of repeated data or collision status to other IMR+ devices.

$\overline{RST}$

Reset
Input, Active LOW

Driving this pin LOW resets the internal logic of the IMR+ device. Reset should be synchronized to the X_1 clock if either expansion or port activity monitor is used.

$RXD+_{0–7}$, $RXD–_{0–7}$

Receive Data
Input

10BASE-T port differential receive inputs (8 ports).

SCLK

Serial Clock
Input

In normal operating mode, serial data (input or output) is clocked (in or out) on the rising edge of the signal on this pin. SCLK is asynchronous to X_1 and can operate up to 10 MHz. In Minimum mode, this pin, together with the SI pin, controls which information is output on the SO pin.

SI

Serial In
Input

In normal operating mode, the SI pin is used for test/management serial input port. Management commands are clocked in on this pin synchronous to the SCLK input. In Minimum mode, this pin, together with the SCLK pin, controls which information is output on the SO pin.

In Minimum mode, the state of SI at the deassertion of $\overline{RST}$ signal determines the programming of automatic polarity detection/correction for 10BASE-T ports.

SO

Serial Out
Output

In normal operating mode, the SO pin is used for test/management serial output port. Management results are clocked out on this pin synchronous to the SCLK input. In Minimum mode, the SO pin is used to serially output the various status information based on the state of the SI and SCLK pins.

SCLK	SI	SO Output
0	0	TP Ports Receive Polarity Status + AUI SQE Test Error Status
0	1	Bit Rate Error (all ports)
1	0	TP Ports Link Status + AUI Loopback Status
1	1	Port Partitioning Status (all ports)

STR

Store
Input/Output

As an output, this pin goes HIGH for two X_1 clock cycle times after the nine carrier sense bits are output on the CRS pin. Note that the carrier sense signals arriving from each port are latched internally, so that an active transition is remembered between samples. The accuracy of the carrier sense signals produced in this manner is 10 bit times (1 μs).

When used in conjunction with the HIMIB device, the STR pin will be configured as an input automatically after a hardware reset. The HIMIB device uses this input to communicate with the IMR+ device. When used with the HIMIB chip, this pin must be pulled up via a high-value resistor.

TEST

Test Pin
Input, Active HIGH

This pin should be tied LOW for normal operation. If this pin is driven HIGH, then the IMR+ device can be programmed for Loopback Test mode. Also, if this pin is HIGH when the $\overline{RST}$ pin is deasserted, the IMR+ device will enter the Minimum mode. An inverted version of the $\overline{RST}$ signal can be used to program the device into the Minimum mode.

Test	SI	Functions
0	0	Normal Management Mode
0	1	Normal Management Mode
1	0	Minimum Mode, Receive Polarity Correction Disabled
1	1	Minimum Mode, Receive Polarity Correction Enabled

$TXD+_{0–7}, TXD–_{0–7}$

Transmit Data Output

10BASE-T port differential drivers (8 ports).

$TXP+_{0–7}, TXP–_{0–7}$

Transmit Predistortion Output

10BASE-T transmit waveform predistortion control differential outputs (8 ports).

X_1

Crystal 1 Crystal Connection

The internal clock generator uses a 20 MHz crystal attached to pins X_1 and X_2. Alternatively, an external 20MHz CMOS clock signal can be used to drive this pin.

X_2

Crystal 2 Crystal Connection

The internal clock generator uses a 20 MHz crystal attached to pins X_1 and X_2. If an external clock source is used, this pin should be left unconnected.

FUNCTIONAL DESCRIPTION

The Am79C981 Integrated Multiport Repeater Plus device is a single chip implementation of an IEEE 802.3/Ethernet repeater (or hub). In addition to the eight integral 10BASE-T ports plus one AUI port comprising the basic repeater, the IMR+ chip also provides the hooks necessary for complex network management and diagnostics. The IMR+ device is also expandable, enabling the implementation of high port count repeaters based on several IMR+ devices.

The IMR+ device interfaces directly with AMD's Am79C987 Hardware Implemented Management Information Base (HIMIB) device to allow a fully managed multiport repeater to be implemented as specified by the Layer Management for 10 Mb/s Baseband Repeaters Standard. When the IMR+ and HIMIB devices are used as a chip set, the HIMIB device maintains complete repeater and per port statistics which can be accessed on demand by a microprocessor through a simple 8-bit parallel port.

The IMR+ chip complies with the full set of repeater basic functions as defined in section 9 of ISO 8802.3 (ANSI/IEEE 802.3c). These functions are summarized below.

Repeater Function

If any single network port senses the start of a valid packet on its receive lines, then the IMR+ device will retransmit the received data to all other enabled network ports. The repeated data will also be presented on the DAT line to facilitate multiple-IMR+ device repeater applications.

Signal Regeneration

When re-transmitting a packet, the IMR+ device ensures that the outgoing packet complies with the 802.3 specification in terms of preamble structure, voltage amplitude, and timing characteristics. Specifically, data packets repeated by the IMR+ chip will contain a minimum of 56 preamble bits before the Start of Frame Delimiter. In addition, the voltage amplitude of the repeated packet waveform will be restored to levels specified in the 802.3 specification. Finally, signal symmetry is restored to data packets repeated by the IMR+ device, removing jitter and distortion caused by the network cabling.

Jabber Lockup Protection

The IMR+ chip implements a built-in jabber protection scheme to ensure that the network is not disabled due to transmission of excessively long data packets. This protection scheme will automatically interrupt the transmitter circuits of the IMR+ device for 96-bit times if the IMR+ device has been transmitting continuously for more than 65,536-bit times. This is referred to as MAU Jabber Lockup Protection (MJLP). The MJLP status for the IMR+ chip can be read through the Management Port using the Get MJLP Status command (M bit returned).

Collision Handling

The IMR+ chip will detect and respond to collision conditions as specified in 802.3. A multiple-IMR+ device repeater implementation also complies with the 802.3 specification due to the inter-IMR+ chip status communication provided by the expansion port. Specifically, a repeater based on one or more IMR+ devices will handle the transmit collision and one-port-left collision conditions correctly as specified in Section 9 of the 802.3 specification.

Fragment Extension

If the total packet length received by the IMR+ device is less than 96 bits, including preamble, the IMR+ chip will extend the repeated packet length to 96 bits by appending a Jam sequence to the original fragment.

Auto Partitioning/Reconnection

Any of the integral TP ports and AUI port can be partitioned under excessive duration or frequency of collision conditions. Once partitioned, the IMR+ device will continue to transmit data packets to a partitioned port, but will not respond (as a repeater) to activity on the partitioned port's receiver. The IMR+ chip will monitor the port and reconnect it once certain criteria indicating port 'wellness' are met. The criteria for reconnection are specified by the 802.3 standard. In addition to the standard reconnection algorithm, the IMR+ device implements an alternative reconnection algorithm which provides a more robust partitioning function for the TP ports and/or the AUI port. Each TP port and the AUI port are partitioned and/or reconnected separately and independently of other network ports.

Either one of the following conditions occuring on any enabled IMR+ device network port will cause the port to partition:

a. A collision condition exists continuously for a time between 1024- to 2048-bit times (AUI port—SQE signal active; TP port—simultaneous transmit and receive)

b. A collision condition occurs during each of 32 consecutive attempts to transmit to that port.

Once a network port is partitioned, the IMR+ device will reconnect that port if the following is met:

a. Standard reconnection algorithm—A data packet longer than 512-bit times (nominal) is transmitted or received by the partitioned port without a collision.

b. Alternate reconnection algorithm—A data packet longer than 512-bit times (nominal) is transmitted by the partitioned port without a collision.

The reconnection algorithm option (standard or alternate) is a global function for the TP ports, i.e. all TP ports use the same reconnection algorithm. The AUI reconnection algorithm option is programmed independently of the TP port reconnection option.

Link Test

The integral TP ports implement the Link Test function as specified in the 802.3 10BASE-T standard. The IMR+ device will transmit Link Test pulses to any TP port after that port's transmitter has been inactive for more than 8 to 17 ms. Conversely, if a TP port does not receive any data packets or Link Test pulses for more than 65 to 132 ms and the Link Test function is enabled for that port then that port will enter link fail state. A port in link fail state will be disabled by the IMR+ chip (repeater transmit and receive functions disabled) until it receives either four consecutive Link Test pulses or a data packet. The Link Test receive function itself can be disabled via the IMR+ chip management port on a port-by-port basis to allow the IMR+ device to interoperate with pre-10BASE-T twisted pair networks that do not implement the Link Test function. This interoperability is possible because the IMR+ device will not allow the TP port to enter link fail state, even if no Link Test pulses or data packets are being received. Note however that the IMR+ chip will always transmit Link Test pulses to all TP ports regardless of whether or not the port is enabled, partitioned, in link fail state, or has its Link Test receive function disabled.

Polarity Reversal

The TP ports have the optional (programmable) ability to invert (correct) the polarity of the received data if the TP port senses that the received data packet waveform polarity is reversed due to a wiring error. This receive circuitry polarity correction allows subsequent packets to be repeated with correct polarity. This function is executed once following reset or link fail, and has a programmable enable/disable option on a port-by-port basis. This function is disabled upon reset and can be enabled via the IMR+ chip Management Port.

Reset

The IMR+ device enters reset state when the $\overline{RST}$ pin is driven LOW. After the initial application of power, the $\overline{RST}$ pin must be held LOW for a minimum of 150 µs (3000 X1 clock cycles). If the $\overline{RST}$ pin is subsequently asserted while power is maintained to the IMR+ device, a reset duration of only 4 µs is required. The IMR+ chip continues to be in the reset state for 10 X1 clocks (0.5 µs) following the rising edge of $\overline{RST}$. During reset, the output signals are placed in their inactive states. This means that all analog signals are placed in their idle states, bidirectional signals (except STR signal) are not driven, active LOW signals are driven HIGH, and all active HIGH signals and the STR pin are driven LOW.

An internal circuit ensures that a minimum reset pulse is generated for all internal circuits. For a $\overline{RST}$ input with a slow rising edge, the input buffer threshold may be crossed several times due to ripple on the input waveform.

In a multiple IMR+ chip repeater the $\overline{RST}$ signal should be applied simultaneously to all IMR+ devices and should be synchronized to the external X1 clock. Reset synchronization is also required when accessing the PAM (Port Activity Monitor).

The SI signal should be held HIGH for at least 500 ns following the rising edge of $\overline{RST}$.

Table 1 summarizes the state of the IMR+ chip following reset.

Table 1. IMR+ Chip After Reset

Function	State After Reset	Pull Up/Pull Down
Active LOW outputs	HIGH	No
Active HIGH outputs	LOW	No
SO Output	HIGH	No
DAT, JAM	HI-IMPEDANCE	Either
STR	LOW	Pull Up*
Transmitters (TP and AUI)	IDLE	No
Receivers (TP and AUI)	ENABLED	Terminated
AUI Partitioning/Reconnection Algorithm	STANDARD ALGORITHM	N/A
TP Port Partitioning/Reconnection Algorithm	STANDARD ALGORITHM	N/A
Link Test Function for TP Ports	ENABLED, TP PORTS IN LINK FAIL	N/A
Automatic Receiver Polarity Reversal Function	DISABLED	N/A

**Only when used with the HIMIB device.*

Expansion Port

The IMR+ chip Expansion Port is comprised of five pins; two are bi-directional signals (DAT and JAM), two are input signals ($\overline{ACK}$ and $\overline{COL}$), and one is an output signal ($\overline{REQ}$). These signals are used when a multiple-IMR+ device repeater application is employed. In this configuration, all IMR+ chips must be clocked synchronously with a common clock connected to the X1 inputs of all IMR+ devices. Reset needs to be synchronized to X1 clock.

The IMR+ device expansion scheme allows the use of multiple IMR+ chips in a single board repeater or a modular multiport repeater with a backplane architecture. The DAT pin is a bidirectional I/O pin which can be used to transfer data between the IMR+ devices in a multiple-IMR+ chip design. The data sent over the DAT line is in NRZ format and is synchronized to the common clock. The JAM pin is another bidirectional I/O pin that is used by the active IMR+ chip to communicate its internal status to the remaining (inactive) IMR+ devices. When JAM is asserted HIGH, it indicates that the active IMR+ device has detected a collision condition and is generating Jam Sequence. During this time when JAM is asserted HIGH, the DAT line is used to indicate whether the active IMR+ chip is detecting collision on one port only or on more than one port. When DAT is driven HIGH by the IMR+ chip (while JAM is asserted by the IMR+ chip), then the active IMR+ device is detecting a collision condition on one port only. This 'one-port-left' signaling is necessary for a multiple-IMR+ device repeater to function correctly as a single multiport repeater unit. The IMR+ chip also signals the 'one port left' collision condition in the event of a runt packet or collision fragment; this signal will continue for one expansion port bus cycle (100 ns) before deasserting $\overline{REQ}$.

The arbitration for access to the bussed bi-directional signals (DAT and JAM) is provided by one output ($\overline{REQ}$) and two inputs ($\overline{ACK}$ and $\overline{COL}$). The IMR+ chip asserts the $\overline{REQ}$ pin to indicate that it is active and wishes to drive the DAT and JAM pins. An external arbiter senses the $\overline{REQ}$ lines from all the IMR+ devices and asserts the $\overline{ACK}$ line when one and only one IMR+ chip is asserting its $\overline{REQ}$ line. If more than one IMR+ chip is asserting its $\overline{REQ}$ line, the arbiter must assert the $\overline{COL}$ signal, indicating that more than one IMR+ device is active. More than one active IMR+ device at a time constitutes a collision condition, and all IMR+ devices are notified of this occurence via the $\overline{COL}$ line of the Expansion Port.

Note that a transition from multiple IMR+ devices arbitrating for the DAT and JAM pins (with $\overline{COL}$ asserted, $\overline{ACK}$ deasserted) to a condition when only one IMR+ chip is arbitrating for the DAT and JAM pins (with $\overline{ACK}$ asserted, $\overline{COL}$ deasserted) involves one expansion port bus cycle (100 ns). During this transitional bus cycle, $\overline{COL}$ is deasserted, $\overline{ACK}$ is asserted, and the DAT and JAM pins are not driven. However, each IMR+ device will remain in the collision state (transmitting jam sequence) during this transitional bus cycle. In subsequent expansion port bus cycles ($\overline{REQ}$ and $\overline{ACK}$ still asserted), the IMR+ devices will return to the 'master and slaves' condition where only one IMR+ device is active (with collision) and is driving the DAT and JAM pins. An understanding of this sequence is crucial if non-IMR+ devices (such as an Ethernet controller) are connected to the expansion bus. Specifically, the last device to back off of the Expansion Port after a multi-IMR+ chip collision must assert the JAM line until it too drops its request for the Expansion Port.

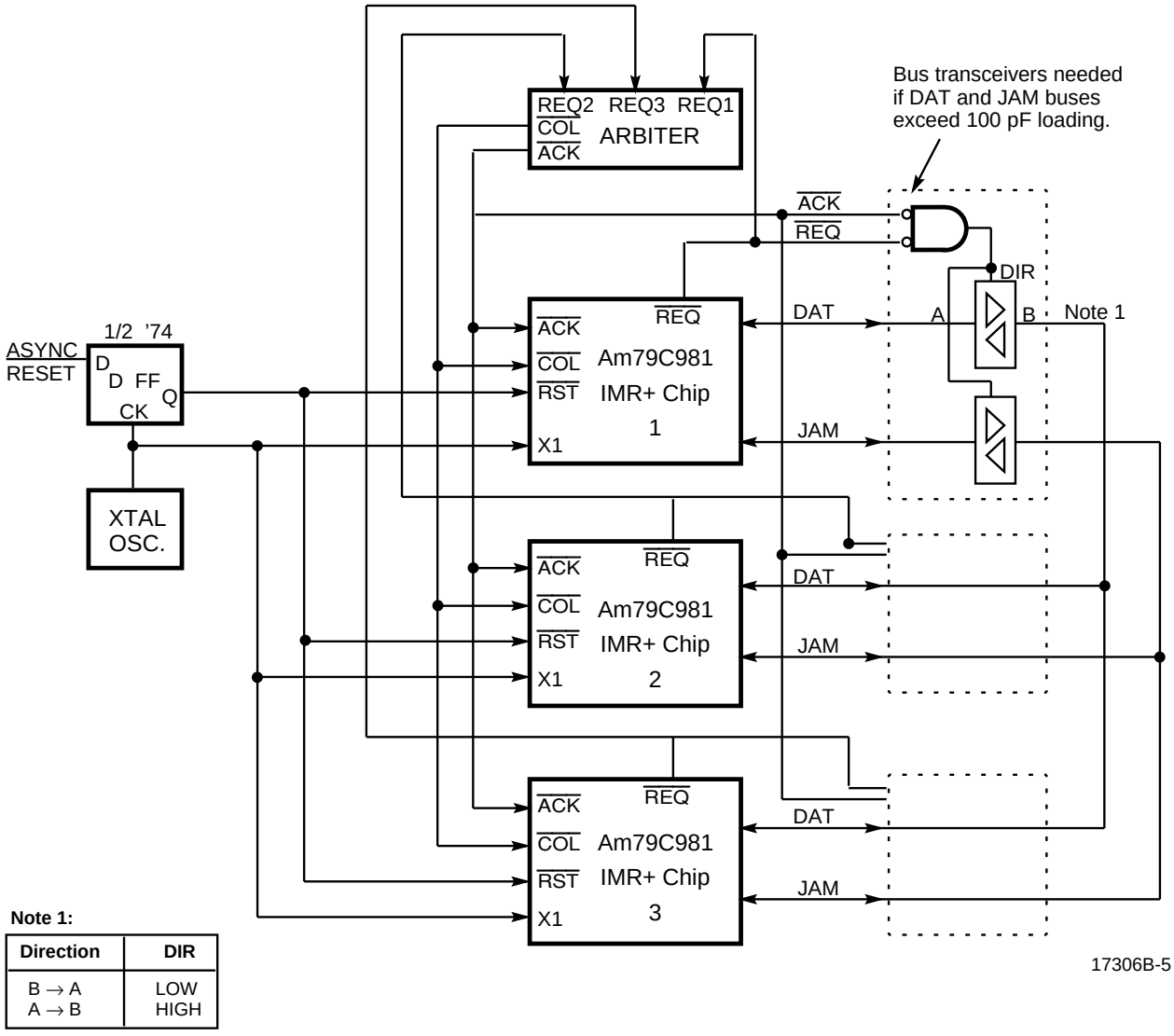
External Arbiter

A simple arbitration scheme is required when multiple IMR+ devices are connected together to increase the total number of repeater ports. The arbiter should have one input ($\overline{REQ1}$...$\overline{REQn}$) for each of the n IMR+ devices to be used, and two global outputs ($\overline{COL}$ and $\overline{ACK}$). This function is easily implemented in a PAL® device, with the following logic equations:

$$\begin{aligned}
ACK &= \overline{REQ1} \,\&\, \overline{REQ2} \,\&\, \overline{REQ3} \,\&\, ... \overline{REQn} \\
&+ \overline{REQ1} \,\&\, REQ2 \,\&\, \overline{REQ3} \,\&\, ... \overline{REQn} \\
&\quad \bullet \\
&\quad \bullet \\
&\quad \bullet \\
&+ \overline{REQ1} \,\&\, \overline{REQ2} \,\&\, \overline{REQ3} \,\&\, ... \; REQn \\
COL &= \overline{ACK} \,\&\, (REQ1 + REQ2 + REQ3 + ... \; REQn)
\end{aligned}$$

Above equations are in positive logic, i.e., a variable is true when asserted.

A single PALCE16V8 will perform the arbitration function for a repeater based on several IMR+ devices.



Note 1:

Direction	DIR
B → A	LOW
A → B	HIGH

Figure 1. Multiple IMR+ Devices

Modular Repeater Design

The expansion port of the IMR+ chip also allows for modular expansion. By sharing the arbitration duties between a backplane bus architecture and several separate repeater modules one can build an expandable repeater based on modular 'plug-in' cards. Each repeater module performs the local arbitration function for the IMR+ devices on that module, and provides signals to the backplane for use by a global arbiter.

For more detailed information, see AMD's IEEE 802.3 Repeater Technical Manual, PID# 17314A.

Repeater MAC Interconnection

Because all repeated data in the IMR+ chip or multi-IMR+ chip design is available on the Expansion Port, all network traffic can be monitored by an external Media Access Controller (MAC) device such as the Am7990, Am79C900, Am79C940, or Am79C960. A repeater with such a controller is capable of providing extensive hub management functions, as well as being addressable as a network node. The MAC device can gather statistics and data concerning the state of the hub and the network, and the network addressability allows a remote management station to monitor this statistical data and to request actions to be performed by the repeater (i.e. port enable/disable).

Figure 2 shows how to interface a repeater based on multiple IMR+ devices to an Ethernet controller such as the Am79C900 ILACC or the Am7990 LANCE. For more information on this design, refer to AMD's IEEE 802.3 Repeater Technical Manual, PID# 17314A.

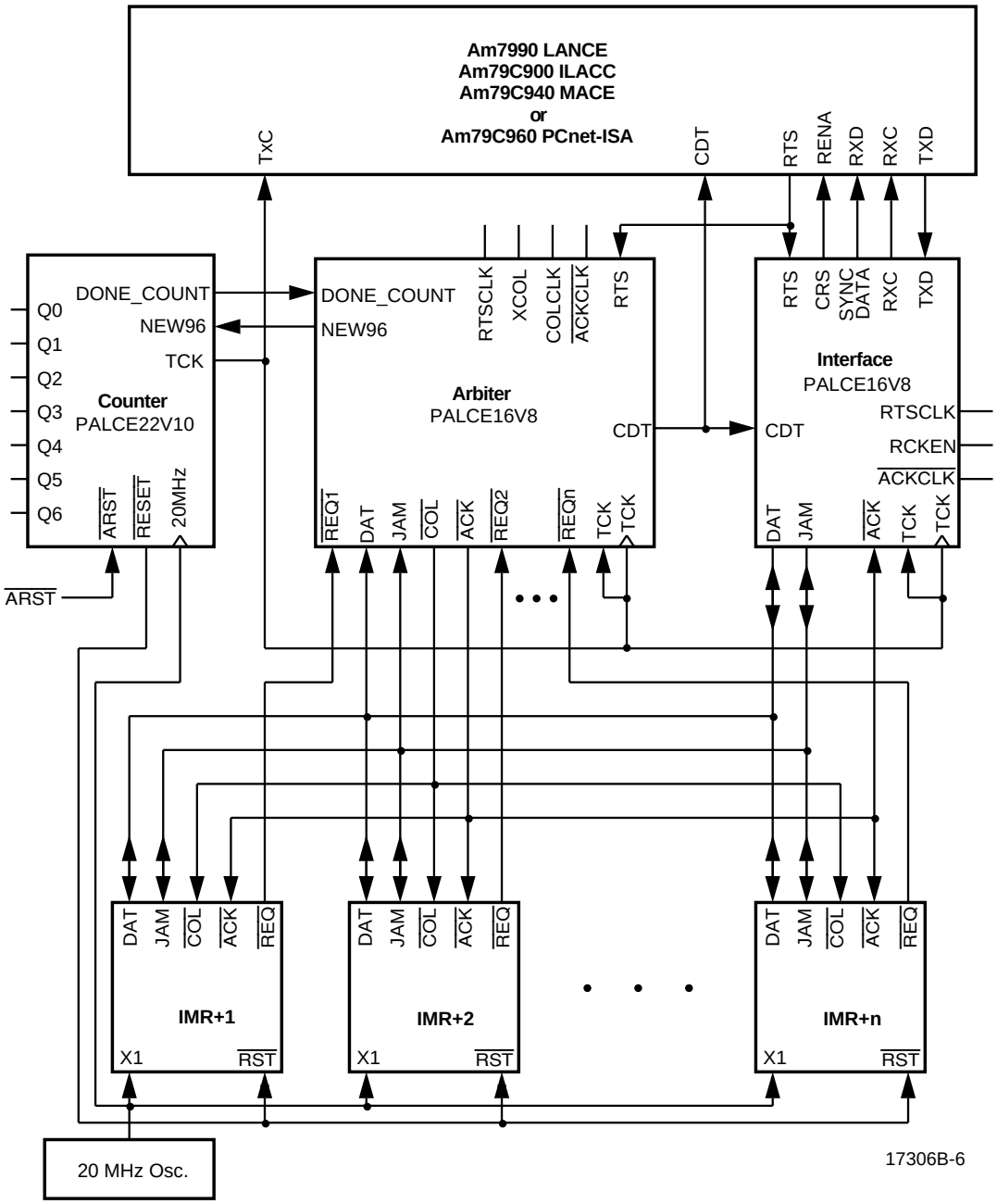


Figure 2. Expandable Modular Repeater

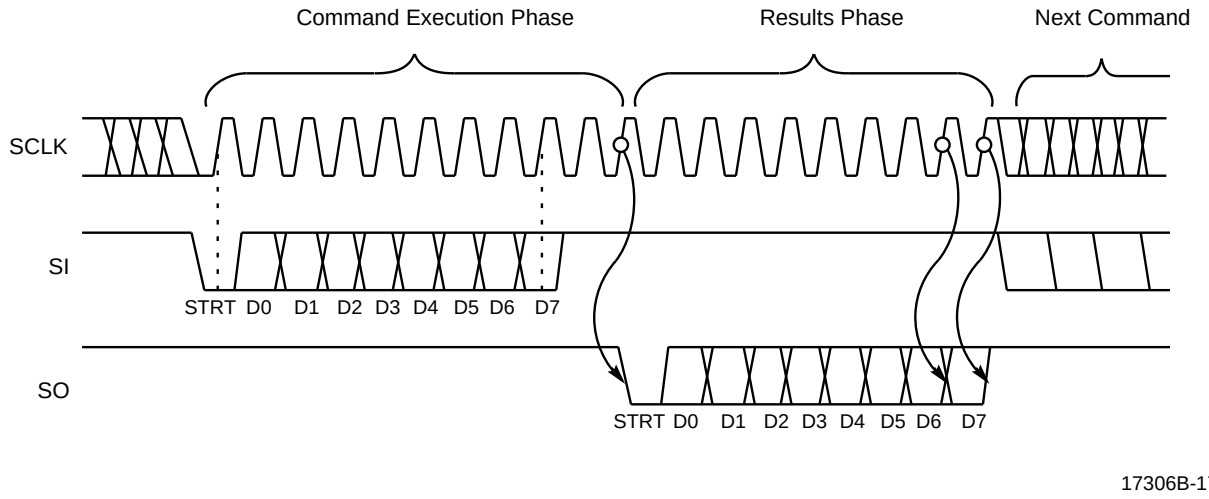
Management Port

The IMR+ device management functions are enabled when the TEST pin is tied LOW. The management commands are byte oriented data and are input serially on the SI pin. Any responses generated during execution of a management command are output serially in a byte-oriented format by the IMR+ device on the SO pin. Both the input and output data streams are clocked with the rising edge of the SCLK pin. The serial command data stream and any associated results data stream are structured in a manner similar to the RS232 serial data format, i.e., one Start Bit followed by eight Data Bits.

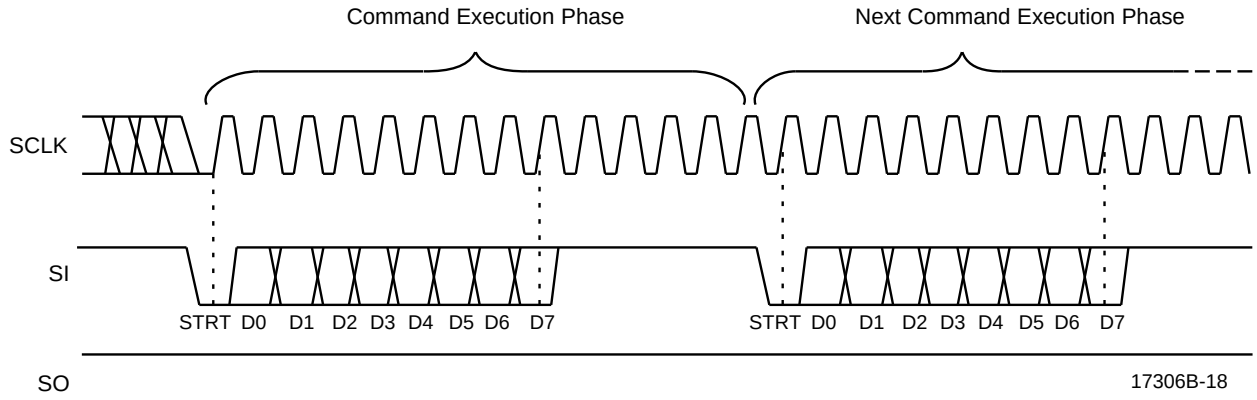
The externally generated clock at the SCLK pin can be either a free running clock synchronized to the input bit patterns or a series of individual transitions meeting the setup and hold times with respect to the input bit pattern. If the latter method is used, it is to be noted that 20 SCLK clock transitions are required for proper execution of management commands that produce SO data, and that 14 SCLK clock transitions are needed to execute management commands that do not produce SO data.

Management Commands

The following section details the operation of each management command available in the IMR+ chip. In all cases, the individual bits in each command byte are shown with the MSB on the left and the LSB on the right. Data bytes are received and transmitted LSB first and MSB last. See Table 2 for a summary of the management commands.



Management Command/Response Timing



Management Command Timing with No Response

Table 2. Management Port Command Summary

Commands	SI Data	SO Data
Set (Write) Opcodes		
IMR+ Chip Programmable Options	0000 1CSA	
Alternate AUI Partitioning Algorithm	0001 1111	
Alternate TP Partitioning Algorithm	0001 0000	
AUI Port Disable	0010 1111	
AUI Port Enable	0011 1111	
TP Port Disable	0010 0###	
TP Port Enable	0011 0###	
Disable Link Test Function (per TP port)	0100 0###	
Enable Link Test Function (per TP port)	0101 0###	
Disable Automatic Receiver Polarity Reversal (per TP port)	0110 0###	
Enable Automatic Receiver Polarity Reversal (per TP port)	0111 0###	
Get (Read) Opcodes		
AUI Port Status (B, S, L Cleared)	1000 1111	PBSL 0000
TP Port Partitioning Status	1000 0000	C7...C0
Bit Rate Status of TP ports	1010 0000	E7...E0
Link Test Status of TP ports	1101 0000	L7...L0
Receive Polarity Status of all TP ports	1110 0000	P7...P0
MJLP Status	1111 0000	M000 0000
Version	1111 1111	XXXX 0001
AUI Port Status (S, L Cleared)	1000 1011	PBSL 0000
AUI Port Status (B Cleared)	1000 1101	PBSL 0000
AUI Port Status (None Cleared)	1000 1001	PBSL 0000

Notes:

1. *Unused opcodes are reserved for future use.*
2. *### is the port number (000 to 111 for TP0 to TP7)*

SET (Write) Opcodes

IMR+ Chip Programmable Options

SI data: 0000 1CSA

SO data: None

IMR+ Chip Programmable Options can be enabled (disabled) by setting (resetting) the appropriate bit in the command string. The three programmable bits are: **C**—CI Reporting; **S—**AUI SQE Test Mask, and **A**—Alternative Port Activity Monitor (PAM) Function. These options can be enabled (disabled) by setting (resetting) the appropriate bit in the command string.

When writing to this register through the Am79C987 HIMIB device, the A and C bits should not be changed (A=0, C=1).

C—CI Reporting

Setting this bit alters the function of the STR pin. In this mode, the STR pin becomes an input in response to the AMD's Am79C987 HIMIB device. Upon deassertion of $\overline{RST}$, the HIMIB automatically sets this bit following IMR/IMR+ device type detection.

When this mode is selected, the CRS output bit string format is modified to include CI carrier bit (in addition to AUI carrier). This bit occupies the bit position immediately preceding the AUI bit in the CRS bit string (10 bits) output. Note that the AUI bit gets asserted if either the CI or DI signal pairs are active.

S—AUI SQE Test Mask

Setting this bit allows the IMR+ chip to ignore activity on the CI signal pair, in the SQE Test Window, following a transmission on the AUI port. This event occurs when the attached MAU has the SQE Test option enabled, therefore generating a burst of CI activity following every transmission. This is interpreted by the IMR+ device as a collision, causing the IMR+ device to generate a full Jam pattern. Although the MAU attached to a repeater is required not to have its SQE test function active, this is a common installation error, causing difficulty in diagnosing network throughput problems.

The SQE Test Window, as defined by the IEEE 802.3 (Section 7.2.2.2.4), is from 6-bit times to 34-bit times (0.6 μs to 3.4 μs). This includes delay introduced by a 50 m AUI. CI activity that occurs outside this window is not ignored and is treated as true collision.

Note that enabling this function does not prevent the reporting of this condition by the IMR+ device and the two functions operate independently.

A—Alternative Port Activity Monitor (PAM) Function

Setting the Alternative Port Activity Monitor Function allows the PAM function to be altered such that the Carrier Sense data is presented unmodified. In default operation the PAM output (Carrier Sense bits in the CRS bit stream) are masked if the port is either disabled or partitioned. This does not allow the Repeater Management software to sense activity on all segments at all times. The ability to monitor partitioned or disabled ports allows fault tolerance to be built into the Repeater Management software.

Alternate AUI Port Partitioning Algorithm

SI data: 00011111
SO data: None

The AUI port Partitioning/Reconnection scheme can be programmed for the alternate (transmit only) reconnection algorithm by invoking this command. To return the AUI back to the standard (transmit or receive) reconnection algorithm, it is necessary to reset the IMR+ device. Standard partitioning algorithm is selected upon reset.

Alternate TP Ports Partitioning Algorithm

SI data: 00010000
SO data: None

The TP ports Partitioning/Reconnection scheme can be programmed for the alternate (transmit only) reconnection algorithm by invoking this command. All TP ports are affected as a group by this command. To return the TP ports back to the standard (transmit or receive) reconnection algorithm, it is necessary to reset the IMR+ device. The standard partitioning algorithm is selected upon reset.

AUI Port Disable

SI data: 00101111
SO data: None

The AUI port will be disabled upon receiving this command. Subsequently, the IMR+ chip will ignore all inputs (Carrier Sense and SQE) appearing at the AUI port and will not transmit any data or Jam Sequence on the AUI port. Issuing this command will also cause the AUI port to have its internal partitioning state machine forced to its idle state. Therefore, a Partitioned Port may be reconnected by first disabling and then re-enabling the port.

AUI Port Enable

SI data: 00111111
SO data: None

This command enables a previously disabled AUI port. Note that a partitioned AUI port may be reconnected by first disabling (AUI Port Disable Command) and then re-enabling the port with this command.

All ports are enabled upon reset.

TP Port Disable

SI data: 00100###
SO data: None

(### is TP port number)

The TP port designated in the command byte will be disabled upon receiving this command. Subsequently, the IMR+ device will ignore all inputs appearing at the disabled port's receive pins and will not transmit any data or JAM Sequence on that port's transmit pins. Issuing this command will also cause a TP port to have its partitioning state machine returned to its Idle State (Port Reconnected). Therefore, a partitioned port may be reconnected by first disabling and then re-enabling the port. The disabled port will continue to report correct Link Test Status.

TP Port Enable

SI data: 00110###
SO data: None

(### is TP port number)

This command enables a previously disabled TP port. Re-enabling a disabled port causes the port to be placed into Link Test Fail state. This ensures that packet fragments received on the port are not repeated to the rest of the network. Note that to force a TP port into the Link Fail state and/or to reconnect a partitioned TP port, the port should first be disabled (TP Port Disable Command) and then re-enabled with this command. All ports are enabled upon reset.

Disable Link Test Function of a TP Port

SI data: 01000###
SO data: None

(### is TP port number)

This command disables the Link Test Function at the TP port designated in the command byte, i.e., the TP port will no longer be disconnected due to Link Fail. A TP port which has its Link Test Function disabled will continue to transmit Link Test Pulses. If a twisted pair port has Link Test disabled, then reading the Link Test Status indicates it being in Link Test Pass.

Enable Link Test Function of a TP Port

SI data: 01010###
SO data: None

(### is TP port number)

This command re-enables the Link Test Function in the TP port designated in the command byte. This command executes only if the designated TP port has had the Link Test Function disabled by the Disable Link Test Function command. Otherwise, the command is ignored. Link Test is enabled upon reset.

Disable Automatic Receiver Polarity Reversal

SI data: 01100###
SO data: None

(### is TP port number)

This command disables the Automatic Receiver Polarity Reversal Function for the TP port designated in the command byte. If this function is disabled on a TP port with reverse polarity (due to a wiring error), then the TP port will fail Link Test due to the reversed polarity of the Link Pulses. If the Link Test Function is also disabled on the TP port, then the received reversed polarity packets would be repeated to all other network ports in the IMR+ chip as inverted data. Automatic Polarity reversal is disabled upon reset.

Enable Automatic Receiver Polarity Reversal

SI data: 01110###
SO data: None

(### is TP port number)

This command enables the Automatic Receiver Polarity Reversal Function for the TP port designated in the command byte. If enabled in a TP port, the IMR+ chip will automatically invert the polarity of that TP port's receiver circuitry if the TP port is detected as having reversed polarity (due to a wiring error). After reversing the receiver polarity, the TP port could then receive subsequent (reverse polarity) packets correctly.

GET (Read) Opcodes

AUI Port Status

SI data: 10001111
SO data: PBSL0000

The combined AUI status allows a single instruction to be used for monitoring AUI port. The four status bits reported are:

P Partitioning Status. This bit is 0 if the AUI port is partitioned and 1 if connected.

B Bit Rate Error. This bit is set to 1 if there has been an instance of FIFO Overflow or Underflow, caused by data received at the AUI port. This bit is cleared when the status is read.

S SQE Test Status. This bit is set to 1 if SQE Test is detected by the IMR+ chip. This bit is cleared when the status is read. A MAU attached to a repeater must have SQE Test disabled. This bit is set even if the AUI port is disabled or partitioned.

L Loop Back Error. The MAU attached to the AUI is required to loopback data transmitted to DO onto the DI circuit. If loopback carrier is not detected by the IMR+ device, then this bit is set to 1 to report this condition. This bit is cleared when the status is read. For a repeater this is the only indication of a broken or missing MAU.

Alternate AUI Port Status

SI data: 10001111
SO data: PBSL0000

There are three further variations of the above command, allowing selective clearing of a combination of B, S, and L bits. They are primarily included for use by the HIMIB chip. These are:

Alternative 1.

SI data: 10001011
SO data: PBSL0000

B is not cleared. S and L are cleared.

Alternative 2.

SI data: 10001101
SO data: PBSL0000

S and L are not cleared. B is cleared.

Alternative 3.

SI data: 10001001
SO data: PBSL0000

None of S, B and L are cleared.

TP Port Partitioning Status

SI data: 10000000
SO data: P7.....P0

Pn = 0 TP port n partitioned

Pn = 1 TP port n connected

The partitioning Status of all eight TP ports are accessed by this command. If a port is disabled, reading it partitioning status will indicate that it is connected.

Bit Rate Error Status of TP Ports

SI data: 10100000
SO data: E7.....E0

This allows a single command to be used to report Bit Rate Error condition (FIFO Overflow or Underflow) of all Twisted Pair ports. The 8 bits of the output pattern correspond to each of the 8 TP ports, with least significant bit corresponding to port 0.

The status bit for a port is set to 1 if there has been an instance when data received from that port has caused a FIFO error.

All status bits stay set until the status is read.

Link Test Status of TP Ports

SI data: 11010000
SO data: L7.....L0

Ln = 0 TP Port n in Link Test Fail
Ln = 1 TP Port n in Link Test Pass

The Link Test Status of all eight TP ports are accessed by this command. A disabled port continues to report correct Link Test Status. Re-enabling a disabled port causes the port to be placed into Link Test Fail state. This ensures that packet fragments received on the port are not repeated to the rest of the network.

Receive Polarity Status of TP Ports

SI data: 11100000
SO data: P7.....P0

Pn = 0 TP Port n Polarity Correct
Pn = 1 TP Port n Polarity Reversed

The statuses of all eight TP port polarities are accessed with this command. The IMR+ chip has the ability to detect and correct reversed polarity on the TP ports' RXD+/– pins. If the polarity is detected as reversed for a TP port, then the IMR+ chip will set the appropriate bit in this command's result byte only if the Polarity Reversal Function is enabled for that port.

MJLP Status

SI data: 11110000
SO data: M00000000

Each IMR+ chip contains an independent MAU Jabber Lock Up Protection Timer. The timer is designed to inhibit the IMR+ device transmit function, if it has been transmitting continuously for more than 65536 Bit Times. The MJLP Status bit (M) is set to 1 if this happens. This bit remains set and is only cleared when the MJLP status is read by using this command.

Version

SI data: 11111111
SO data: XXXX0001

This command (1111 1111) can be used to determine the device version.

The IMR+ chip responds by the bit pattern: XXXX 0001

The IMR chip (Am79C980) responds by the bit pattern: XXXX 0000

Minimum Mode

The Minimum Mode reconfigures the IMR+ device Management Port and is intended to provide support for the low end, non-managed repeaters, requiring minimal external logic to provide LED indication of:

- Twisted Pair Ports Link Status indication and AUI Loopback Status
- Port Partitioning Status
- Twisted Pair Ports Receiver Polarity Status and AUI SQE Test Error Status
- Port Bit Rate Error Status

The Minimum Mode is selected by controlling the state of the TEST pin while $\overline{RST}$ is asserted. If TEST is High (asserted), while reset is active ($\overline{RST}$ LOW), then Minimum Mode is selected. The state of SI pin, at the deassertion of the $\overline{RST}$ signal, determines whether the IMR+ chip is to be programmed for Automatic Polarity Detection/Correction.

When entering the Minimum Mode, the TEST input has to be deasserted on the rising edge of reset. A maximum delay of 100 ns is allowed to account for slow devices. The following table summarizes the different modes available.

Test	SI	Functions
0	0	Normal Management Mode
0	1	Normal Management Mode
1	0	Minimum Mode, Receive Polarity Correction disabled
1	1	Minimum Mode, Receive Polarity Correction enabled

In Minimum Mode, the SO pin is used to serially output the various status information based on the state of the SI and SCLK pins. A summary of the status information is provided in the following table.

SCLK	SI	SO Output
0	0	TP Ports Receive Polarity Status + AUI SQE Test Error Status.
0	1	Bit Rate Error (all ports).
1	0	TP Ports Link Status + AUI LoopBack Status
1	1	Port Partitioning Status (all ports)

When SI = 0 then SO will output the related AUI status bits (LoopBack or SQE), followed by the 8 TP status bits (Link or Polarity), starting with the TP port 0.

When SI = 1, the Port Partitioning Status or Port Bit Rate Error Status are scanned out with the AUI first and TP ports following. TP Port 0 is scanned out first.

Note that the Bit Rate Error, AUI Loopback, and AUI SQE Test Error status bits stay set until they are scanned out.

The state of SI and SCLK inputs is checked at the end of every STR cycle. The rising edge of the X1 clock, occurring before falling edge of STR, is used to strobe in the state of the SI and SCLK pins.

In this Minimum Mode, the Management Port mode is not active. To exit the Minimum mode, the IMR+ device must reset into the normal Management Port mode.

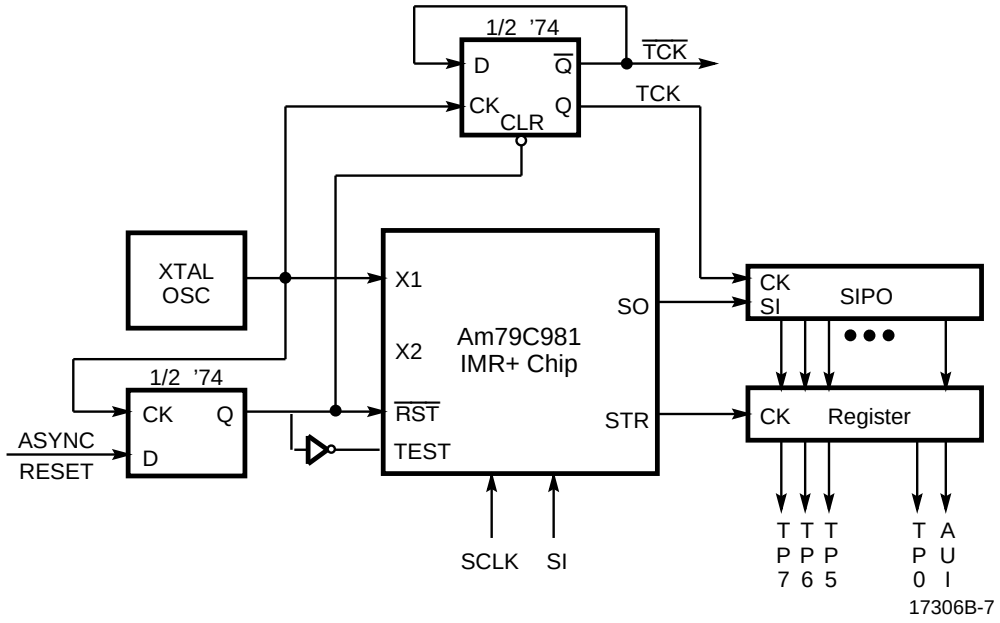
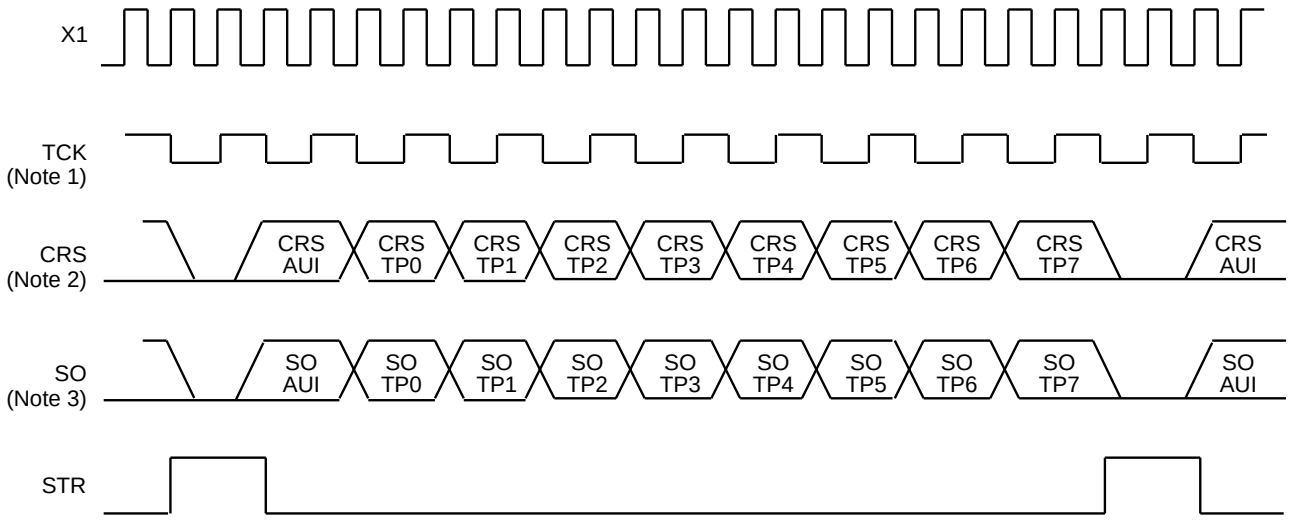


Figure 3. Minimum Mode, Non-Intelligent Repeater Example



Notes:

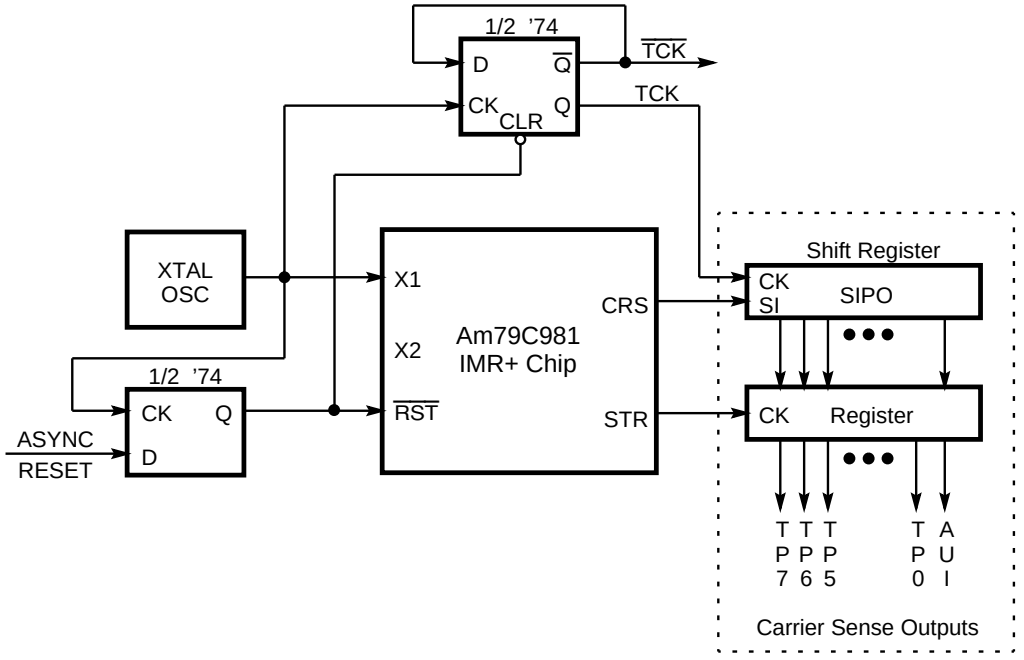
1. *Externally generated signal illustrates internal IMR+ chip clock phase relationship.*
2. *CRS timing with the C-bit cleared (IMR+ Chip Programmable Options)*
3. *For Minimum Hub Mode*

Figure 4. Management Port Minimum Mode and Port Activity Monitor Signal Relationship

Port Activity Monitor

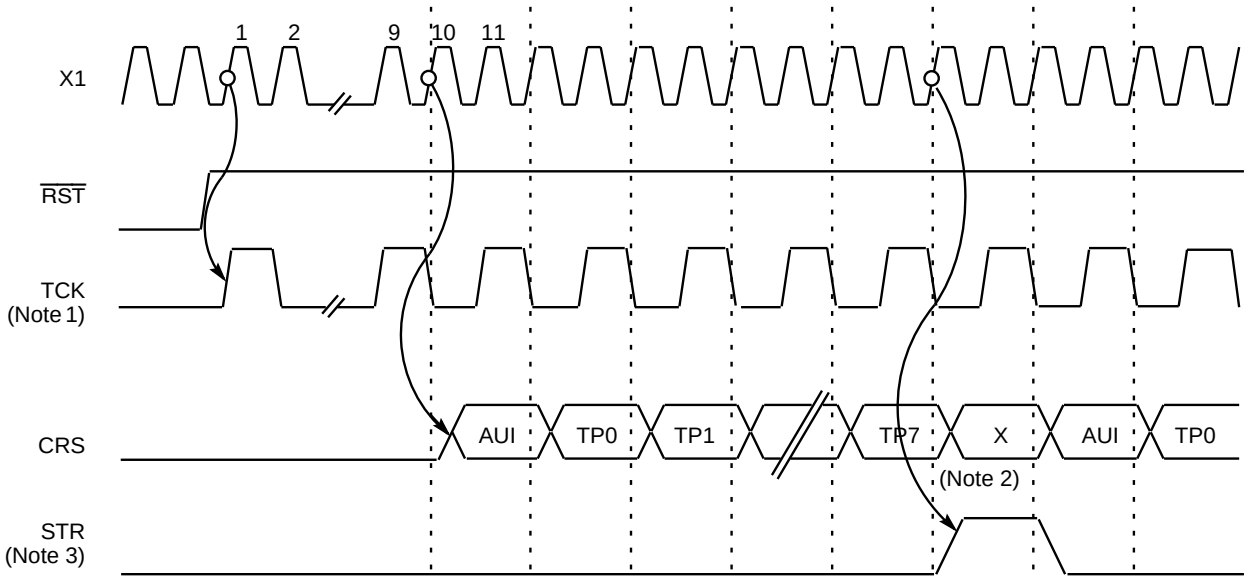
Two pins, CRS and STR, are used to serially output the state of the internal Carrier Sense signals from the AUI and the eight TP ports. This function together with external hardware and/or software can be used to monitor repeater receive and/or collision activity.

The following diagram shows typical external hardware employed to convert the serial bit stream into parallel form. The accuracy of the CRS signals is 10 Bit Times (BT) (1 µs). Specifically, a transition to active state by any of the internal carrier sense bits that lasts for less than 10BT is latched internally and is used to set the appropriate bit during the next sample period.



17306B-9

Figure 5a. Port Activity Monitor Implementation



17306B-10

Notes:

1. *Externally generated signal illustrates internal IMR+ chip clock phase relationship.*
2. *IMR+ chip standalone, X will be low. When attached to a HIMIB device, X reflects the state of the CI pair.*
3. *STR signal is not available when the IMR+ chip is attached to HIMIB device, and must be generated externally.*

Figure 5b. Port Activity Monitor Implementation (Continued)

Loopback Test Mode

The IMR+ chip can be programmed to enter Loopback Mode on all network ports. This is accomplished by first driving the TEST pin HIGH, then clocking (using the SCLK pin) a minimum of three 0s into the SI pin. This causes the IMR+ chip to loop all received data on each port back to each port's corresponding transmit outputs. Specifically, the AUI DI input is passed unaltered to the AUI DO output, and each RXD input on the twisted pair ports is passed (unaltered) to the respective TXD and TXP outputs. Only receive data that passes the required amplitude squelch criteria is looped back to the transmit outputs. Note that the data is looped back unaltered, meaning that no signal retiming or regeneration takes place. Therefore, any signal distortion present on the receive data paths will be retransmitted.

In Minimum Mode, the Loopback Test Mode cannot be accessed. The IMR+ device will return to normal operation when the TEST pin is again driven LOW.

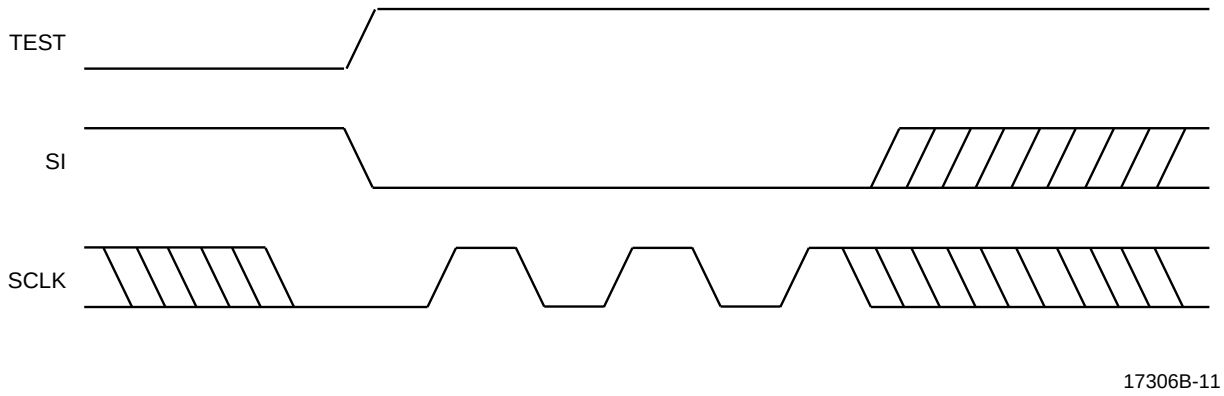
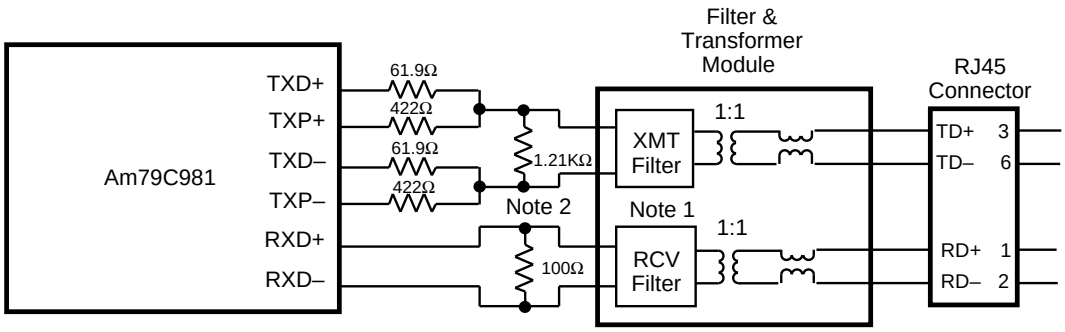


Figure 6. Programming the IMR+ Device for Loopback Mode

IMR+ Chip External Components

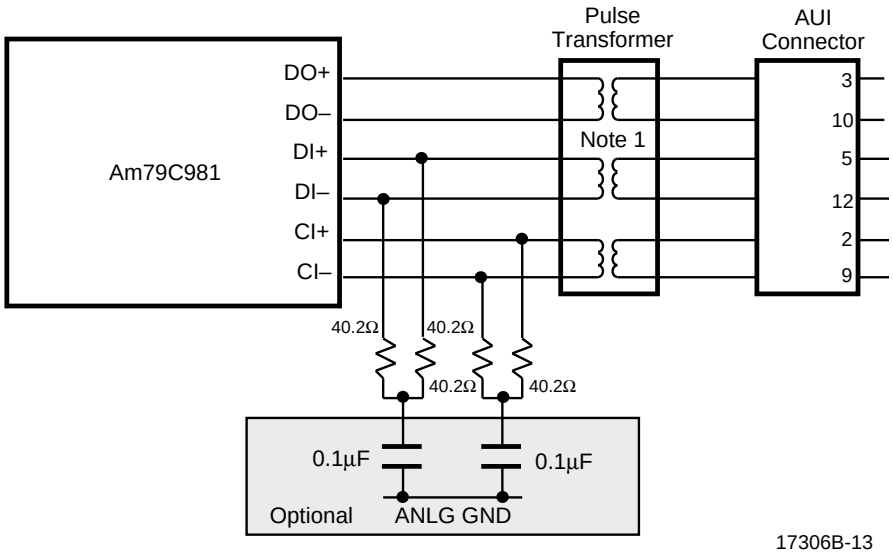
Figure 6 shows a typical twisted pair port external components schematic. The resistors used should have a 1% tolerance to ensure interoperability with 10BASE-T compliant networks. The filters and pulse transformers are necessary devices that have a major influence on the performance and compliance of the 10BASE-T ports of the repeater. Specifically, the transmitted waveforms are heavily influenced by the filter characteristics and the twisted pair receivers employ several criteria to continuously monitor the incoming signal's amplitude and timing characteristics to determine when and if to assert the internal carrier sense. For these reasons, it is crucial that the values and tolerances of the external components be as specified. Several manufacturers produce a module that combines the functions of the transmit and receive filters and the pulse transformers into one package.



Notes:

1. *Compatible filter modules, with a brief description of package type and features are included in the Appendix.*
2. *The resistor values are recommended for general purpose use and should allow compliance to the 10BASE-T specification for template fit and jitter performance. However, the overall performance of the transmitter is also affected by the transmit filter configuration.*

Figure 7a. Typical TP Port External Components



Notes:

1. *Compatible AUI transformer modules, with a brief description of package type and features are included in the Appendix.*
2. *The differential input DI± and the CI± pairs are externally terminated by two 40.2 Ω ±1% resistors and one optional common-mode bypass capacitor. The differential input impedance, ZIDF, and the common-mode input impedance, ZICM, are specified so that the Ethernet specification for cable termination impedance is met using standard 1% resistor terminators. If SIP devices are used, 39 Ω is the nearest usable equivalent value.*

Figure 7b. Typical AUI Port Components

APPLICATIONS

A fully managed multiport repeater can be easily built by interfacing the IMR+ chip with the Hardware Implemented Management Information Base (HIMIB), Am79C987 device. The HIMIB device interfaces with all common Microprocessor System Busses with a minimum of external logic. Note that additional buffering of DAT and JAM are required for most applications. For more information, refer to AMD's IEEE 802.3 Repeater Technical Manual (PID# 17314A).

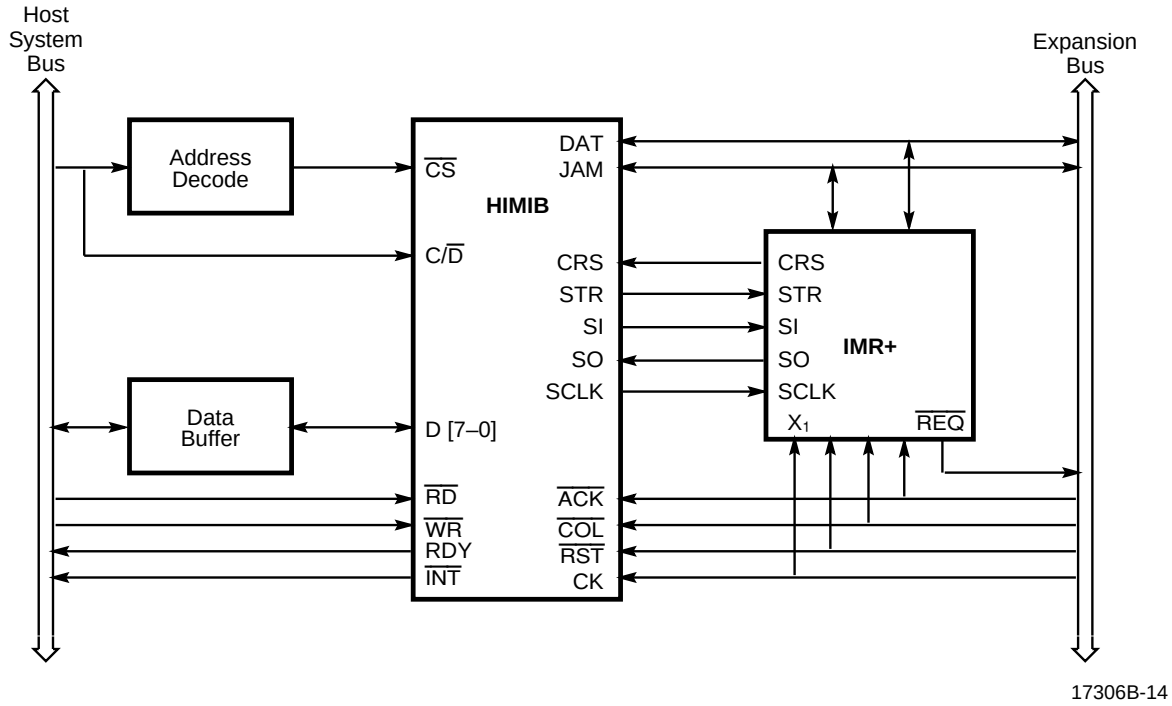


Figure 8. Simplified ISA-HUB Block Diagram

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature Under Bias . . . . . 0 to 70°C

Supply Voltage referenced to
AV_{SS} or DV_{SS} (AV_{DD}, DV_{DD}) . . . . . –0.3 to +6 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) . . . . . 0 to +70°C

Supply Voltage (AV_{DD}, DV_{DD}) . . . . . 5 V to ±5%

Operating ranges define those limits between which the functionality of the device is guaranteed

.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
Digital I/O					
V_{IL}	Input LOW Voltage	DV_{SS} = 0.0 V	–0.5	0.8	V
V_{IH}	Input HIGH Voltage		2.0	DV_{DD}+0.5	V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA	–	0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = –0.4 mA	2.4	–	V
I_{IL}	Input Leakage Current (also DAT and JAM as inputs)	$DV_{SS}<V_{IN}<DV_{DD}$	–	10	µA
V_{ILX}	X_1 Crystal Input LOW Voltage	DV_{SS} = 0.0 V	–0.5	1.0	V
V_{IHX}	X_1 Crystal Input HIGH Voltage	DV_{SS} = 0.0 V	3.8	DV_{DD}+0.5	V
I_{ILX}	Crystal Input LOW Current	$V_{IN} = DV_{SS}$	–	10	µA
I_{IHX}	Crystal Input HIGH Current	$V_{IN} = DV_{DD}$	–	10	µA
AUI Port					
I_{IAXD}	Input Current at DI+/- and CI+/- pairs	$AV_{SS} < V_{IN} < AV_{DD}$	–500	+500	µA
V_{AICM}	DI+,DI-,CI+,CI- Open Circuit Input Common Mode Voltage (bias)	I_{IN} = 0A, AV_{SS} = 0 V	AV_{DD} – 3.0	AV_{DD}–1.0	V
V_{AIDV}	Differential Mode Input Voltage Range (DI, CI)	AV_{DD} = 5.0 V	–2.5	+2.5	V
V_{ASQ}	DI, CI Squelch Threshold		–275	–160	mV
V_{ATH}	DI Switching Threshold	(Note 1)	–35	+35	mV
V_{AOD}	Differential Output Voltage |(DO+) – (DO-)|	R_L = 78 Ω	620	1100	mV
V_{AODI}	DO Differential Output Voltage Imbalance	R_L = 78 Ω	–25	+25	mV
V_{AOD}OFF	DO Differential Idle Output Voltage	R_L = 78 Ω	–40	+40	mV
I_{AOD}OFF	DO Differential Idle Output Current	R_L = 78 Ω (Note 1)	–1	+1	mA
V_{AOCM}	DO+/- Common Mode Output Voltage	R_L = 78 Ω	2.5	AV_{DD}	V

DC CHARACTERISTICS (continued)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
Twisted Pair Ports					
I_{IRXD}	Input current at RXD+/-	$AV_{SS}<V_{IN}<AV_{DD}$	–500	+500	µA
R_{RXD}	RXD differential input resistance	(Note 1)	10	–	KΩ
V_{TIVB}	RXD+,RXD- open circuit input voltage (bias)	I_{IN} = 0 mA	AV_{DD}–3.0	AV_{DD}–1.5	V
V_{TID}	Differential Mode input voltage range (RXD)	AV_{DD} = 5.0 V	–3.1	+3.1	V
V_{TSQ+}	RXD positive squelch threshold (peak)	Sinusoid 5 MHz <f< 10 MHz	300	520	mV
V_{TSQ-}	RXD negative squelch threshold (peak)	Sinusoid 5 MHz <f< 10 MHz	–520	–300	mV
V_{THS+}	RXD post-squelch positive threshold (peak)	Sinusoid 5 MHz <f< 10 MHz	150	293	mV
V_{THS-}	RXD post-squelch negative threshold (peak)	Sinusoid 5 MHz <f< 10 MHz	–293	–150	mV
V_{RXDTH}	RXD switching threshold	(Note 1)	–60	+60	mV
V_{TXH}	TXD+/- and TXP+/- output HIGH voltage	DV_{SS} = 0 V (Note 2)	DV_{DD}–0.6	DV_{DD}	V
V_{TXL}	TXD+/- and TXP+/- output LOW voltage	DV_{DD} = 5 V (Note 2)	DV_{SS}	DV_{SS}+0.6	V
V_{TXI}	TXD+/- and TXP+/- differential output voltage imbalance		–40	+40	mV
V_{TXOFF}	TXD+/- and TXP+/- differential idle output voltage	DV_{DD} = 5 V	–	40	mV
R_{TXD}	TXD+/- differential driver output impedance	(Note 1)	–	40	Ω
R_{TXP}	TXP+/- differential driver output impedance	(Note 1)	–	80	Ω
Power Supply Current					
I_{DD}	Power supply current (idle)	f_{X1} = 20 MHz	–	180	mA
	Power supply current (transmitting – no TP load)	f_{X1} = 20 MHz	–	300	mA
	Power supply current (transmitting – with TP load)	f_{X1} = 20 MHz	–	(Note 8)	mA

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
Clock and Reset					
t_{X1}	X1 Clock Period		49.995	50.005	ns
t_{X1H}	X1 Clock HIGH		20	30	ns
t_{X1L}	X1 Clock LOW		20	30	ns
t_{X1R}	X1 Clock Rise Time		–	10	ns
t_{X1F}	X1 Clock Fall Time		–	10	ns
t_{PRST}	Reset pulse width after power on ($\overline{RST}$ pin LOW)		150	–	µs
t_{RST}	Reset pulse width ($\overline{RST}$ pin LOW)		4	–	µs
t_{RSTSET}	$\overline{RST}$ HIGH setup time with respect to X1 Clock		20	–	ns
t_{RSTHLD}	$\overline{RST}$ LOW hold time with respect to X1 Clock		0	–	ns
Management Port					
t_{SCLK}	SCLK Clock Period		100	–	ns
t_{SCLKH}	SCLK Clock HIGH		30	–	ns
t_{SCLKL}	SCLK Clock LOW		30	–	ns
t_{SCLKR}	SCLK Clock Rise Time		–	10	ns
t_{SCLKF}	SCLK Clock Fall Time		–	10	ns
t_{SISET}	SI input setup time with respect to SCLK rising edge		10	–	ns
t_{SIHLD}	SI input hold time with respect to SCLK rising edge		10	–	ns
t_{SODLY}	SO output delay with respect to SCLK rising edge	C_L = 100 pF	–	40	ns
t_{X1HCRS}	X1 rising edge to CRS valid	C_L = 100 pF	5	40	ns
t_{X1HSTH}	X1 rising edge to STR HIGH	C_L = 100 pF	–	40	ns
t_{X1HSTL}	X1 rising edge to STR LOW	C_L = 100 pF	–	40	ns
$t_{TESTSET}$	TEST input setup time with respect to SCLK rising edge		10	–	ns
$t_{TESTHLD}$	TEST input hold time with respect to SCLK rising edge		10	–	ns
t_{STRSET}	STR setup time		5	–	ns
t_{STRHLD}	STR hold time		12	–	ns
Expansion Port					
t_{X1HRL}	X1 rising edge to $\overline{REQ}$ driven LOW	C_L = 100 pF	14	40	ns
t_{X1HRH}	X1 rising edge to $\overline{REQ}$ driven HIGH	C_L = 100 pF	14	40	ns
t_{X1HDR}	X1 rising edge to DAT/JAM driven	C_L = 100 pF	14	40	ns
t_{X1HDZ}	X1 rising edge to DAT/JAM not driven	C_L = 100 pF	14	40	ns

SWITCHING CHARACTERISTICS (continued)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
Expansion Port (Continued)					
t_{DJSET}	DAT/JAM setup time		10	–	ns
t_{DJHOLD}	DAT/JAM hold time		14	–	ns
t_{CASET}	$\overline{COL}/\overline{ACK}$ setup time		5	–	ns
t_{CAHOLD}	$\overline{COL}/\overline{ACK}$ hold time		14	–	ns
t_{MHSET}	TEST setup time with respect to $\overline{RST}$ to enter Minimum Hub Mode		200	–	ns
t_{MHHLD}	TEST hold time with respect to $\overline{RST}$ to enter Minimum Hub Mode		0	100	ns
$t_{SCLKSET}$	SI, SCLK set up time with respect to X1		50	–	ns
$t_{SCLKHLD}$	SI, SCLK hold time with respect to X1		50	–	ns
AUI Port					
t_{DOTD}	X1 rising edge to DO toggle		–	30	ns
t_{DOTR}	DO+,DO- rise time (10% to 90%)		2.5	5.0	ns
t_{DOTF}	DO+,DO- fall time (90% to 10%)		2.5	5.0	ns
t_{DORM}	DO+,DO- rise and fall time mismatch		–	1.0	ns
t_{DOETD}	DO+/- End of Transmission		275	375	ns
t_{PWODI}	DI pulse width accept/reject threshold	$\|V_{IN}\| > \|V_{ASQ}\|$ (Note 3)	15	45	ns
t_{PWKDI}	DI pulse width maintain/turn-off threshold	$\|V_{IN}\| > \|V_{ASQ}\|$ (Note 4)	136	200	ns
t_{PWOCI}	CI pulse width accept/reject threshold	$\|V_{IN}\| > \|V_{ASQ}\|$ (Note 5)	10	26	ns
t_{PWKCI}	CI pulse width maintain/turn-off threshold	$\|V_{IN}\| > \|V_{ASQ}\|$ (Note 6)	90	160	ns
Twisted Pair Ports					
t_{TXTD}	X1 rising edge to TXD+,TXP+ TXD-,TXP- transition delay		–	50	ns
t_{TR}	TXD+,TXD-,TXP+,TXP- rise time		–	20	ns
t_{TF}	TXD+,TXD-,TXP+,TXP- fall time		–	20	ns
t_{TM}	TXD+,TXD-,TXP+,TXP- rise and fall time mismatch		–	6	ns
t_{TETD}	Transmit End of Transmission		275	375	ns
t_{PWKRD}	RXD pulse width maintain/turn-off threshold	$\|V_{IN}\| > \|V_{THS}\|$ (Note 7)	130	200	ns
t_{PERLP}	Idle signal period		8	24	ms
t_{PWLP}	Idle Link Test pulse width (TXD+)		75	120	ns
t_{PWPLP}	Idle Link Test pulse width (TXP+,TXP-)		40	60	ns

SWITCHING CHARACTERISTICS (continued)

Notes:

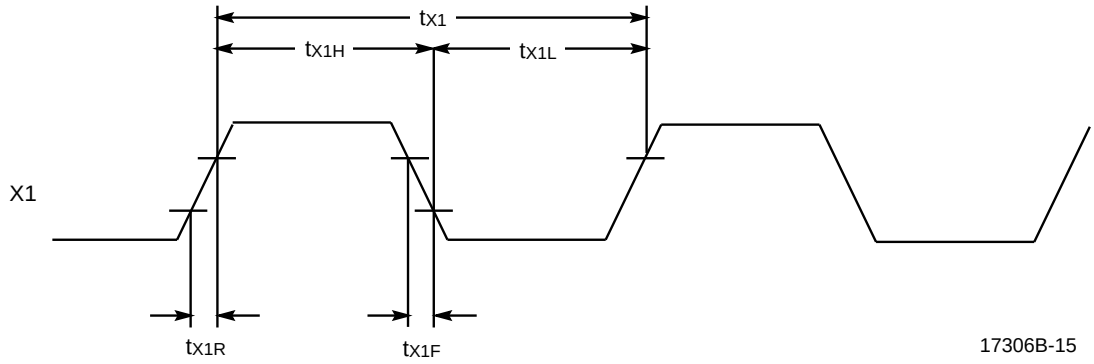
1. *Parameter not tested.*
2. *Uses switching test load.*
3. *DI pulses narrower than t_{PWODI} (min) will be rejected; pulses wider than t_{PWODI} (max) will turn internal DI carrier sense on.*
4. *DI pulses narrower than t_{PWKDI} (min) will maintain internal DI carrier sense on; pulses wider than t_{PWKDI} (max) will turn internal DI carrier sense off.*
5. *CI pulses narrower than t_{PWOCI} (min) will be rejected; pulses wider than t_{PWOCI} (max) will turn internal CI carrier sense on.*
6. *CI pulses narrower than t_{PWKCI} (min) will maintain internal CI carrier sense on; pulses wider than t_{PWKCI} (max) will turn internal CI carrier sense off.*
7. *RXD pulses narrower than t_{PWKRD} (min) will maintain internal RXD carrier sense on; pulse wider than t_{PWKRD} (max) will turn internal RXD carrier sense off.*
8. *For the typical twisted pair load as shown in Figure 7, using a 100 Ω cable, an additional 28 mA (max) of I_{DD} current is required for each twisted pair port used. Less than 18% of the power associated with this additional current is dissipated by the IMR+ chip; the remainder is dissipated externally in the twisted pair load and cable.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

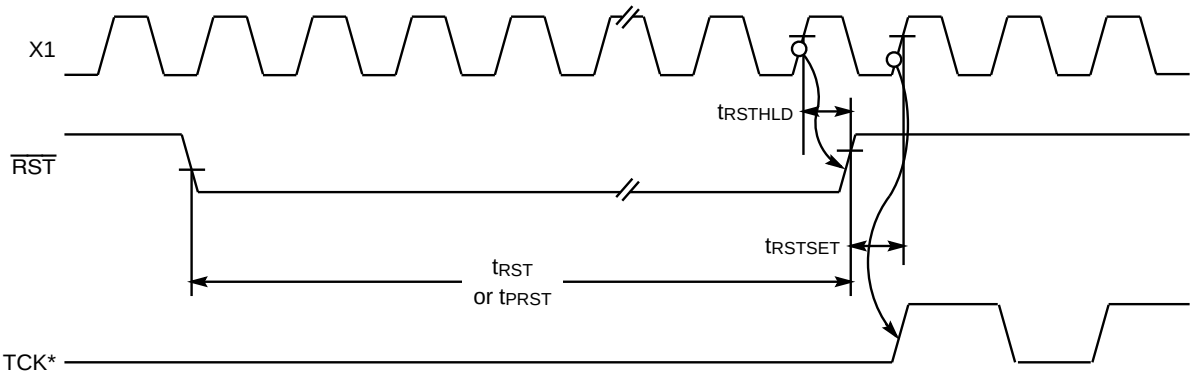
KS000010

SWITCHING WAVEFORMS



Clock Timing

SWITCHING WAVEFORMS

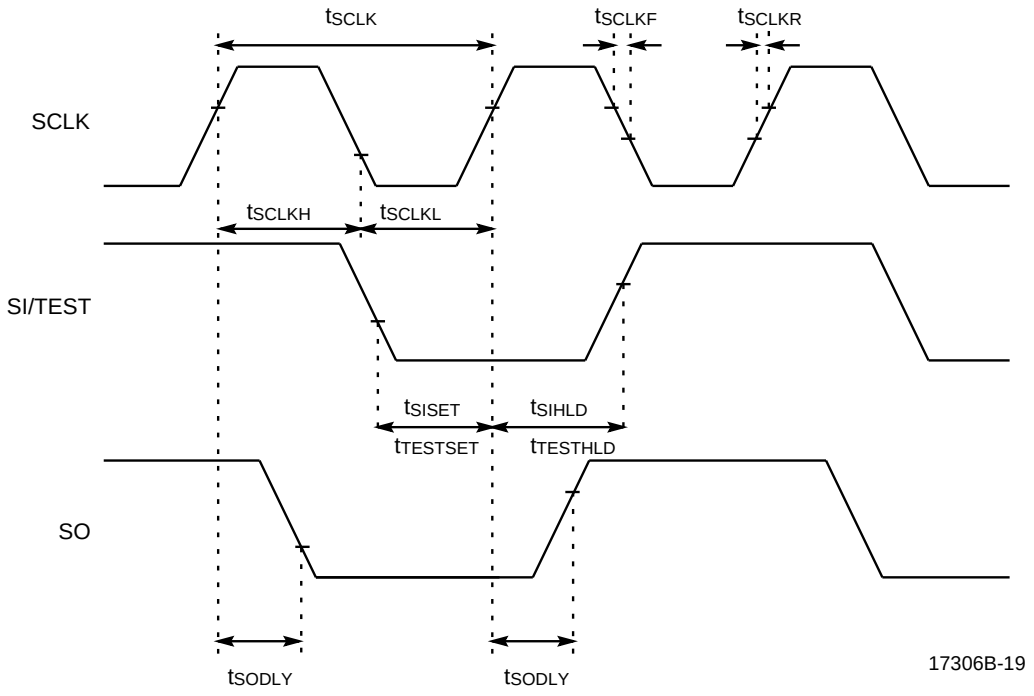


Notes:

t_{RSTSET} refers to synchronous Reset Timing.

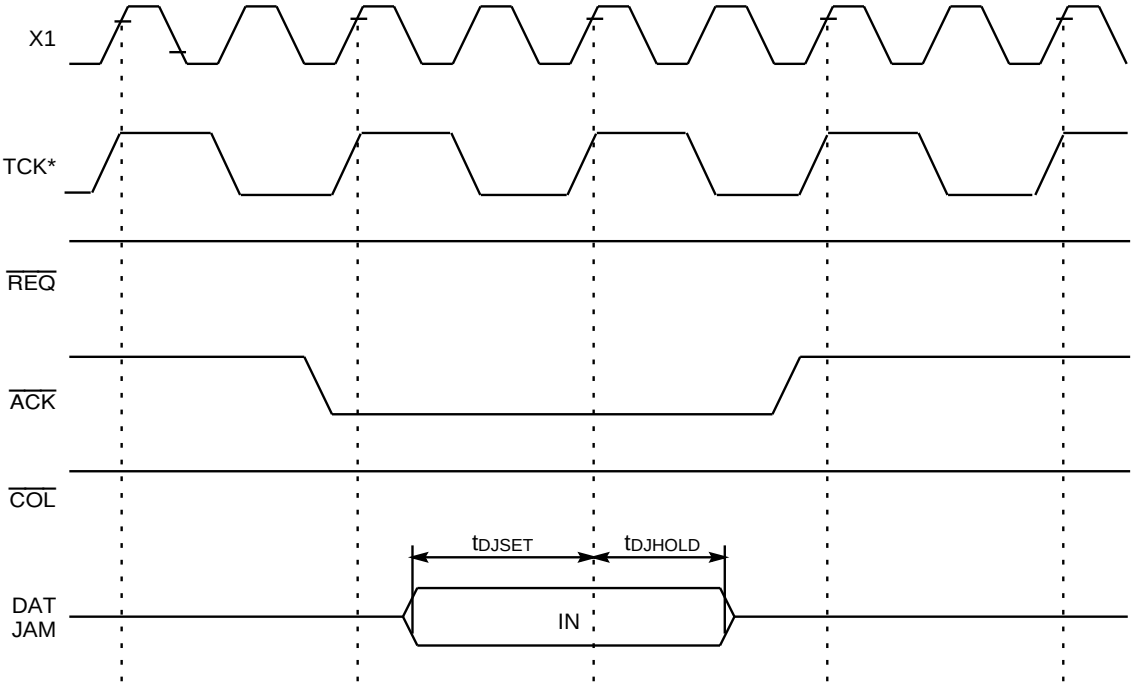
**Externally generated (Figure 4) signal illustrates internal IMR+ device clock phase relationships.*

Reset Timing



Management Port Clock Timing

SWITCHING WAVEFORMS

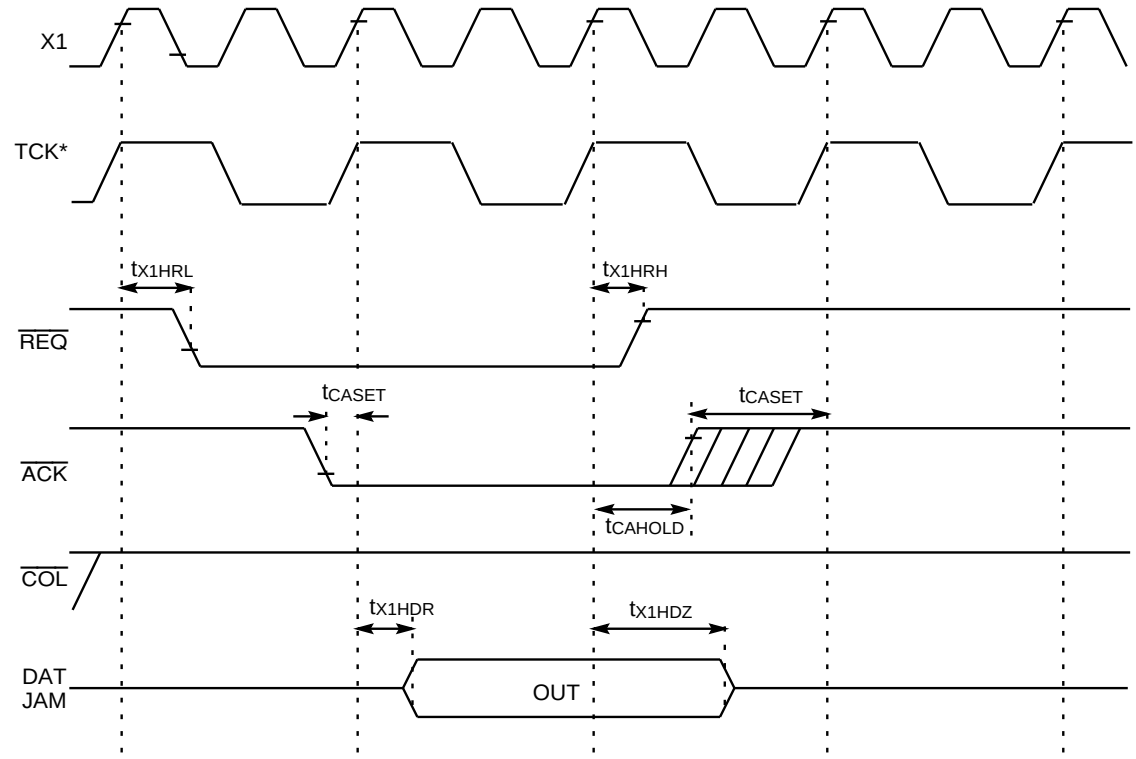


Note:

**Externally generated (Figure 4) signal illustrates internal IMR+ chip clock phase relationships.*

17306B-20

Expansion Port Input Timing



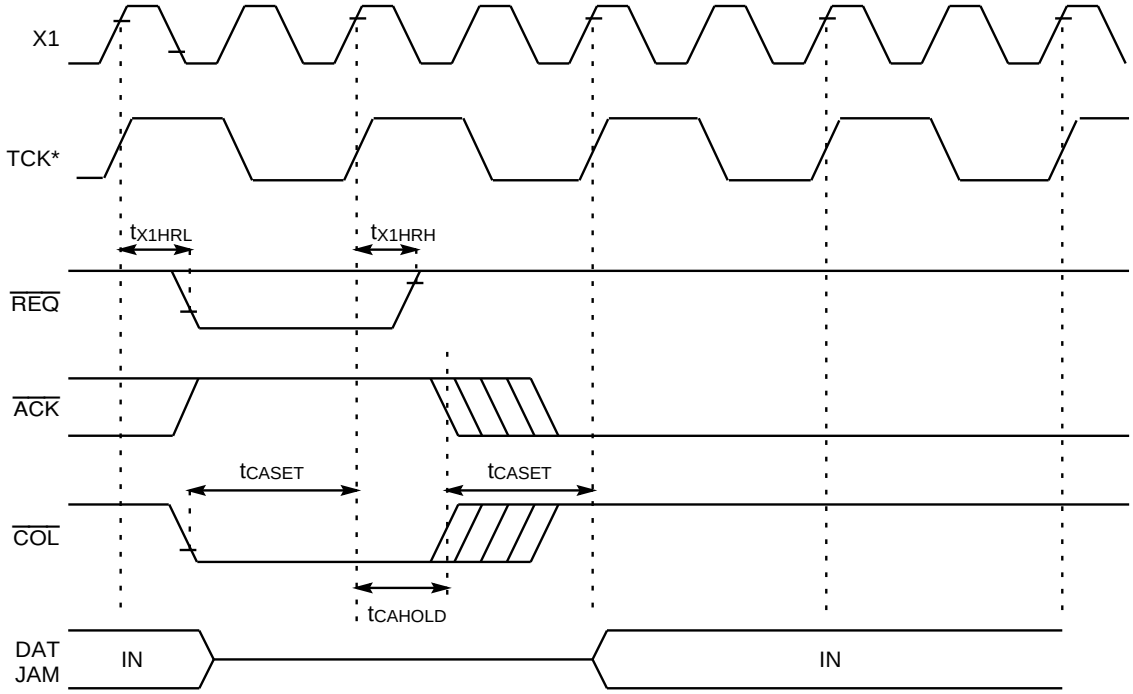
Note:

**Externally generated (Figure 4) signal illustrates internal IMR+ chip clock phase relationships.*

17306B-21

Expansion Port Output Timing

SWITCHING WAVEFORMS

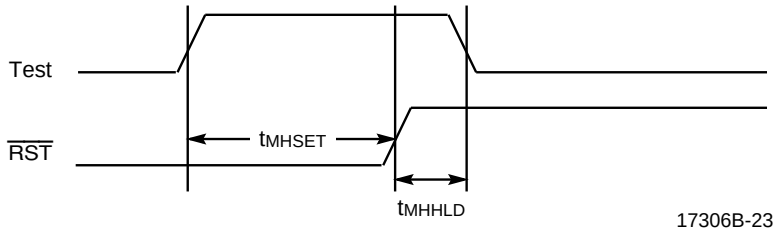


17306B-22

Note:

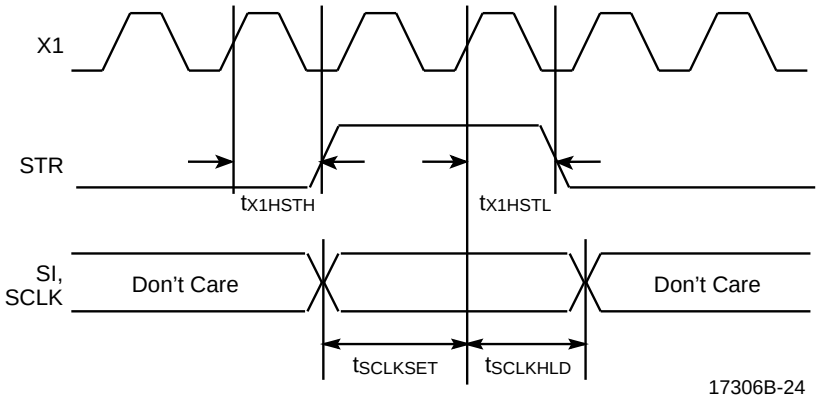
**Externally generated (Figure 4) signal illustrates internal IMR+ chip clock phase relationships.*

Expansion Port Collision Timing



17306B-23

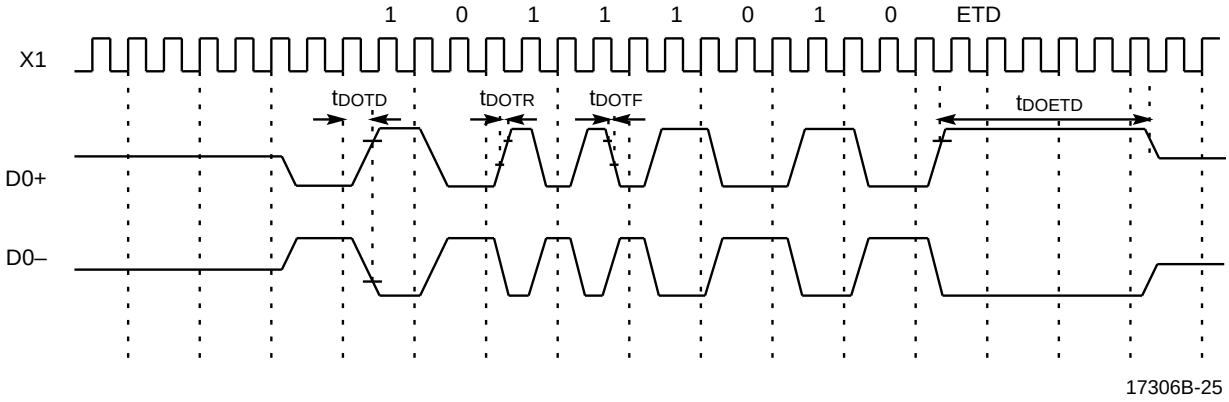
To Enter Minimum Mode



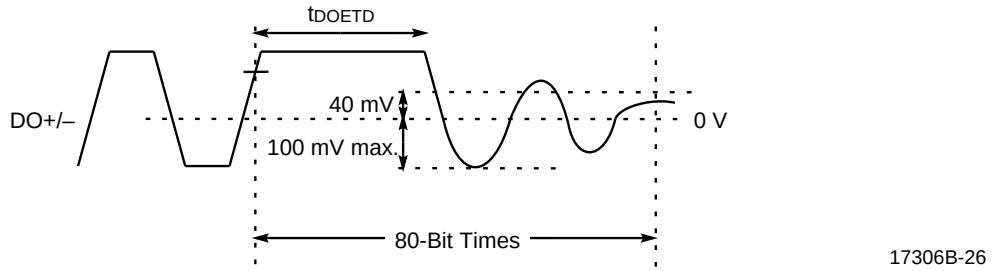
17306B-24

Minimum Mode

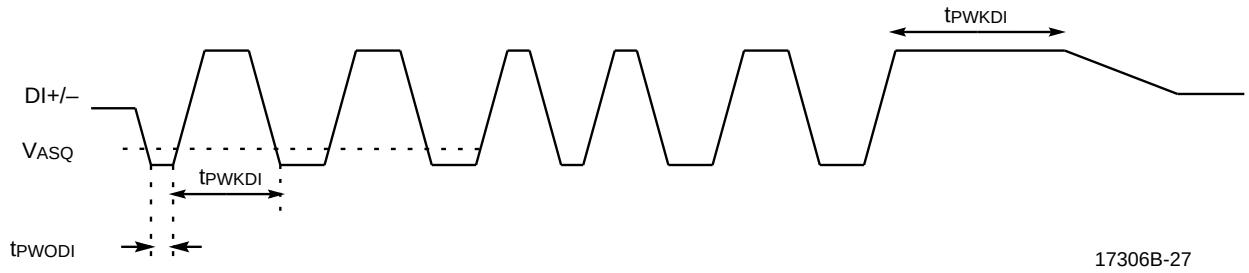
SWITCHING WAVEFORMS



AUI DO Timing Diagram

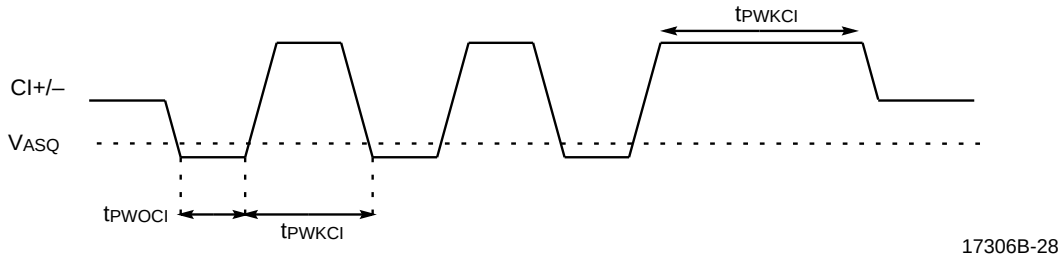


AUI Port DO ETD Waveform

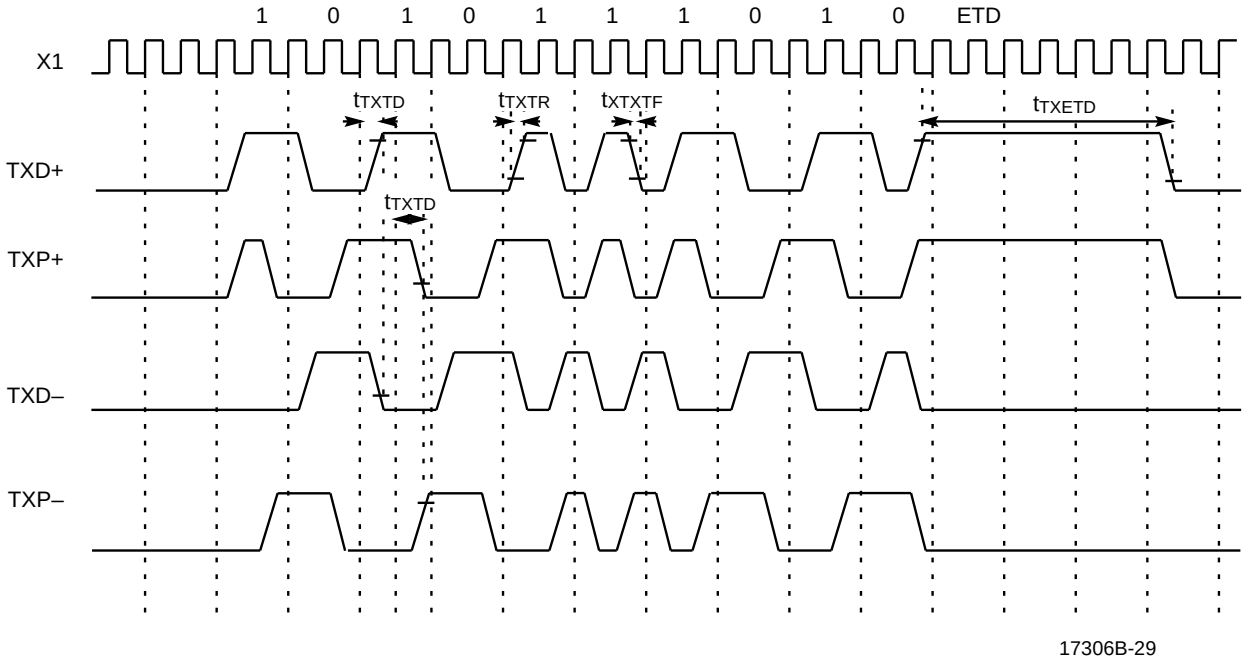


AUI Receive Timing Diagram

SWITCHING WAVEFORMS

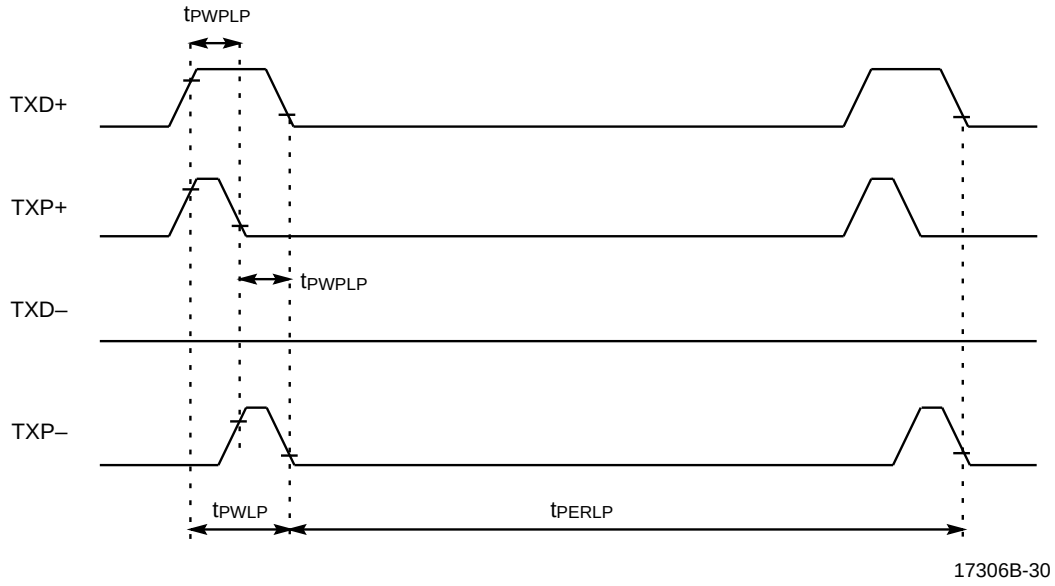


AUI Collision Timing Diagram

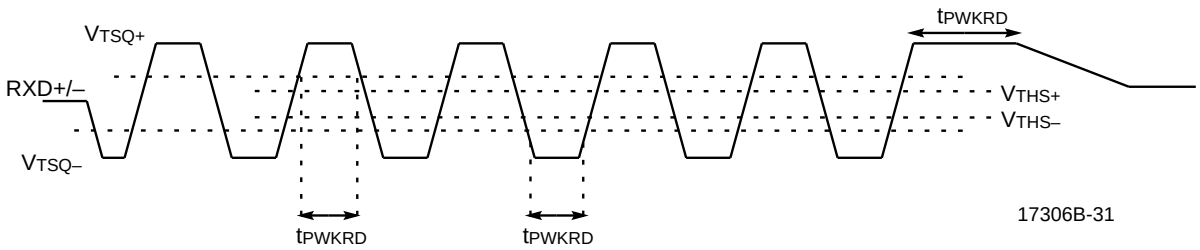


TP Ports Output Timing Diagram

SWITCHING WAVEFORMS

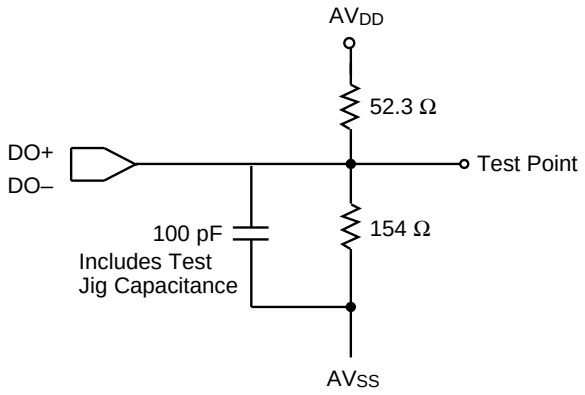


TP Idle Link Test Pulse

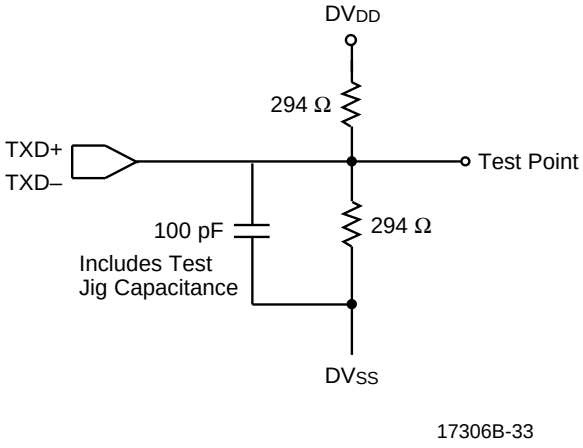


TP Receive Timing Diagram

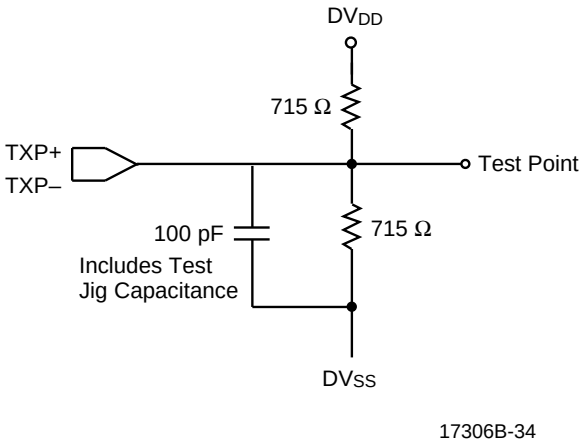
SWITCHING TEST CIRCUITS



AUI DO Switching Test Circuit



TXD Switching Test Circuit



TXP Outputs Test Circuit

APPENDIX

A 10BASE-T INTERFACE

The table below lists the recommended resistor values and filter and transformer modules for the IMR+ device.

IMR+ Device Compatible 10BASE-T Media Interface Modules

¶ Manufacturer	Part #	Package	Description
Bel Fuse	S556-5999-32	16-pin SMD	Transmit and receive filters, transformers and common mode chokes.
Bel Fuse	0556-2006-14	10-pin SIL	Transmit and receive filters, transformers and common mode chokes.
Bel Fuse	A556-2006-DE	16-pin 0.3" DIL	Transmit and receive filters and transformers.
Bel Fuse	A556-2006-00	16-pin DIL	Transmit filter, transformers and common mode choke. Receive filter and transformer.
Halo Electronics	FS02-101Y4	"Slim SIP"	Transmit and receive filters and transformers.
Halo Electronics	FS12-101Y4	"Slim SIP"	Transmit and receive filters and transformers, transmit common mode reduction choke.
Halo Electronics	FS22-101Y4	"Slim SIP"	Transmit and receive filters, transformers and common mode chokes.
Halo Electronics	FD02-101G	16-pin 0.3" DIL	Transmit and receive filters and transformers.
Halo Electronics	FD12-101G	16-pin 0.3" DIL	Transmit and receive filters and transformers, transmit common mode choke.
Halo Electronics	FD22-101G	16-pin 0.3" DIL	Transmit and receive filters, transformers and common mode chokes.
Halo Electronics	FD22-101R2	16-pin 0.3" DIL	Termination and equalization resistors, transmit and receive filters, transformers and common mode chokes.
Nano Pulse	5408-37	16-pin SMD	7 pole transmit and receive filters with 1CT:1CT Xfmrs (transmit & receive) and a separate common mode choke for each channel.
Nano Pulse	5408-40	9-pin SIP	7 pole transmit and receive filters with 1CT:1CT Xfmrs (transmit & receive) and a separate common mode choke for each channel.
Nano Pulse	6612-21	12-pin DIL	7 pole transmit and receive filters with 1CT:1CT Xfmrs (transmit & receive) and a separate common mode choke for each channel.
PCA Electronics	EPA1990A	16-pin 0.3" DIL	Transmit and receive filters and transformers.
PCA Electronics	EPA1990AG	SMT device	Transmit and receive filters and transformers.
PCA Electronics	EPA2013D	16-pin 0.3" DIL	Transmit and receive filters and transformers, transmit common mode choke.
PCA Electronics	EPA2013DG	SMT device	Transmit and receive filters and transformers, transmit common mode choke.
Pulse Engineering	78Z034C	16-pin DIL	Transmit and receive filters and transformers, transmit common mode chokes.
Pulse Engineering	78Z1120B-01	16-pin DIL	Transmit and receive filters and transformers.
Pulse Engineering	78Z1122B-01	16-pin DIL	Transmit and receive filters, transformers and common mode chokes.
Pulse Engineering	PE-68017S	10-pin SIL	Transmit and receive filters, transformers and common mode chokes.
Pulse Engineering	PE-68026	16-pin SMT	Transmit and receive filters, transformers and common mode chokes.
Pulse Engineering	PE-68056	16-pin SMT	Transmit and receive filters, transformers and common mode chokes.
Pulse Engineering	PE-68032	13-pin PCMCIA-SMT	Transmit and receive filters and transformers, transmit common mode chokes.
TDK	TLA-3M601-RS	10-pin SIP	Transmit and receive filters and transformers, transmit common mode chokes.
TDK	TLA-3M102(-T)	16-pin SMD	Integrated resistors, transmit and receive filters and transformers, transmit common mode chokes.
TDK	TLA-3M103(-T)	16-pin SMD	Transmit and receive filters and transformers, transmit common mode chokes.
Valor Electronics	PT3877	16-pin 0.3" DIL	Transmit and receive filters and transformers.
Valor Electronics	PT3983	8-pin 0.3" DIL	Transmit and receive common mode chokes.
Valor Electronics	FL1012	16-pin 0.3" DIL	Transmit and receive filters and transformers, transmit common mode chokes.

APPENDIX B

Glossary

Active Status

In a non-collision state, an IMR+ chip is considered active if it is receiving data on any one of its network ports, or is in the process of broadcasting (repeating) FIFO data from a recently completed data reception. In a collision state (the IMR+ device is generating Jam Sequence), an IMR+ device is considered active if any one or more network ports is receiving data. The IMR+ device asserts the $\overline{REQ}$ line to indicate that it is active.

Collision

In a carrier sense multiple access/collision detection (CSMA/CD) network such as Ethernet, only one node can successfully transfer data at any one time. When two or more separate nodes (DTEs or repeaters) are simultaneously transmitting data onto the network, a Collision state exists. In a repeater using one or more IMR+ devices, a Collision state exists when more than one network port is receiving data at any instant, or when any one or more network ports receives data while the IMR+ device is transmitting (repeating) data, or when the CI+/- pins become active (nominal 10 MHz signal) on the AUI port.

Jam Sequence

A signal consisting of alternating 1s and 0s that is generated by the IMR+ device when a Collision state is detected. This signal is transmitted by the IMR+ device to indicate to the network that one or more network ports in the repeater is involved in a collision.

Network Port

Any of the eight 10BASE-T ports or the AUI port present in the IMR+ device (i.e. not the Expansion Port or the Management Port).

Partitioning

A network port on a repeater has been partitioned if the repeater has internally 'disconnected' it from the repeater due to localized faults that would otherwise bring the entire network down. These faults are generally cable shorts and opens that tend to cause excessive collisions at the network ports. The partitioned network port will be internally re-connected if the network port starts behaving correctly again, usually when successful 'collisionless' transmissions and/or receptions resume.

Receive Collision

A network port is in a Receive Collision state when it detects collision and is not one of the colliding network 'nodes'. This applies mainly to a non-transmitting AUI port because a remote collision is clearly identified by the presence of a nominal 10 MHz signal on the CI+/- pins. However, any repeater port would be considered to be in a receive collision state if the repeater unit is receiving data from that port as the 'one-port-left' in the collision sequence.

Transmit Collision

A network port is in a Transmit Collision state when collision occurs while that port is transmitting. On the AUI port, Transmit Collision is indicated by the presence of a nominal 10 MHz signal on the CI+/- pins while the AUI port is transmitting on the DO+/- pins. On a 10BASE-T port, Transmit Collision occurs when incoming data appears on the RXD+/- pins while the 10BASE-T port is transmitting on the TXD+/- and TXP+/- pins.