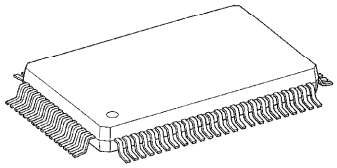
TENTATIVE TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9284BF

CD SINGLE CHIP PROCESSOR WITH BUILT-IN 1BIT DA CONVERTER

The TC9284BF is a single chip processor for sync separation protection / synchronization, EFM demodulation, error correction / interpolation, microcomputer interface, CLV servo a focus tracking servo in CD player system. And, built-in 1bit DA converter. In combination with the TA8190F / TA8191F / TA2031F / TA2035F / TA2065F / TA2077F, which are focus tracking servo LSI, a CD player system can be composed very simply.



QFP80-P-1420-0.80A

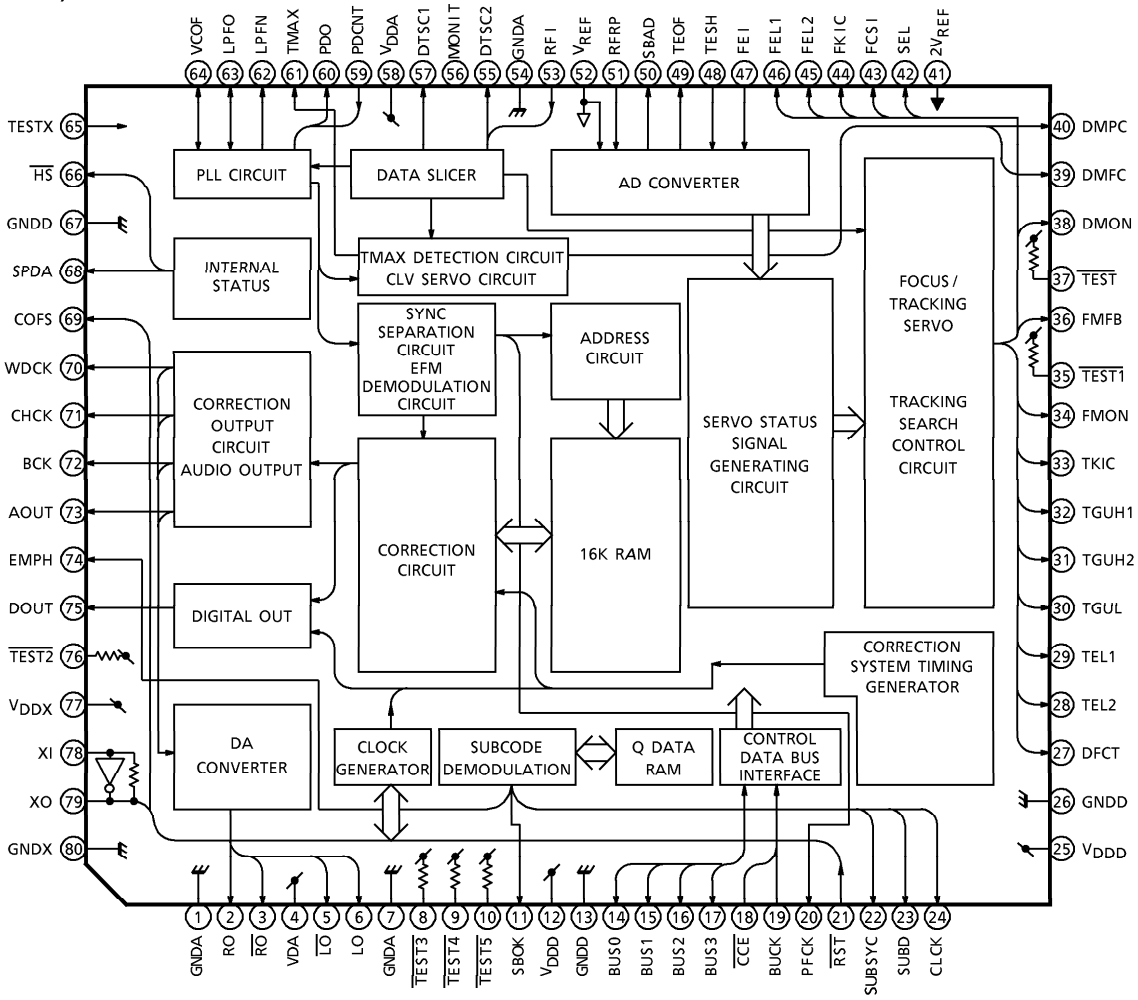
Weight : 1.57g (Typ.)

FEATURES

- Positive sync pattern detection, sync signal protection and synchronization.
- Built-in EFM demodulation and subcode demodulation circuit.
- Has the correction capacity of single and double corrections for C1 and C2 correcting units, respectively, using CIRC correction theoretical format.
- Jitter absorbing capacity of ±5 frames.
- Built-in 16K RAM.
- Built-in digital out circuit.
- Smooth muting through zero cross detection.
- Read timing free subcode Q data.
- Built-in data slicer and analog PLL (free-adjustment VCO adopted) circuit.
- Focus / tracking loop gain auto adjusting function incorporated.
- Built-in AFC and APC circuits for disc motor CLV servo.
- Built-in focus tracking servo control circuit.
- Tracking search control capable of coping with all modes.
- Built-in 1bit DA converter.
  Function of DA converter.
  (1) Built-in 8-time oversampling digital filter.
  (2) Built-in soft mute function.
- Built-in microcomputer interface circuit.
- Double speed play is possible.
- In CMOS structure, high speed and low power dissipation.
- 80 pin flat package.

PIN CONNECTION / BLOCK DIAGRAM

(Top view)



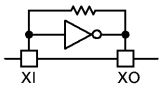
PIN FUNCTION

PIN No.	SYMBOL	I / O	FUNCTIONAL DESCRIPTION	REMARKS
1	GNDA	—	Analog grand terminal for DA converter (R channel)	—
2	RO	O	R channel data forward output terminal.	—
3	$\overline{RO}$	O	R channel data reverse output terminal.	—
4	V_{DA}	—	Analog power supply terminal for DA converter.	—
5	$\overline{LO}$	O	L channel data reverse output terminal.	—
6	LO	O	L channel data forward output terminal.	—
7	GNDA	—	Analog grand terminal for DA converter (L channel)	—
8	$\overline{TEST3}$	I	Test terminal. Normally, keep at "H" level or open.	With pull-up resistor
9	$\overline{TEST4}$	I	Test terminal. Normally, keep at "H" level or open.	
10	$\overline{TEST5}$	I	Test terminal. Normally, keep at "H" level or open.	
11	SBOK	O	Subcode Q data CRC check adjusting result output terminal. The adjusting result is OK at "H" level.	—
12	V_{DDD}	—	Digital supply voltage terminal. (+5V)	—
13	GNDD	—	Digital ground terminal.	—
14 ~ 17	BUS0 ~ BUS3	I / O	Command and data sending / receiving input / output terminals.	Schmitt input Open drain output With pull-up resistor
18	$\overline{CCE}$	I	Command and data sending / receiving chip enable signal input terminal. The bus line becomes active at "L" level.	Schmitt input
19	BUCK	I	Command and data sending / receiving clock input terminal.	
20	PFCK	O	Regeneration system frame periodic signal output terminal. 7.35kHz	—
21	$\overline{RST}$	I	Reset input terminal. The internal system is reset at "L" level.	With pull-up resistor
22	SUBSYC	O	Subcode sync signal output terminal.	—
23	SUBD	O	Subcode P~W output terminals.	—
24	CLCK	I	Subcode P~W data readout clock input terminal.	—
25	V_{DDD}	—	Digital supply voltage terminal.	—
26	GNDD	—	Digital ground terminal.	—
27	DFCT	O	Defect detection signal output terminal. V_{REF} when defect is detected. Normally, HiZ.	—
28	TEL2	O	Tracking gain adjusting analog switch output terminals V_{REF} or HiZ.	—
29	TEL1			
30	TGUL	O	Tracking servo loop low frequency phase compensator change-over analog switch output terminal. HiZ (gain up) when detecting shock. Normally, V_{REF}.	—

PIN FUNCTION

<table>
<tr><th>PIN No.</th><th>SYMBOL</th><th>I / O</th><th>FUNCTIONAL DESCRIPTION</th><th>REMARKS</th></tr>
<tr><td>31</td><td>TGUH2</td><td rowspan="2">O</td><td rowspan="2">Tracking servo loop middle / high frequency phase compensator change-over analog switch output terminals.
HiZ (gain up) when detecting shock. Normally, V_{REF}.
TGUH1 is used at normal regeneration and TGUH2 is used at double speed regeneration.</td><td rowspan="2">—</td></tr>
<tr><td>32</td><td>TGUH1</td></tr>
<tr><td>33</td><td>TKIC</td><td>O</td><td>Tracking actuator kick signal output terminal. Kicks in the outer circumferential direction at "H" level and in the inner circumferential direction at "L" level.</td><td>3-state output</td></tr>
<tr><td>34</td><td>FMON</td><td>O</td><td>Feed servo ON / OFF analog switch output terminals.
Servo on at "HiZ".
Servo off at "V_{REF}".</td><td>—</td></tr>
<tr><td>35</td><td>$\overline{TEST1}$</td><td>I</td><td>Test terminal. Normally, keep at "H" level or open.</td><td>With pull-up resistor</td></tr>
<tr><td>36</td><td>FMFB</td><td>O</td><td>Feed motor FWD / BWD feeding control signal output terminal.
Feed in the outer circumferential direction at "H" level and in the inner circumferential direction at "L" level.</td><td>3-state output</td></tr>
<tr><td>37</td><td>$\overline{TEST}$</td><td>I</td><td>Test terminal. Normally, keep at "H" level or open.</td><td>With pull-up resistor</td></tr>
<tr><td>38</td><td>DMON</td><td>O</td><td>Disc motor driving circuit gain change-over analog switch output terminal.</td><td>—</td></tr>
<tr><td>39</td><td>DMFC</td><td>O</td><td>Disc motor CLV servo AFC signal output terminal.
<table>
<tr><th>COMMAND</th><th>DMFC OUTPUT</th><th>OPERATION</th></tr>
<tr><td>DMFK</td><td>H</td><td>Motor acceleration</td></tr>
<tr><td>DMSV</td><td>PWM</td><td>CLV servo ON</td></tr>
<tr><td>DMBK</td><td>L</td><td>Motor deceleration</td></tr>
<tr><td>DMOFF</td><td>V_{REF}</td><td>CLV servo OFF</td></tr>
</table></td><td>3-state output</td></tr>
<tr><td>40</td><td>DMPC</td><td>O</td><td>Disc motor CLV servo APC signal output terminal.</td><td>3-state output</td></tr>
<tr><td>41</td><td>$2V_{REF}$</td><td>I</td><td>Double times reference voltage input terminal. ($V_{REF} \times 2$)</td><td>—</td></tr>
<tr><td>42</td><td>SEL</td><td>O</td><td>Servo mode indicating signal output terminal.
<table>
<tr><th>SEL</th><th>LD ON / OFF</th><th>FOCUS SERVO</th><th>OPERATION</th></tr>
<tr><td>L</td><td>OFF</td><td>OFF</td><td>LD OFF</td></tr>
<tr><td>HiZ</td><td>ON</td><td>OFF</td><td>Focus Search</td></tr>
<tr><td>H</td><td>ON</td><td>ON</td><td>Normal play, etc.
Focus Servo ON : FOK)</td></tr>
</table></td><td>3-state output</td></tr>
</table>

<table>
<tr><th>PIN No.</th><th>SYMBOL</th><th>I / O</th><th>FUNCTION DESCRIPTION</th><th>REMARKS</th></tr>
<tr><td>43</td><td>FCSI</td><td>O</td><td>Focus actuator driving signal output terminal in the focus search mode.
<table>
<tr><th>COMMAND</th><th>FCSI OUTPUT</th><th>OPERATION</th></tr>
<tr><td>FORST</td><td>H</td><td>Lens gets for away from disc</td></tr>
<tr><td>FOSET</td><td>L</td><td>Lens gets near disc</td></tr>
<tr><td>Others</td><td>HiZ</td><td>Other than focus search</td></tr>
</table></td><td>3-state output</td></tr>
<tr><td>44</td><td>FKIC</td><td>O</td><td>Focus actuator driving signal output terminal in the focus gain adjusting mode.
<table>
<tr><th>COMMAND</th><th>FKIC OUTPUT</th><th>OPERATION</th></tr>
<tr><td>FGASR</td><td>H</td><td>Lens gets for away from disc</td></tr>
<tr><td>FGASS</td><td>L</td><td>Lens gets near disc</td></tr>
<tr><td>Others</td><td>HiZ</td><td>Other than focus adjustment</td></tr>
</table></td><td>3-state output</td></tr>
<tr><td>45</td><td>FEL2</td><td rowspan="2">O</td><td rowspan="2">Fucus again adjusting analog switch output terminals.</td><td rowspan="2">—</td></tr>
<tr><td>46</td><td>FEL1</td></tr>
<tr><td>47</td><td>FEI</td><td>I</td><td>Focus error signal input terminal.</td><td>Analog output</td></tr>
<tr><td>48</td><td>TESH</td><td>I</td><td>Tracking error signal input sample holding analog switch input terminal.</td><td>—</td></tr>
<tr><td>49</td><td>TEOF</td><td>O</td><td>Tracking servo operation ON / OFF analog switch output terminal.
V_{REF} when the tracking servo is OFF.</td><td>—</td></tr>
<tr><td>50</td><td>SBAD</td><td>I</td><td>Sub beam adding signal input terminal.</td><td rowspan="2">Analog input</td></tr>
<tr><td>51</td><td>RFRP</td><td>I</td><td>RF ripple signal input terminal.</td></tr>
<tr><td>52</td><td>V_{REF}</td><td>I</td><td>Reference voltage input terminal. (+ 2.1V)</td><td>—</td></tr>
<tr><td>53</td><td>RFI</td><td>I</td><td>RF signal input terminal.</td><td>Analog input</td></tr>
<tr><td>54</td><td>GNDA</td><td>—</td><td>Analog ground terminal.</td><td>—</td></tr>
<tr><td>55</td><td>DTSC2</td><td>O</td><td>Data slice control EFM signal passive output terminal.</td><td>—</td></tr>
<tr><td>56</td><td>MONIT</td><td>O</td><td>Internal signal (EFMO, PLCK, LOCK and MBOV) output terminal. Selected by command.</td><td>—</td></tr>
<tr><td>57</td><td>DTSC1</td><td>O</td><td>Data slice control EFM signal negative output terminal.</td><td>—</td></tr>
<tr><td>58</td><td>V_{DDA}</td><td>—</td><td>Analog supply voltage terminal. (+ 5V)</td><td>—</td></tr>
<tr><td>59</td><td>PDCNT</td><td>I</td><td>PDO output control terminal.
At “L” level, PDO output is made to HiZ by force.</td><td>—</td></tr>
<tr><td>60</td><td>PDO</td><td>O</td><td>Phase error signal output terminal between EFM signal and PLCK.</td><td>3-state output</td></tr>
</table>

<table>
<tr><th>PIN No.</th><th>SYMBOL</th><th>I / O</th><th>FUNCTIONAL DESCRIPTION</th><th>REMARKS</th></tr>
<tr><td>61</td><td>TMAX</td><td>O</td><td>TMAX signal output terminal.
Hiz at time of system clock.
<table><tr><th>TMAX PERIOD</th><th>TMAX OUTPUT</th></tr><tr><td>Longer than specified period</td><td>L</td></tr><tr><td>Shorter than specified period</td><td>H ($2V_{REF}$)</td></tr><tr><td>Specified period</td><td>HiZ</td></tr></table></td><td>3-state output</td></tr>
<tr><td>62</td><td>LPFN</td><td>I</td><td>LPF amplifier inverting input terminal for PLL.</td><td>—</td></tr>
<tr><td>63</td><td>LPFO</td><td>O</td><td>LPF amplifier output terminal for PLL.</td><td>—</td></tr>
<tr><td>64</td><td>VCOF</td><td>I</td><td>VCO filter terminal.</td><td>—</td></tr>
<tr><td>65</td><td>TESTX</td><td>I</td><td>Test terminal.</td><td>—</td></tr>
<tr><td>66</td><td>$\overline{HS}$</td><td>O</td><td>Double speed monitor output terminal.
Double speed operation at “L” level.</td><td>—</td></tr>
<tr><td>67</td><td>GNDD</td><td>—</td><td>Digital ground terminal.</td><td>—</td></tr>
<tr><td>68</td><td>SPDA</td><td>O</td><td>Processor status signal output terminal.
Correction process judging result, memory buffer capacity, etc.</td><td>—</td></tr>
<tr><td>69</td><td>COFS</td><td>O</td><td>Correction system frame periodic signal output terminal. 7.35kHz.</td><td>—</td></tr>
<tr><td>70</td><td>WDCK</td><td>O</td><td>Word clock output terminal.
Normally, 88.2kHz.</td><td>—</td></tr>
<tr><td>71</td><td>CHCK</td><td>O</td><td>Channel clock output terminal.
Normally, 44.1kHz.</td><td>—</td></tr>
<tr><td>72</td><td>BCK</td><td>O</td><td>Bit clock output terminal.
Normally, 1.4112MHz.</td><td>—</td></tr>
<tr><td>73</td><td>AOUT</td><td>O</td><td>Audio data output terminal.</td><td>—</td></tr>
<tr><td>74</td><td>EMPH</td><td>O</td><td>Emphasis ON / OFF indication signal output terminal.
Emphasis ON at “H” level.</td><td>—</td></tr>
<tr><td>75</td><td>DOUT</td><td>O</td><td>Digital out output terminal.</td><td>—</td></tr>
<tr><td>76</td><td>$\overline{TEST2}$</td><td>I</td><td>Test terminal. Normally, keep at “H” level or open.</td><td>With pull-up resistor</td></tr>
<tr><td>77</td><td>V_{DDX}</td><td>O</td><td>Oscillator supply voltage terminal.</td><td>—</td></tr>
<tr><td>78</td><td>XI</td><td>I</td><td rowspan="2">Crystal oscillator connecting terminal.</td><td rowspan="2">  </td></tr>
<tr><td>79</td><td>XO</td><td>O</td></tr>
<tr><td>80</td><td>GNDX</td><td>O</td><td>Oscillator grand terminal.</td><td>—</td></tr>
</table>

MAXIMUM RATINGS (Ta = 25°C)

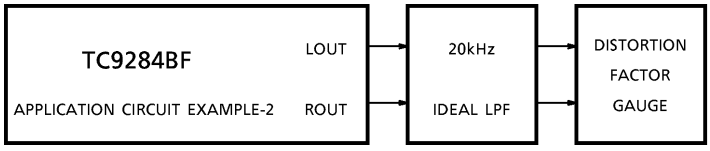
CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{DD}	−0.3~6.0	V
Input Voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Power Dissipation	P_D	1250	mW
Operating Temperature	T_{opr}	−35~85	°C
Storage Temperature	T_{stg}	−55~150	°C

ELECTRICAL CHARACTERISTICS
(Unless otherwise specified, V_{DD} = 5V, $2V_{REF}$ = 4.2V, V_{REF} = 2.1V, Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage		V_{DD}	—	Ta = −35~85°C		4.5	5.0	5.5	V
Operating Supply Current		I_{DD}	—	XI = 16.9344MHz In normal mode		—	40	70	mA
Input Voltage	"H" Level	V_{IH} (1)	—	Whole input terminals except BUS0~3, BUCK and $\overline{CCE}$		3.5	—	V_{DD} + 0.3	V
	"L" Level	V_{IL} (1)				0	—	1.5	
	"H" Level	V_{IH} (2)	—	BUS0~3, BUCK, $\overline{CCE}$ (Schmitt input)		4.0	—	V_{DD} + 0.3	
	"L" Level	V_{IL} (2)				0	—	1.0	
Input Current	"H" Level	I_{IH}	—	V_{IH} = 5V	CMOS input terminals except analog input terminal	—	—	1.0	μA
	"L" Level	I_{IL}		V_{IL} = 0V		−1.0	—	—	
Try State Leak Current	"H" Level	I_{TLH}	—	V_{IH} = 5V		—	—	1.0	μA
	"L" Level	I_{TLL}		V_{IL} = 0V		−1.0	—	—	
Output Current	"H" Level	I_{OH} (1)	—	V_{OH} = 4.6V	WDCK, CHCK, BCK, AOUT, DOUT, XO $V_{OUT} = V_{DD}$	—	—	−2.0	mA
	"L" Level	I_{OL} (1)		V_{OL} = 0.4V		2.0	—	—	
	"H" Level	I_{OH} (2)	—	V_{OH} = 4.6V	SBOK, PFCK, SUBSYC, SUBD, CLCK, SEL, $\overline{HS}$, FCSI, FKIC, PDCNT, MONIT, COFS, SPDA $V_{OUT} = V_{DD}$	—	—	−0.5	
	"L" Level	I_{OL} (2)		VOL = 0.4V		1.0	—	—	
	"H" Level	I_{OH} (3)	—	V_{OH} = 3.8V	TKIC, FMFB, DMFC, DMPC, TMAX $V_{OUT} = 2V_{REF}$	—	—	−0.4	
	"L" Level	I_{OL} (3)		V_{OL} = 0.4V		1.0	—	—	
	"H" Level	I_{OH} (4)	—	V_{OH} = 3.8V	PDO $V_{OUT} = 2V_{REF}$	—	—	−1.0	
	"L" Level	I_{OL} (4)		V_{OL} = 0.4V		1.0	—	—	
Analog Switch OFF Current	"H" Level	I_{OFH}	—	V_{IH} = 5V		—	—	1.0	μA
	"L" Level	I_{OFL}		V_{IL} = 0V		−1.0	—	—	

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Analog Switch ON Resistance	R_{ON} (1)	—	FEL1 / 2, TEL1 / 2, FMON, TGUL, TGUH1 / 2, DFCT, TEOF, DMON	—	—	0.3	kΩ
	R_{ON} (2)		TESH	—	—	0.6	
Pull-up Resistance	R_{UP} (1)	—	$\overline{RST}$	—	50	—	kΩ
	R_{UP} (2)		$\overline{TEST}$, $\overline{TEST1}$~5	—	30	—	
	R_{UP} (3)		BUS3~0	8	—	—	
Oscillation Amplifier Feedback Resistance	R_N	—	XI XO between	2	4	6	kΩ
Operating Frequency Ratio	f_{op}	—	XI	6	—	28	MHz
Total Harmonic Distortion + Noise	THD + N	1	1kHz sine wave Full-scale input	—	−85	−80	dB
S / N Ratio	S / N	1		90	98	—	dB
Dynamic Range	DR	1	1kHz sine wave −60dB input conversion	90	95	—	dB
Cross-talk	CT	1	1kHz sine wave Full-scale input	—	−95	−85	dB

TEST CIRCUIT 1 : Application circuit example-2 is used.



LPF : SHIBASOKU 725C BUILT-IN FILTER
DISTORTION FACTOR GAUGE : SHIBASOKU 725C OR EQUIVALENT

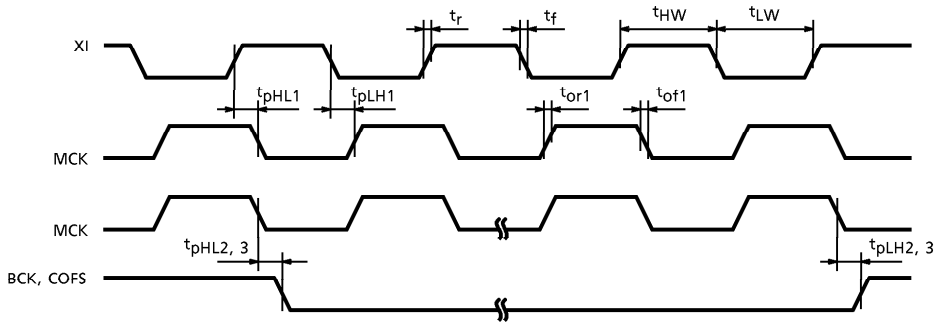
MEASURING ITEM	DISTORTION FACTOR GAUGE FILTER SETTING A WEIGHT
THD + N, CT	OFF
S / N, DR	ON

A WEIGHT : IEC-A OR EQUIVALENT

AC CHARACTERISTICS

(1) Clock system timing

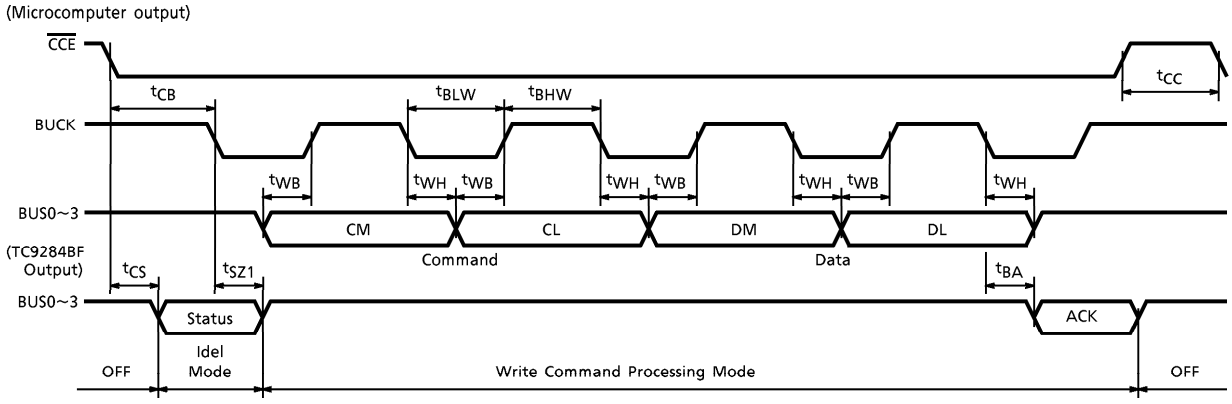
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Clock Pulse Width	"H" Level	t_{HW}	—	XI input	18	—	—	ns
	"L" Level	t_{LW}			18	—	—	
Input Rising Time		t_r			—	—	10	
Input Falling Time		t_f			—	—	10	
Transfer Time (1)	"H" Level	t_{pHL1}	—	XI→MCK	—	—	60	ns
	"L" Level	t_{pLH1}			—	—	60	
Transfer Time (2)	"H" Level	t_{pHL2}	—	MCK→BCK	—	—	60	
	"L" Level	t_{pLH2}			—	—	60	
Transfer Time (3)	"H" Level	t_{pHL3}	—	MCK→COFS	—	—	100	
	"L" Level	t_{pLH3}			—	—	100	
Output Rising Time (1)		t_{or1}	—	MCK, BCK	—	—	15	ns
Output Falling Time (1)		t_{of1}			—	—	15	
Output Rising Time (2)		t_{or2}	—	COFS	—	—	40	ns
Output Falling Time (2)		t_{of2}			—	—	40	



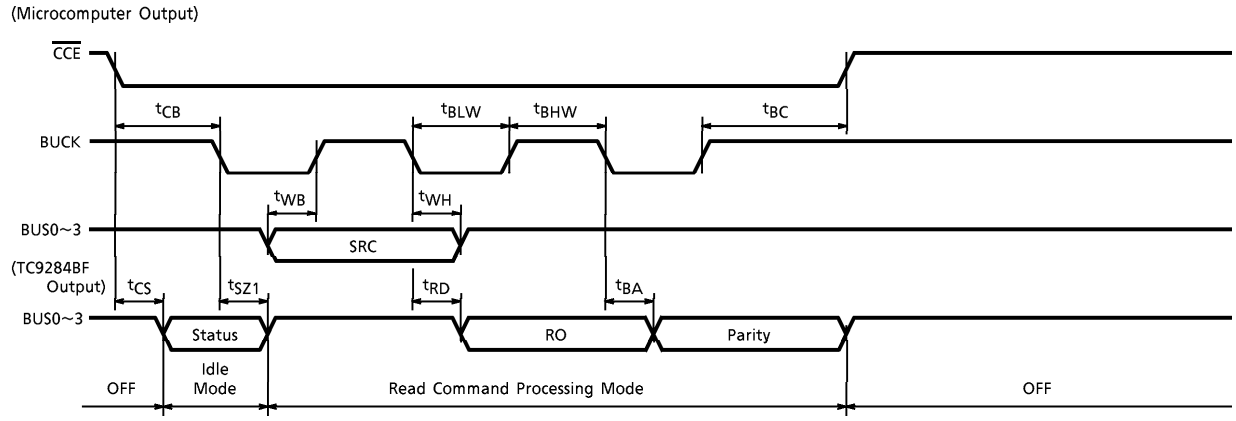
(2) Microcomputer interface timing

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Clock Pulse Width (1)	"H" Level	t_{BHW}	—	BUCK	10	—	—	μs
	"L" Level	t_{BLW}			10	—	—	
Clock Pulse Width (2)	"H" Level	t_{CC}	—	$\overline{CCE}$	6	—	—	
Delay Time (1)		t_{CB}	—	$\overline{CCE}$→BUCK	—	—	6	μs
Delay Time (2)		t_{WB}	—	Command Data→BUCK	0	—	—	
Delay Time (3)		t_{CS}	—	$\overline{CCE}$→Status Output	—	—	6	
Delay Time (4)		t_{BC}	—	BUCK→$\overline{CCE}$	6	—	—	
Setup Time (1)		t_{RD}	—	BUCK→Read Data Output	—	—	6	μs
Setup Time (2)		t_{BA}	—	BUCK→ACK, Each Parity Output	—	—	6	
Hold time (1)		t_{SZ1}	—	BUCK→Status, ACK, Each Parity Output	—	—	6	μs
Hold time (2)		t_{SZ2}	—	$\overline{CCE}$→Status Output	—	—	6	
Hold time (3)		t_{WH}	—	BUCK→Command Data	6	—	—	

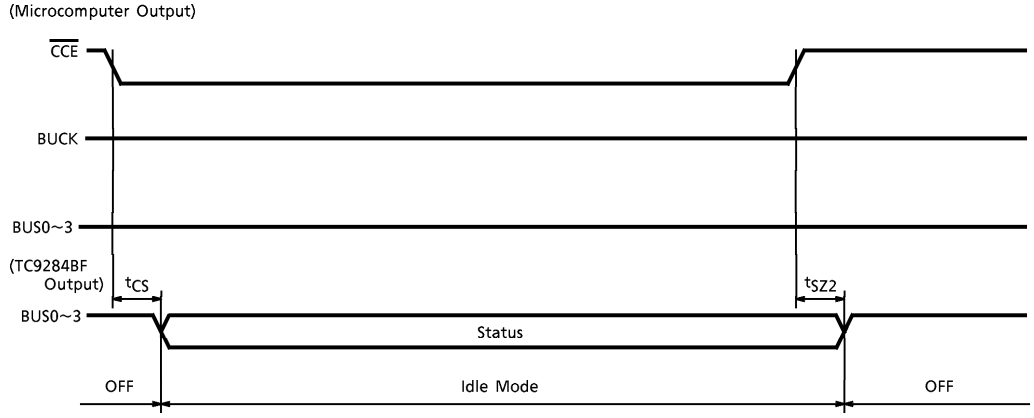
(a) Write command processing mode



(b) Read command processing mode

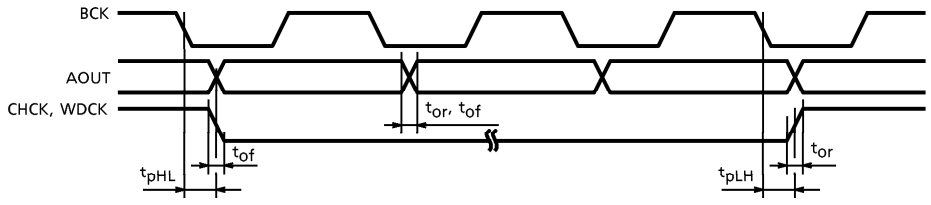


(c) Idle mode



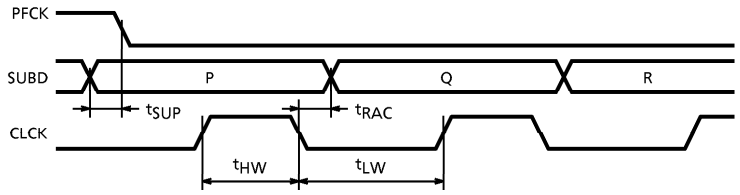
(3) Data output timing

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Transfer Time	"H" Level	t_{pHL}	—	BCK→AOUT, WDCK, CHCK	—	—	30	ns
	"L" Level	t_{pLH}	—		—	—	30	
Output Rising Time		t_{or}	—	AOUT, WDCK, CHCK	—	—	15	ns
Output Falling Time		t_{of}	—		—	—	15	



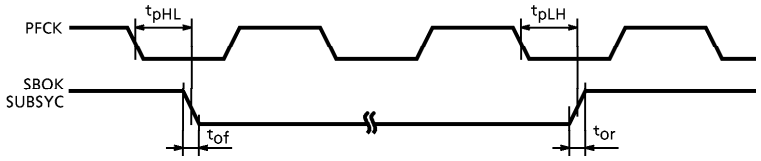
(4) Output timing for subcode P~W

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Clock Pulse Width	"H" Level	t_{HW}	—	CLCK	2	—	—	μs
	"L" Level	t_{LW}	—		2	—	—	
Setup Time		t_{SUP}	—	PFCK→SUBD	0.4	—	—	μs
Read Access Time		t_{RAC}	—	CLCK→SUBD	1.2	—	—	



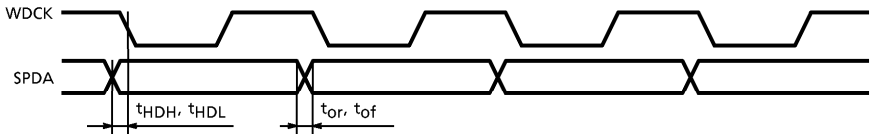
(5) Output timing for subcode Q

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Transfer Time	"H" Level	t_{pHL}	—	PFCK→SBOK, SUBSYC	−50	—	200	ns
	"L" Level	t_{pLH}	—		−50	—	200	
Output Rising Time		t_{or}	—	SBOK, SUBSYC	—	—	40	ns
Output Falling Time		t_{of}	—		—	—	40	



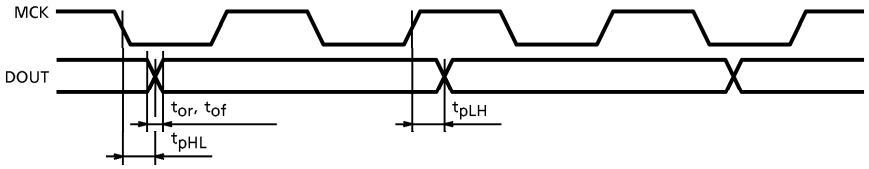
(6) Status signal output timing

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Hold Time	"H" Level	t_{HDH}	—	WDCK→SPDA	—	—	200	ns
	"L" Level	t_{HDL}	—		—	—	200	
Output Rising Time		t_{or}	—	SPDA	—	—	40	ns
Output Falling Time		t_{of}	—		—	—	40	

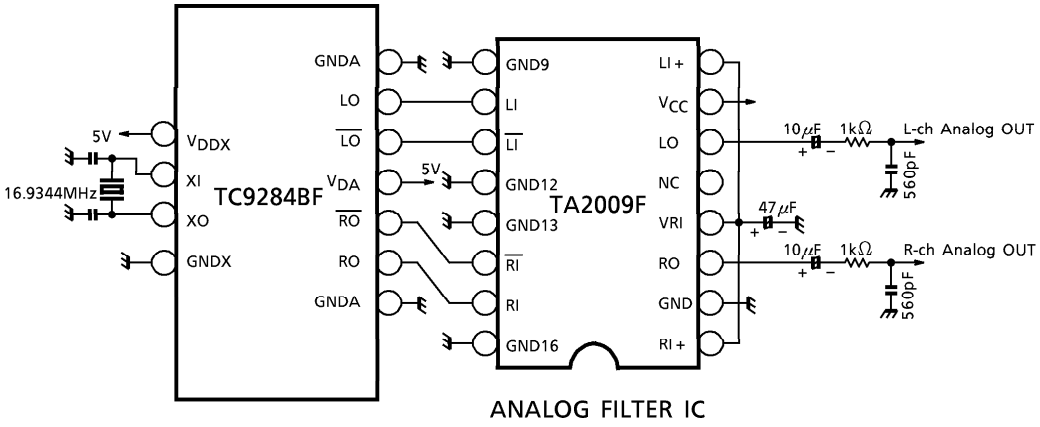


(7) Digital out output timing

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Transfer Time	"H" Level	t_{pHL}	—	MCK→DOUT	—	—	60	ns
	"L" Level	t_{pLH}	—		—	—	60	
Output Rising Time		t_{or}	—	DOUT	—	—	14	ns
Output Falling Time		t_{of}	—		—	—	14	

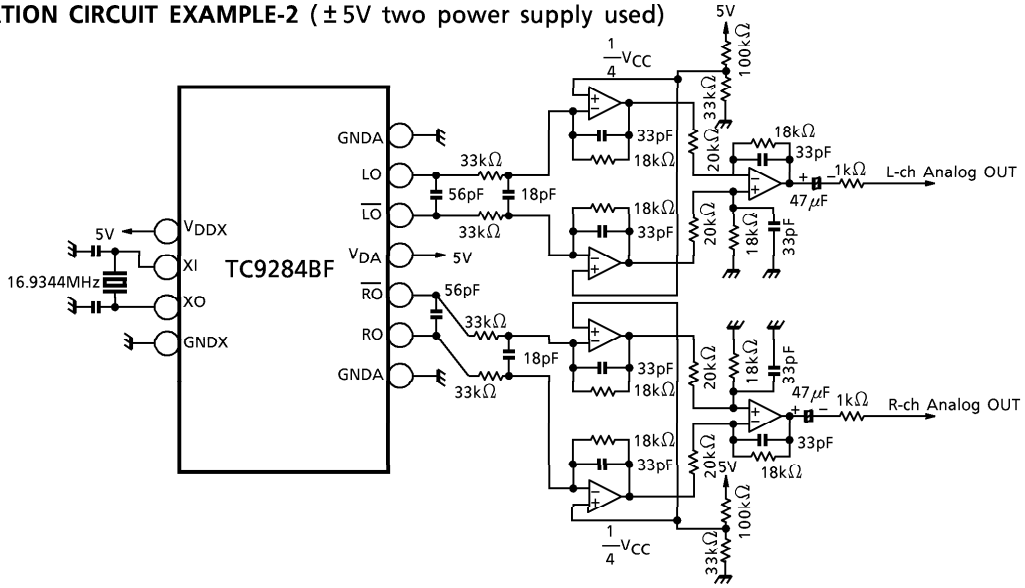


APPLICATION CIRCUIT EXAMPLE-1 (+5V single power supply used)



ANALOG FILTER IC

APPLICATION CIRCUIT EXAMPLE-2 (±5V two power supply used)

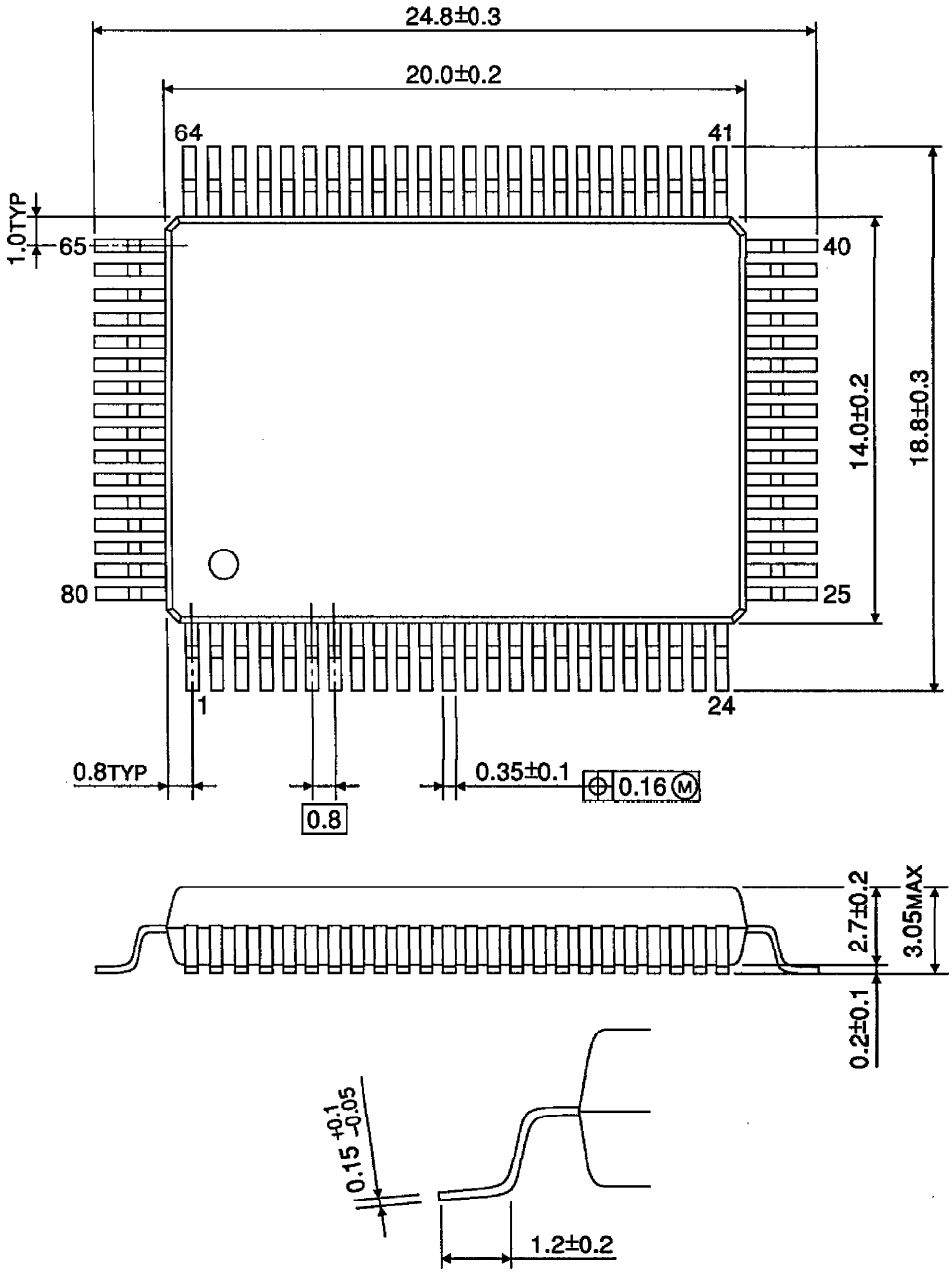


(Cautions)

- Quality of crystal oscillation wave form largely affect S/N ratio and noise distortion. Further, this is also true then system clock is input externally through the XI terminal.
- The wiring between the TC9284BF output and the TA2009F input must be made the shortest.
- The condenser between V_{DD} and GND shall be connected as close to the pin as possible.

OUTLINE DRAWING

QFP80-P-1420-0.80A Unit : mm



Weight : 1.57g (Typ.)