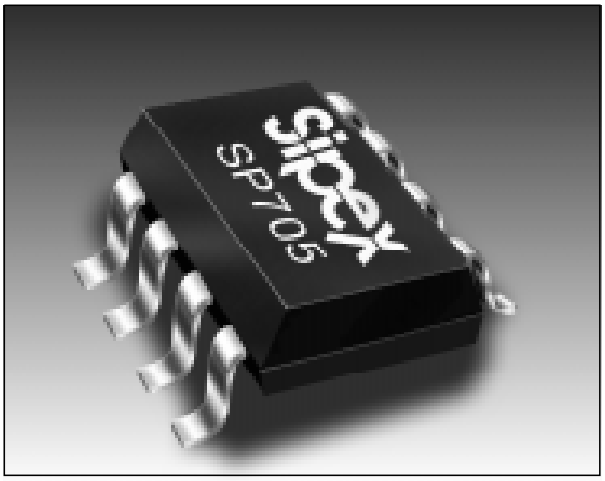
SP705-708/813L/813M

Low Power Microprocessor Supervisory Circuits

- Precision Voltage Monitor:
  SP705/707/813L at 4.65V
  SP706/708/813M at 4.40V
- RESET Pulse Width - 200ms
- Independent Watchdog Timer - 1.6s Timeout (SP705/706/813L/813M)
- 60µA Maximum Supply Current
- Debounced TTL/CMOS Manual Reset Input
- $\overline{\text{RESET}}$ Asserted Down to V_{CC} = 1V
- Voltage Monitor for Power Failure or Low Battery Warning
- Available in 8-pin PDIP, NSOIC, and µSOIC packages



Now available in Lead Free

- Pin Compatible Enhancement to Industry Standard 705-708/813L Series
- Functionally Compatible to Industry Standard 1232 Series

DESCRIPTION…

The **SP705-708/813L/813M** series is a family of microprocessor (µP) supervisory circuits that integrate myriad components involved in discrete solutions which monitor power-supply and battery in µP and digital systems. The **SP705-708/813L/813M** series will significantly improve system reliability and operational efficiency when compared to solutions obtained with discrete components. The features of the **SP705-708/813L/813M** series include a watchdog timer, a µP reset, a Power Fail Comparator, and a manual-reset input. The **SP705-708/813L/813M** series is ideal for applications in automotive systems, computers, controllers, and intelligent instruments. The **SP705-708/813L/813M** series is an ideal solution for systems in which critical monitoring of the power supply to the µP and related digital components is demanded.

Part Number	RESET Threshold	RESET Active	Manual RESET	Watchdog	PFI Accuracy
SP705	4.65 V	LOW	YES	YES	4%
SP706	4.40 V	LOW	YES	YES	4%
SP707	4.65 V	LOW and HIGH	YES	NO	4%
SP708	4.40 V	LOW and HIGH	YES	NO	4%
SP813L	4.65 V	HIGH	YES	YES	4%
SP813M	4.40V	HIGH	YES	YES	4%

ABSOLUTE MAXIMUM RATINGS

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

V_{cc} ..... -0.3V to +6.0V
All Other Inputs (Note 1) ..... -0.3V to (Vcc+0.3V)

Input Current:
V_{cc} 20mA
GND 20mA
Output Current (all outputs) 20mA
ESD Rating 4KV

Continuous Power Dissipation
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
Mini SO (derate 4.10mW/°C above +70°C) 330mW

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10s) ..... +300°C

SPECIFICATIONS

V_{CC} = 4.75V to 5.50V for SP705/707/813L, V_{CC} = 4.50V to 5.50V for SP706/708/813M, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted, typical at 25ºC.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Operating Voltage Range, V_{CC}	1.0		5.5	V	
Supply Current, I_{SUPPLY}		40	60	µA	$\overline{MR}$=V_{CC} or Floating, WDI Floating
Reset Threshold	4.50 4.25	4.65 4.40	4.75 4.50	V	SP705, SP707, SP813L, Note 2 SP706, SP708, SP813M, Note 2
Reset Threshold Hysteresis		40		mV	Note 2
Reset Pulse Width, t_{RS}	140	200	280	ms	Note 2
RESET Output Voltage	V_{CC}-1.5 0.8		 0.40 0.30	V	Note 2 I_{SOURCE} = 800µA I_{SOURCE}=4µA, V_{CC}=1.1V I_{SINK} = 3.2mA V_{CC} = 1V, I_{SINK} = 50µA
Watchdog Timeout Period, t_{WD}	1.00	1.60	2.25	s	SP705, SP706, SP813L, SP813M
WDI Pulse Width, t_{WP}	1			µs	V_{IL} = 0.4V, V_{IH} = 0.8XV_{CC}
WDI Input Threshold, LOW HIGH	 3.5		 0.8	V	SP705, SP706, SP813L, SP813M V_{CC} = 5V
WDI Input Current	 -75	30 -20	75	µA	SP705, SP706, SP813L, SP813M WDI = V_{CC} SP705, SP706, SP813L, SP813M WDI = 0V

SPECIFICATIONS

V_{CC} = 4.75V to 5.50V for SP705/707/813L,813M, V_{CC} = 4.50V to 5.50V for SP706/708, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted, typical at 25ºC.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
$\overline{WDO}$ Output Voltage	V_{CC}-1.5		0.40	V	I_{SOURCE}=800µA I_{SINK}=3.2mA
$\overline{MR}$ Pull-Up Current	100	250	600	µA	$\overline{MR}$ = 0V
$\overline{MR}$ Pulse Width, t_{MR}	150			ns	
$\overline{MR}$ Input Threshold LOW HIGH	 2.0		0.8	V	
$\overline{MR}$ to Reset Out Delay, t_{MD}			250	ns	Note 2
PFI Input Threshold	1.20	1.25	1.30	V	V_{CC} = 5V
PFI Input Current	-25.00	0.01	25.00	nA	
$\overline{PFO}$ Output Voltage	V_{CC}-1.5		0.4	V	I_{SOURCE} = 800µA I_{SINK} = 3.2mA

Note 1: The input voltage limits on PFI and $\overline{MR}$ can be exceeded if the input current is less than 10mA.
Note 2: Applies to both $\overline{RESET}$ in the SP705-SP708 and RESET in the SP707/708/813L/813M.

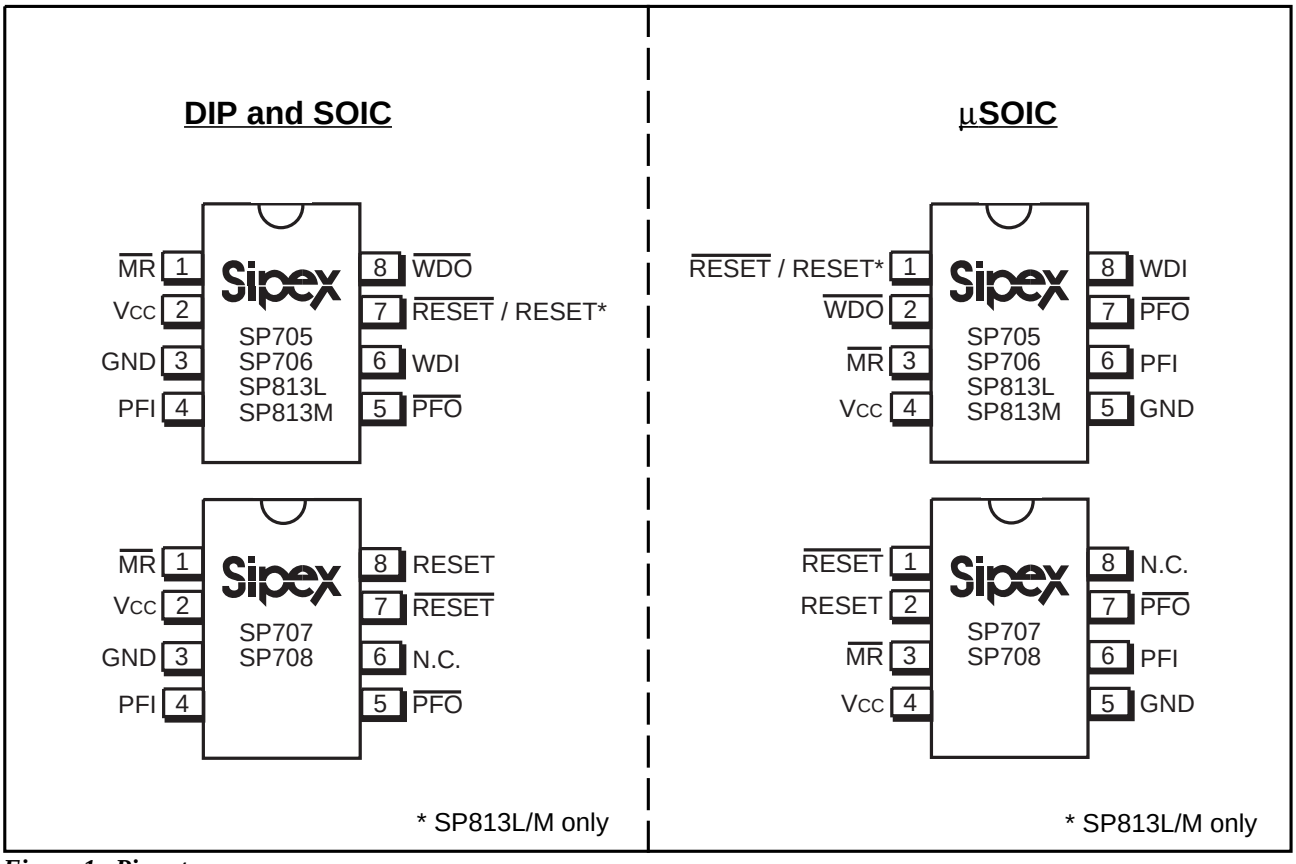


Figure 1. Pinouts

NAME	FUNCTION	PIN DESCRIPTION					
		SP705/706		SP707/708		SP813L/813M	
		DIP/ SOIC	µSOIC	DIP/ SOIC	µSOIC	DIP/ SOIC	µSOIC
$\overline{MR}$	Manual Reset - This input triggers a reset pulse when pulled below 0.8V. This active-LOW input has an internal 250µA pull-up current. It can be driven from a TTL or CMOS logic line or shorted to ground with a switch	1	3	1	3	1	3
V_{CC}	+5V power supply	2	4	2	4	2	4
GND	Ground reference for all signals	3	5	3	5	3	5
PFI	Power-Fail Input - When this voltage monitor input is less than 1.25V, $\overline{PFO}$ goes LOW. Connect PFI to ground or V_{CC} when not in use.	4	6	4	6	4	6
$\overline{PFO}$	Power-Fail Output - This output is HIGH until PFI is less than 1.25V.	5	7	5	7	5	7
WDI	Watchdog Input - If this input remains HIGH or LOW for 1.6s, the internal watchdog timer times out and $\overline{WDO}$ goes LOW. Floating WDI or connecting WDI to a high-impedance tri-state buffer disables the watchdog feature. The internal watchdog timer clears whenever $\overline{RESET}$ is asserted, WDI is tri-stated, or whenever WDI sees a rising or falling edge.	6	8	-	-	6	8
N.C.	No Connect.	-	-	6	8	-	-
$\overline{RESET}$	Active-LOW $\overline{RESET}$ Output - This output pulses LOW for 200ms when triggered and stays LOW whenever V_{CC} is below the reset threshold (4.65V for the SP705/707/813L and 4.40V for the SP706/708). It remains LOW for 200ms after V_{CC} rises above the reset threshold or $\overline{MR}$ goes from LOW to HIGH. A watchdog timeout will not trigger $\overline{RESET}$ unless $\overline{WDO}$ is connected to $\overline{MR}$.	7	1	7	1	-	-
$\overline{WDO}$	Watchdog Output - This output pulls LOW when the internal watchdog timer finishes its 1.6s count and does not go HIGH again until the watchdog is cleared. $\overline{WDO}$ also goes LOW during low-line conditions. Whenever V_{CC} is below the reset threshold, $\overline{WDO}$ stays LOW. However, unlike $\overline{RESET}$, $\overline{WDO}$ does not have a minimum pulse width. As soon as V_{CC} is above the reset threshold, $\overline{WDO}$ goes HIGH with no delay.	8	2	-	-	8	2
RESET	Active-HIGH RESET Output - This output is the complement of $\overline{RESET}$. Whenever RESET is HIGH, $\overline{RESET}$ is LOW, and vice versa. Note the SP813L/813M has a reset output only.	-	-	8	2	7	1

Table 1. Device Pin Description

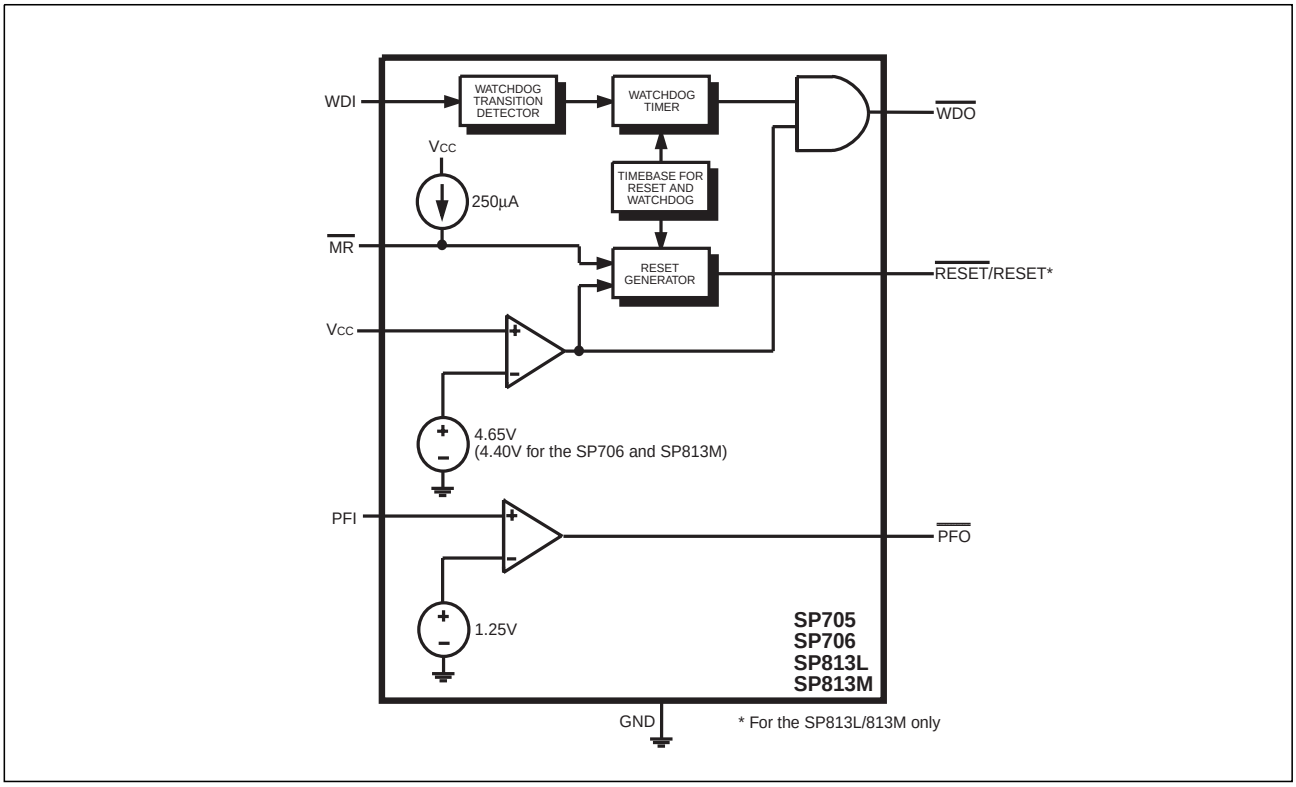


Figure 2. Internal Block Diagram for the SP705/706/813L/813M

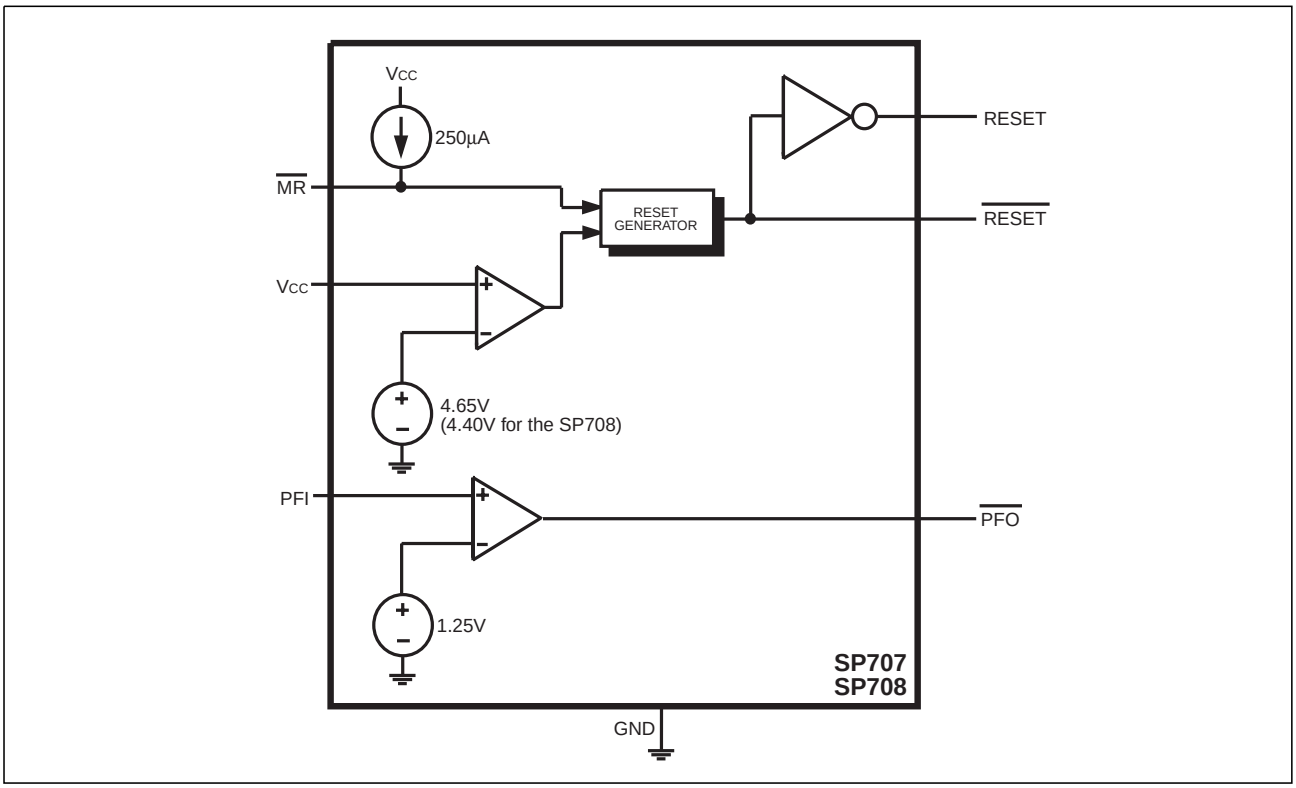


Figure 3. Internal Block Diagram for the SP707/708

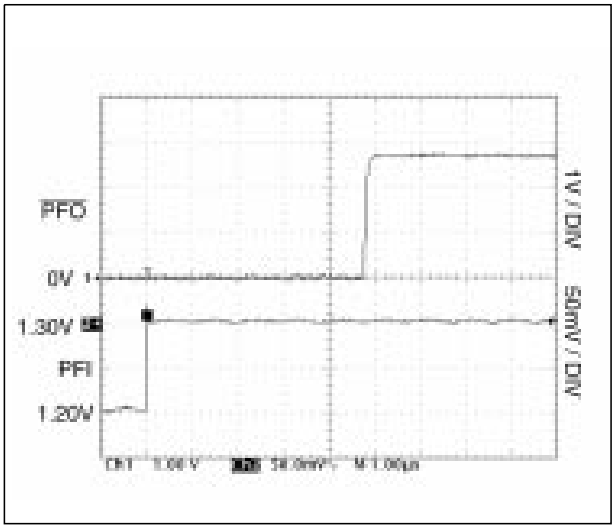


Figure 4A. Power-Fail Comparator De-assertion Response Time.

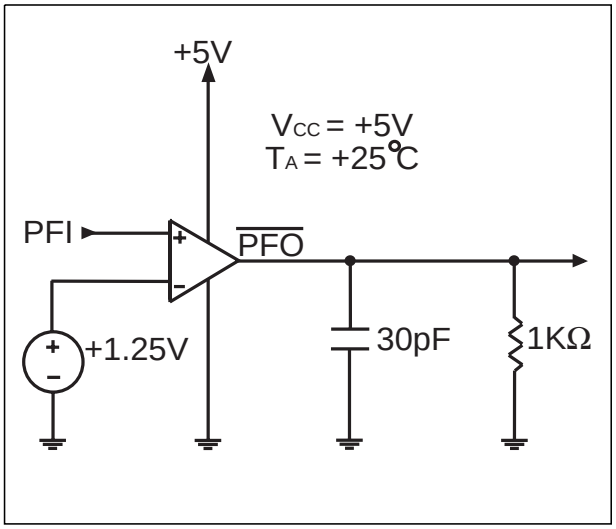


Figure 4B. Circuit for the Power-Fail Comparator De-assertion Response Time.

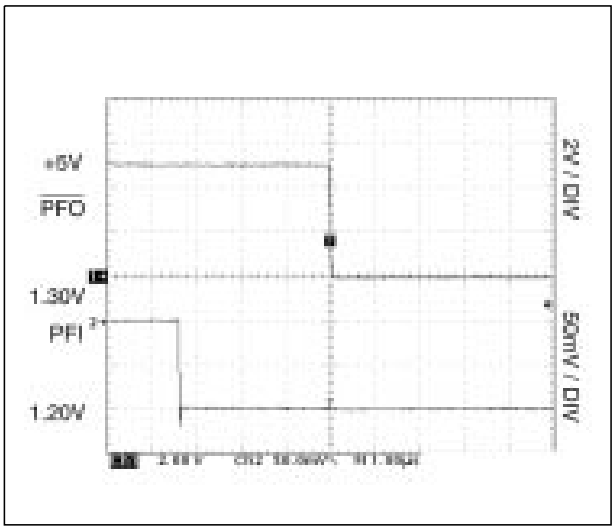


Figure 5A. Power-Fail Comparator Assertion Response Time.

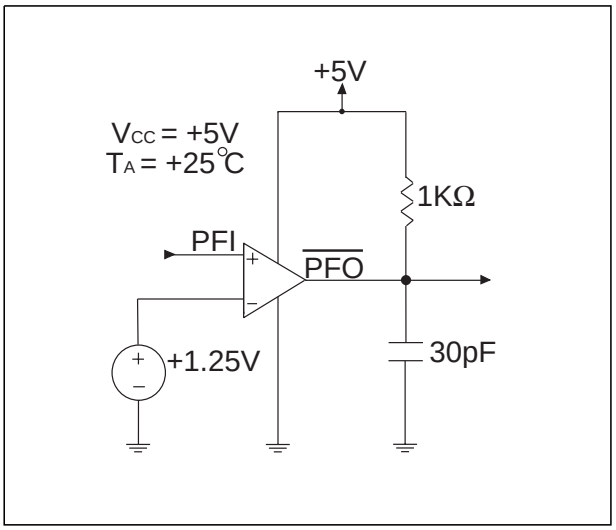


Figure 5B. Circuit for the Power-Fail Comparator Assertion Response Time.

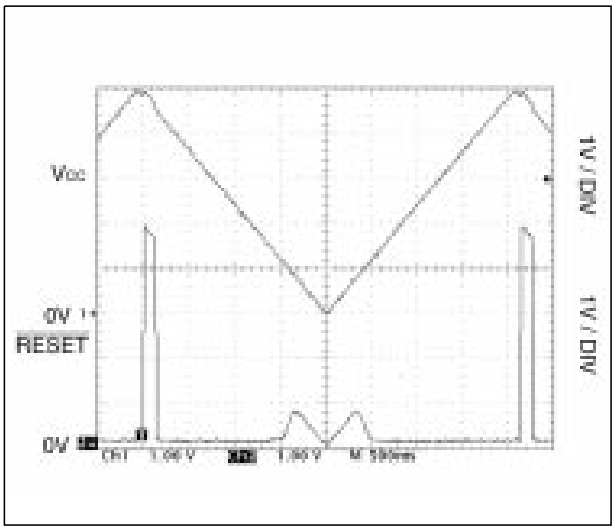


Figure 6A. SP705/707 $\overline{RESET}$ Output Voltage vs. Supply Voltage.

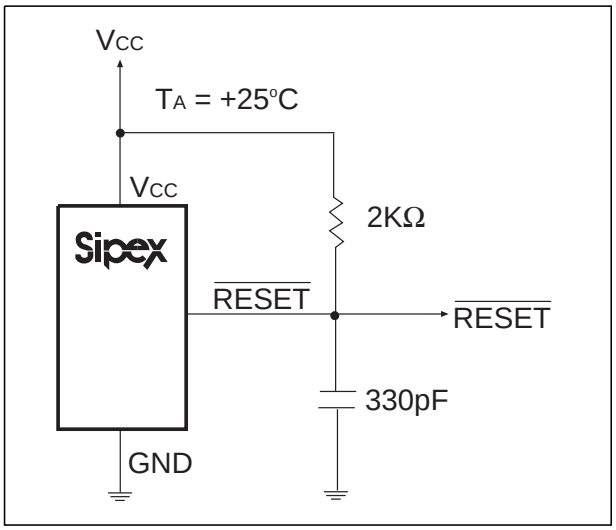


Figure 6B. Circuit for the SP705/707 $\overline{RESET}$ Output Voltage vs. Supply Voltage.

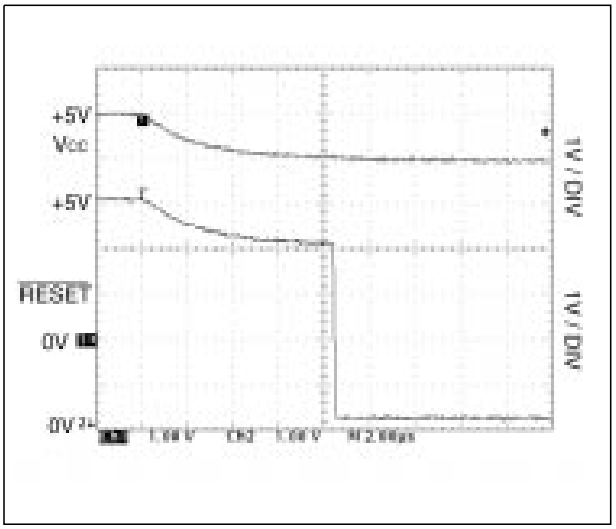


Figure 7A. SP705/707 $\overline{\text{RESET}}$ Response Time

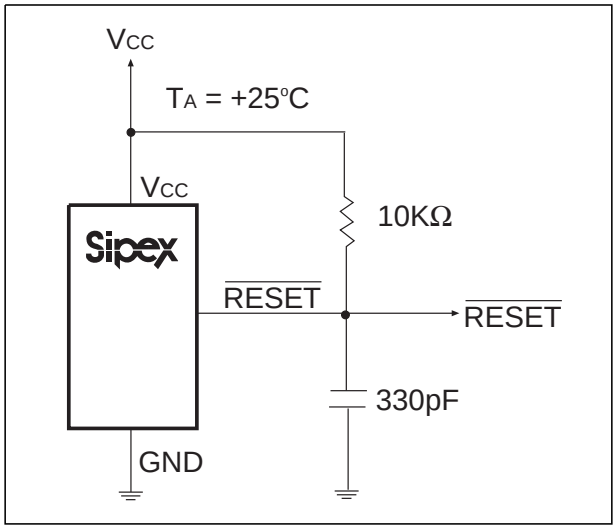


Figure 7B. Circuit for the SP705/707 $\overline{\text{RESET}}$ Response Time

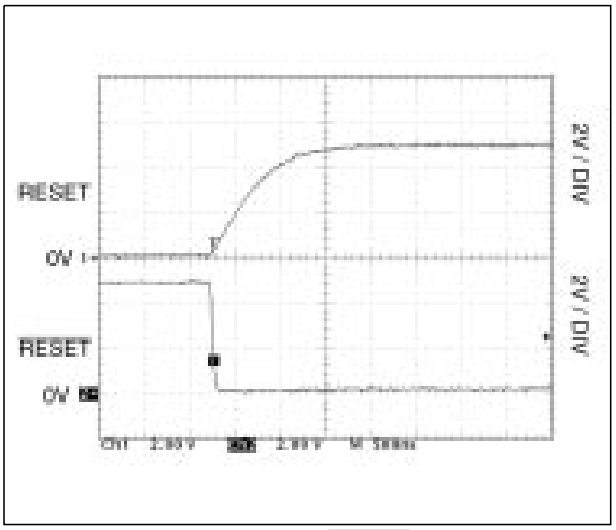


Figure 8. SP707 RESET and $\overline{\text{RESET}}$ Assertion

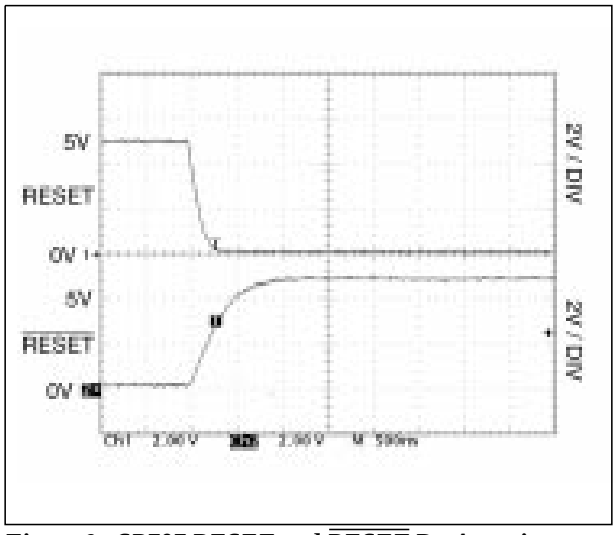


Figure 9. SP707 RESET and $\overline{\text{RESET}}$ De-Assertion

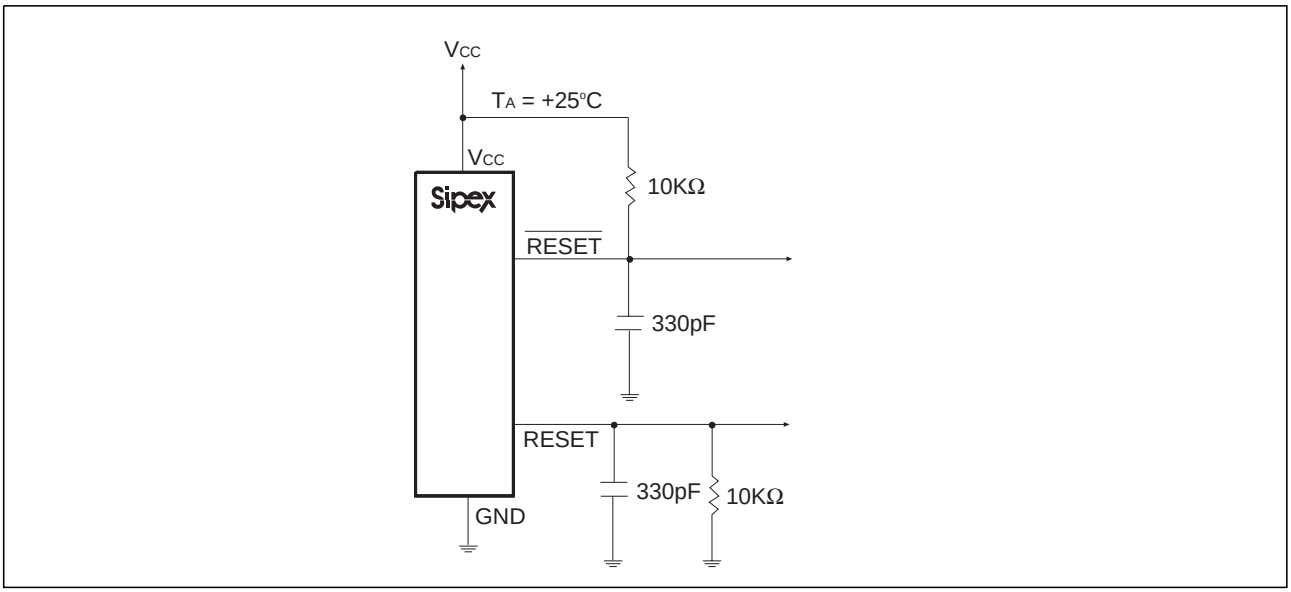


Figure 10. Circuit for the SP707 RESET and $\overline{\text{RESET}}$ Assertion and De-Assertion

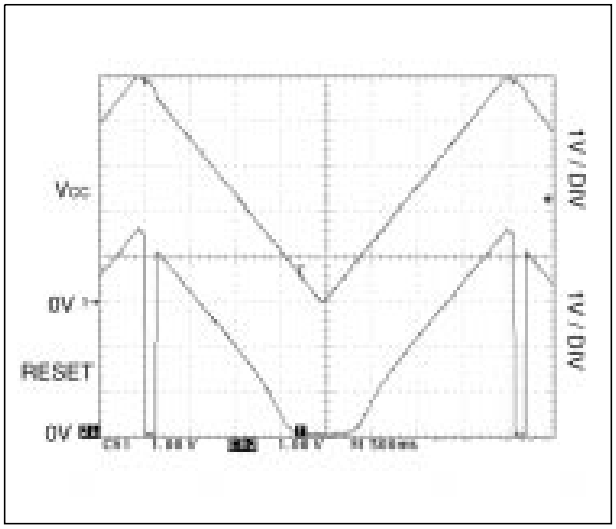


Figure 11. SP707/708/813L/813M RESET Output Voltage vs. Supply Voltage

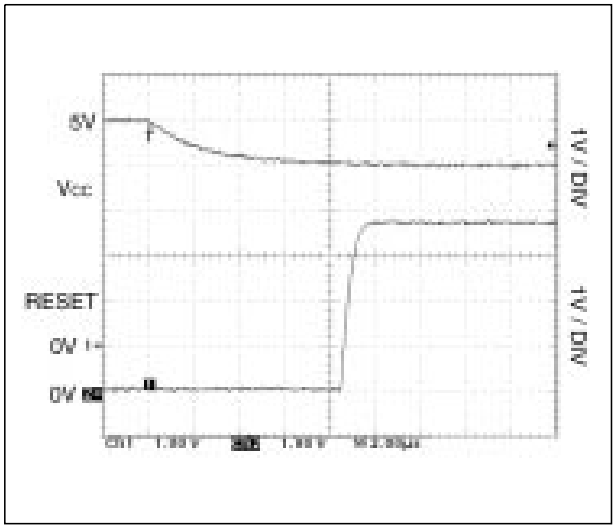


Figure 12. SP813L/813M RESET Response Time

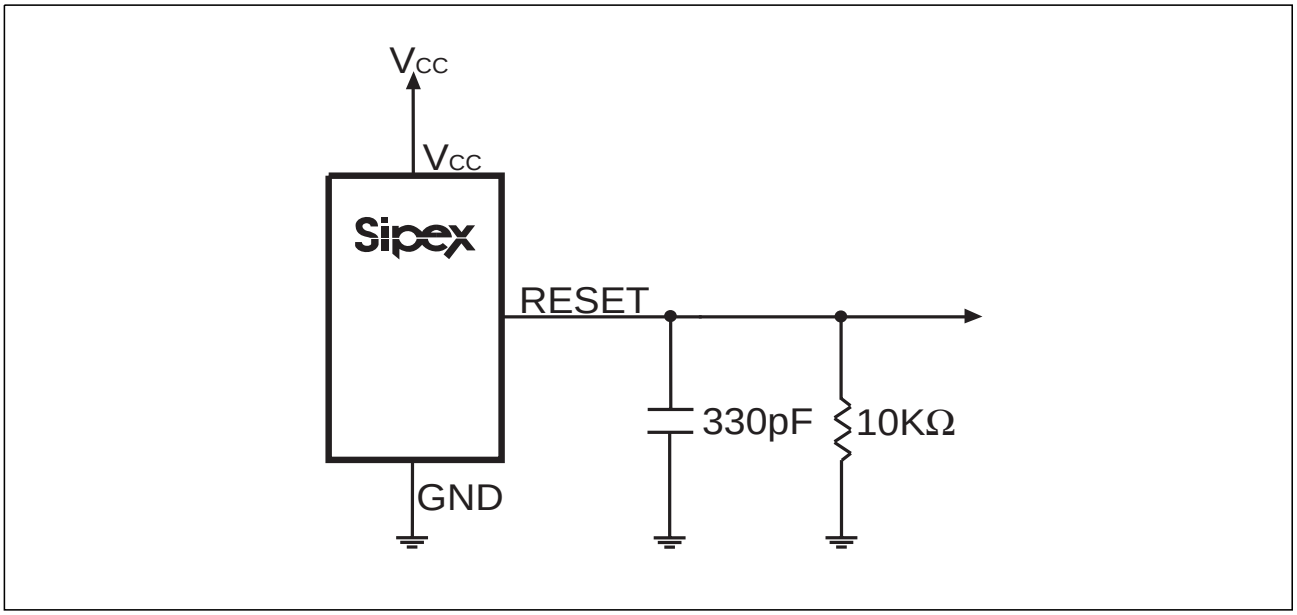


Figure 13. Circuit for the SP707/708/813L/813M RESET Output Voltage vs. Supply Voltage and the SP813L/813M RESET Response Time

FEATURES

The **SP705-708/813L/813M** series provides four key functions:
1. A reset output during power-up, power-down and brownout conditions.
2. An independent watchdog output that goes LOW if the watchdog input has not been toggled within 1.6 seconds.
3. A 1.25V threshold detector for power-fail warning, low battery detection, or monitoring a power supply other than +5V.
4. An active-LOW manual-reset that allows RESET to be triggered by a pushbutton switch.

The **SP707/708** devices are the same as the **SP705/706** devices except for the active-HIGH RESET substitution of the watchdog timer. The **SP813L** is the same as the **SP705** except an active-HIGH RESET is provided rather than an active-LOW $\overline{\text{RESET}}$. The **SP705/707/813L** devices generate a reset when the supply voltage drops below 4.65V. The **SP706/708/813M** devices generate a reset below 4.40V.

The **SP705-708/813L/813M** series is ideally suited for applications in automotive systems, intelligent instruments, and battery-powered computers and controllers. The **SP705-708/813L/813M** series is ideally applied in environments where monitoring of power supply to a µP and its related components is critical.

THEORY OF OPERATION

The **SP705-708/813L/813M** series is a microprocessor (µP) supervisory circuit that monitors the power supplied to digital circuits such as microprocessors, microcontrollers, or memory. The series is an ideal solution for portable, battery-powered equipment that requires power supply monitoring. Implementing this series will reduce the number of components and overall complexity. The watchdog functions of this product family will continuously oversee the operational status of a system. The operational features and benefits of the **SP705-708/813L/813M** series are described in more detail below.

RESET Output

A microprocessor's reset input starts the µP in a known state. The **SP705-708/813L/813M** series asserts reset during power-up and prevents code execution errors during power-down or brownout conditions.

On power-up, once V_{CC} reaches 1V, $\overline{\text{RESET}}$ is a guaranteed logic LOW of 0.4V or less. As V_{CC} rises, $\overline{\text{RESET}}$ stays LOW. When V_{CC} rises above the reset threshold, an internal timer releases $\overline{\text{RESET}}$ after 200ms. $\overline{\text{RESET}}$ pulses LOW whenever V_{CC} dips below the reset threshold, such as in a brownout condition. When a brownout condition occurs in the middle of a previously initiated reset pulse, the pulse continues for at least another 140ms. On power-down, once V_{CC} falls below the reset threshold, $\overline{\text{RESET}}$ stays LOW and is guaranteed to be 0.4V or less until V_{CC} drops below 1V.

The **SP707/708/813L/813M** active-HIGH RESET output is simply the complement of the $\overline{\text{RESET}}$ output and is guaranteed to be valid with V_{CC} down to 1.1V. Some µPs, such as Intel's 80C51, require an active-HIGH reset pulse.

Watchdog Timer

The **SP705/706/813L/813M** watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within 1.6 seconds and WDI is not tri-stated, $\overline{\text{WDO}}$ goes LOW. As long as $\overline{\text{RESET}}$ is asserted or the WDI input is tri-stated, the watchdog timer will stay cleared and will not count. As soon as $\overline{\text{RESET}}$ is released and WDI is driven HIGH or LOW, the timer will start counting. Pulses as short as 50ns can be detected.

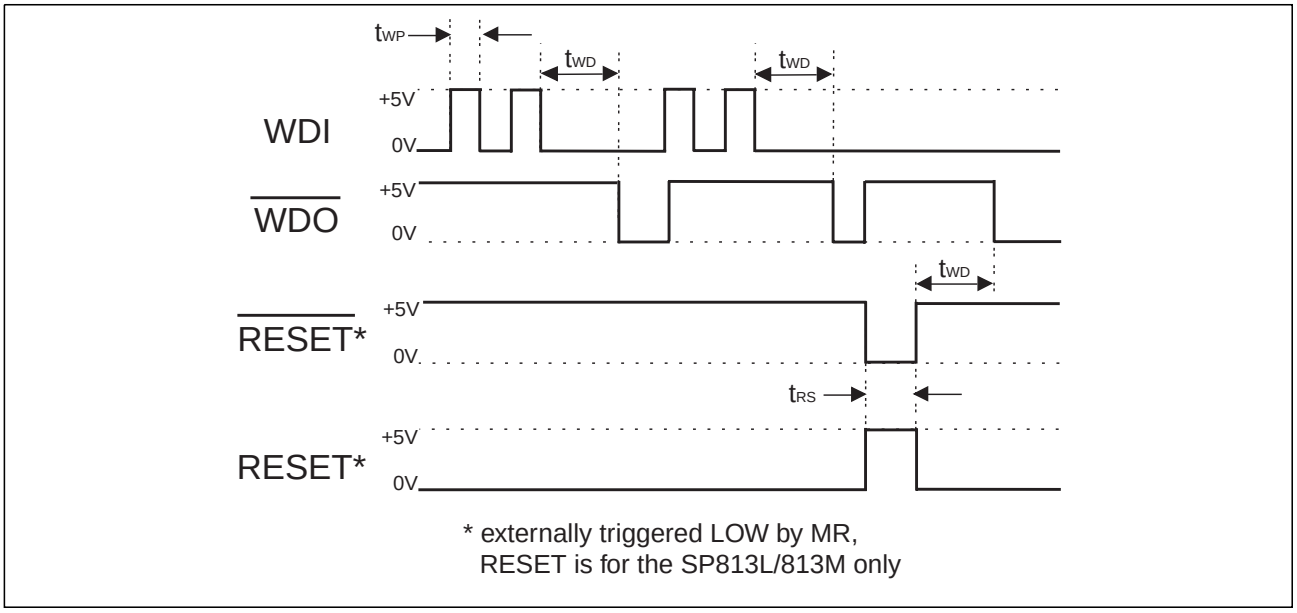


Figure 14. SP705/706/813L/813M Watchdog Timing Waveforms

Typically, $\overline{WDO}$ will be connected to the non-maskable interrupt input (NMI) of a µP. When V_{CC} drops below the reset threshold, $\overline{WDO}$ will go LOW whether or not the watchdog timer has timed out. Normally this would trigger an NMI but $\overline{RESET}$ goes LOW simultaneously, and thus overrides the NMI.

If WDI is left unconnected, $\overline{WDO}$ can be used as a low-line output. Since floating WDI disables the internal timer, $\overline{WDO}$ goes LOW only when V_{CC} falls below the reset threshold, thus functioning as a low-line output.

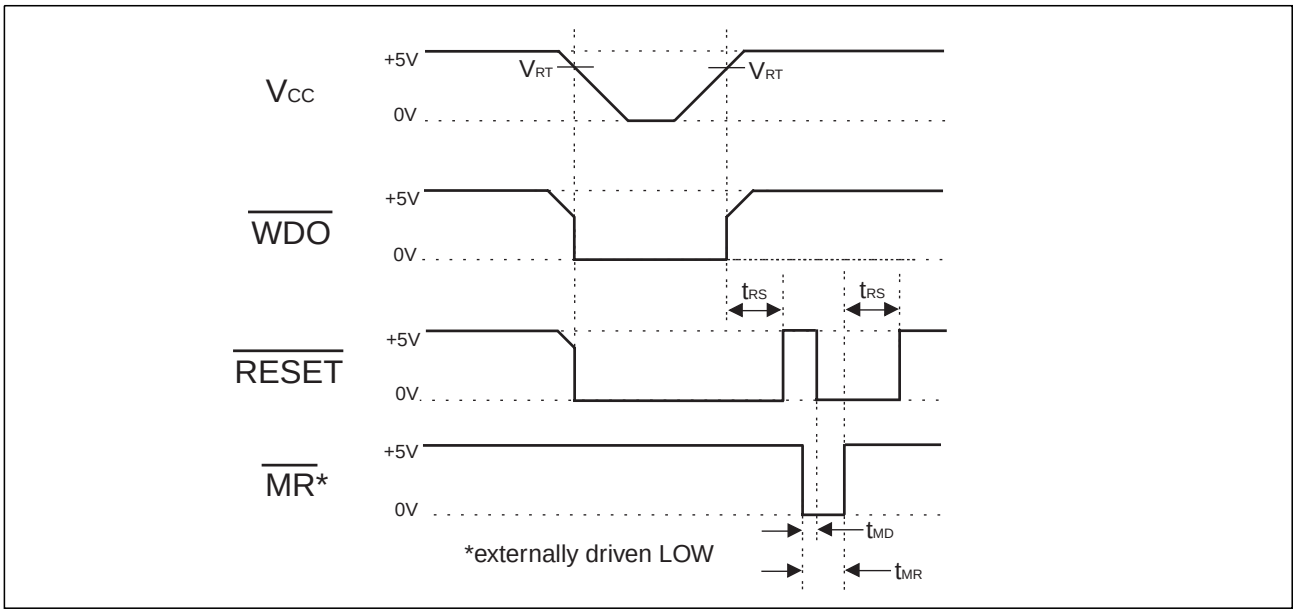


Figure 15. SP705/706 Timing Diagrams with WDI Tri-stated. The SP707/708/813L/813M RESET Output is the Inverse of the $\overline{RESET}$ Waveform Shown.

Power-Fail Comparator

The power-fail comparator can be used for various purposes because its output and noninverting input are not internally connected. The inverting input is internally connected to a 1.25V reference.

To build an early-warning circuit for power failure, connect the PFI pin to a voltage divider as shown in *Figure 16*. Choose the voltage divider ratio so that the voltage at PFI falls below 1.25V just before the +5V regulator drops out. Use $\overline{PFO}$ to interrupt the µP so it can prepare for an orderly power-down.

Manual Reset

The manual-reset input ($\overline{MR}$) allows RESET to be triggered by a pushbutton switch. The switch is effectively debounced by the 140ms minimum RESET pulse width. $\overline{MR}$ is TTL/CMOS logic compatible, so it can be driven by an external logic line. $\overline{MR}$ can be used to force a watchdog timeout to generate a RESET pulse in the **SP705/706/813L/813M**. Simply connect $\overline{WDO}$ to $\overline{MR}$.

Ensuring a Valid $\overline{RESET}$ Output Down to V_{CC} = 0V

When V_{CC} falls below 1V, the **SP705/706/707/708** $\overline{RESET}$ output no longer sinks current, it becomes an open circuit. High-impedance CMOS logic inputs can drift to undetermined voltages if left undriven. If a pull-down resistor is added to the $\overline{RESET}$ pin, any stray charge or leakage currents will be shunted to ground, holding $\overline{RESET}$ LOW. The resistor value is not critical. It should be about 100KΩ, large enough not to load $\overline{RESET}$ and small enough to pull $\overline{RESET}$ to ground.

Monitoring Voltages Other Than the Unregulated DC Input

Monitor voltages other than the unregulated DC by connecting a voltage divider to PFI and adjusting the ratio appropriately. If required, add hysteresis by connecting a resistor (with a value approximately 10 times the sum of the two resistors in the potential divider network) between PFI and $\overline{PFO}$. A capacitor between PFI and GND will reduce the power-fail circuit's

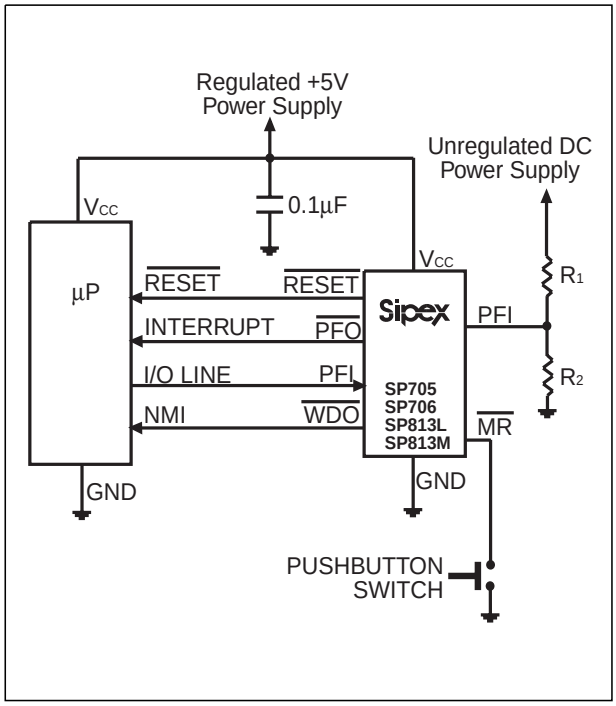


Figure 16. Typical Operating Circuit

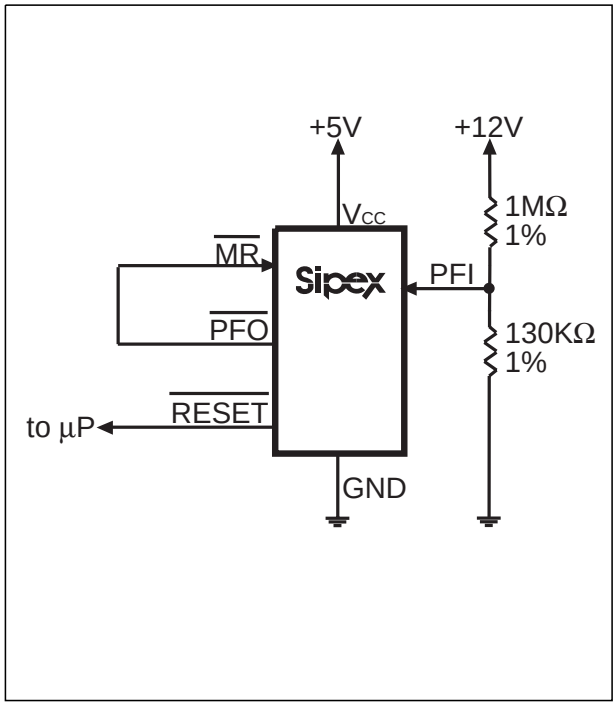


Figure 17. Monitoring Both +5V and +12V Power Supplies

sensitivity to high-frequency noise on the line being monitored. $\overline{\text{RESET}}$ can be used to monitor voltages other than the +5V V_{CC} line. Connect $\overline{\text{PFO}}$ to $\overline{\text{MR}}$ to initiate a $\overline{\text{RESET}}$ pulse when PFI drops below 1.25V. *Figure 17* shows the **SP705/706/707/708** configured to assert $\overline{\text{RESET}}$ when the +5V supply falls below the RESET threshold, or when the +12V supply falls below approximately 11V.

Monitoring a Negative Voltage Supply

The power-fail comparator can also monitor a negative supply rail, shown in *Figure 18*. When the negative rail is good (a negative voltage of large magnitude), $\overline{\text{PFO}}$ is LOW. By adding the resistors and transistor as shown, a HIGH $\overline{\text{PFO}}$ triggers RESET. As long as $\overline{\text{PFO}}$ remains HIGH, the **SP705-708/813L/813M** will keep RESET asserted (where $\overline{\text{RESET}}$ = LOW and RESET = HIGH). Note that this circuit's accuracy depends on the PFI threshold tolerance, the V_{CC} line, and the resistors.

Interfacing to mPs with Bidirectional RESET Pins

µPs with bidirectional RESET pins, such as the Motorola 68HC11 series, can contend with the **SP705/706/707/708** $\overline{\text{RESET}}$ output. If, for example, the $\overline{\text{RESET}}$ output is driven HIGH and the µP wants to pull it LOW, indeterminate logic levels may result. To correct this, connect a 4.7KΩ resistor between the $\overline{\text{RESET}}$ output and the µP reset I/O, as shown if *Figure 19*. Buffer the $\overline{\text{RESET}}$ output to other system components.

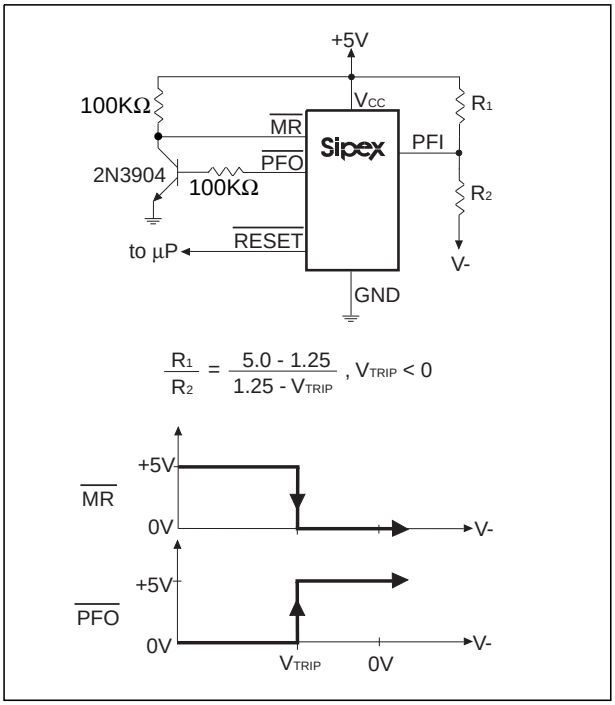


Figure 18. Monitoring a Negative Voltage Supply

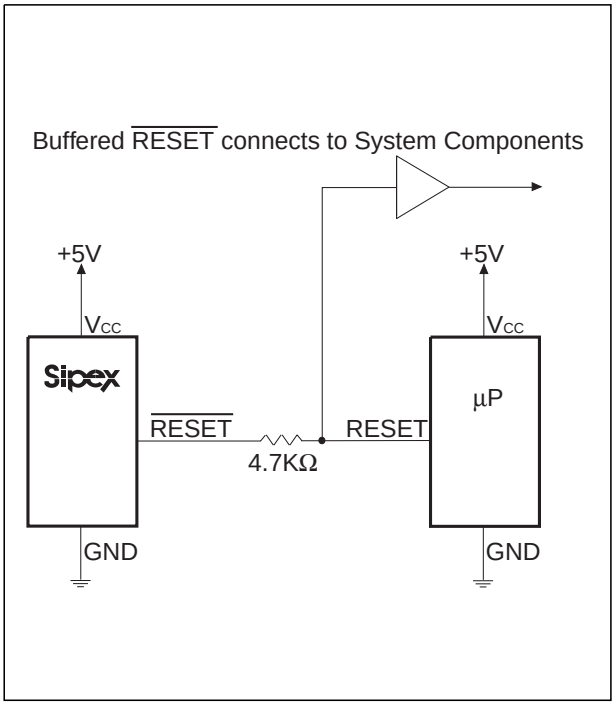


Figure 19. Interfacing to Microprocessors with Bidirectional RESET I/O for the SP705/706/707/708

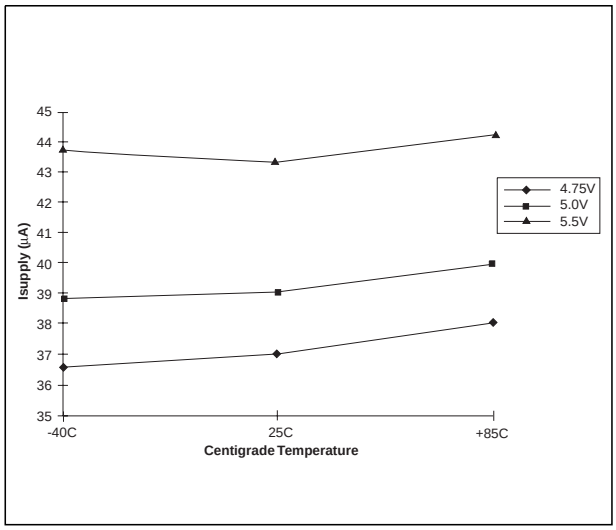


Figure 20. Supply Current vs. Temperature

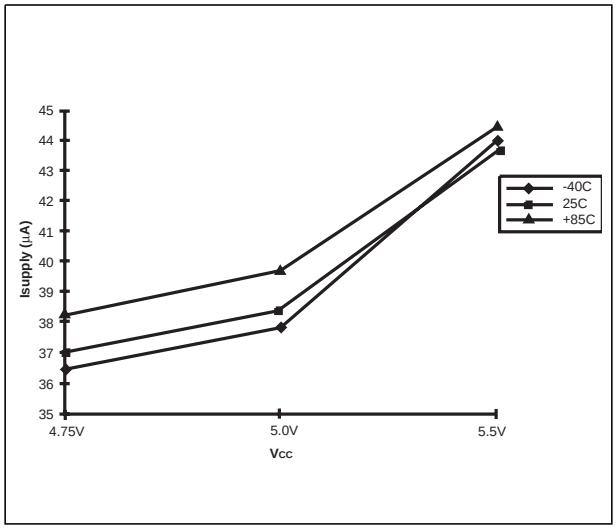


Figure 21. Supply Current vs. Supply Voltage

Applications

The **SP705-708/813L/813M** series offers unmatched performance and the lowest power consumption for these industry standard devices. Refer to *Figures 20* and *21* for supply current performance characteristics rated against temperature and supply voltages.

Table 2 shows how the **SP705-708/813L/813M** series can be used instead of the Dallas Semiconductor DS1232LP/LPS. *Table 2* illustrates to a designer the advantages and trade-offs of the **SP705-708/813L/813M** series compared to the Dallas Semiconductor device. While the names of the pin descriptions may differ, the functions are the same or very similar.

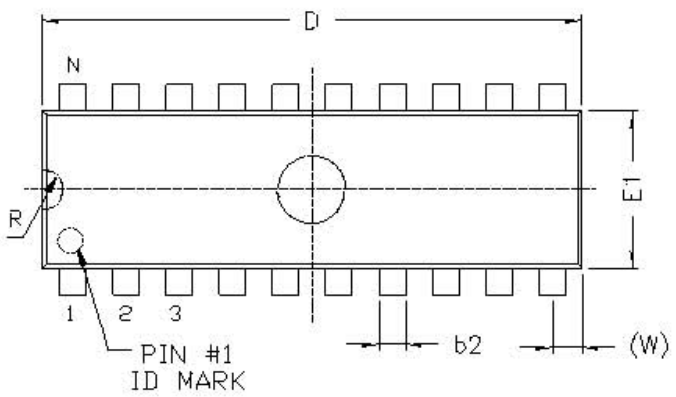
Unlike the DS1232, the **SP705-708/813L/813M** series has a separate watchdog output pin $\overline{\text{WDO}}$ which can be simply connected to the $\overline{\text{MR}}$ input to generate a Reset signal. The DS1232 has pin selectable features, while the **SP705-708/813L/813M** series has more fixed functions of reset threshold and watchdog time-out delay. For most applications, the fixed functions will be preferred, with the benefit of reduced cost due to a less complex part. In addition, the **SP705-708/813L/813M** series has a power fail input and output function not available with the DS1232 that is useful for monitoring systems with unregulated supply voltages. The **SP705-708/813L/813M** series is available in one of the industry's smallest space-saving package sizes, the µSOIC.

Function	Dallas DS1232LP/LPS		Sipex Alternative Part Number			
	Pin Number DIP or SOIC	Pin Description	Sipex Part Number	Pin Number		Pin Description
				DIP or SOIC	µSOIC	
Manual Reset	1	$\overline{\text{PBRST}}$	**SP705-708/ 813L/813M**	1	3	$\overline{\text{MR}}$
WDI Time Delay Set	2	TD	**SP705-708/ 813L/813M**	N/A	N/A	1.6sec by design
V_{CC} Trip 4.6V	3	TOL=GND	**SP705/707/ 813L**	N/A	N/A	4.6V by design
V_{CC} Trip 4.4V	3	TOL=V_{CC}	**SP706/708/ 813M**	N/A	N/A	4.4V by design
Ground	4	GND	**SP705-708/ 813L/813M**	3	5	GND
Reset Active HIGH	5	RST	**SP707/708**	8	2	RESET
Reset Active HIGH	5	RST	**SP813L/813M**	7	1	RESET
Reset Active LOW	6	$\overline{\text{RST}}$	**SP705-708**	7	1	$\overline{\text{RESET}}$
Watchdog Input	7	$\overline{\text{ST}}$ (H to L)	**SP705/706/ 813L/813M**	6	8	WDI (any trans.)
Voltage Input	8	V_{CC}	**SP705-708/ 813L/813M**	2	4	V_{CC}
Power Fail Input	N/A	N/A	**SP705-708/ 813L/813M**	4	6	PFI
Power Fail Output	N/A	N/A	**SP705-708/ 813L/813M**	5	7	$\overline{\text{PFO}}$
Watchdog Output	N/A	N/A	**SP705/706/ 813L/813M**	8	2	$\overline{\text{WDO}}$

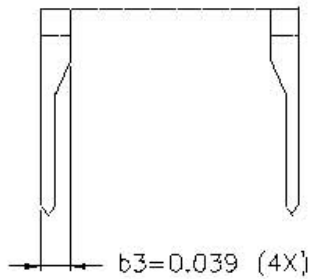
Table 2. Device Overview on Dallas Semiconductor

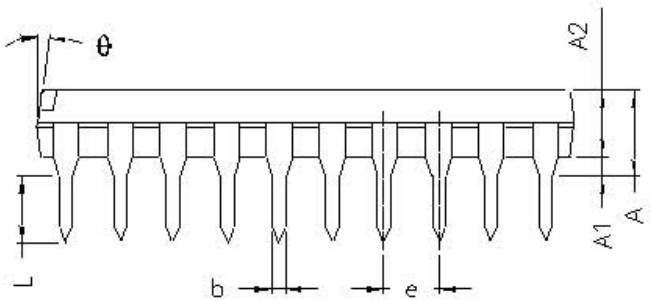
REVISION HISTORY			
REV.	DESCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	04/26/06	JL

REMARKS:
FOR 8LD AND 16LD
ALL END LEADS (4X)
ARE HALF LEAD TYPES

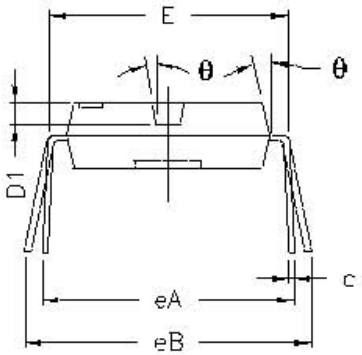


Top View





Side View

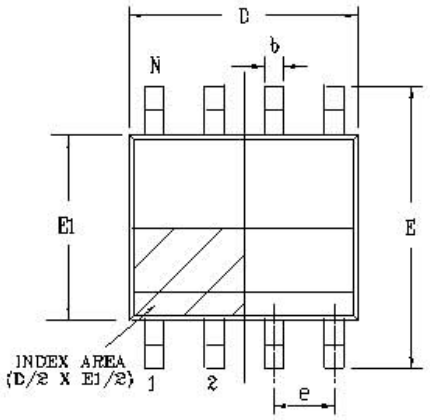


Front View

8 Pin PDIP JEDEC MS-001 Variation BA						
SYMBOLS	DIMENSIONS IN INCH (Control Unit)			DIMENSIONS IN MM (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	0.210	—	—	5.33
A1	0.015	—	—	0.38	—	—
A2	0.115	0.130	0.195	2.92	3.30	4.95
b	0.014	0.018	0.022	0.36	0.46	0.56
b2	0.045	0.060	0.070	1.14	1.52	1.78
c	0.008	0.010	0.014	0.20	0.25	0.36
D1	0.030	—	0.060	0.76	—	1.52
E	0.300	0.310	0.325	7.62	7.87	8.26
E1	0.240	0.250	0.280	6.10	6.35	7.11
e	0.100 BSC			2.54 BSC		
eA	0.300 BSC			7.62 BSC		
eB	—	—	0.430	—	—	10.92
L	0.115	0.130	0.150	2.92	3.30	3.81
W	0.075 REF			1.91 REF		
R	0.030 BSC			0.76 BSC		
θ	4°	7°	10°	4°	7°	10°
D	0.355	0.365	0.400	9.02	9.27	10.16
N	8			8		

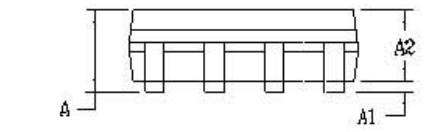
Solved by Sipex		SIPEX CORPORATION	
		8 PIN PDIP PACKAGE OUTLINE	
Packaging Approval:		Drawing No: 8-PIN PDIP	
By: JL	Date: 04/26/06	Revision: A	Sheet: 1 OF 1

REVISION HISTORY			
REV.	DESCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	08/16/05	JL
B	DRAWING FORMAT MODIFICATION	07/19/08	JL

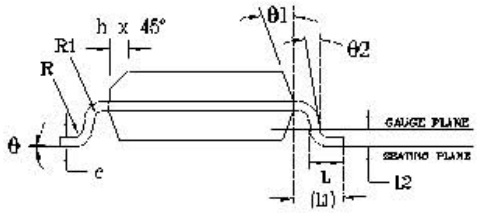


Top View

8 Pin SOICN JEDEC MS-012 Variation AA						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	—	1.75	0.053	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	1.25	—	1.65	0.049	—	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
L1	1.04 REF			0.041 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
θ2	0°	—	—	0°	—	—
D	4.90 BSC			0.193 BSC		
N	8			8		



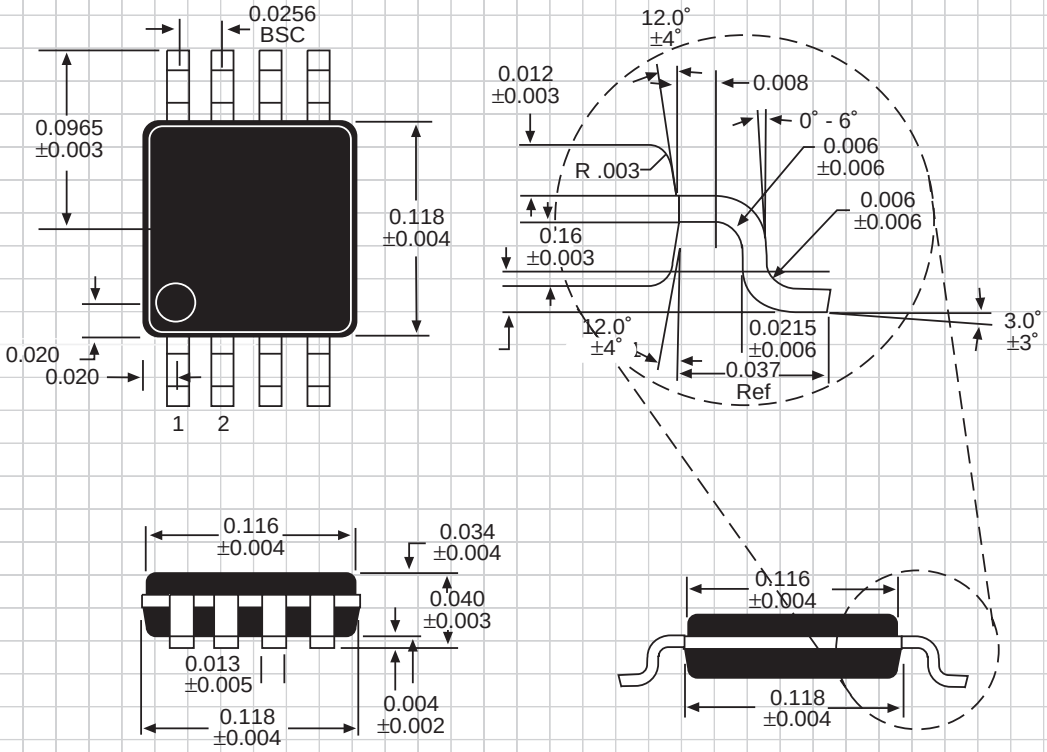
Side View



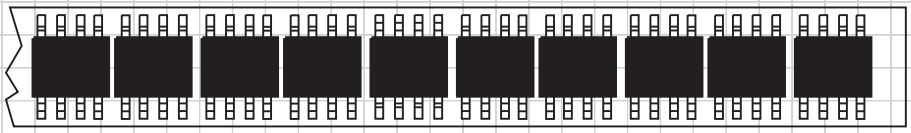
Front View

Solved by Sipex	SIPEX CORPORATION	
	8 PIN SOICN PACKAGE OUTLINE	
Packaging Approval:	Drawing No: 8-PIN SOICN	
By: JL / Date: 07/19/08	Revision: B	Sheet: 1 OF 1

PACKAGE: PLASTIC MICRO SMALL OUTLINE (µSOIC)



All package dimensions in inches



50 µSOIC devices per tube

ORDERING INFORMATION

Model	Temperature Range	Package
SP705CP	0°C to +70°C	8–pin Plastic DIP
SP705CN	0°C to +70°C	8–pin Narrow SOIC
SP705CU	0°C to +70°C	8-pin µSOIC
SP705EP	-40°C to +85°C	8–pin Plastic DIP
SP705EN	-40°C to +85°C	8–pin Narrow SOIC
SP705EU	-40°C to +85°C	8-pin µSOIC
SP706CP	0°C to +70°C	8–pin Plastic DIP
SP706CN	0°C to +70°C	8–pin Narrow SOIC
SP706CU	0°C to +70°C	8-pin µSOIC
SP706EP	-40°C to +85°C	8–pin Plastic DIP
SP706EN	-40°C to +85°C	8–pin Narrow SOIC
SP706EU	-40°C to +85°C	8-pin µSOIC
SP707CP	0°C to +70°C	8–pin Plastic DIP
SP707CN	0°C to +70°C	8–pin Narrow SOIC
SP707CU	0°C to +70°C	8-pin µSOIC
SP707EP	-40°C to +85°C	8–pin Plastic DIP
SP707EN	-40°C to +85°C	8–pin Narrow SOIC
SP707EU	-40°C to +85°C	8-pin µSOIC
SP708CP	0°C to +70°C	8–pin Plastic DIP
SP708CN	0°C to +70°C	8–pin Narrow SOIC
SP708CU	0°C to +70°C	8-pin µSOIC
SP708EP	-40°C to +85°C	8–pin Plastic DIP
SP708EN	-40°C to +85°C	8–pin Narrow SOIC
SP708EU	-40°C to +85°C	8-pin µSOIC
SP813LCP	0°C to +70°C	8–pin Plastic DIP
SP813LCN	0°C to +70°C	8–pin Narrow SOIC
SP813LCU	0°C to +70°C	8-pin µSOIC
SP813LEP	-40°C to +85°C	8–pin Plastic DIP
SP813LEN	-40°C to +85°C	8–pin Narrow SOIC
SP813LEU	-40°C to +85°C	8-pin µSOIC
SP813MCP	0°C to +70°C	8–pin Plastic DIP
SP813MCN	0°C to +70°C	8–pin Narrow SOIC
SP813MCU	0°C to +70°C	8-pin µSOIC
SP813MEP	-40°C to +85°C	8–pin Plastic DIP
SP813MEN	-40°C to +85°C	8–pin Narrow SOIC
SP813MEU	-40°C to +85°C	8-pin ¨µSOIC

Please consult the factory for pricing and availability on a Tape-On-Reel option.

Sipex Corporation

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sales@sipex.com

233 South Hillview Drive
Milpitas, CA 95035
TEL: (408) 934-7500
FAX: (408) 935-7600

Available in lead free packaging. To order, add "-L" suffix to the part number. Example: SP813MEU /TR=Tape & Reel. SP813MEU-L/TR = lead free.