## SP5511



### **Bidirectional I<sup>2</sup>C Bus 4-Address Synthesiser**

DS3090 - 4.0 January 1997

The SP5511 is a single-chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard  $l^2C$  BUS format. In 18-lead plastic DIL package, the SP5511 has three addressable current-limited output ports (P0-P3) and four bi-directional output ports (P0-P2) and four addressable bi-directional open-collector ports (P4-P7) of which P6 is also a 3-bit 5-level ADC input. The information on these ports can be read via the  $l^2C$  BUS. The SP5511S is a variant in a 16-lead miniature plastic package, without P0-P2 but functionally identical in other respects to the SP5511.

The device has four programmable  $I^2C$  BUS addresses, allowing two or more synthesisers to be used in a system.

#### **FEATURES**

- Complete 1.3GHz Single Chip System
- Programmable via the I<sup>2</sup>C BUS
- Low Power Consumption (240mW Typ.)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 7 Controllable Outputs, 4 Bi-directional (SP5511)
- 4 Bi-directional Controllable Outputs (SP5511S)
- 5-Level ADC
- Variable I<sup>2</sup>C BUS Address for Picture in Picture TV
- ESD Protection \*
  - \* Normal ESD handling precautions should be observed.

#### **APPLICATIONS**

Cable Tuning SystemsVCRs

#### **ORDERING INFORMATION**

SP5511 NA DP (18-lead plastic package) SP5511S NA MP (16-lead miniature plastic package)

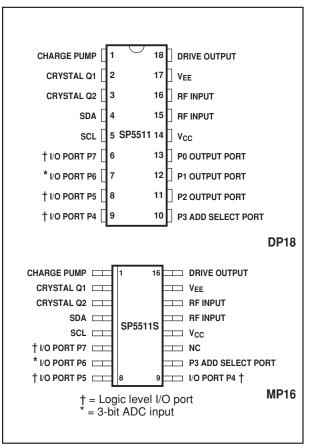


Fig. 1 Pin connections – top view

#### SP5511

#### **ELECTRICAL CHARACTERISTICS**

 $T_{AMB} = -10^{\circ}$ C to  $+80^{\circ}$ C,  $V_{CC} = +4^{\circ}$ SV to  $+5^{\circ}$ SV. All pin references are to the SP5511 (DP18 package). These Characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated. Reference frequency 4MHz unless otherwise stated.

Characteristic	Pin		Value		Units	Conditions	
Characteristic	Pin	Min.	Тур.	Max.	Units	Conditions	
Supply current Prescaler input voltage	14 15,16	12.5	48	60 300	mA mVrms	V <sub>CC</sub> = 5V 80MHz to 1GHz	
	-, -	30		300	mVrms	1.3GHz, see Fig. 5	
Prescaler input impedance	15,16		50		Ω		
Prescaler input capacitance			2		pF		
SDA, SCL							
Input high voltage	4,5	3		5.2	V		
Input low voltage	4,5	0		1.5	V		
Input high current	4,5			10	μA	Input voltage = V <sub>CC</sub>	
Input low current	4,5			-10	μA	Input voltage = 0V	
Leakage current	4,5			10	μΑ	When $V_{CC} = 0V$	
SDA							
Output voltage	4			0.4	V	Sink current = 3mA	
Charge pump current low	1		±50		μA	Byte 4, bit 2 = 0, pin 1 = 2V	
Charge pump current high	1		±170		μA	Byte 4, bit 2 = 1, pin 1 = 2V	
Charge pump output leakage current	1			±5	nA	Byte 4, bit 4 = 1, pin 1 = 2V	
Charge pump drive output current	18	500				V pin 18 = 0·7V	
Charge pump amplifier gain			6400				
Recommended crystal series resistance		10		200	Ω	Parallel resonant crystal (note 2)	
Crystal oscillator drive level			40		mV p-p		
Crystal oscillator negative resistance	2	750			Ω		
Output Ports							
P0-P2 sink current (see note 1)	11-13	0.7	1	1.5	mA	$V_{OUT} = 12V$	
P0-P2 leakage current (see note 1)	11-13			10	μA	$V_{OUT} = 13.2V$	
P4-P7 sink current	6-9	10			mA	$V_{OUT} = 0.7V$	
P4-P7 leakage current	6-9			10	μA	$V_{OUT} = 13.2V$	
Input Ports							
P3 input current high	10			1	mA	V pin 10 = 13·2V	
P3 input current low	10			-0.2	mA	V pin 10 = 0V	
P4, P5, P7 input voltage low	6,8,9			0.8	V V		
P4, P5, P7 input voltage high	6,8,9	2.7					
P6 input current high	7			+10	μΑ	See Table 3 for ADC levels	
P6 input current low	7			-10	μA		

NOTES

Ports P0-P2 not present on the SP5511S
 The maximum resistance quoted refers to all conditions, including start-up.

#### ABSOLUTE MAXIMUM RATINGS

All voltages are referred to  $V_{\text{EE}}$  and pin 3 at 0V

Parameter	P	in	Va	lue	Units	Conditions	
Falameter	SP5511	SP5511S	Min.	Max.	Units	Conditions	
Supply voltage	14	12	-0.3	7	V		
RF input voltage	15,16	13,14		2.5	V р-р		
Port voltage	6-9,11-13	6-9	-0.3	14	V	Port in off state	
	6-9	6-9	-0.3	6	V	Port in on state	
	11-13	-	-0.3	14	V	Port in on state	
	10	10	-0.3	$V_{CC}+0.3$	V		
Total port output current	6-9,11-13	6-9		50	mA		
RF input DC offset	15-16	13-14	-0.3	$V_{CC}$ +0·3	V		
Charge pump DC offset	1	1	-0.3	$V_{CC}$ +0·3	V		
Drive output DC offset	18	16	-0.3	$V_{CC}$ +0·3	V		
Crystal oscillator DC offset	2	2	-0.3	$V_{CC}$ +0·3	V		
SDA, SCL input voltage	4,5	4,5	-0.3	V <sub>CC</sub> +0·3	V	With V <sub>CC</sub> applied	
			-0.3	5.5	V	V <sub>CC</sub> not applied	
Storage temperature			-55	+150	°C		
Junction temperature				+150	°C		
DP18 thermal resistance, chip-to-ambient				78	°C/W		
DP18 thermal resistance, chip-to-case				24	°C/W		
MP16 thermal resistance, chip-to-ambient				111	°C/W		
MP16 thermal resistance, chip-to-case				41	°C/W		
Power consumption at 5.5V				363	mW		

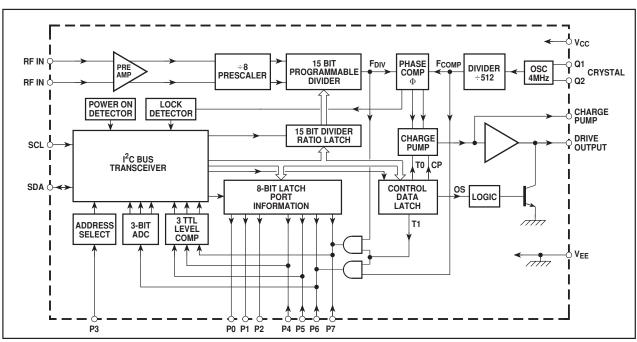


Fig. 2 Block diagram. (Ports P0-P2 not present on SP5511S)

#### SP5511

#### **FUNCTIONAL DESCRIPTION**

The SP5511 is programmed from an I<sup>2</sup>C BUS. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I<sup>2</sup>C Bus format. The synthesiser can either accept new data (write mode) or send data (read mode). The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I<sup>2</sup>C BUS system. Table 4 shows how the address is selected by applying a voltage to P3. The address input circuit is shown in Fig.6.The LSB of the address Byte (R/W) sets the device into read mode if it is high and write mode if it is low. When the SP5511 receives a correct address Byte it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data Bytes are programmed. When the SP5511 is programmed into the read mode the controlling device accepting the data must pull down the SDA line during the following acknowledge period to read another status Byte.

#### WRITE MODE (FREQUENCY SYNTHESIS)

When the device is in the write mode Bytes 2+3 select the synthesised frequency while Bytes 4+5 select the output port states and charge pump information.

Once the correct address is received and acknowledged, the first Bit of the next Byte determines whether that Byte is interpreted as Byte 2 or 4, a logic 0 for frequency information and a logic 1 for charge pump and output port information. Additional data Bytes can be entered without the need to readdress the device until an  $I^2C$  stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid-byte (i.e., by another device on the bus) then the previously programmed byte is maintained.

Frequency data from Bytes 2 and 3 is stored in a 15-bit shift register and is used to control the division ratio of the 15-bit programmable divider which is preceded by a divide-by-8 prescaler and amplifier to give excellent sensitivity at the local oscillator input; see Fig 5. The input impedance is shown in Figs. 7 and 8.

The programmed frequency can be calculated by multiplying the programmed division ratio by 8 times the comparison frequency  $\rm F_{\rm COMP}.$ 

When frequency data is entered, the phase comparator, via the charge pump and varactor drive amplifier, adjusts the

local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2 or provided by an onchip 4MHz crystal controlled oscillator.

Note that the comparison frequency is 7.8125kHz when a 4MHz reference is used.

Bit 2 of Byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for  $\pm 170 \mu A$  and a logic 0 for  $\pm 50 \mu A$ , allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. Bit 4 of Byte 4 (T0) disables the charge pump if set to a logic 1. Bit 8 of Byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1. Bit 3 of Byte 4 (T1) selects a test mode where the phase comparator inputs are available on P6 and P7, a logic 1 connects  $F_{COMP}$  to P6 and  $F_{DIV}$  to P7.

Byte 5 programs the output ports P0-P7, a logic 0 for a high impedance output, logic 1 for low impedance (on).

#### **READ MODE**

When the device is in the read mode the status data read from the device on the SDA line takes the form shown in Table 2.

Bit 1 (POR) is the power on reset indicator and is set to a logic 1 if the power supply to the device has dropped below a nominal 3V and the programmed information lost (e.g., when the device is initially turned on). The POR is set to 0 when the read sequence is terminated by a stop command. The outputs are all set to high impedance when the device is initially powered up. Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2, I1, I0) show the status of the I/O Ports P7, P5 and P4 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic1). These inputs will then respond to data complying with standard TTL voltage levels. Bits 6, 7 and 8 (A2,A1,A0) combine to give the output of the 5-level ADC.

The 5-level ADC can be used to feed AFC information to the microprocessor from the IF section of the television, as illustrated in Fig. 4.

Addre	ess			1	1	0	0	0	MA1	MA0	0	Α	Byte 1
		nable	divider	0	2 <sup>14</sup>	2 <sup>13</sup>	2 <sup>12</sup>	211	2 <sup>10</sup>	2 <sup>9</sup>	2 <sup>8</sup>	A	Byte 2
-			divider	2 <sup>7</sup>	- 2 <sup>6</sup>	- 2 <sup>5</sup>	_ 2 <sup>4</sup>	- 2 <sup>3</sup>	- 2 <sup>2</sup>	_ 2 <sup>1</sup>	2 <sup>0</sup>	A	Byte 3
			nd test bits	- 1	CP		ТО	1	1	1	_ OS	A	Byte 4
I/O port control bits			P7	P6	P5	P4	P3	P2*	P1*	P0*	A	Byte 5	
			Table 1	Write	data f	ormat	(MSB	trans	mitted	l first)			
										,			
Addre	ess			1	1	0	0	0	MA1	MA0	1	Α	Byte 1
Status	s by	te		POR	FL	12	11	10	A2	A1	A0	А	Byte 2
				Ta	ble 2	Read	data f	ormat					
						_							
A2	A1	A0	Voltage in	nput t	o P6								
<b>A2</b>	<b>A1</b>	<b>A0</b> 0	Voltage in 0.6V <sub>CC</sub> 1	-		-			MA1	MA0	Volta	ge ing	out to P3
			0.6V <sup>CC</sup> 1	to 13:	2V	_			<b>MA1</b>	<b>MA0</b>			
1	0	0	0.6V <sub>CC</sub> 1	to 13: to 0:6	2V V <sub>CC</sub>	_					0\	∕ to 0·	1V <sub>CC</sub>
1 0	0 1	0	$0.6V_{CC}$ $0.45V_{CC}$ $0.3V_{CC}$ to	to 13: to 0:6 0 0:45	2V V <sub>CC</sub> V <sub>CC</sub>				0	0	0\ C	/ to 0∙ pen c	1V <sub>CC</sub> ircuit
1 0 0	0 1 1	0 1 0	0.6V <sub>CC</sub> 1	to 13: to 0:6 0 0:45 to 0:3	2V V <sub>cc</sub> V <sub>cc</sub>				0	0	0\ C 0·4V	/ to 0∙ pen c	ircuit 0·6V <sub>cc</sub> †
1 0 0 0	0 1 1 0	0 1 0 1 0	$0.6V_{CC} + 0.000$ $0.45V_{CC} + 0.000$ $0.3V_{CC} + 0.000$ $0.15V_{CC} + 0.000$ $0.000 + 0.000$	to 13. to 0.6 0.45 to 0.3 0.15V <sub>0</sub>	2V V <sub>cc</sub> V <sub>cc</sub>				0 0 1 1	0 1 0 1	0\ C 0·4V 0·\$	V to 0∙ Open c C <sub>CC</sub> to 0 OV <sub>CC</sub> t	1V <sub>CC</sub> ircuit 0·6V <sub>CC</sub> †
1 0 0 0	0 1 1 0 0	0 1 0 1 0	$0.6V_{CC} + 0.000$ $0.45V_{CC} + 0.000$ $0.3V_{CC} + 0.000$ $0.15V_{CC} + 0.000$ $0.000 + 0.000$ $0.000 + 0.000$	to 13. to 0.6 0.45 to 0.3 0.15V <sub>c</sub>	2V V <sub>cc</sub> V <sub>cc</sub> V <sub>cc</sub>		it		0 0 1 1	0 1 0 1	0\ C 0·4V 0·\$	V to 0∙ Open c C <sub>CC</sub> to 0 OV <sub>CC</sub> t	$1V_{CC}$ ircuit $0.6V_{CC}^{\dagger}$ o $V_{CC}$
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 1 0 0	0 1 0 7 7 able	$0.6V_{CC} + 0.000$ $0.45V_{CC} + 0.000$ $0.3V_{CC} + 0.000$ $0.15V_{CC} + 0.000$ $0.000 + 0.000$ $0.000 + 0.000$	to 13: to 0:6 0 0:45 to 0:3 0:15V <sub>0</sub> /s	2V V <sub>cc</sub> V <sub>cc</sub> V <sub>cc</sub>	•		(see	0 0 1 1 <i>Ta</i>	0 1 0 1 able 4	0\ C 0·4V 0·\$	V to 0∙ Open c C <sub>CC</sub> to 0 OV <sub>CC</sub> t	$1V_{CC}$ ircuit $0.6V_{CC}^{\dagger}$ o $V_{CC}$
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 1 0 0	0 1 0 7 <i>Table</i>	0.6V <sub>CC</sub> 1 0.45V <sub>CC</sub> 1 0.3V <sub>CC</sub> tc 0.15V <sub>CC</sub> 1 0V to 0 0 3 ADC level	to 13: to 0:6 0 0:45 to 0:3 0:15V <sub>c</sub> /s Ack	2V V <sub>cc</sub> V <sub>cc</sub> V <sub>cc</sub>	addres	ss bits		0 0 1 1 <i>Ta</i>	0 1 0 1 able 4	0\ C 0·4V 0·\$	V to 0∙ Open c C <sub>CC</sub> to 0 OV <sub>CC</sub> t	$1V_{CC}$ ircuit $0.6V_{CC}^{\dagger}$ o $V_{CC}$
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 1 0 0	0 1 0 7 <i>Table</i>	0.6V <sub>CC</sub> 1 0.45V <sub>CC</sub> 1 0.3V <sub>CC</sub> to 0.15V <sub>CC</sub> 1 0V to 0 0 3 ADC level	to 13: to 0.6 0.45 to 0.3 $0.15V_{c}$ s r/s $V_{c}$ Var Cha	2V V <sub>CC</sub> V <sub>CC</sub> V <sub>CC</sub> xnowle	addres ump c	ss bits current		0 0 1 1 <i>Ta</i>	0 1 0 1 able 4	0\ C 0·4V 0·\$	V to 0∙ Open c C <sub>CC</sub> to 0 OV <sub>CC</sub> t	$1V_{CC}$ ircuit $0.6V_{CC}^{\dagger}$ o $V_{CC}$
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 1 0 0 <b>A</b> MA CP	0 1 0 <i>Table</i>	0.6V <sub>CC</sub> 1 0.45V <sub>CC</sub> 1 0.3V <sub>CC</sub> tc 0.15V <sub>CC</sub> 1 0V to 0 0 3 ADC level	to 13: to 0:6 0 0:45 to 0:3 1:15V <sub>c</sub> /s Ack Var Cha Tes	2V V <sub>CC</sub> V <sub>CC</sub> v <sub>CC</sub> cc xnowle iable a arge P	addres ump c e sele	ss bits current ction	selec	0 0 1 1 <i>Ta</i>	0 1 0 1 able 4	0\ C 0·4V 0·\$	V to 0∙ Open c C <sub>CC</sub> to 0 OV <sub>CC</sub> t	$1V_{CC}$ ircuit $0.6V_{CC}^{\dagger}$ o $V_{CC}$
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 0 <i>Table</i>	0.6V <sub>CC</sub> 1 0.45V <sub>CC</sub> 1 0.3V <sub>CC</sub> to 0.15V <sub>CC</sub> 1 0V to 0 <i>3 ADC level</i>	to 13: to 0:6 0:45 to 0:3 0:15V <sub>0</sub> /s Ack Var Cha Cha Cha Cha	2V V <sub>CC</sub> V <sub>CC</sub> V <sub>CC</sub> cc arge P arge P arge p actor	addres ump c e sele ump c drive (	ss bits current ction lisable Output	t selec	0 0 1 1 <i>Ta</i>	0 1 0 1 able 4 4)	0\ C 0·4V 0·\$	V to 0∙ Open c C <sub>CC</sub> to 0 OV <sub>CC</sub> t	$1V_{CC}$ ircuit $0.6V_{CC}^{\dagger}$ o $V_{CC}$
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 1 0 0 0 A MA CP T1 T0 OS P7,	0 1 0 <i>Table</i> 1, MA	0.6V <sub>cc</sub> 1 0.45V <sub>cc</sub> 1 0.3V <sub>cc</sub> to 0.15V <sub>cc</sub> 1 0V to 0 0 3 ADC level	to 13: to 0:6 0:45 to 0:3 0:15V <sub>0</sub> /s Ack Var Cha Cha Cha Cha	2V V <sub>CC</sub> V <sub>CC</sub> V <sub>CC</sub> xnowle iable a arge P st mod arge p	addres ump c e sele ump c drive (	ss bits current ction lisable Output	t selec	0 0 1 1 Table	0 1 0 1 able 4 4)	0\ C 0·4V 0·\$	V to 0∙ Open c C <sub>CC</sub> to 0 OV <sub>CC</sub> t	$1V_{CC}$ ircuit $0.6V_{CC}^{\dagger}$ o $V_{CC}$
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 0 <i>Table</i> , P6, F	0.6V <sub>CC</sub> 1 0.45V <sub>CC</sub> 1 0.3V <sub>CC</sub> to 0.15V <sub>CC</sub> 1 0V to 0 0 <i>3 ADC level</i> 0 <b>5</b> , P4, P1*, P0*	to 13. to 0.6 0.45 to 0.3 1.15V <sub>C</sub> 's Ack Var Cha Cha Cha Cha Cha Cha	2V V <sub>CC</sub> V <sub>C</sub>	addres ump c e sele ump d drive ( utput j	ss bits current ction lisable Output port st	t selec disat ates	0 0 1 1 Table	0 1 0 1 able 4 4)	0\ C 0·4V 0·\$	V to 0∙ Open c C <sub>CC</sub> to 0 OV <sub>CC</sub> t	$1V_{CC}$ ircuit $0.6V_{CC}^{\dagger}$ o $V_{CC}$
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 1 0 0 0 A MA CP T1 T0 OS P7,	0 1 0 <i>Table</i> , P6, F , P2*,	$0.6V_{CC} + 1$ $0.45V_{CC} + 1$ $0.3V_{CC} + 1$ $0.15V_{CC} + 1$ $0V + 10 + 0$ $0V + 10 + 0$ $0V + 0 + 0$	to 13: to 0:6 0 0:45 to 0:3 0:15Vc /s Ack Var Cha Cha Cha Cha Cha Cha Cha	2V V <sub>cc</sub> V <sub>c</sub> v <sub></sub>	addres ump c e sele ump d drive ( utput p n Rese	ess bits current ction lisable Dutput port st et indic	t selec disat ates cator	0 0 1 1 Table	0 1 0 1 able 4 4)	0\ C 0·4V 0·\$	V to 0∙ Open c C <sub>CC</sub> to 0 OV <sub>CC</sub> t	$1V_{CC}$ ircuit $0.6V_{CC}^{\dagger}$ o $V_{CC}$
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 1 0 0 0 A MA CP T1 T0 OS P7, P3, P0 FL	0 1 0 <i>Table</i> , P6, F , P2*,	0.6V <sub>CC</sub> 1 0.45V <sub>CC</sub> 1 0.3V <sub>CC</sub> to 0.15V <sub>CC</sub> 1 0V to 0 0 3 ADC level 0 5, P4, P1*, P0*	to 13: to 0:6 0 0:45 to 0:3 0:15Vc /s Ack Var Cha Cha Cha Cha Cha Cha Cha Cha Cha Cha	2V V <sub>cc</sub> V <sub>cc</sub> v v <sub>cc</sub> v	addres ump c e sele ump d drive ( utput j n Rese ck dete	es bits current oction lisable Dutput port st oort st et indic	t selec disat ates cator	0 0 1 1 Table	0 1 0 1 <i>able 4</i> 4)	0 C 0·4V 0·5	/ to 0· open c f <sub>cc</sub> to ( 9V <sub>cc</sub> t ss sel	1V <sub>CC</sub> ircuit 0·6V <sub>CC</sub> † o V <sub>CC</sub>

† Programmed by connecting a  $15k\Omega$  resistor between pin 10 and  $V_{CC}$  \* Don't care condition on SP5511S.

Fig. 3 Data formats

SP5511 APPLICATION

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6.

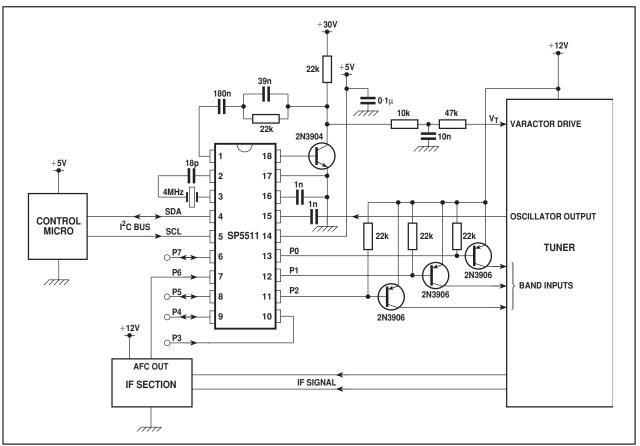


Fig. 4 Typical application

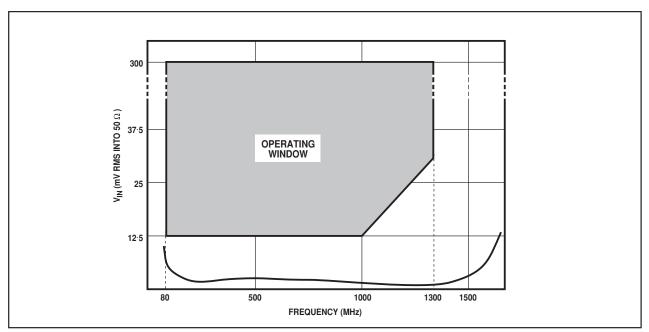


Fig. 5 Typical input sensitivity

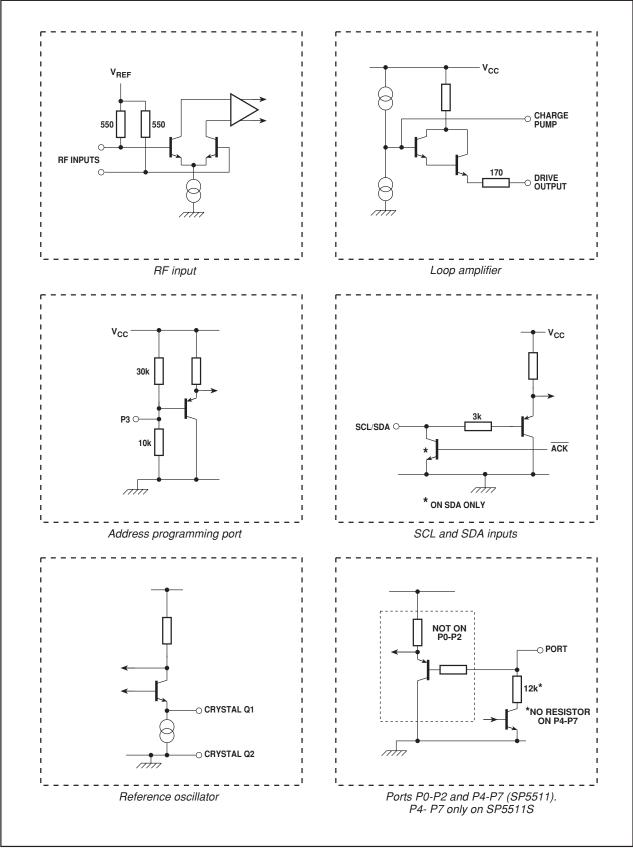


Fig. 6 SP5511 input/output interface circuits

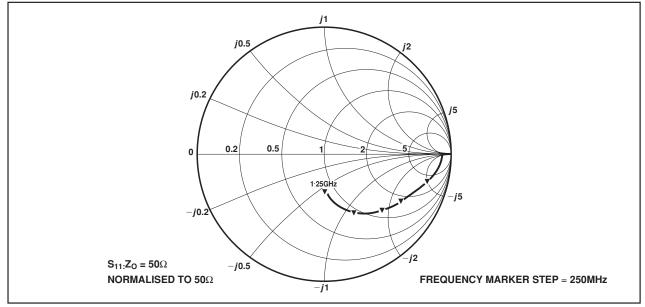


Fig. 7 Typical input impedance, SP5511

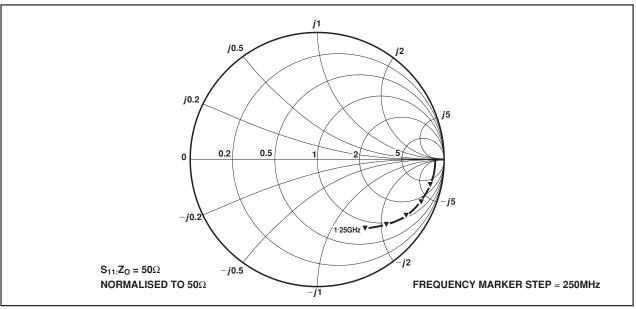
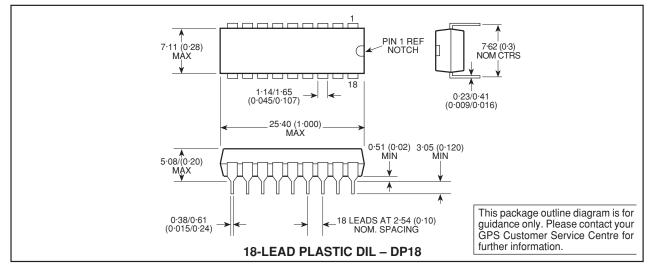


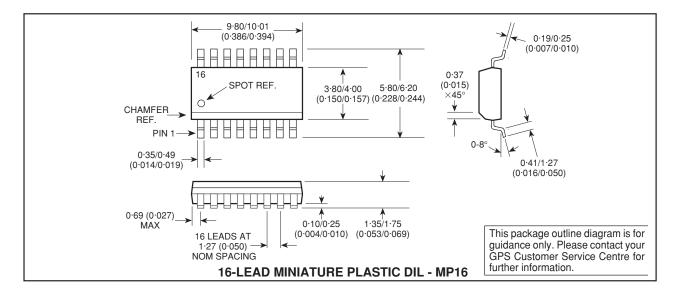
Fig. 8 Typical input impedance, SP5511S

#### PACKAGE DETAILS

SP5511

Dimensions are shown thus: mm (in).







# For more information about all Zarlink products visit our Web Site at

#### www.zarlink.com

Information relating to products and services furnished herein by Zarlink Semiconductor Inc. or its subsidiaries (collectively "Zarlink") is believed to be reliable. However, Zarlink assumes no liability for errors that may appear in this publication, or for liability otherwise arising from the application or use of any such information, product or service or for any infringement of patents or other intellectual property rights owned by third parties which may result from such application or use. Neither the supply of such information or purchase of product or service conveys any license, either express or implied, under patents or other intellectual property rights owned by Zarlink or licensed from third parties by Zarlink, whatsoever. Purchasers of products are also hereby notified that the use of product in certain ways or in combination with Zarlink, or non-Zarlink furnished goods or services may infringe patents or other intellectual property rights owned by Zarlink or licensed from third parties by Zarlink.

This publication is issued to provide information only and (unless agreed by Zarlink in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. The products, their specifications, services and other information appearing in this publication are subject to change by Zarlink without notice. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user's responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. Manufacturing does not necessarily include testing of all functions or parameters. These products are not suitable for use in any medical products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to Zarlink's conditions of sale which are available on request.

Purchase of Zarlink's I<sup>2</sup>C components conveys a licence under the Philips I<sup>2</sup>C Patent rights to use these components in and I<sup>2</sup>C System, provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips.

Zarlink, ZL and the Zarlink Semiconductor logo are trademarks of Zarlink Semiconductor Inc.

Copyright Zarlink Semiconductor Inc. All Rights Reserved.

TECHNICAL DOCUMENTATION - NOT FOR RESALE