

# **SP5510**

# 1.3GHz Bidirectional I<sup>2</sup>C BUS Controlled Synthesiser

Supersedes version in April 1994 Consumer IC Handbook, HB3120 - 2.0

DS2184 - 4.0 Janaury 1997

The SP5510 is a single-chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard  $I^2C$  BUS format. The device has four addressable current-limited output ports (P0-P3) and four bi-directional open-collector ports (P4-P7), one of which (P6) is also a 3-bit 5-level ADC input. The information on these ports can be read via the  $I^2C$  BUS. The SP5510S is a variant in a 16-lead miniature plastic package, without P0-P2 but functionally identical in other respects.

Both variants have one fixed I<sup>2</sup>C BUS address and three programmable addresses, allowing two or more synthesisers to be used in a system.

## **FEATURES**

- Complete 1.3GHz Single Chip System
- Programmable via the I<sup>2</sup>C BUS
- Low Power Consumption (215mW Typ.)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 8 Controllable Outputs, 4 Bi-directional(SP5510)
- 5 Controllable Outputs, 4 Bi-directional (SP5510S)
- 5-Level ADC
- Variable I<sup>2</sup>C BUS Address for Picture in Picture TV
- ESD Protection \*
  - \* Normal ESD handling precautions should be observed.

#### **APPLICATIONS**

- Cable Tuning Systems
- VCRs

#### **ORDERING INFORMATION**

SP5510 NA DP (18-lead plastic package) SP5510S NA MP (16-lead miniature plastic package)

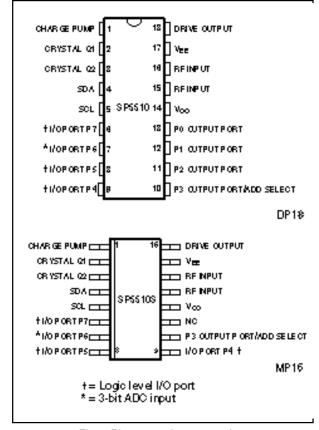


Fig. 1 Pin connections - top view

# SP5510

# **ELECTRICAL CHARACTERISTICS**

 $T_{AMB} = -10^{\circ}\text{C}$  to  $+80^{\circ}\text{C}$ ,  $V_{CC} = +4.5\text{V}$  to +5.5V. All pin references are to the SP5510 (DP18 package). These Characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated. Reference frequency 4MHz unless otherwise stated.

Chavastaviatia	Dim	Value			Heita	Oznatkiona	
Characteristic	Pin	Min.	Тур.	Max.	Units	Conditions	
Supply current	14		43	53	mA	V <sub>CC</sub> = 5V	
Prescaler input voltage	15,16	12.5		300	mVrms	50MHz to 1GHz	
Prescaler input voltage		30		300	mVrms	1·3GHz, see Fig. 5	
Prescaler input impedance	15,16		50				
Prescaler input capacitance			2		pF		
SDA, SCL							
Input high voltage	4,5	3		5.5	V		
Input low voltage	4,5	0		1.5	V		
Input high current	4,5			10	μΑ	Input voltage = V <sub>CC</sub>	
Input low current	4,5			-10	μΑ	Input voltage = 0V	
Leakage current	4,5			10	μΑ	When $V_{CC} = 0V$	
SDA							
Output voltage	4			0.4	V	Sink current = 3mA	
Charge pump current low	1		±50		μΑ	Byte 4, bit 2 = 0, pin 1 = 2V	
Charge pump current high	1		±170		μΑ	Byte 4, bit 2 = 1, pin 1 = 2V	
Charge pump output leakage current	1			±5	nA	Byte 4, bit 4 = 1, pin 1 = 2V	
Charge pump drive output current	18	500				V pin 18 = 0·7V	
Charge pump amplifier gain			6400				
Recommended crystal series resistance		10		200		Parallel resonant crystal (note 2)	
Crystal oscillator drive level			40		mV p-p		
Crystal oscillator negative resistance	2	750					
Output Ports							
P0-P3 sink current (see note 1)	10-13	0.7	1	1.5	mA	$V_{OUT} = 12V$	
P0-P3 leakage current (see note 1)	10-13			10	μΑ	V <sub>OUT</sub> = 13·2V	
P4-P7 sink current	6-9	10			mA	$V_{OUT} = 0.7V$	
P4-P7 leakage current	6-9			10	μΑ	$V_{OUT} = 13.2V$	
Input Ports							
P3 input current high	10			+10	μΑ	V pin 10 = 13·2V	
P3 input current low	10			-10	μΑ	V pin 10 = 0V	
P4, P5, P7 input voltage low	6,8,9			0⋅8	V		
P4, P5, P7 input voltage high	6,8,9	2.7			V		
P6 input current high	7			+10	μΑ	See Table 3 for ADC levels	
P6 input current low	7			-10	μΑ		

#### NOTES

Ports P0-P2 not present on the SP5510S.
 The maximum resistance quoted refers to all conditions, including start-up.

### **ABSOLUTE MAXIMUM RATINGS**

All voltages are referred to  $V_{\text{EE}}$  and pin 3 at 0V. Pin references are for SP5510 (DP18 package)

Parameter	Pin	Va	lue	Units	Conditions	
ratameter	- 111	Min.	Max.	Offics	Conditions	
Supply voltage	14	-0.3	7	V		
RF input voltage	15,16		2.5	V p-p		
Port voltage	6-13 6-9 10-13	-0·3 -0·3	14 6 14	V V V	Port in off state Port in on state Port in on state	
Total port output current	6-13		50	mA		
RF input DC offset	15-16	-0.3	V <sub>CC</sub> +0·3	V		
Charge pump DC offset	1	-0.3	V <sub>CC</sub> +0·3	V		
Drive output DC offset	18	-0.3	V <sub>CC</sub> +0·3	V		
Crystal oscillator DC offset	2	-0.3	V <sub>CC</sub> +0·3	V		
SDA, SCL input voltage	4,5	-0·3 -0·3	V <sub>CC</sub> +0·3 5·5	V V	With $V_{CC}$ applied $V_{CC}$ not applied	
Storage temperature		-55	+150	°C		
Junction temperature			+150	°C		
DP18 thermal resistance, chip-to-ambient DP18 thermal resistance, chip-to-case			78 24	°C/W °C/W		
MP16 thermal resistance, chip-to-ambient MP16 thermal resistance, chip-to-case			111 41	°C/W °C/W		
Power consumption at 5·5V			321	mW		

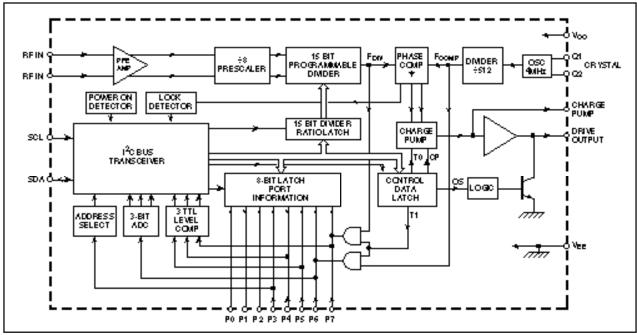


Fig. 2 Block diagram. (Ports P0-P2 not present on SP5510S)

#### **FUNCTIONAL DESCRIPTION**

The SP5510 is programmed from an I<sup>2</sup>C BUS. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I<sup>2</sup>C Bus format. The synthesiser can either accept new data (write mode) or send data (read mode). The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I<sup>2</sup>C BUS system. Table 4 shows how the address is selected by applying a voltage to P3. The LSB of the address Byte (R/W) sets the device into read mode if it is high and write mode if it is low. When the SP5510 receives a correct address Byte it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data Bytes are programmed. When the SP5510 is programmed into the read mode the controlling device accepting the data must pull down the SDA line during the following acknowledge period to read another status Byte.

#### WRITE MODE (FREQUENCY SYNTHESIS)

When the device is in the write mode Bytes 2+3 select the synthesised frequency while Bytes 4+5 select the output port states and charge pump information.

Once the correct address is received and acknowledged, the first Bit of the next Byte determines whether that Byte is interpreted as Byte 2 or 4, a logic 0 for frequency information and a logic 1 for charge pump and output port information. Additional data Bytes can be entered without the need to readdress the device until an I<sup>2</sup>C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid-byte (i.e., by another device on the bus) then the previously programmed byte is maintained.

Frequency data from Bytes 2 and 3 is stored in a 15-bit shift register and is used to control the division ratio of the 15-bit programmable divider which is preceded by a divide-by-8 prescaler and amplifier to give excellent sensitivity at the local oscillator input; see Fig 5. The input impedance is shown in Figs. 7 and 8.

The programmed frequency can be calculated by multiplying the programmed division ratio by 8 times the comparison frequency  $F_{\text{COMP}}$ .

When frequency data is entered, the phase comparator, via the charge pump and varactor drive amplifier, adjusts the

local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2 or provided by an on-chip 4MHz crystal controlled oscillator.

Note that the comparison frequency is 7.8125 kHz when a 4MHz reference is used.

Bit 2 of Byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for  $\pm 170\mu A$  and a logic 0 for  $\pm 50\mu A$ , allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. Bit 4 of Byte 4 (T0) disables the charge pump if set to a logic 1. Bit 8 of Byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1. Bit 3 of Byte 4 (T1) selects a test mode where the phase comparator inputs are available on P6 and P7, a logic 1 connects  $F_{COMP}$  to P6 and  $F_{DIV}$  to P7.

Byte 5 programs the output ports P0-P7, a logic 0 for a high impedance output, logic 1 for low impedance (on).

#### **READ MODE**

When the device is in the read mode the status data read from the device on the SDA line takes the form shown in Table 2.

Bit 1 (POR) is the power on reset indicator and is set to a logic 1 if the power supply to the device has dropped below a nominal 3V and the programmed information lost (e.g., when the device is initially turned on). The POR is set to 0 when the read sequence is terminated by a stop command. The outputs are all set to high impedance when the device is initially powered up. Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2, I1, I0) show the status of the I/O Ports P7, P5 and P4 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic1). These inputs will then respond to data complying with standard TTL voltage levels. Bits 6, 7 and 8 (A2,A1,A0) combine to give the output of the 5-level ADC.

The 5-level ADC can be used to feed AFC information to the microprocessor from the IF section of the television, as illustrated in Fig. 4.

#### **MSB LSB Address** 1 1 0 0 MA1 MA0 0 Byte 1 2<sup>14</sup> 2<sup>13</sup> 2<sup>12</sup> 2<sup>11</sup> 2<sup>10</sup> 2<sup>9</sup> Programmable divider 2<sup>8</sup> Byte 2 0 2<sup>0</sup> $2^7$ $2^6$ $2^5$ $2^4$ 2<sup>3</sup> $2^2$ Programmable divider 2<sup>1</sup> Byte 3 Α Charge pump and test bits 1 CP T1 T0 1 1 1 os Α Byte 4 P2\* P0\* P5 P4 P1\* Byte 5 I/O port control bits P7 P6 P3

Table 1 Write data format (MSB transmitted first)

Address	1	1	0	0	0	MA1	MA0	1	Α	Byte 1
Status byte	POR	FL	12	l1	10	A2	A1	Α0	Α	Byte 2

Table 2 Read data format

A2	<b>A</b> 1	Α0	Voltage input to P6	
1	0	0	0.6V <sub>CC</sub> to 13.2V	
0	1	1	0·45V <sub>CC</sub> to 0·6V <sub>CC</sub>	
0	1	0	0.3V <sub>CC</sub> to 0.45V <sub>CC</sub>	
0	0	1	0·15V <sub>CC</sub> to 0·3V <sub>CC</sub>	
0	0	0	0V to 0·15V <sub>CC</sub>	

Table	3	ADC:	levels
Iable	J	$\Delta D C$	16 4619

MA1	MAO	Voltage input to P3
0	0	0V to 0·2V <sub>CC</sub>
0	1	Always valid
1	0	0.3V <sub>CC</sub> to 0.7V <sub>CC</sub>
1	1	0.8V <sub>CC</sub> to 13.2V

Table 4 Address selection

A : Acknowledge bit

MA1, MA0 : Variable address bits (see Table 4)
CP : Charge Pump current select

T1 : Test mode selection
T0 : Charge pump disable

OS : Varactor drive Output disable Switch

P7, P6, P5, P4, : Control output port states

P3, P2\*, P1\*, P0\*

POR : Power On Reset indicator FL : Phase lock detect flag

**12, 11, 10** : Digital information from ports P7, P5 and P4 respectively

A2, A1, A0 : 5-level ADC data from P6 (see Table 3)

#### NOTE

\* Don't care condition on SP5510S.

Fig. 3 Data formats

# SP5510

# **APPLICATION**

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6.

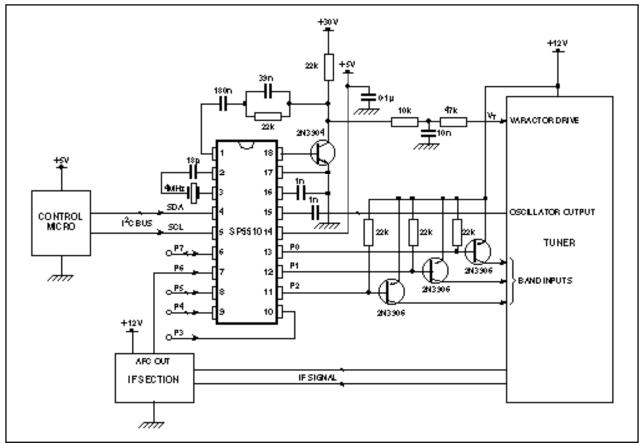


Fig. 4 Typical application

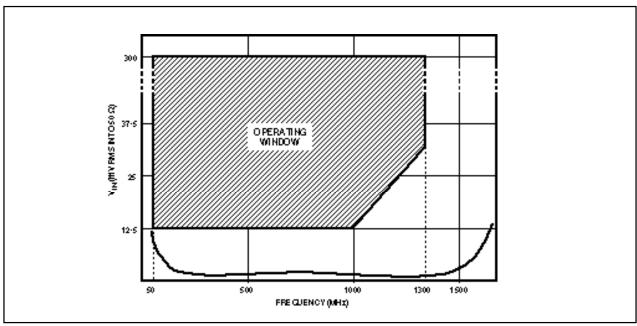


Fig. 5 Typical input sensitivity

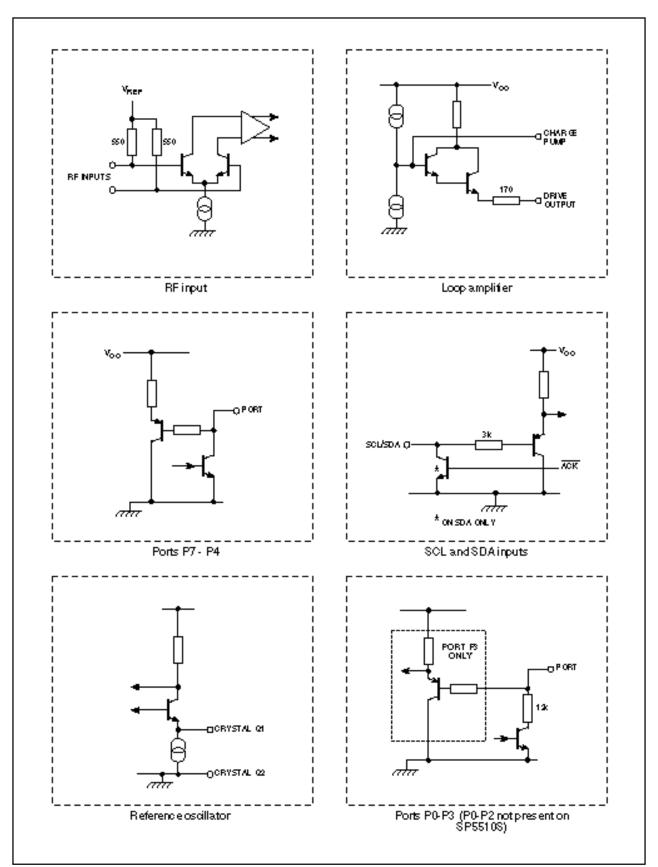


Fig. 6 SP5510 input/output interface circuits

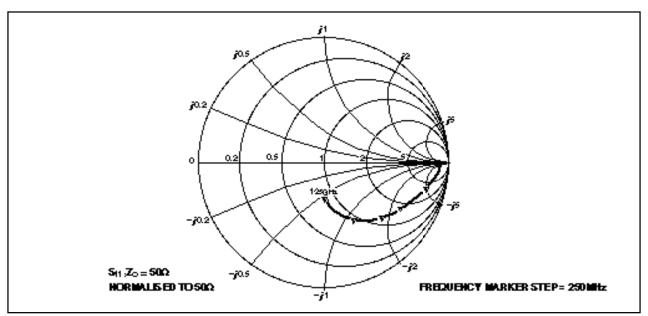


Fig. 7 Typical input impedance, SP5510

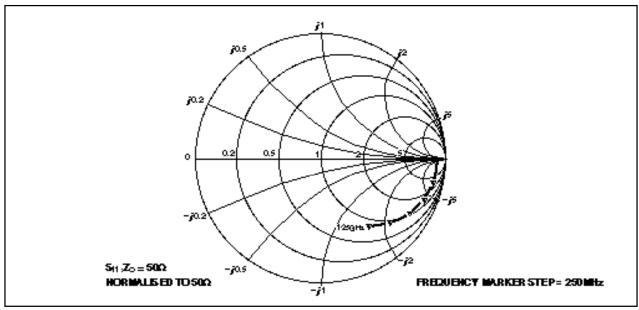


Fig. 8 Typical input impedance, SP5510S



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