

## OVERVIEW

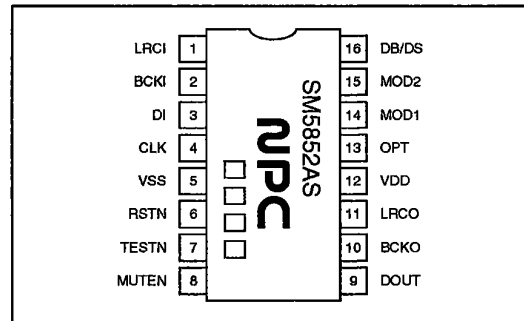
The SM5852AS is a digital signal processor IC that features Digital Dynamic Bass Boost (DDBB) and Digital Dynamic-range compression Sound (DDS) functions, making it ideal for use in digital audio playback equipment. It is TTL-compatible and is designed for a 44.1 kHz sampling frequency.

The SM5852AS operates from a 3.2 to 5.5 V supply and is available in 16-pin SOPs.

## FEATURES

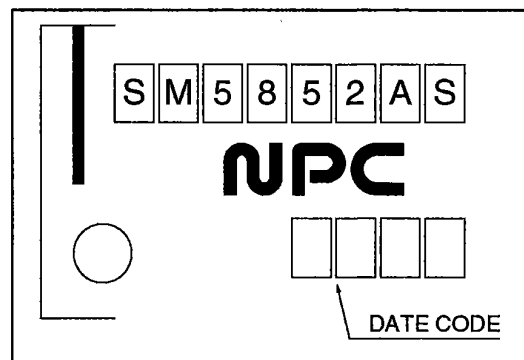
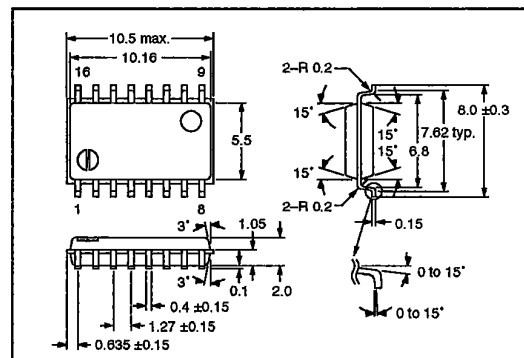
- 2-channel (L, R) signal processing
  - Digital Dynamic Bass Boost (DDBB) function
  - Digital Dynamic-range compression Sound (DDS) function
  - DDBB/DDS function switching
  - DDBB/DDS processing OFF mode
  - Variable dynamic gain selection (MIN, MID, MAX)
- System compatibility
  - 16-bit serial I/O interface
  - 2s complement data with msb first
  - 384fs system clock frequency
  - TTL-compatible
  - 3.2 to 5.5 V operation
  - 16-pin SOP
- Other features
  - Molygate<sup>®</sup> CMOS process
  - Soft mute and reset functions
  - High-precision arithmetic operation

## PINOUT

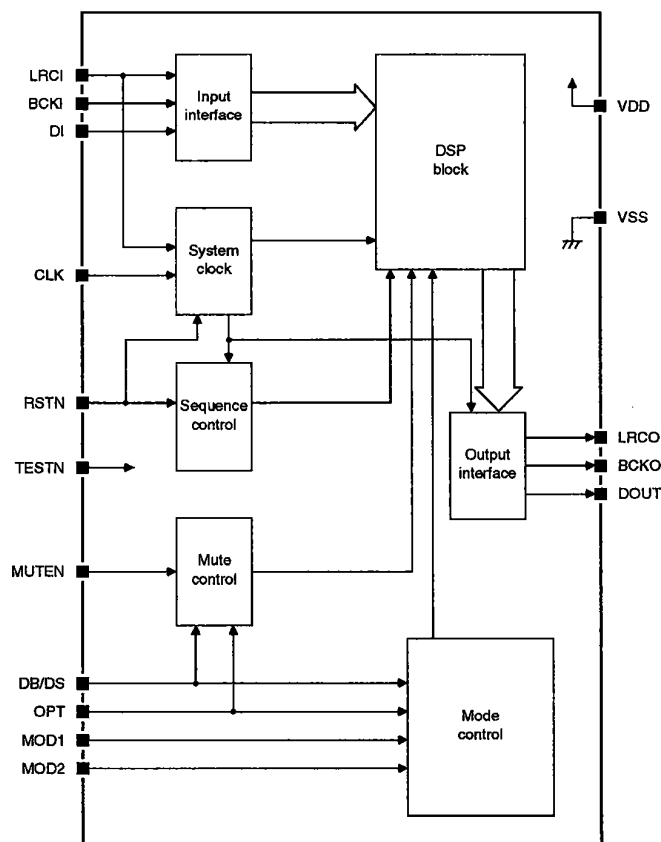


## PACKAGE DIMENSIONS AND MARKINGS

Unit: mm



## BLOCK DIAGRAM



## PIN DESCRIPTION

Number	Name	Description
1	LRCI	Sampling rate (fs) clock input. Internal pull-up resistor
2	BCKI	Bit-clock input. Internal pull-up resistor
3	DI	Serial data input. Internal pull-up resistor
4	CLK	System clock input
5	VSS	Ground
6	RSTN	Reset when LOW. Internal pull-up resistor
7	TESTN	Test when LOW. Internal pull-up resistor
8	MUTEN	Mute when LOW. Internal pull-up resistor
9	DOUT	Serial data output
10	BCKO	Bit-clock output
11	LRCO	Sampling rate (fs) clock output
12	VDD	3.2 to 5.5 V supply voltage
13	OPT	Tied to DB/DS. Internal pull-up resistor
14	MOD1	DDBB/DDS gain-select 1. Internal pull-up resistor

## SM5852AS

Number	Name	Description
15	MOD2	DDBB/DDS gain-select 2. Internal pull-up resistor
16	DB/DS	DDBB/DDS function switch. DDBB when HIGH and DDS when LOW. Internal pull-up resistor

### SPECIFICATIONS

#### Absolute Maximum Ratings

$$V_{SS} = 0 \text{ V}$$

Parameter	Symbol	Rating	Unit
Supply voltage range	$V_{DD}$	-0.3 to 7.0	V
Input voltage range	$V_I$	-0.3 to $V_{DD} + 0.3$	V
Power dissipation	$P_D$	250	mW
Operating temperature range	$T_{opr}$	-20 to 80	deg. C
Storage temperature range	$T_{stg}$	-40 to 125	deg. C
Soldering temperature	$T_{SLD}$	255	deg. C
Soldering time	$t_{SLD}$	10	s

#### Recommended Operating Conditions

$$V_{SS} = 0 \text{ V}, T_a = 25 \text{ deg. C}$$

Parameter	Symbol	Rating	Unit
Supply voltage	$V_{DD}$	5.0	V
Supply voltage range	$V_{DD}$	3.2 to 5.5	V

### DC Electrical Characteristics

#### Standard voltage operation

$$V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, V_{SS} = 0 \text{ V}, T_a = -20 \text{ to } 80 \text{ deg. C unless otherwise noted}$$

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Current consumption	$I_{DD}$	$V_{DD} = 5.0 \text{ V}$ . See note 1.	-	16	23	mA
LOW-level input voltage. See note 2.	$V_{IL}$		-	-	0.5	V
HIGH-level input voltage. See note 2.	$V_{IH}$		2.4	-	-	V
LOW-level output voltage. See note 3.	$V_{OL}$	$I_{OL} = 1.6 \text{ mA}$	-	-	0.4	V
HIGH-level output voltage. See note 3.	$V_{OH}$	$I_{OH} = -0.4 \text{ mA}$	2.5	-	-	V
CLK LOW-level input leakage current	$I_{LL}$	$V_I = 0 \text{ V}$	-	-	1.0	$\mu\text{A}$

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Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
CLK HIGH-level input leakage current. See note 2.	$I_{LH}$	$V_I = V_{DD}$	–	–	1.0	$\mu A$
Input current. See note 2.	$I_{IL}$	$V_I = 0 V$	–	–	20	$\mu A$

### Notes

1. Clock input frequency is 384fs (16.9344 MHz). Unloaded output. Measurements based on NPC specified input data.
2. Pins LRCl, BCKI, DI, RSTN, TESTN, MUTEN, OPT, MOD1, MOD2 and DB/DS
3. Pins LRcO, BCKO and DOUT

### Low-voltage operation

$V_{DD} = 3.2$  to  $4.5 V$ ,  $V_{SS} = 0 V$ ,  $T_a = -20$  to  $70 \text{ deg. C}$  unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Current consumption	$I_{DD}$	$V_{DD} = 3.4 V$ . See note 1.	–	7	10	mA
LOW-level input voltage. See note 2.	$V_{IL}$		–	–	0.5	V
HIGH-level input voltage. See note 2.	$V_{IH}$		2.4	–	–	V
LOW-level output voltage. See note 3.	$V_{OL}$	$I_{OL} = 0.8 \text{ mA}$	–	–	0.4	V
HIGH-level output voltage. See note 3.	$V_{OH}$	$I_{OH} = -0.2 \text{ mA}$	2.5	–	–	V
CLK LOW-level input leakage current	$I_{LL}$	$V_I = 0 V$	–	–	1.0	$\mu A$
CLK HIGH-level input leakage current. See note 2.	$I_{LH}$	$V_I = V_{DD}$	–	–	1.0	$\mu A$
Input current. See note 2.	$I_{IL}$	$V_I = 0 V$	–	–	12	$\mu A$

### Notes

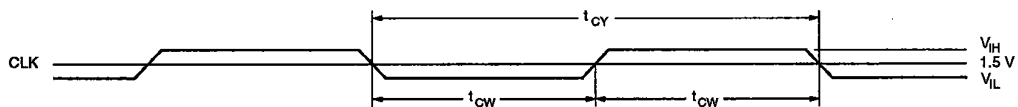
1. Clock input frequency is 384fs (16.9344 MHz). Unloaded output. Measurements based on NPC specified input data.
2. Pins LRCl, BCKI, DI, RSTN, TESTN, MUTEN, OPT, MOD1, MOD2 and DB/DS
3. Pins LRcO, BCKO and DOUT

**AC Electrical Characteristics**

**System clock (384fs)**

$V_{DD} = 3.2$  to  $4.5$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $70$  deg. C or  $V_{DD} = 4.5$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $80$  deg. C

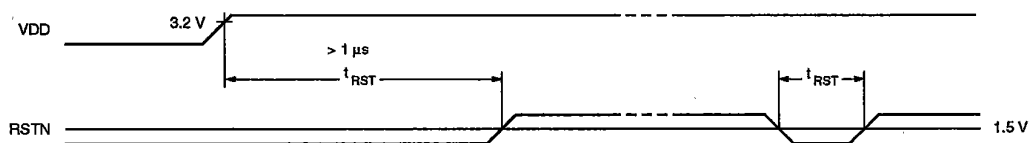
Parameter	Symbol	Rating			Unit
		min	typ	max	
Clock pulsewidth	$t_{CW}$	24	–	500	ns
Clock pulse cycle	$t_{CY}$	50	59	1000	ns



**System reset (RSTN)**

$V_{DD} = 3.2$  to  $4.5$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $70$  deg. C or  $V_{DD} = 4.5$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $80$  deg. C

Parameter	Symbol	Rating			Unit
		min	typ	max	
Reset pulsewidth at power-on	$t_{RST}$	1.0	–	–	$\mu$ s
Reset pulsewidth at other times		0.05	–	1.0	

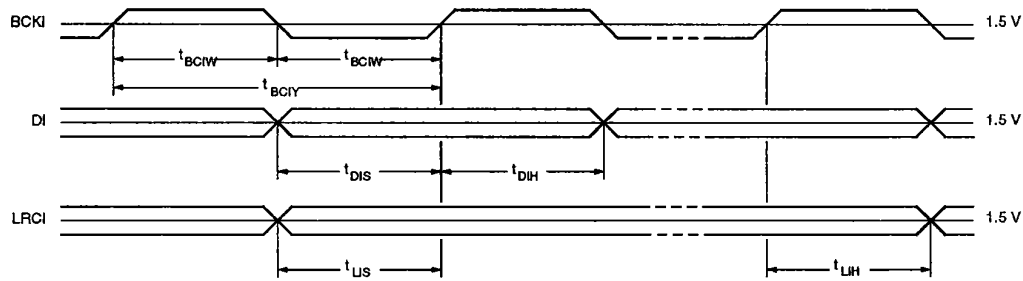


**Serial input timing**

$V_{DD} = 3.2$  to  $4.5$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $70$  deg. C or  $V_{DD} = 4.5$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $80$  deg. C

Parameter	Symbol	Rating			Unit
		min	typ	max	
BCKI pulsewidth	$t_{BCW}$	100	–	–	ns
BCKI pulse cycle	$t_{BCY}$	200	–	–	ns
DI setup time	$t_{DIS}$	75	–	–	ns
DI hold time	$t_{DIH}$	75	–	–	ns
LRCI setup time	$t_{LIS}$	75	–	–	ns
LRCI hold time	$t_{LIH}$	75	–	–	ns

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### DDBB/DDS function switch (DB/DS, OPT)

$V_{DD} = 3.2$  to  $4.5$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $70$  deg. C or  $V_{DD} = 4.5$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $80$  deg. C

Parameter	Symbol	Rating			Unit
		min	typ	max	
Minimum pulsewidth	$t_w$	2/fs	–	–	ns

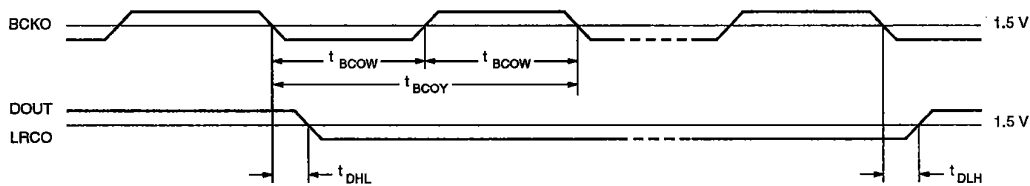
#### Note

If the level on DB/DS and OPT is changed, an input level of 2/fs ( $2 \times$  LRCI cycles) must be maintained. If the signal pulsewidth is less than 2/fs, the input signal may be ignored.

### Serial output timing

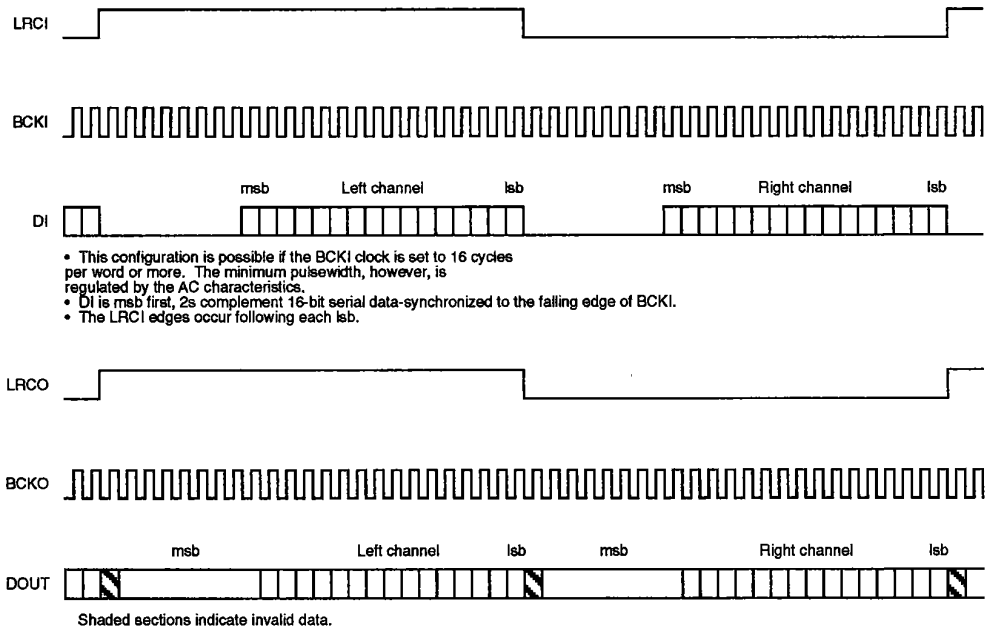
$V_{DD} = 3.2$  to  $4.5$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $70$  deg. C,  $C_L = 15$  pF or  $V_{DD} = 4.5$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $80$  deg. C,  $C_L = 15$  pF

Parameter	Symbol	Rating			Unit
		min	typ	max	
BCKO pulsewidth	$t_{BCOW}$	180	1/96fs	–	ns
BCKO pulse cycle	$t_{BCOY}$	400	1/48fs	–	ns
DOUT and LRCO output delay time	$t_{DHL}$	–20	–	60	ns
	$t_{DLH}$	–20	–	60	ns



**FUNCTIONAL DESCRIPTION**

**Input/Output Timing**



**Digital Dynamic Bass Boost (DDBB) Function**

The Digital Dynamic Bass Boost (DDBB) function enhances the low-frequency components of the left and right channels through filtering and signal processing. An application-specific, 3rd-order, IIR

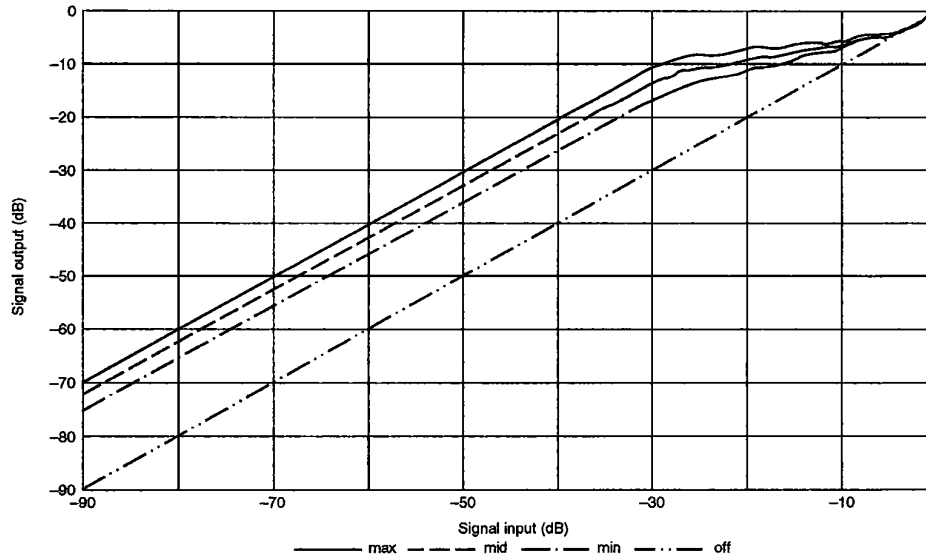
lowpass filter isolates the low-frequency components of the signal, which are then amplified according to DDBB/DDS gain select function states.

**Digital Dynamic Bass Boost (DDBB) gain selection truth table**

DB/DS, OPT	MOD1	MOD2	Gain mode
HIGH	LOW	LOW	MAX
HIGH	HIGH	LOW	MID
HIGH	LOW	HIGH	MIN
HIGH	HIGH	HIGH	OFF

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### Low frequency-band gain response



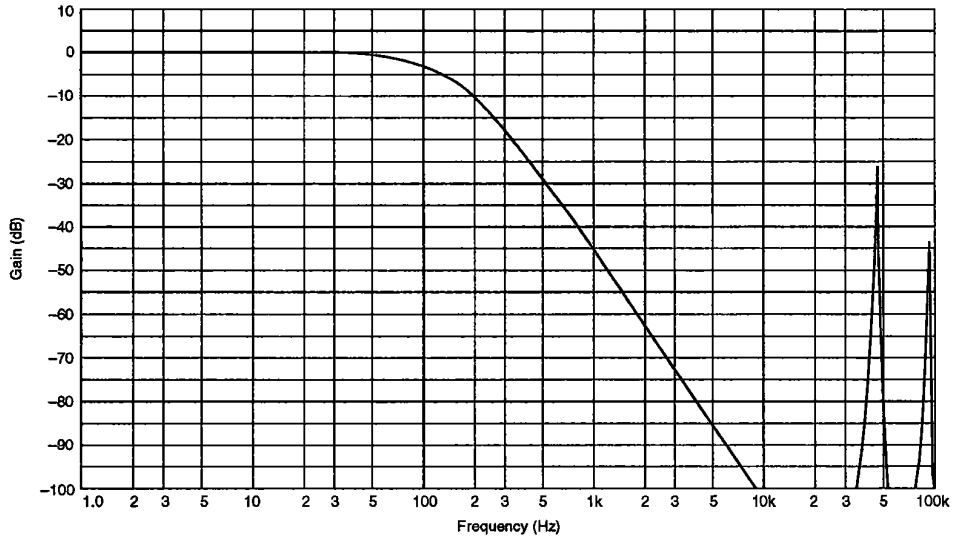
### Input/output gain characteristics

Gain mode	Maximum gain (dB)	Output level (dB)		
		For Input level less than -30.1 dB	For -30.1 to -3.4 dB input level	For -3.4 to 0 dB input level
MAX	20	20 linear	-10.1 to -3.4	linear
MID	17	17 linear	-13.1 to -3.4	linear
MIN	14	14 linear	-16.1 to -3.4	linear
OFF	0	linear	linear	linear

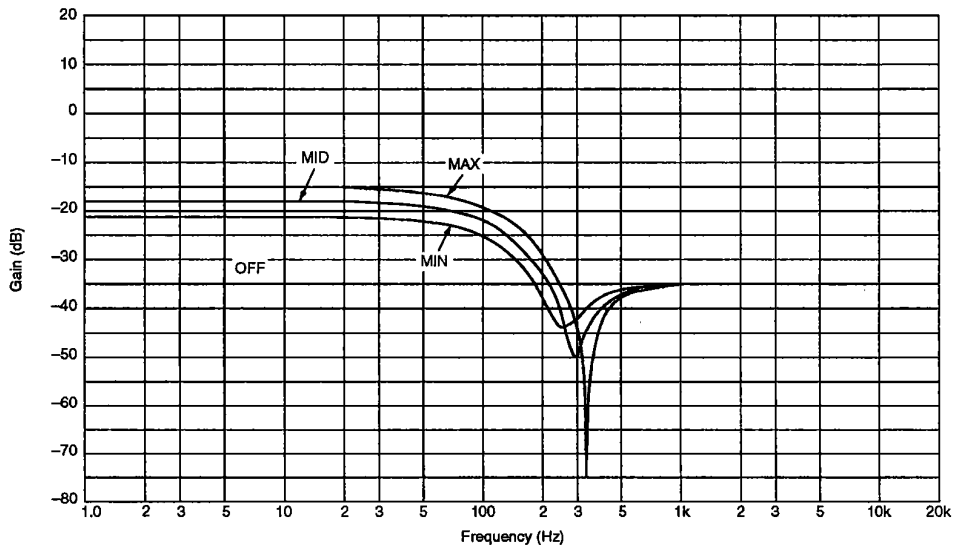


Filter characteristics

DDBB lowpass filter characteristics



DDBB mode general characteristics



## Digital Dynamic-range Compression Sound (DDS) Function

The Digital Dynamic-range compression Sound

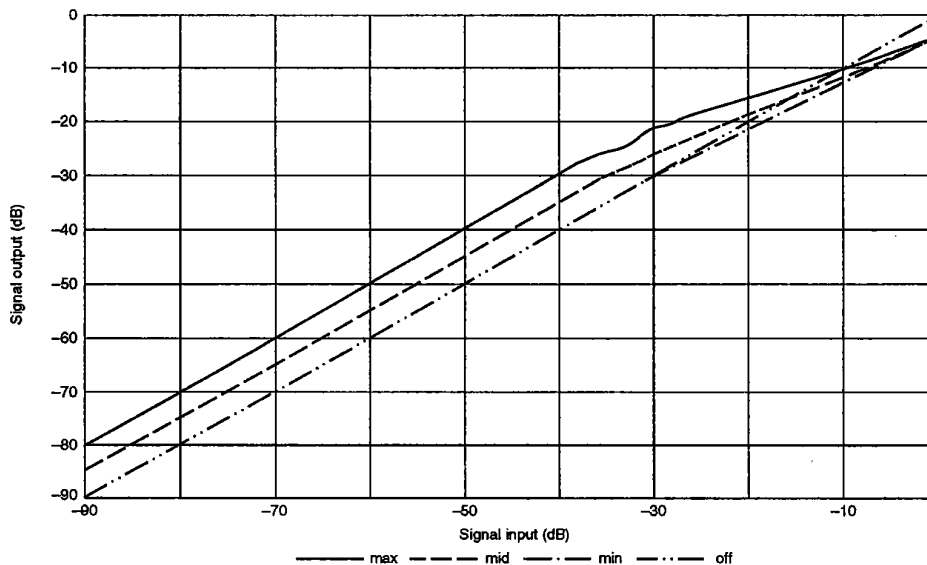
(DDS) function compresses the signal according to

the DDBB/DDS gain select function states.

Digital Dynamic-range compression Sound (DDS) gain selection truth table

DB/DS, OPT	MOD1	MOD2	Gain mode
LOW	LOW	LOW	MAX
LOW	HIGH	LOW	MID
LOW	LOW	HIGH	MIN
LOW	HIGH	HIGH	OFF

### Input/output gain response



### Input/output gain characteristics

Output level (dB)
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### DB/DS, OPT Switching Characteristics

To eliminate spurious signals or noise during DB/DS (and OPT) switching, the soft mute function attenuates the signal by  $\infty$  dB, before the internal setting of the DB/DS pin is changed. Once the internal setting has been changed, the soft mute function is cancelled. Consequently, it takes approximately 46.4 ms for the state of DB/DS to change.

If attenuation is initiated through the MUTEN function, the internal state for DB/DS changes instantaneously.

### Soft Mute Function

The soft mute function can be used to fade out or fade in the audio signal. By toggling MUTEN from HIGH to LOW, attenuation (from 0 to  $\infty$  dB) is achieved over approximately 23.2 ms. Toggling MUTEN from LOW to HIGH amplifies the audio

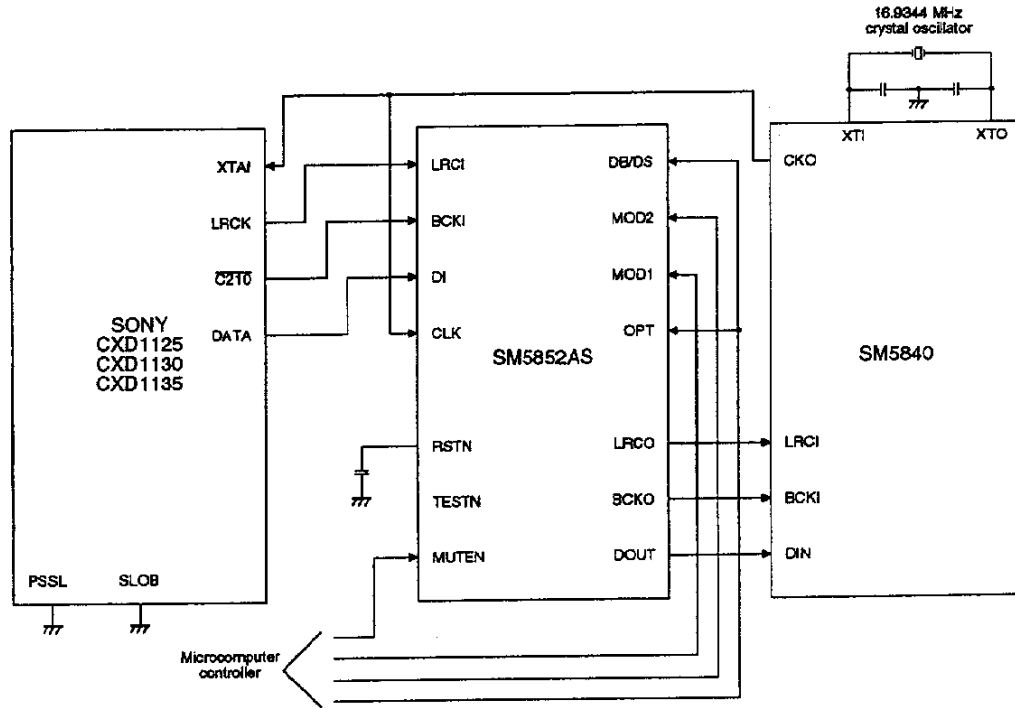
signal back to its minimum level of attenuation ( $\infty$  to 0 dB). If MUTEN is changed while attenuation is changing, the attenuation responds smoothly in the new direction.

### Reset Function


The RSTN pin should be set LOW at power-on or when synchronization is re-initiated. When RSTN is LOW, the internal clock is stopped. In this state, a through current of indeterminate value flows internally after a time interval of 1  $\mu$ s. Therefore, RSTN should not remain LOW for more than 1  $\mu$ s except during power-on.

When RSTN changes from LOW to HIGH, the reset function is cancelled, internal data is reset and an initialization routine runs for 4fs. Output data is muted until initialization has been completed.

TYPICAL APPLICATION



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