NIPPON PRECISION CIRCUITS LTD.

SM5874AM

D/A Converter

OVERVIEW

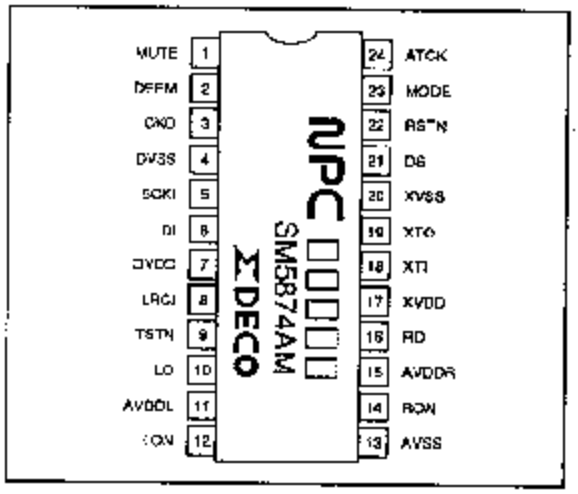
The SM5874AM is a third-order, 2-channel Σ-Δ (sigma-delta) D/A converter for digital audio applications. It incorporates an 8-times oversampling digital filter, deemphasis filter, attenuator and soft mute circuits. Double-speed dubbing is supported.

The SM5874AM operates from a 2.7 to 5.5 V voltage supply and is available in 24-pin SSOPs.

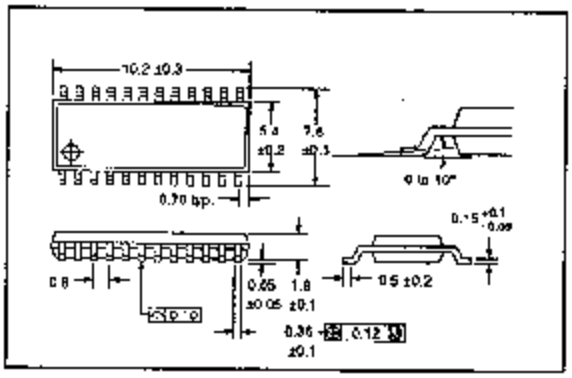
FEATURES

- Double-speed dubbing mode (4.5 to 5.5 V supply only)
- 44.1 kHz sampling frequency
- 16.9344 MHz system clock (384fs or 192fs)
- 16-bit, MSB-first, serial data input (≤ 64fs bit clock)
- 8-times oversampling digital filter
  - 32 dB stopband attenuation
  - ±0.05 dB passband ripple
  - −0.34 dB passband compensation for 70 kHz lowpass filter
- With deemphasis enabled
  - 36 dB stopband attenuation
  - −0.09 to 0.23 dB deviation from ideal deemphasis characteristic
  - −0.34 dB passband compensation for 70 kHz lowpass filter
- 64-step attenuator
- Third-order noise shaper
- 32fs oversampling Σ-Δ (sigma-delta) D/A converter
- Molybdenum-gate CMOS process
- 2.7 to 5.5 V operating supply voltage
- 24-pin SSOP

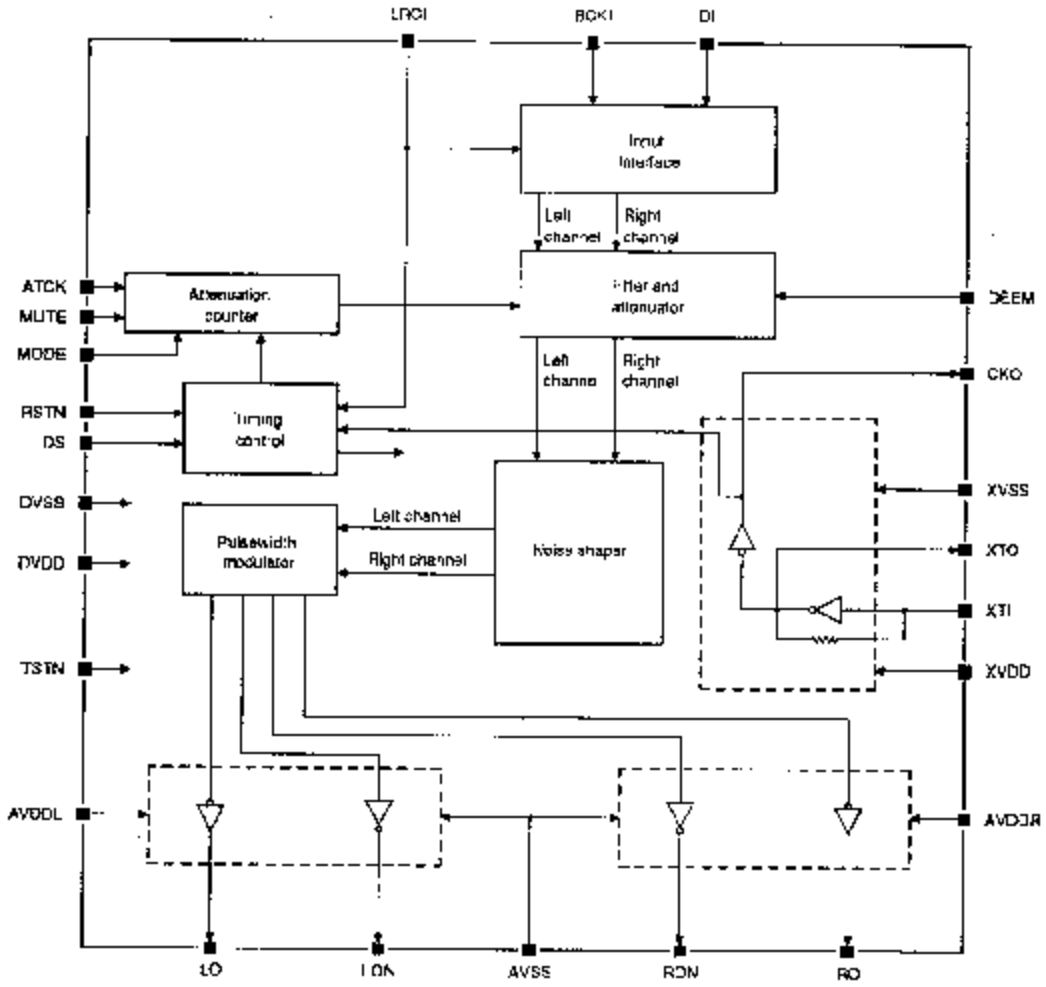
PINOUT



PACKAGE DIMENSIONS



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Description
1	MUTE	Ip	Soft mute enable when MODE is HIGH. Mute is active when HIGH. Attenuator level direction control when MODE is LOW. The attenuator direction is down when HIGH.
2	DEEM	Ip	Deemphasis enable. Deemphasis is ON when HIGH.
3	CKO	O	16.9344 MHz clock output
4	DVSS	–	Digital ground
5	BCKI	Ip	Bit clock input
6	DI	Ip	Serial data input
7	DVDD	–	Digital supply voltage
8	LRCI	Ip	Sample rate clock. Left-channel input when HIGH, and right-channel input when LOW.
9	TSTN	Ip	Test pin. Leave this pin open or tie it HIGH for normal operation.
10	LO	O	Left-channel normal-polarity analog output
11	AVDDL	–	Analog supply voltage

Number	Name	I/O	Description
13	AVSS		Analog ground
14	RDN	O	Right-channel inverse-polarity analog output
15	AVDDR	–	Analog supply voltage
16	RO	O	Right-channel normal-polarity analog output
17	XVDD	–	Oscillator circuit supply voltage
18	XTI	I	16.9344 MHz crystal oscillator connection or external clock input
19	XTO	O	Crystal oscillator connection
20	XVSS	–	Oscillator circuit ground
21	DS	Ip	Double-speed mode select. Double-speed mode is selected when HIGH.
22	RSTN	Ip	Active-LOW reset input
23	MODE	Ip	Soft mute or attenuator mode select. Soft mute mode is selected when HIGH, and attenuator mode when LOW.
24	ATCK	Ip	Attenuator level setting clock. Disabled when MODE is HIGH.

Note
I = input, Ip = input with pull-up resistor, O = output

SPECIFICATIONS

Absolute Maximum Ratings

$DV_{SS} = AV_{SS} = XV_{SS} = 0$ V, $AV_{DD} = AV_{DDL} = AV_{DDR}$

Parameter	Symbol	Rating	Unit
Supply voltage range	DV_{DD}, AV_{DD}, XV_{DD}	–0.3 to 7.0	V
Input voltage range. See note.	V_{IN}	DV_{SS} – 0.3 to DV_{DD} + 0.3	V
XTI input voltage range	V_{IN}	XV_{SS} – 0.3 to XV_{DD} + 0.3	V
Power dissipation	P_D	250	mW
Storage temperature range	T_{stg}	–40 to 125	deg. C
Soldering temperature	T_{sld}	255	deg. C
Soldering time	t_{sld}	10	s

Note
Pins MUTE, DEEM, BCKI, DI, LRCI, TSTN, DS, RSTN, MODE and ATCK

Recommended Operating Conditions

Normal-voltage mode

$DV_{SS} = AV_{SS} = XV_{SS} = 0$ V, $AV_{DD} = AV_{DDL} = AV_{DDR}$

Parameter	Symbol	Condition	Unit
Supply voltage range	DV_{DD}, AV_{DD}, XV_{DD}	4.5 to 5.5	V
Supply voltage differences	$DV_{DD} - XV_{DD}$, $DV_{DD} - AV_{DD}$, $XV_{DD} - AV_{DD}$, $DV_{SS} - XV_{SS}$, $DV_{SS} - AV_{SS}$, $XV_{DD} - AV_{SS}$	±0.1	V
Operating temperature range	T	–40 to 85	deg. C

Low-voltage mode

$DV_{SS} = AV_{SS} = XV_{SS} = 0$ V, $AV_{DD} = AV_{DDL} = AV_{DDR}$

Parameter	Symbol	Condition	Unit
Supply voltage range	DV_{DD}, AV_{DD}, XV_{DD}	2.7 to 4.5	V
Supply voltage differences	$DV_{DD} - XV_{DD}$, $DV_{DD} - AV_{DD}$, $XV_{DD} - AV_{DD}$, $DV_{SS} - XV_{SS}$, $DV_{SS} - AV_{SS}$, $XV_{SS} - AV_{SS}$	±0.1	V
Operating temperature range	T_{opr}	−20 to 70	deg. C

DC Characteristics

Normal-voltage mode

$DV_{SS} = AV_{SS} = XV_{SS} = 0$ V, $DV_{DD} = AV_{DD} = XV_{DD} = 4.5$ to 5.5 V, $AV_{DD} = AV_{DDL} = AV_{DDR}$, $T_a = -40$ to 85 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
DVDD supply current	I_{DDD}	See note 3.	–	15	25	mA
XVDD supply current	I_{DDX}	See note 3.	–	2	5	mA
AVDD total supply current	I_{DDA}	See note 3.	–	1	2	mA
XTI HIGH-level input voltage	V_{IH1}	Clock input	$0.7XV_{DD}$	–	–	V
XTI LOW-level input voltage	V_{IL1}	Clock input	–	–	$0.3XV_{DD}$	V
XTI AC input voltage	V_{INAC}	AC coupling	$0.3XV_{DD}$	–	–	V_{p-p}
HIGH-level input voltage	V_{IH2}	See note 1.	2.4	–	–	V
LOW-level input voltage	V_{IL2}	See note 1.	–	–	0.5	V
HIGH-level analog output voltage	V_{OHA}	$I_{OH} = -1$ mA. See note 2.	$AV_{DD} - 0.3$	–	–	V
LOW-level analog output voltage	V_{OLA}	$I_{OL} = 1$ mA See note 2.	–	–	0.3	V
CKO HIGH-level output voltage	V_{OHC}	$I_{OH} = -1$ mA	$DV_{DD} - 0.4$	–	–	V
CKO LOW-level output voltage	V_{OLC}	$I_{OL} = 1$ mA	–	–	0.4	V
XTI HIGH-level input current	I_{IH1}	$V_{IN} = XV_{DD}$	–	12	25	µA
XTI LOW-level input current	I_{IL1}	$V_{IN} = 0$ V	–	12	25	µA
LOW-level input current	I_{IL2}	$V_{IN} = 0$ V See note 1.	–	12	25	µA
Input leakage current	I_{LH}	$V_{IN} = DV_{DD}$ See note 1.	–	–	1.0	µA

Notes

1. Pins MUTE, DEEM, BCKI, DI, LRCI, TSTN, DS, RSTN, MODE and ATCK
2. Pins LO, LON, RO and RON
3. $DV_{DD} = AV_{DD} = XV_{DD} = 5$ V, DS = 5 V (double-speed mode), $f_{XTI} = 16.9344$ MHz, no load on any output pin, NPC-specification input data sequence

Low-voltage mode

DV_{SS} = AV_{SS} = XV_{SS} = 0 V, DV_{DD} = AV_{DD} = XV_{DD} = 2.7 to 4.5 V, AV_{DD} = AV_{DDL} = AV_{DDR}, T_a = −20 to 70 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
DVDD supply current	I_{DDD}	See note 3	–	6	9	mA
XVDD supply current	I_{DDX}	See note 3	–	1	3	mA
AVDD total supply current	I_{DDA}	See note 3.	–	0.5	1	mA
XTI HIGH-level input voltage	V_{IH1}	Clock input	0.7XV$_{DD}$	–	–	V
XTI LOW-level input voltage	V_{IL1}	Clock input	–	–	0.3XV$_{DD}$	V
XTI AC input voltage	V_{IHAC}	AC coupling	0.3XV$_{DD}$	–	–	V_{p-p}
HIGH-level input voltage	V_{IH2}	See note 1.	2.4	–	–	V
LOW-level input voltage	V_{IL2}	See note 1.	–	–	0.5	V
HIGH-level analog output voltage	V_{OHA}	I_{OH} = −0.5 mA See note 2.	AV$_{DD}$ − 0.3	–	–	V
LOW-level analog output voltage	V_{OLA}	I_{OL} = 0.5 mA. See note 2.	–	–	0.3	V
CKO HIGH-level output voltage	V_{OHC}	I_{OH} = −0.5 mA	DV$_{DD}$ − 0.4	–	–	V
CKO LOW-level output voltage	V_{OLC}	I_{OL} = 0.5 mA	–	–	0.4	V
XTI HIGH-level input current	I_{IH1}	V_{IN} = XV$_{DD}$	–	4	15	µA
XTI LOW-level input current	I_{IL1}	V_{IN} = 0 V	–	4	15	µA
LOW-level input current	I_{IL2}	V_{IN} = 0 V. See note 1.	–	4	15	µA
Input leakage current	I_{LH}	V_{IN} = DV$_{DD}$. See note 1.	–	–	1.0	µA

Notes

1. Pins MUTE, DEEM, BCKI, DI, LRCI, TSTN, DS, RSTN, MODE and ATCK
2. Pins LO, LON, RO and RON
3. DV_{DD} = AV_{DD} = XV_{DD} = 3 V, DS = 0 V (normal-speed mode), f_{XTI} = 16.9344 MHz, no load on any output pin, NPC-specification input data sequence

AC Characteristics

Normal-voltage mode: DV_{SS} = AV_{SS} = XV_{SS} = 0 V, DV_{DD} = AV_{DD} = XV_{DD} = 4.5 to 5.5 V, AV_{DD} = AV_{DDL} = AV_{DDR}, T_a = −40 to 85 deg. C
Low-voltage mode: DV_{SS} = AV_{SS} = XV_{SS} = 0 V, DV_{DD} = AV_{DD} = XV_{DD} = 2.7 to 4.5 V, AV_{DD} = AV_{DDL} = AV_{DDR}, T_a = −20 to 70 °C

System clock (XTI)

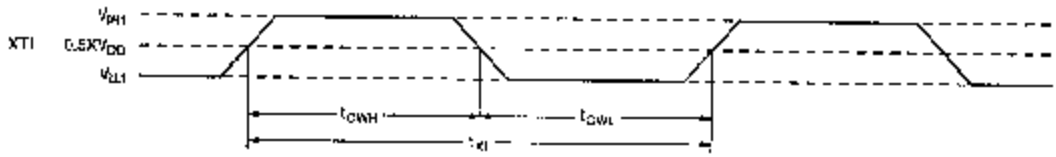
Crystal oscillator

Parameter	Symbol	Rating			Unit
		min	typ	max	
Oscillator frequency	fosc	40	16.9344	17.8	MHz

External clock input

Parameter	Symbol	Rating			Unit
		min	typ	max	
HIGH-level clock pulsewidth	t_{CWH}	26	29.5	125	ns
LOW-level clock pulsewidth	t_{CWL}	26	29.5	125	ns
Clock period	t_X	56	59.0	250	ns

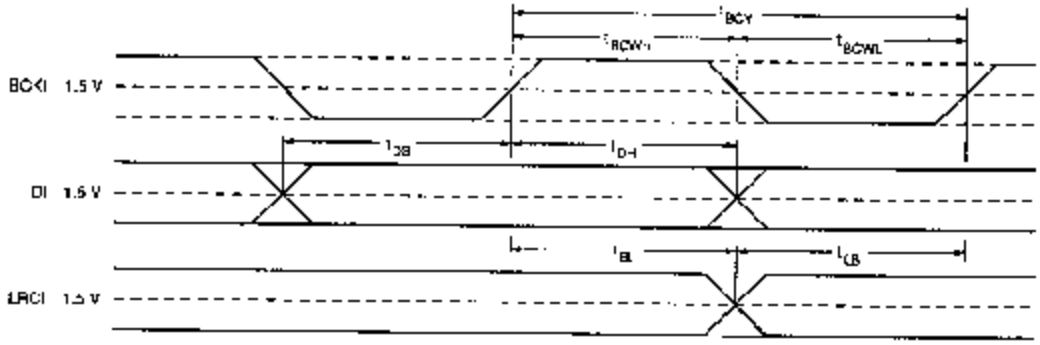
External clock input waveform



Serial data input (BCKI, DI, LRCI)

Parameter	Symbol	Rating			Unit
		min	typ	max	
BCKI HIGH-level pulsewidth	t_{BCWH}	50	–	–	ns
BCKI LOW-level pulsewidth	t_{BCWL}	50	–	–	ns
BCKI pulse cycle time	t_{BCY}	6[illegible]	–	–	ns
DI setup time	t_{DS}	30	–	–	ns
DI hold time	t_{DH}	30	–	–	ns
Last BCKI rising edge to LRCI edge delay	t_{BL}	50	–	–	ns
LRCI edge to first BCKI rising edge delay	t_{LB}	50	–	–	ns

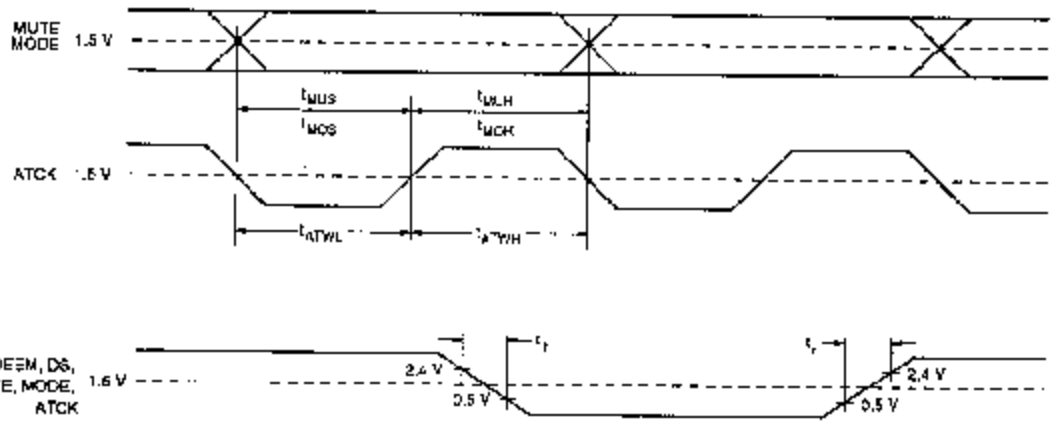
Serial data input waveform



Control inputs (MUTE, MODE, ATCK, DEEM, DS)

Parameter	Symbol	Rating			Unit
		min	typ	max	
ATCK LOW-level pulsewidth	t_{ATWL}	1/2fs	–	–	µs
ATCK HIGH-level pulsewidth	t_{ATWH}	1/2fs	–	–	µs
MUTE setup time	t_{MUS}	100	–	–	ns
MUTE hold time	t_{MUH}	100	–	–	ns
MODE setup time	t_{MOS}	100	–	–	ns
MODE hold time	t_{MOH}	100	–	–	ns
Rise time	t_r	–	–	50	ns
Fall time	t_f	–	–	50	ns

Control input waveforms



Reset Input (RSTN)

Parameter	Symbol	Rating			Unit
		min	typ	max	
RSTN LOW-level pulsewidth (after power supply stabilizes)	t_{RSTN}	50		–	ns

AC Analog Characteristics

Normal-voltage mode

DV_{SS} = AV_{SS} = XV_{SS} = 0 V, DV_{DD} = AV_{DD} = XV_{DD} = 5 V, AV_{DD} = AV_{DDL} = AV_{DDR}, DS = 0 V, DEEM = 0 V, crystal oscillator, f_{osc} = 16.9344 MHz, T_a = 25 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Total harmonic distortion	THD + N	f = 1 kHz, V = 0 dB	–	0.0025	0.0035	%
Theoretical output level. See note 1.	V_{OUT1}	f = 1 kHz, V_i = 0 dB	–	1.53	–	V_{rms}
EVA board output level	V_{OUT2}	f = 1 kHz, V_i = 0 dB	1.8	2.0	2.2	V_{rms}
Dynamic range	DR	f = 1 kHz, V_i = –60 dB	90	96	–	dB
Signal-to-noise ratio. See note 2.	S/N	f = 1 kHz, V_i = 0 dB/– ∞	94	100	–	dB
Channel separation	Ch. Sep	f = 1 kHz, V_i = – ∞/0 dB	84	90	–	dB

Notes

1. The measurement circuit block diagram is shown in figure 1. The measurement circuit itself is shown in figure 2.
2. The theoretical output level of the device is $0.3058AV_{DD}$ V_{rms}.
3. Signal-to-noise is measured following a device reset, with DATA = 0 (DI = LOW). Under these conditions, the signal-to-noise ratio includes noise-shaper noise.

Low-voltage mode

DV_{SS} = AV_{SS} = XV_{SS} = 0 V, DV_{DD} = AV_{DD} = XV_{DD} = 3 V, AV_{DD} = AV_{DDL} = AV_{DDR}, DS = 0 V, DEEM = 0 V, crystal oscillator, f_{osc} = 16.9344 MHz, T_a = 25 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Total harmonic distortion	THD + N	f = 1 kHz, V_i = 0 dB	–	0.0030	–	%
Theoretical output level. See note 1.	V_{OUT1}	f = 1 kHz, V_i = 0 dB	–	0.92	–	V_{rms}
EVA board output level	V_{OUT2}	f = 1 kHz, V_i = 0 dB	–	1.2	–	V_{rms}
Dynamic range	DR	f = 1 kHz, V_i = –60 dB	–	94	–	dB
Signal-to-noise ratio. See note 2.	S/N	f = 1 kHz, V_i = 0 dB/– ∞	–	96	–	dB
Channel separation	Ch. Sep	f = 1 kHz, V_i = – ∞/0 dB	–	88	–	dB

Notes

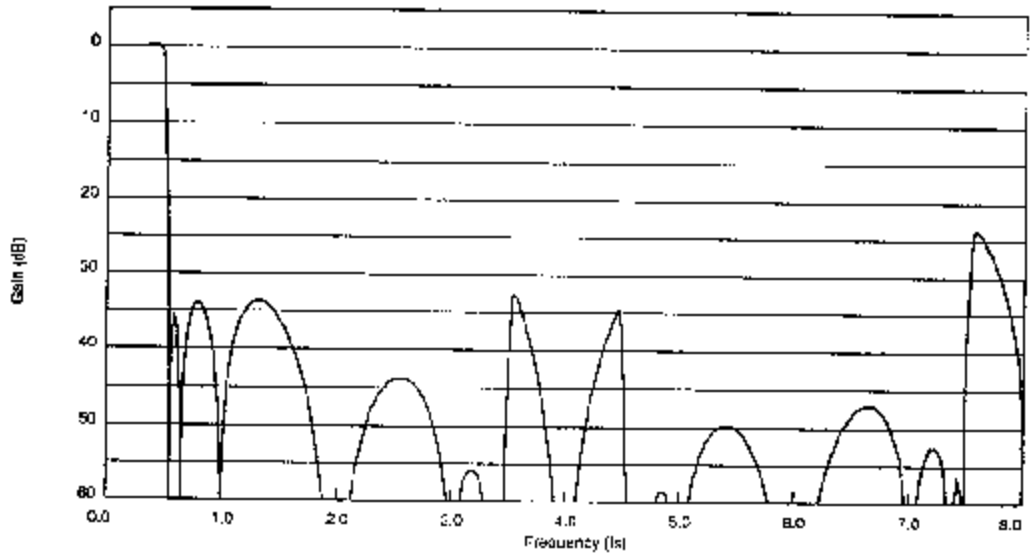
1. The measurement circuit block diagram is shown in figure 1. The measurement circuit itself is shown in figure 2.
2. The theoretical output level of the device is $0.3058AV_{DD}$ V_{rms}.
3. Signal-to-noise is measured following a device reset, with DATA = 0 (DI = LOW). Under these conditions, the signal-to-noise ratio includes noise-shaper noise.

Theoretical Filter Characteristics

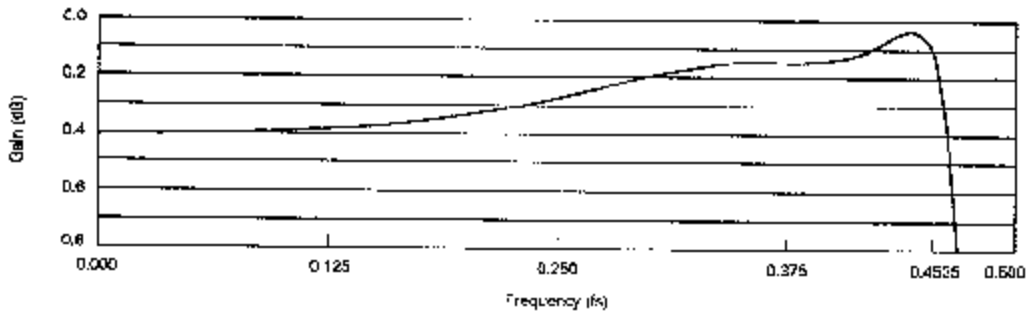
Deemphasis OFF

Parameter	Frequency band		Rating			Unit
	f	@ fs = 44.1 kHz	min	typ	max	
Passband ripple	0 to 0.4535fs	0 to 20.0 kHz	−0.05	–	0.05	dB
Stopband attenuation	0.5465fs to 7.4535fs	24.1 to 328.7 kHz	32	–	–	dB
Filter post-compensation	0.4535fs	20.0 kHz	–	−0.34	–	dB

Overall frequency characteristic (deemphasis OFF)



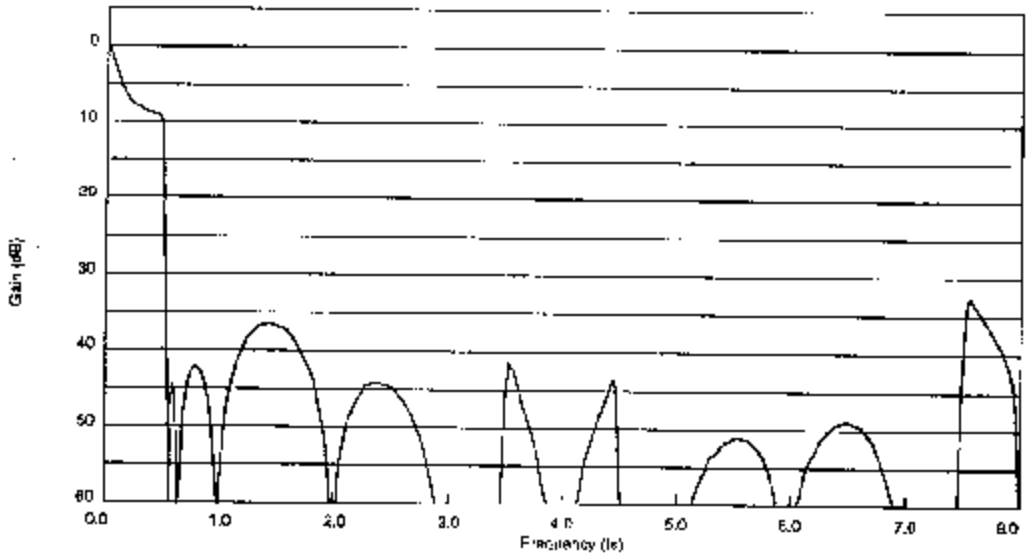
Passband characteristic (deemphasis OFF)



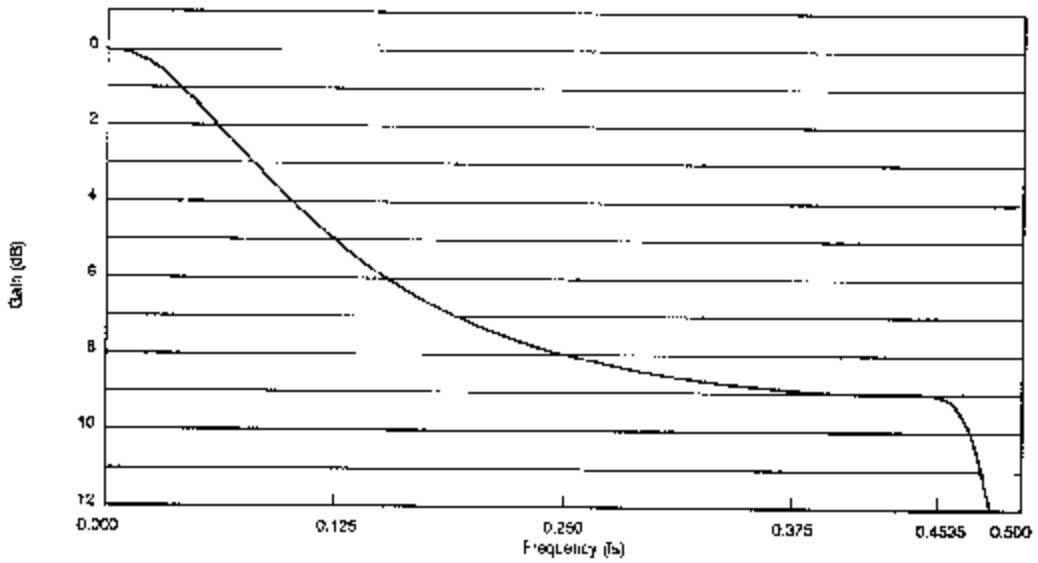
Deemphasis ON

Parameter	Frequency band		Rating			Unit
	f	@ fs = 44.1 kHz	min	typ	max	
Passband ripple	0 to 0.4535fs	0 to 20.0 kHz	−0.09	–	0.23	dB
Stopband attenuation	0.5465fs to 7.4535fs	24.1 to 328.7 kHz	36	–	–	dB
Filter post-compensation	0.4535fs	20.0 kHz	–	0.34	–	dB

Overall frequency characteristic (deemphasis ON)



Passband characteristic (deemphasis ON)



Measurement Circuits

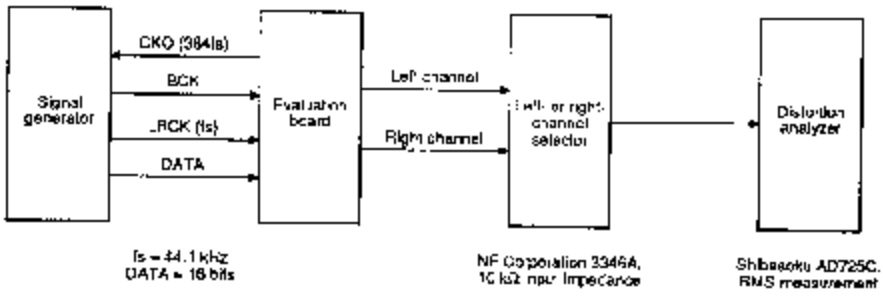


Figure 1. Measurement circuit block diagram

Notes

1. Input impedance = 10 kΩ. NF Pty. Ltd. 3346A circuit design block.
2. RMS measurement. Shibasoku Pty. Ltd. AD725C.

Measurement conditions

Parameter	Symbol	3346A channel selector position	AD725C distortion analyzer setting
Total harmonic distortion	THD + N	THRU	20 kHz lowpass filter is ON. 400 Hz highpass filter is OFF.
Output level	VOUT		
Dynamic range	DR	D-RANGE	
Signal-to-noise ratio	S/N	THRU	20 kHz lowpass filter is ON. 400 Hz highpass filter is OFF. JIS* A-weighted filter is ON.
Channel separation	Ch. Sep	THRU	20 kHz lowpass filter is ON. 400 Hz highpass filter is OFF.

* Japanese Industrial Standard

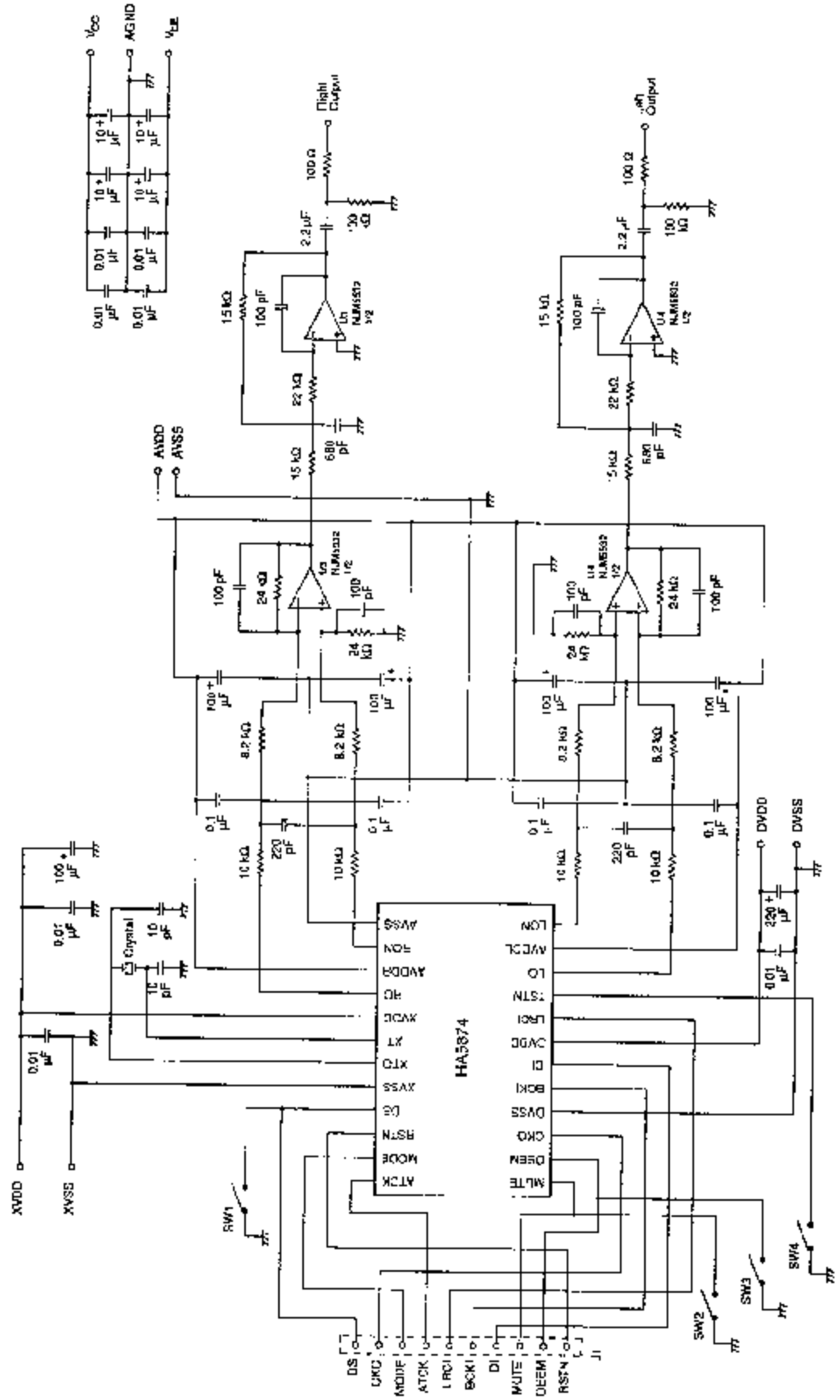


Figure 2. Measurement circuit

FUNCTIONAL DESCRIPTION

System Clock

The system clock oscillates at either 192fs or 384fs, selected by the level on DS. This feature allows double-speed playback selection where the sampling frequency is 88.2 kHz.

Table 1. System clock selection

Parameter	Symbol	Condition	Rating	Unit
XTI input frequency	F_{xi}	DS is HIGH, fs = 88.2 kHz	16.9344	MHz
		DS is LOW, fs = 44.1 kHz	16.9344	
CKO output frequency	F_{ck}	DS is HIGH.	192	fs
		DS is LOW.	384	
Internal system clock period	T_{sys}	DS is HIGH.	t_{xi}	s
		DS is LOW.	t_{xi}	

Note

t_{xi} is the input clock period.

As the stability and signal-to-noise ratio of the system clock greatly affects the AC analog characteristics, care should be taken to ensure that the clock is free from jitter.

The system clock can be generated by connecting a crystal between XTI and XTO.

Alternatively, an external clock can be input on XTI. In this case, XTO is left unconnected. Because XTI is connected internally to the feedback resistor around the internal CMOS inverter, the external clock input can be AC-coupled. A buffered clock signal is output on CKO.

System Reset

The SM5874AM needs to be reset after power-up or when either of the LRCI or XTI clocks stop. A LOW-level pulse on RSTN will resynchronize the internal arithmetic and output clocks on the first rising edge of LRCI after RSTN returns HIGH.

When RTSN goes LOW, the PWM outputs are muted with a 50% duty-cycle signal. Mute is released on the eighth rising edge of LRCI after RSTN returns HIGH.

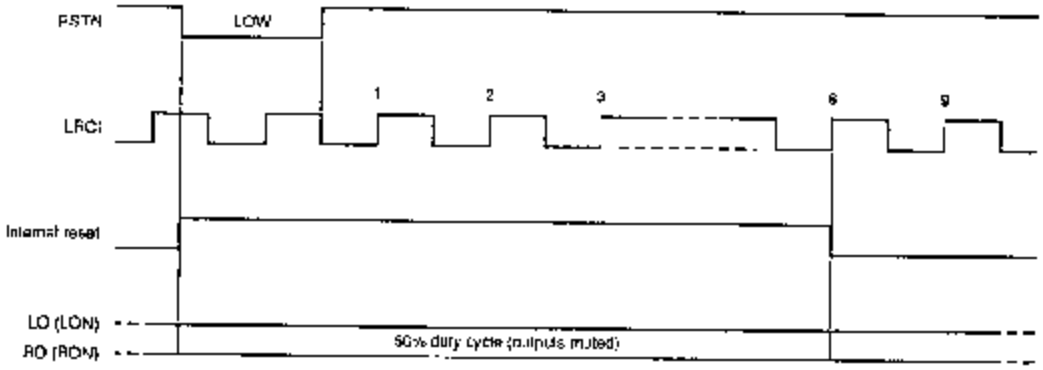


Figure 3. System reset timing

Audio Data Input

The input data is input on DI in MSB-first, 16-bit, 2s-complement serial data format. Each bit is clocked into the internal shift register on the rising edge of BCKI, where BCKI is between 32fs and 64fs inclusive.

The timing of the arithmetic and output circuits is independent of the timing of the input data to prevent jitter on the input clock from feeding through to the output clock. Provided that the frequency ratio between LRCI and the system clock (XTI) is maintained at the same value, any phase difference between LRCI and XTI does not affect device operation.

Deemphasis Filter

The deemphasis filter is designed to operate at 44.1 kHz. Deemphasis is enabled by taking DEEM HIGH.

Attenuation

Attenuation mode is selected when MODE is LOW. The level of attenuation is determined by the value of the 6-bit up/down counter, DATT. The signal data is multiplied by the value of DATT. DATT changes on the rising edge of ATCK. The direction of change is controlled by MUTE—down when MUTE is HIGH, and up when MUTE is LOW.

The gain of the signal is given by

$$\text{Gain} = 20 \times \log_{10}(\text{DATT}/63)\ \text{dB}$$

DATT is reset to 63 on a device reset, and when the logic level on MODE changes. This corresponds to 0 dB gain.

Table 2. Attenuation/gain list

DATT	Gain
63	0.0dB
62	−0.139 dB
61	−0.280 dB
60	−0.424 dB
59	−0.570 dB
58	−0.718 dB
57	−0.869 dB
56	−1.023 dB
55	−1.180 dB
54	−1.339 dB
53	−1.501 dB
52	−1.667 dB
51	−1.835 dB
50	−2.007 dB
49	−2.183 dB
48	−2.362 dB
47	−2.545 dB
46	−2.732 dB
45	−2.923 dB
44	−3.118 dB
43	−3.317 dB
42	−3.522 dB
41	−3.731 dB
40	−3.946 dB
39	−4.166 dB
38	−4.391 dB
37	−4.623 dB
36	−4.861 dB
35	−5.105 dB
34	−5.357 dB
33	−5.617 dB
32	−5.884 dB

Table 2. Attenuation/gain list—continued

DATT	Gain
31	−6.160 dB
30	−6.444 dB
29	−6.739 dB
28	−7.044 dB
27	−7.360 dB
26	−7.687 dB
25	−8.028 dB
24	−8.383 dB
23	−8.752 dB
22	−9.136 dB
21	−9.542 dB
20	−9.966 dB
19	−10.412 dB
18	−10.881 dB
17	−11.378 dB
16	−11.904 dB
15	−12.465 dB
14	−13.064 dB
13	−13.708 dB
12	−14.403 dB
11	−15.159 dB
10	−15.987 dB
9	−15.902 dB
8	−17.925 dB
7	−19.085 dB
6	−20.424 dB
5	−22.007 dB
4	−23.946 dB
3	−26.444 dB
2	−29.986 dB
1	−35.987 dB
0	− ∞

Soft Mute

Soft mute mode is selected when MODE is HIGH. The up/down counter is switched to internal clock drive, and soft mute operation is controlled by MUTE only.

When MUTE goes HIGH, the up/down counter counts down. The total time to go from 0 to maximum mute is 1024/fs. At 44.1 kHz, this is approximately 23.2 ms.

Soft mute is released when MUTE returns LOW, and the gain is increased gradually to 0 dB.

Mute is cancelled on a device reset or when the logic level on MODE changes.

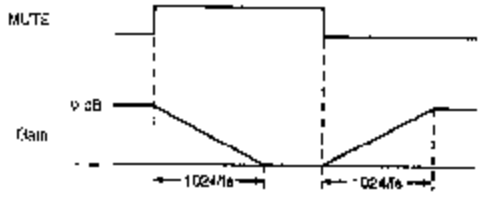
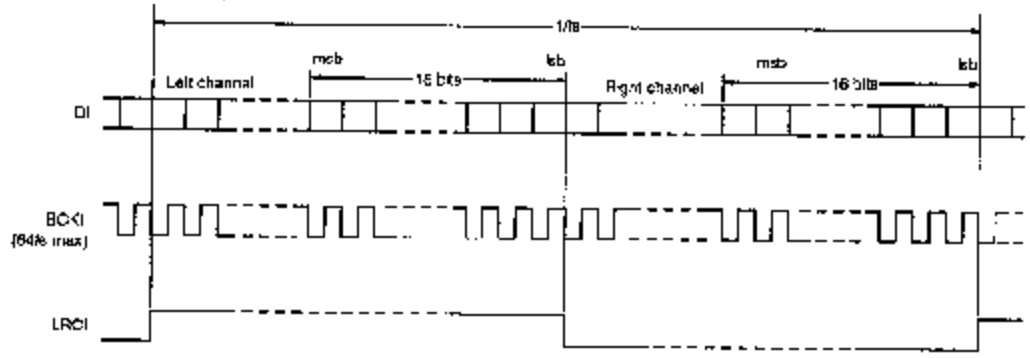


Figure 4. Soft mute operation

TIMING CHARTS

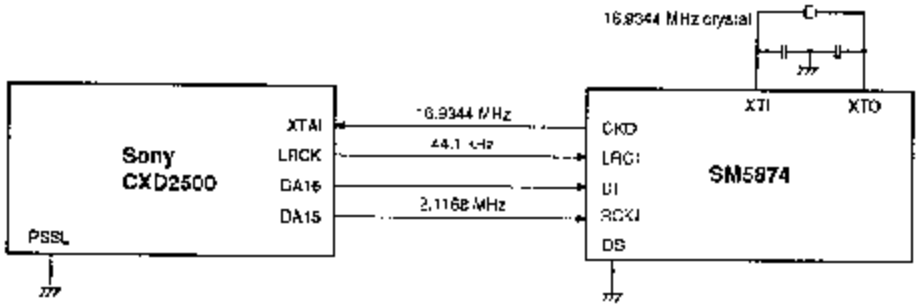
Input Timing

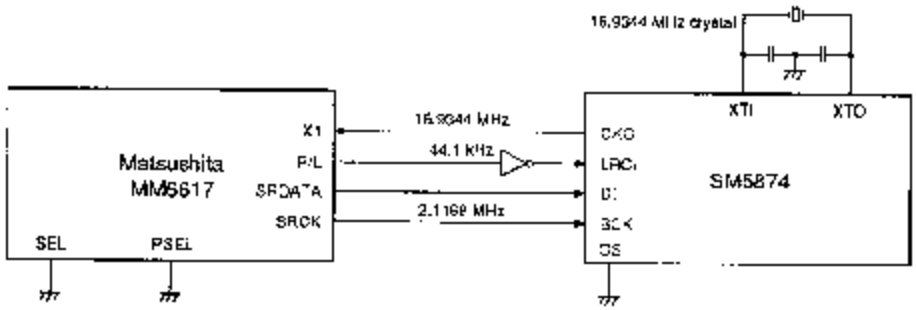


APPLICATION CIRCUITS

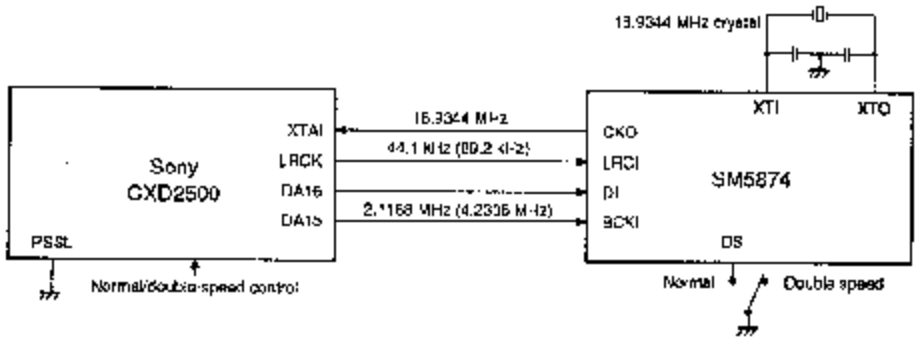
Input Interfaces

Normal replay mode





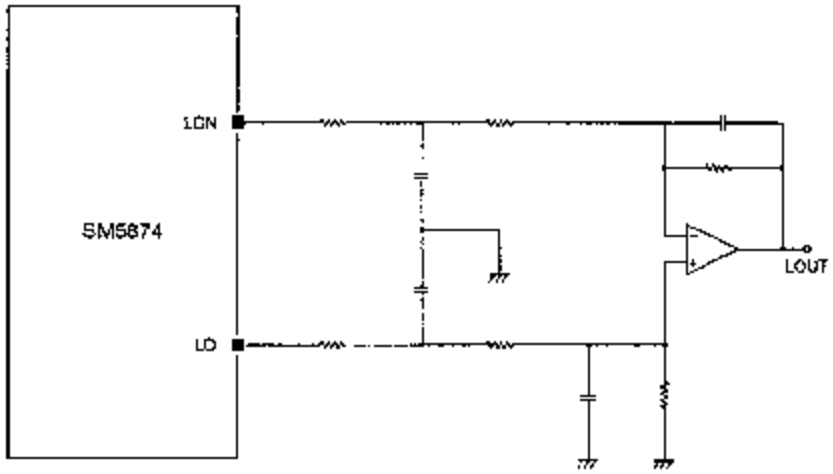
Double-speed replay mode



Note
The values in parenthesis are for double-speed mode.

Analog Output Circuit

The left channel only has been shown to avoid duplication.



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