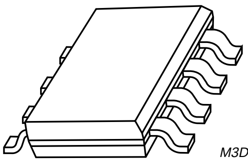


PHN203

Dual N-channel TrenchMOS™ logic level FET

Rev. 03 — 26 January 2004 **Product data**

1. Product profile

1.1 Description

Dual logic level N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- Logic level threshold
- Fast switching
- Dual device
- Surface mount package.

1.3 Applications

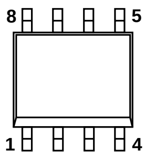
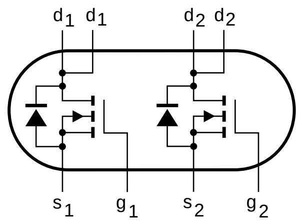
- DC-to-DC converters
- Lithium-ion battery applications.

1.4 Quick reference data

- $V_{DS} \leq 30$ V
- $P_{tot} \leq 2$ W
- $I_D \leq 6.3$ A
- $R_{DSon} \leq 30$ mΩ.

2. Pinning information

Table 1: Pinning - SOT96-1 (SO8), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	source1 (s1)	 SOT96-1 (SO8)	
2	gate1 (g1)		
3	source2 (s2)		
4	gate2 (g2)		
5,6	drain2 (d2)		
7,8	drain1 (d1)		

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3. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
PHN203	SO8	Plastic small outline package; 8 leads	SOT96-1

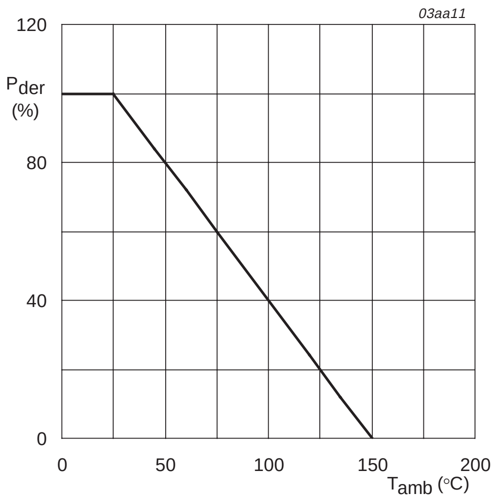
4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

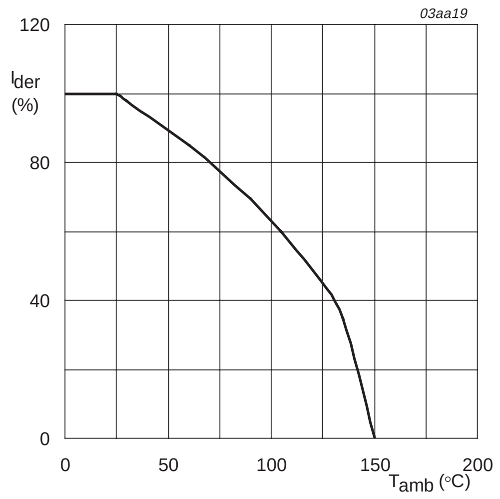
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage (DC)	25 °C ≤ T_j ≤ 150 °C		-	30	V
V_{DGR}	drain-gate voltage (DC)	25 °C ≤ T_j ≤ 150 °C; R_{GS} = 20 kΩ		-	30	V
V_{GS}	gate-source voltage (DC)			-	±20	V
I_D	drain current (DC)	T_{amb} = 25 °C; pulsed; t_p ≤ 10 s; Figure 2 and 3	[1]	-	6.3	A
		T_{amb} = 70 °C; pulsed; t_p ≤ 10 s; Figure 2	[1]	-	5	A
I_{DM}	peak drain current	T_{amb} = 25 °C; pulsed; t_p ≤ 10 µs; Figure 3	[1]	-	18	A
P_{tot}	total power dissipation	T_{amb} = 25 °C; pulsed; t_p ≤ 10 s; Figure 1	[1]	-	2	W
T_{stg}	storage temperature			–55	+150	°C
T_j	junction temperature			–55	+150	°C
Source-drain diode						
I_S	source (diode forward) current (DC)	T_{amb} = 25 °C; pulsed; t_p ≤ 10 s	[1]	-	2	A
I_{SM}	peak source (diode forward) current	T_{amb} = 25 °C; pulsed; t_p ≤ 10 µs	[1]	-	4.1	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; I_D = 8.7 A; t_p = 0.2 ms; V_{DD} ≤ 30 V; R_{GS} = 50 Ω; V_{GS} = 10 V; starting T_j = 25 °C		-	37.8	mJ

[1] Single device conducting.



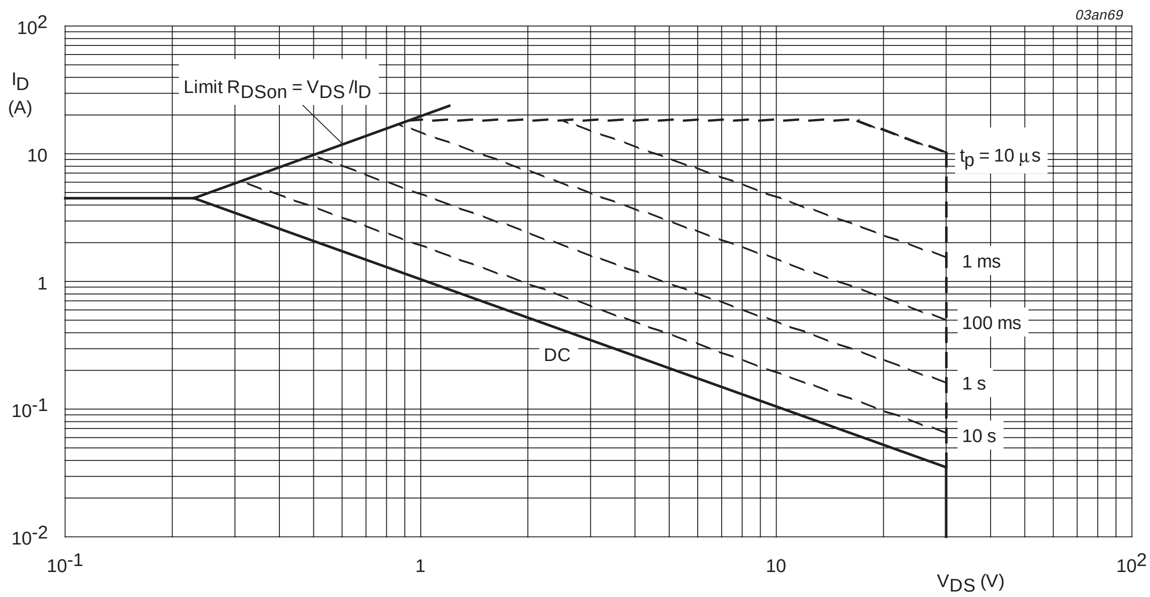
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of ambient temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of ambient temperature.



T_{amb} = 25 °C; I_{DM} is single pulse; V_{GS} = 10 V

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint; $t_p \leq 10$ s; Figure 4	-	-	62.5	K/W

5.1 Transient thermal impedance

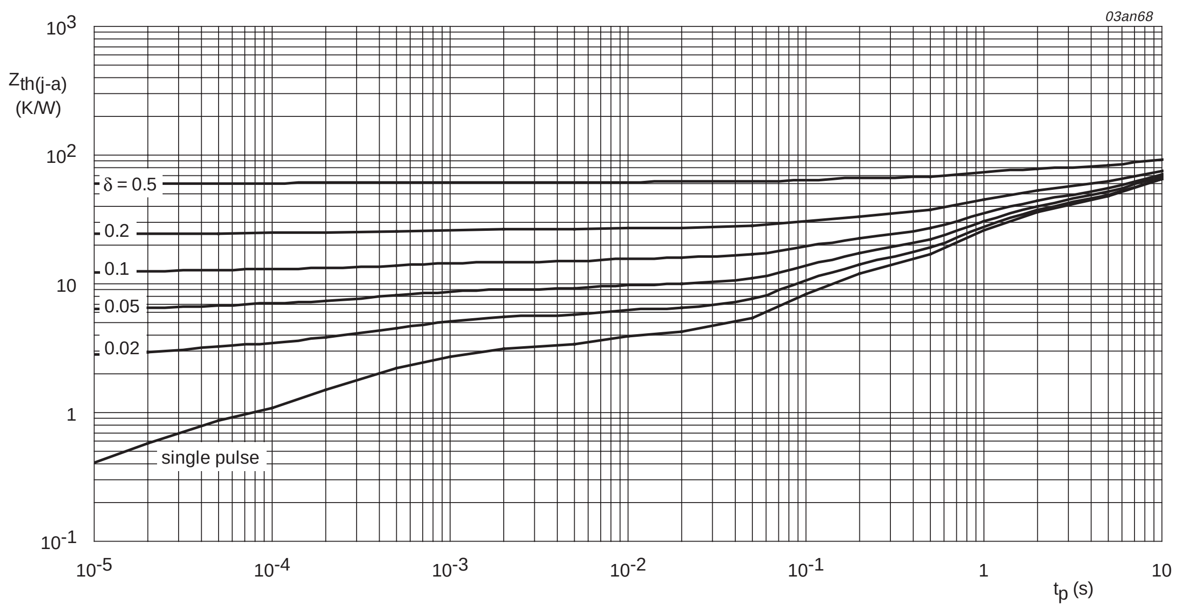


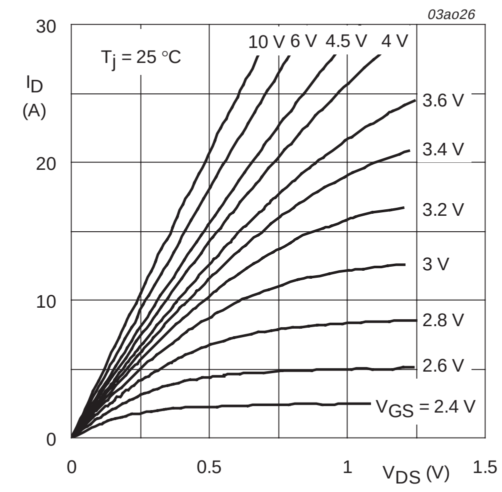
Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration.

6. Characteristics

Table 5: Characteristics

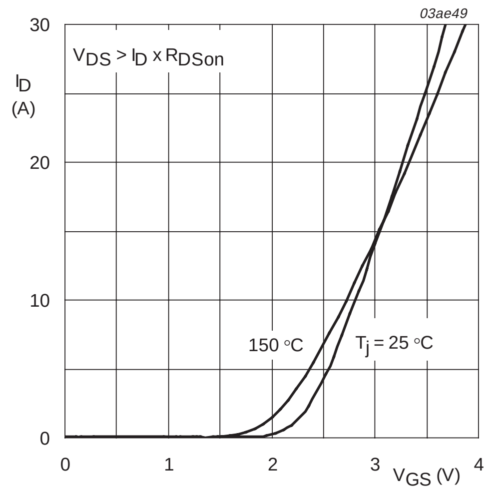
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V				
		T_j = 25 °C	30	-	-	V
		T_j = –55 °C	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 9				V
		T_j = 25 °C	1	1.5	2	V
		T_j = 150 °C	0.6	-	-	V
		T_j = –55 °C	-	-	2.2	V
I_{DSS}	drain-source leakage current	V_{DS} = 24 V; V_{GS} = 0 V				
		T_j = 25 °C	-	-	1	µA
		T_j = 150 °C	-	-	10	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 7 A; Figure 7 and 8				
		T_j = 25 °C	-	24	30	mΩ
		T_j = 150 °C	-	40.8	51	mΩ
		V_{GS} = 4.5 V; I_D = 3.5 A; Figure 7 and 8	-	30	55	mΩ
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	I_D = 7 A; V_{DD} = 15 V; V_{GS} = 10 V; Figure 13	-	14.6	-	nC
Q_{gs}	gate-source charge		-	2	-	nC
Q_{gd}	gate-drain (Miller) charge		-	3	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 20 V; f = 1 MHz; Figure 11	-	560	-	pF
C_{oss}	output capacitance		-	125	-	pF
C_{rss}	reverse transfer capacitance		-	85	-	pF
$t_{d(on)}$	turn-on delay time	V_{DD} = 25 V; R_L = 25 Ω; V_{GS} = 10 V; R_G = 6 Ω	-	5	-	ns
t_r	rise time		-	6	-	ns
$t_{d(off)}$	turn-off delay time		-	21	-	ns
t_f	fall time		-	11	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 1.25 A; V_{GS} = 0 V; Figure 12	-	0.75	1	V
t_{rr}	reverse recovery time	I_S = 2 A; dI_S/dt = –100 A/µs; V_{GS} = 0 V	-	30	-	ns



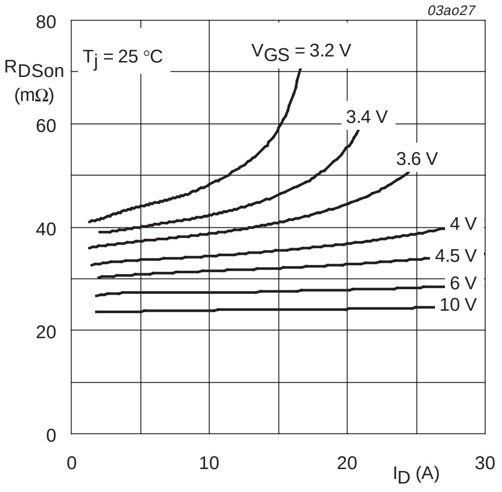
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



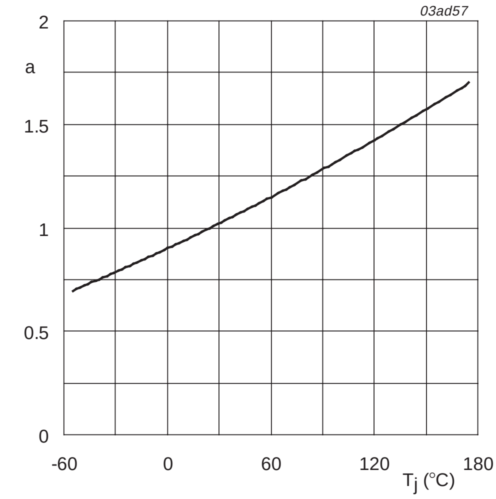
T_j = 25 °C and 150 °C; V_{DS} > I_D x R_{DSon}

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



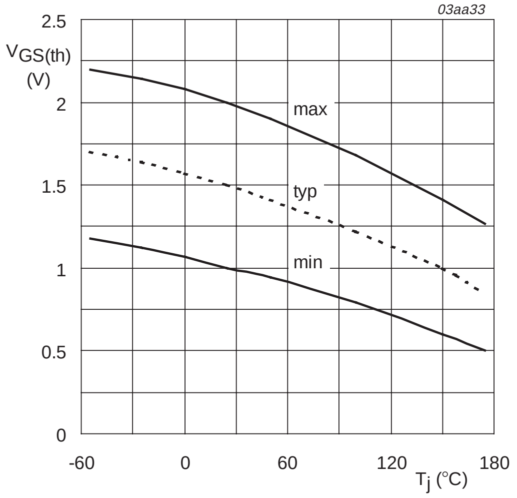
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



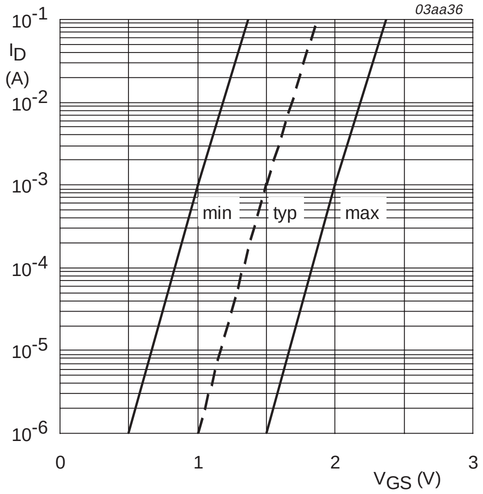
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



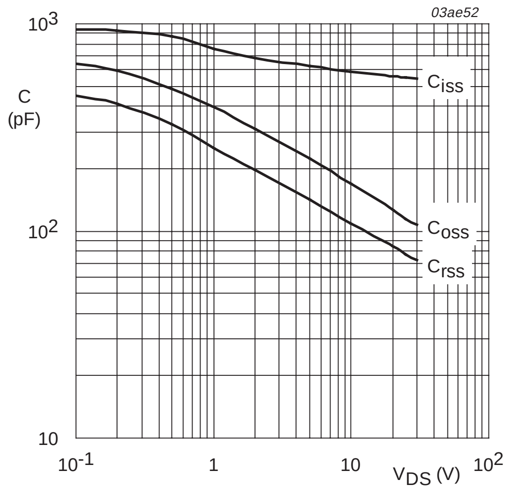
I_D = 1 mA; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



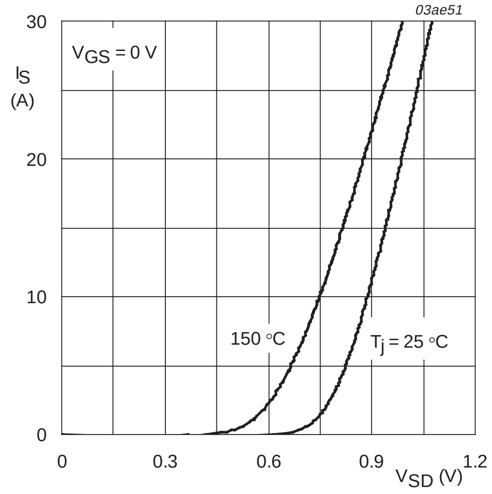
T_j = 25 °C; V_{DS} = 5 V

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



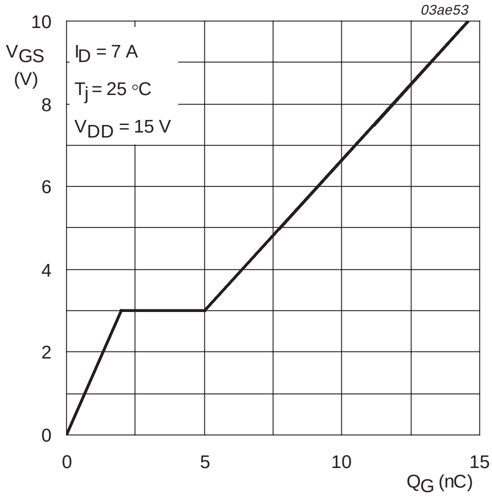
V_{GS} = 0 V; f = 1 MHz

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



T_j = 25 °C and 150 °C; V_{GS} = 0 V

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

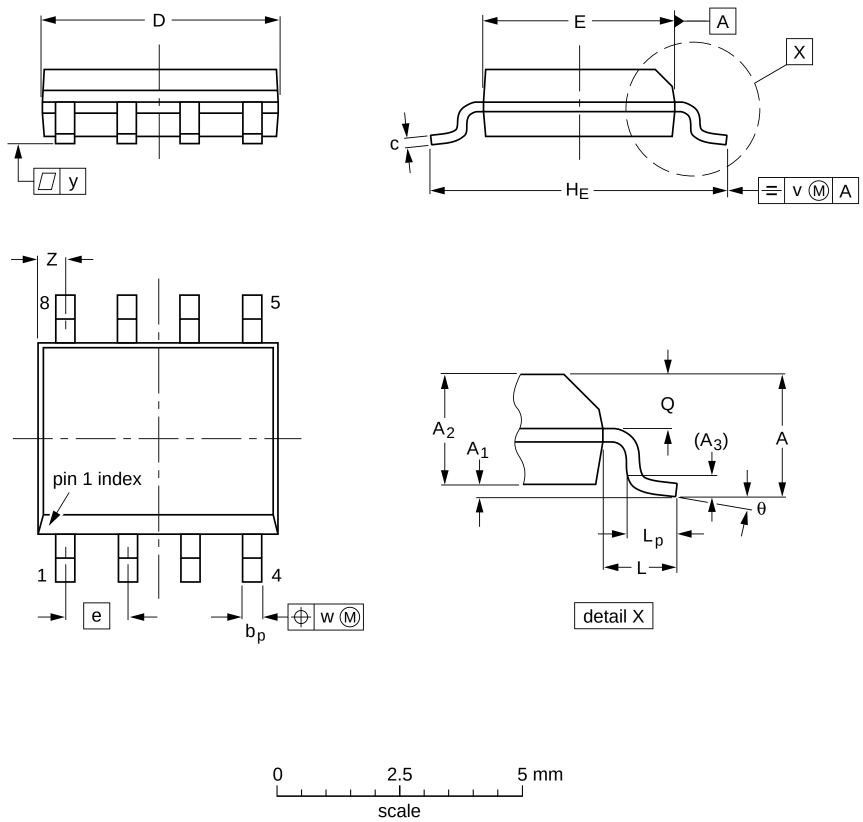


I_D = 7 A; V_{DD} = 15 V

Fig 13. Gate-source voltage as a function of gate charge; typical values.

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm — **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 14. SOT96-1 (SO8).

8. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
03	20040126	HZG469	**Product data (9397 750 12541); supersedes Product specification PHN203 Rev 1.000 of January 1999** Modifications: • Updated to latest standards. • Section 4 “Limiting values” V_{DS} max value increased. • Section 4 “Limiting values” I_D with both mosfets conducting removed. • Section 4 “Limiting values” I_{DM} corrected. • Section 6 “Characteristics” $V_{(BR)DSS}$ test conditions modified and limit increased. • Section 6 “Characteristics” $V_{GS(th)}$ limits tightened. • Section 6 “Characteristics” I_{DSS} test conditions and limits modified. • Section 6 “Characteristics” R_{DSon} test currents increased and typical values improved. • Section 6 “Characteristics” $Q_{g(tot)}$, Q_{gs}, Q_{gd} conditions changed and typical values improved. • Section 6 “Characteristics” C_{iss}, C_{oss}, C_{rss} typical values improved. • Section 6 “Characteristics” $t_{d(on)}$, t_r, $t_{d(off)}$, t_f test conditions modified and typical values improved. • Section 6 “Characteristics” V_{SD} test conditions and typical and limit values modified. • Section 5 “Thermal characteristics” Figure 4 modified. • Section 4 “Limiting values” Figure 3 modified. • Section 6 “Characteristics” Figure 5, 6, 7, 8, 11, 12 and13 modified.

9. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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For sales office addresses, send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

Fax: +31 40 27 24825

Contents

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