# Dual Low Power Operational Amplifier, Single or Dual Supply

# OP-221

## FEATURES

- **Excellent $TCV_{OS}$ Match** ..... **2μV/°C Max**
- **Low Input Offset Voltage** ..... **150μV Max**
- **Low Supply Current** ..... **550μA Max**
- **Single Supply Operation** ..... **+5V to +30V**
- **Low Input Offset Voltage Drift** ..... **0.75μV/°C**
- **High Open-Loop Gain** ..... **1500V/mV Min**
- **High PSRR** ..... **3μV/V**
- **Wide Common-Mode Voltage Range** ..... **V− to within 1.5V of V+**
- **Pin Compatible with 1458, LM158, LM2904**
- **Available in Die Form**

## ORDERING INFORMATION †

| $T_A$ = +25°C $V_{OS}$ MAX (μV) | PACKAGE TO-99 | PACKAGE CERDIP 8-PIN | PACKAGE PLASTIC 8-PIN | OPERATING TEMPERATURE RANGE |
|---|---|---|---|---|
| 150 | OP-221AJ/883 | OP221AZ* | – | MIL |
| 150 | – | OP221EZ | – | IND |
| 300 | OP221BJ | – | – | MIL |
| 500 | OP221CJ | – | – | MIL |
| 500 | OP221GJ | OP221GZ | OP221GP | XIND |
| 500 | – | – | OP221GS | XIND |

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

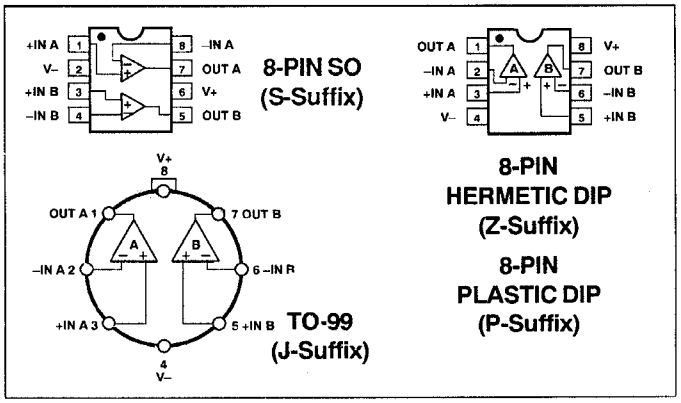
## GENERAL DESCRIPTION

The OP-221 is a monolithic dual operational amplifier that can be used either in single or dual supply operation. The wide supply voltage range, wide input voltage range, and low supply current drain of the OP-221 make it well-suited for operation from batteries or unregulated power supplies.

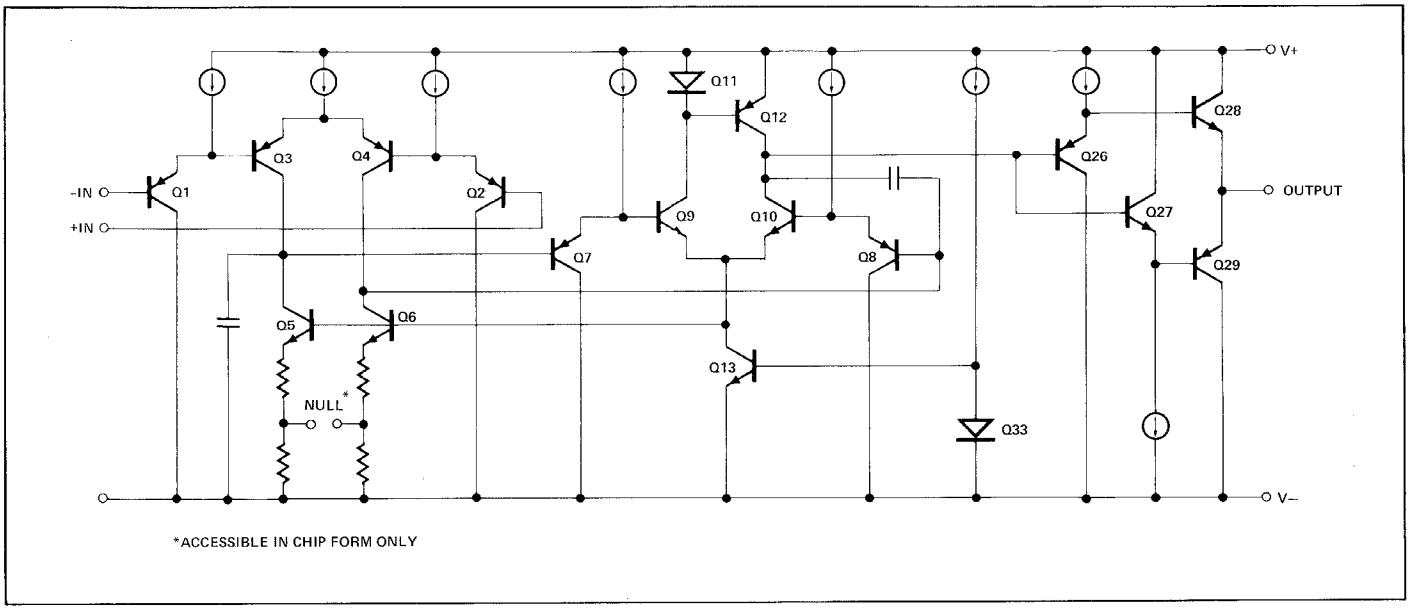
The excellent specifications of the individual amplifiers combined with the tight matching and temperature tracking between channels provide high performance in instrumentation amplifier designs. The individual amplifiers feature very low input offset voltage, low offset voltage drift, low noise voltage, and low bias current. They are fully compensated and protected.

Matching between channels is provided on all critical parameters including input offset voltage, tracking of offset voltage vs. temperature, non-inverting bias currents, and common-mode rejection.

## PIN CONNECTIONS




## SIMPLIFIED SCHEMATIC (Each Amplifier)



## ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage ..... 30V or Supply Voltage
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... –65°C to +150°C
Operating Temperature Range
OP-221A, B, C ..... –55°C to +125° C
OP-221E ..... –25°C to +85°C
OP-221G ..... –40°C to +85°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Junction Temperature ($T_j$) ..... –65°C to +150°C

| PACKAGE TYPE | $\Theta_{JA}$ (Note 2) | $\Theta_{JC}$ | UNITS |
|---|---|---|---|
| TO-99 (J) | 150 | 18 | °C/W |
| 8-Pin Hermetic DIP (Z) | 148 | 16 | °C/W |
| 8-Pin Plastic DIP (P) | 103 | 43 | °C/W |
| 8-Pin SO (S) | 158 | 43 | °C/W |

**NOTES:**
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. $\Theta_{JA}$ is specified for worst case mounting conditions, i.e., $\Theta_{JA}$ is specified for device in socket for TO, CerDIP and P-DIP packages; $\Theta_{JA}$ is specified for device soldered to printed circuit board for SO package.

## ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $T_A = 25°C$, unless otherwise noted.

| PARAMETER | SYMBOL | CONDITIONS | OP-221A/E MIN | OP-221A/E TYP | OP-221A/E MAX | OP-221B MIN | OP-221B TYP | OP-221B MAX | OP-221C/G MIN | OP-221C/G TYP | OP-221C/G MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage | $V_{OS}$ | | — | 75 | 150 | — | 150 | 300 | — | 250 | 500 | µV |
| Input Offset Current | $I_{OS}$ | $V_{CM} = 0$ | — | 0.5 | 3 | — | 1 | 5 | — | 1.5 | 7 | nA |
| Input Bias Current | $I_B$ | $V_{CM} = 0$ | — | 50 | 80 | — | 60 | 100 | — | 70 | 120 | nA |
| Input Voltage Range | IVR | V+ = 5V, V– = 0V (Note 2) | 0/3.5 | — | — | 0/3.5 | — | — | 0/3.5 | — | — | V |
| | | $V_S = \pm 15V$ | –15/13.5 | — | — | –15/13.5 | — | — | –15/13.5 | — | — | |
| Common-Mode Rejection Ratio | CMRR | V+ = 5V, V– = 0V<br>$0V \le V_{CM} \le 3.5V$<br>$V_S = \pm 15V$ | 90 | 100 | — | 85 | 90 | — | 75 | 85 | — | dB |
| | | $-15V \le V_{CM} \le 13.5V$ | 95 | 100 | — | 90 | 95 | — | 80 | 90 | — | |
| Power Supply Rejection Ratio | PSRR | $V_S = \pm 2.5V$ to $\pm 15V$ | — | 3 | 10 | — | 10 | 32 | — | 32 | 100 | µV/V |
| | | V– = 0V, V+ = 5V to 30V | — | 6 | 18 | — | 18 | 57 | — | 57 | 180 | |
| Large-Signal Voltage Gain | $A_{VO}$ | $V_S = \pm 15V$, $R_L = 10k\Omega$<br>$V_O = \pm 10V$ | 1500 | — | — | 1000 | — | — | 800 | — | — | V/mV |
| Output Voltage Swing | $V_O$ | V+ = 5V, V– = 0V,<br>$R_L = 10k\Omega$ | 0.7/4.1 | — | — | 0.7/4.1 | — | — | 0.8/4 | — | — | V |
| | | $V_S = \pm 15V$, $R_L = 10k\Omega$ | ±13.8 | — | — | ±13.8 | — | — | ±13.5 | — | — | |
| Slew Rate | SR | $R_L = 10k\Omega$, (Note 1) | 0.2 | 0.3 | — | 0.2 | 0.3 | — | 0.2 | 0.3 | — | V/µs |
| Bandwidth | BW | | — | 600 | — | — | 600 | — | — | 600 | — | kHz |
| Supply Current (Both Amplifiers) | $I_{SY}$ | $V_S = \pm 2.5V$, No Load | — | 450 | 550 | — | 500 | 600 | — | 550 | 650 | µA |
| | | $V_S = \pm 15V$, No Load | — | 600 | 800 | — | 800 | 850 | — | 850 | 900 | |

**NOTES:**
1. Sample tested.
2. Guaranteed by CMRR test limits.

## ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55°C \le T_A \le +125°C$ for OP-221A, B, and C, $-25°C \le T_A \le +85°C$ for OP-221E, $-40°C \le T_A \le +85°C$ for OP-221G, unless otherwise noted.

| PARAMETER | SYMBOL | CONDITIONS | OP-221A/E MIN | OP-221A/E TYP | OP-221A/E MAX | OP-221B MIN | OP-221B TYP | OP-221B MAX | OP-221C/G MIN | OP-221C/G TYP | OP-221C/G MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Average Input Offset Voltage Drift (Note 1) | $TCV_{OS}$ | | — | 0.75 | 1.5 | — | 1.2 | 2 | — | 2 | 3 | µV/°C |
| Input Offset Voltage | $V_{OS}$ | | — | 150 | 300 | — | 250 | 450 | — | 400 | 700 | µV |
| Input Offset Current | $I_{OS}$ | $V_{CM} = 0$ | — | 1 | 5 | — | 1.5 | 7 | — | 2 | 10 | nA |
| Input Bias Current | $I_B$ | $V_{CM} = 0$ | — | 55 | 100 | — | 65 | 120 | — | 80 | 140 | nA |
| Input Voltage Range | IVR | V+ = 5V, V– = 0V (Note 2) | 0/3.2 | — | — | 0/3.2 | — | — | 0/3.2 | — | — | V |
| | | $V_S = \pm 15V$ | –15/13.2 | — | — | –15/13.2 | — | — | 15/13.2 | — | — | |
| Common-Mode Rejection Ratio | CMRR | V+ = 5V, V– = 0V<br>$0V \le V_{CM} \le 3.2V$<br>$V_S = \pm 15V$ | 85 | 90 | — | 80 | 85 | — | 70 | 80 | — | dB |
| | | $-15V \le V_{CM} \le 13.2V$ | 90 | 95 | — | 85 | 90 | — | 75 | 85 | — | |

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 2.5V$ to $\pm 15V$, $-55°C \le T_A \le +125°C$ for OP-221A, B, and C, $-25°C \le T_A \le +85°C$ for OP-221E, $-40°C \le T_A \le +85°C$ for OP-221G, unless otherwise noted. *(Continued)*

| PARAMETER | SYMBOL | CONDITIONS | OP-221A/E MIN | OP-221A/E TYP | OP-221A/E MAX | OP-221B MIN | OP-221B TYP | OP-221B MAX | OP-221C/G MIN | OP-221C/G TYP | OP-221C/G MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Power Supply Rejection Ratio | PSRR | $V_S = \pm 2.5V$ to $\pm 15V$ | — | 6 | 18 | — | 18 | 57 | — | 57 | 180 | µV/V |
| | | $V- = 0V$, $V+ = 5V$ to $30V$ | — | 10 | 32 | — | 32 | 100 | — | 100 | 320 | |
| Large-Signal Voltage Gain | $A_{VO}$ | $V_S = \pm 15V$, $R_L = 10k\Omega$, $V_O = \pm 10V$ | 1000 | — | — | 800 | — | — | 600 | — | — | V/mV |
| Output Voltage Swing | $V_O$ | $V+ = 5V$, $V- = 0V$, $R_L = 10k\Omega$ | 0.8/3.8 | — | — | 0.8/3.8 | — | — | 0.9/3.7 | — | — | V |
| | | $V_S = \pm 15V$, $R_L = 10k\Omega$ | $\pm 13.5$ | $\pm 14$ | — | $\pm 13.5$ | $\pm 14$ | — | $\pm 13.2$ | — | — | |
| Supply Current (Both Amplifiers) | $I_{SY}$ | $V_S = \pm 2.5V$, No Load | — | 500 | 650 | — | 550 | 700 | — | 600 | 750 | µA |
| | | $V_S = \pm 15V$, No Load | — | 700 | 900 | — | 900 | 950 | — | 950 | 1000 | |

**NOTES:**
1. Sample tested.
2. Guaranteed by CMRR test limits.

**MATCHING CHARACTERISTICS** at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

| PARAMETER | SYMBOL | CONDITIONS | OP-221A/E MIN | OP-221A/E TYP | OP-221A/E MAX | OP-221B MIN | OP-221B TYP | OP-221B MAX | OP-221C/G MIN | OP-221C/G TYP | OP-221C/G MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage Match | $\Delta V_{OS}$ | | — | 50 | 200 | — | 150 | 400 | — | 250 | 600 | µV |
| Average Noninverting Bias Current | $I_B+$ | | — | — | 80 | — | — | 100 | — | — | 120 | nA |
| Noninverting Input Offset Current | $I_{OS}+$ | | — | 2 | 5 | — | 2 | 5 | — | 4 | 10 | nA |
| Common-Mode Rejection Ratio Match (Note 1) | ΔCMRR | $V_{CM} = -15V$ to $+13.5V$ | 92 | — | — | 87 | — | — | 72 | — | — | dB |
| Power Supply Rejection Ratio Match (Note 2) | ΔPSRR | $V_S = \pm 2.5V$ to $\pm 15V$ | — | — | 14 | — | — | 44 | — | — | 140 | µV/V |

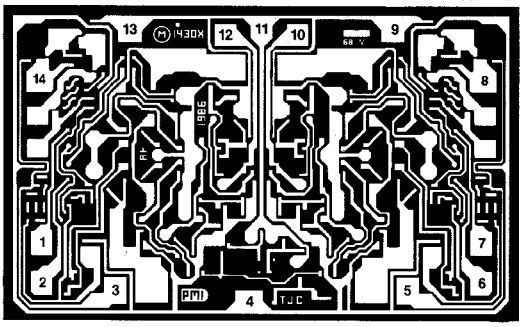
**MATCHING CHARACTERISTICS** at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$ for OP-221A, B, and C, $-25°C \le T_A \le +85°C$ for OP-221E, $-40°C \le T_A \le +85°C$ for OP-221G, unless otherwise noted. Grades E and G are sample tested.

| PARAMETER | SYMBOL | CONDITIONS | OP-221A/E MIN | OP-221A/E TYP | OP-221A/E MAX | OP-221B MIN | OP-221B TYP | OP-221B MAX | OP-221C/G MIN | OP-221C/G TYP | OP-221C/G MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage Match | $\Delta V_{OS}$ | | — | 100 | 400 | — | 250 | 600 | — | 400 | 800 | µV |
| Average Noninverting Bias Current | $I_B+$ | $V_{CM} = 0$ | — | — | 100 | — | — | 120 | — | — | 140 | nA |
| Input Offset Voltage Tracking | $TC\Delta V_{OS}$ | | — | 1 | 2 | — | 1 | 3 | — | 3 | 5 | µV/°C |
| Noninverting Input Offset Current | $I_{OS}+$ | $V_{CM} = 0$ | — | 3 | 7 | — | 3 | 7 | — | 6 | 12 | nA |
| Common-Mode Rejection Ratio Match (Note 1) | ΔCMRR | $V_{CM} = -15V$ to $+13.2V$ | 87 | 90 | — | 82 | 85 | — | 72 | 80 | — | dB |
| Power Supply Rejection Ratio Match (Note 2) | ΔPSRR | | — | — | 26 | — | — | 78 | — | — | 250 | µV/V |

**NOTES:**
1. ΔCMRR is $20 \log_{10} V_{CM}/\Delta CME$, where $V_{CM}$ is the voltage applied to both noninverting inputs and ΔCME is the difference in common-mode input-referred error.
2. ΔPSRR is: $\frac{\text{Input-Referred Differential Error}}{\Delta V_S}$

# OP-221

## DICE CHARACTERISTICS



DIE SIZE 0.097 × 0.063 inch, 6111 sq. mils
(2.464 × 1.600 mm, 3.94 sq. mm)

NOTE: All V+ PADS ARE INTERNALLY CONNECTED.

1. INVERTING INPUT (A)
2. NONINVERTING INPUT (A)
3. BALANCE (A)
4. V−
5. BALANCE (B)
6. NONINVERTING INPUT (B)
7. INVERTING INPUT (B)
8. BALANCE (B)
9. V+
10. OUT (B)
11. V+
12. OUT (A)
13. V+
14. BALANCE (A)

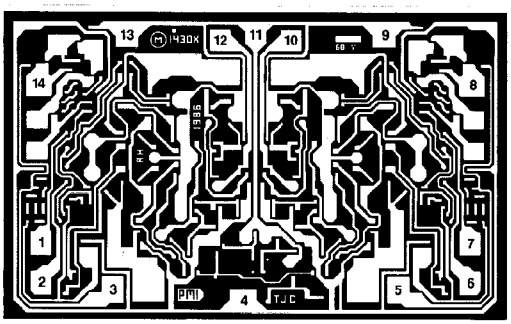
**WAFER TEST LIMITS** at $V_S = \pm 2.5V$ to $\pm 15V$, $T_A = 25°C$, unless otherwise noted.

| PARAMETER | SYMBOL | CONDITIONS | OP-221N LIMIT | OP-221G LIMIT | OP-221GR LIMIT | UNITS |
|---|---|---|---|---|---|---|
| Input Offset Voltage | $V_{OS}$ | | 200 | 350 | 500 | μV MAX |
| Input Offset Current | $I_{OS}$ | $V_{CM} = 0$ | 3.5 | 5.5 | 7 | nA MAX |
| Input Bias Current | $I_B$ | $V_{CM} = 0$ | 85 | 105 | 120 | nA MAX |
| Input Voltage Range | IVR | V+ = 5V, V− = 0V | 0/3.5 | 0/3.5 | 0/3.5 | V MIN/MAX |
| | | $V_S = \pm 15V$ | −15/13.5 | −15/13.5 | −15/13.5 | V MIN |
| Common-Mode Rejection Ratio | CMRR | V− = 0V, V+ = 5V, $0V \le V_{CM} \le 3.5V$ | 88 | 83 | 75 | dB MIN |
| | | $V_S = \pm 15V$, $-15V \le V_{CM} \le 13.5V$ | 93 | 88 | 80 | |
| Power Supply Rejection Ratio | PSRR | $V_S = \pm 2.5V$ to $\pm 15V$ | 12.5 | 40 | 100 | μV/V MAX |
| | | V− = 0V, V+ = 5V to 30V | 22.5 | 70 | 180 | |
| Large-Signal Voltage Gain | $A_{VO}$ | $V_S = \pm 15V$, $R_L = 10k\Omega$ | 1500 | 1000 | 800 | V/mV MIN |
| Output Voltage Swing | $V_O$ | V+ = 5V, V− = 0V, $R_L = 10k\Omega$ | 0.7/4.1 | 0.7/4.1 | 0.8/4 | V MIN/MAX |
| | | $V_S = \pm 15V$, $R_L = 10k\Omega$ | ±13.8 | ±13.8 | ±13.5 | V MIN |
| Supply Current (Both Amplifiers) | $I_{SY}$ | $V_S = \pm 2.5V$, No Load | 560 | 610 | 650 | μA MAX |
| | | $V_S = \pm 15V$, No Load | 810 | 860 | 900 | |

**NOTE:**
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

# OP-221

## DICE CHARACTERISTICS



DIE SIZE 0.097 × 0.063 inch, 6111 sq. mils
(2.464 × 1.600 mm, 3.94 sq. mm)

**NOTE:** All V+ PADS ARE INTERNALLY CONNECTED.

1. INVERTING INPUT (A)
2. NONINVERTING INPUT (A)
3. BALANCE (A)
4. V−
5. BALANCE (B)
6. NONINVERTING INPUT (B)
7. INVERTING INPUT (B)
8. BALANCE (B)
9. V+
10. OUT (B)
11. V+
12. OUT (A)
13. V+
14. BALANCE (A)

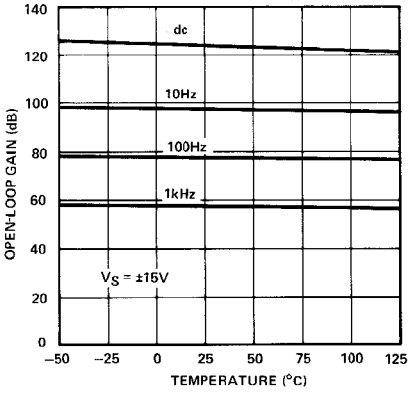
**WAFER TEST LIMITS** at $V_S = \pm 2.5V$ to $\pm 15V$, $T_A = 25°C$, unless otherwise noted.

| PARAMETER | SYMBOL | CONDITIONS | OP-221N LIMIT | OP-221G LIMIT | OP-221GR LIMIT | UNITS |
|---|---|---|---|---|---|---|
| Input Offset Voltage | $V_{OS}$ | | 200 | 350 | 500 | μV MAX |
| Input Offset Current | $I_{OS}$ | $V_{CM} = 0$ | 3.5 | 5.5 | 7 | nA MAX |
| Input Bias Current | $I_B$ | $V_{CM} = 0$ | 85 | 105 | 120 | nA MAX |
| Input Voltage Range | IVR | V+ = 5V, V− = 0V<br>$V_S = \pm 15V$ | 0/3.5<br>−15/13.5 | 0/3.5<br>−15/13.5 | 0/3.5<br>−15/13.5 | V MIN/MAX<br>V MIN |
| Common-Mode Rejection Ratio | CMRR | V− = 0V, V+ = 5V, $0V \le V_{CM} \le 3.5V$<br>$V_S = \pm 15V$, $-15V \le V_{CM} \le 13.5V$ | 88<br>93 | 83<br>88 | 75<br>80 | dB MIN |
| Power Supply Rejection Ratio | PSRR | $V_S = \pm 2.5V$ to $\pm 15V$<br>V− = 0V, V+ = 5V to 30V | 12.5<br>22.5 | 40<br>70 | 100<br>180 | μV/V MAX |
| Large-Signal Voltage Gain | $A_{VO}$ | $V_S = \pm 15V$<br>$R_L = 10k\Omega$ | 1500 | 1000 | 800 | V/mV MIN |
| Output Voltage Swing | $V_O$ | V+ = 5V, V− = 0V, $R_L = 10k\Omega$<br>$V_S = \pm 15V$, $R_L = 10k\Omega$ | 0.7/4.1<br>±13.8 | 0.7/4.1<br>±13.8 | 0.8/4<br>±13.5 | V MIN/MAX<br>V MIN |
| Supply Current (Both Amplifiers) | $I_{SY}$ | $V_S = \pm 2.5V$, No Load<br>$V_S = \pm 15V$, No Load | 560<br>810 | 610<br>860 | 650<br>900 | μA MAX |

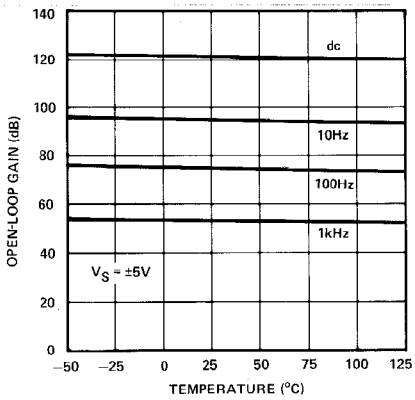
**NOTE:**
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

## TYPICAL PERFORMANCE CHARACTERISTICS

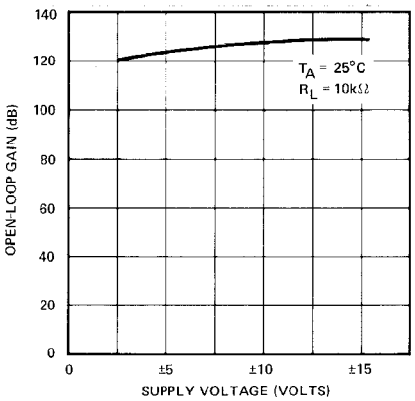
### OPEN-LOOP GAIN AT ±15V vs TEMPERATURE



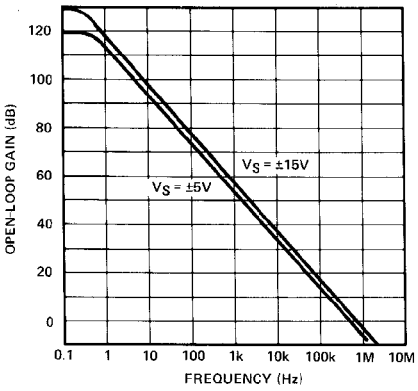

### OPEN-LOOP GAIN AT ±5V vs TEMPERATURE



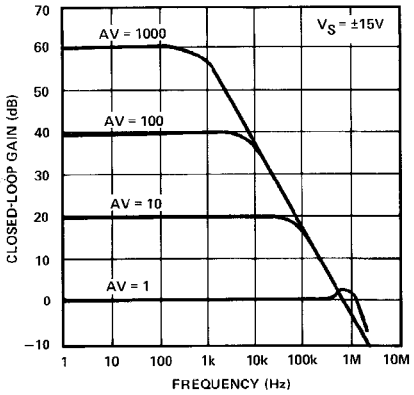

### OPEN-LOOP GAIN vs SUPPLY VOLTAGE



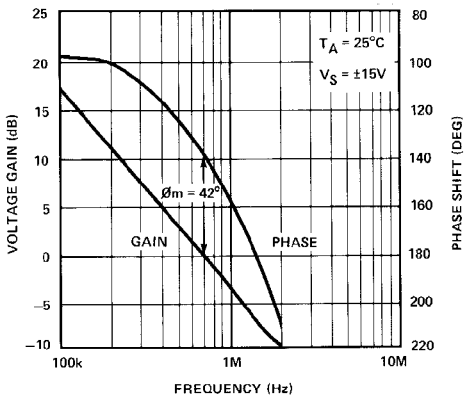

### OPEN-LOOP GAIN vs FREQUENCY



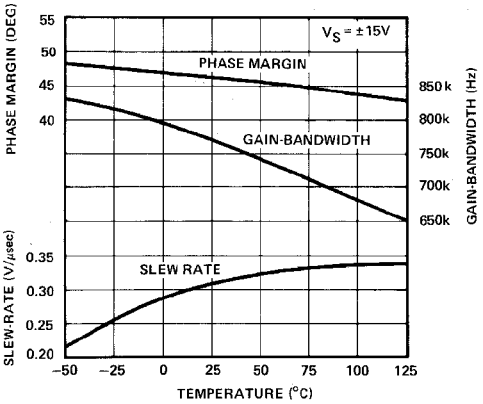

### CLOSED-LOOP GAIN vs FREQUENCY



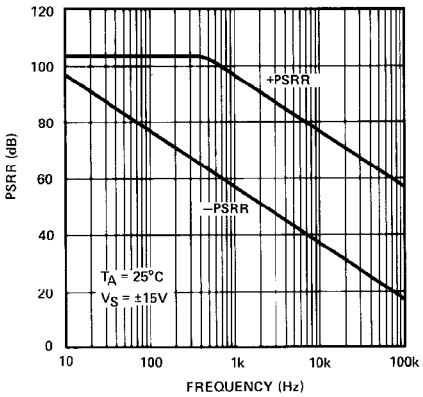

### GAIN AND PHASE SHIFT vs FREQUENCY



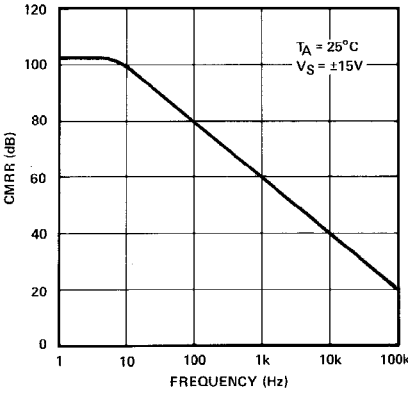

### PHASE MARGIN, GAIN-BANDWIDTH, AND SLEW RATE vs TEMPERATURE




### PSRR vs FREQUENCY

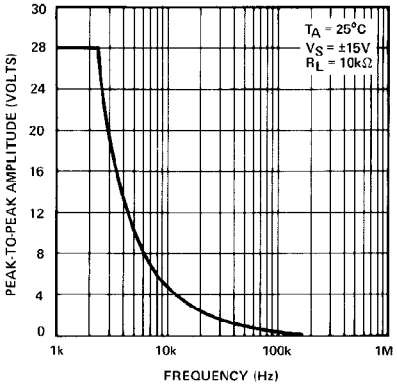



### CMRR vs FREQUENCY

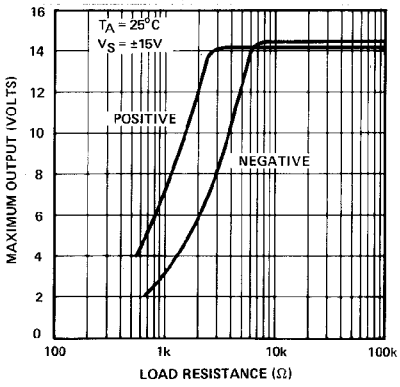


## TYPICAL PERFORMANCE CHARACTERISTICS

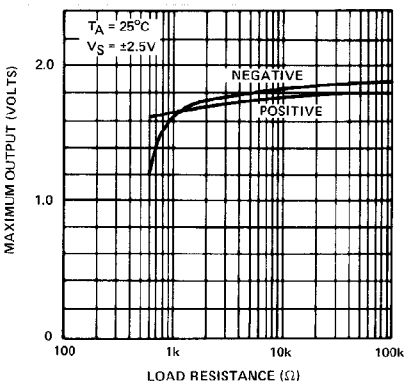
### MAXIMUM OUTPUT SWING vs FREQUENCY



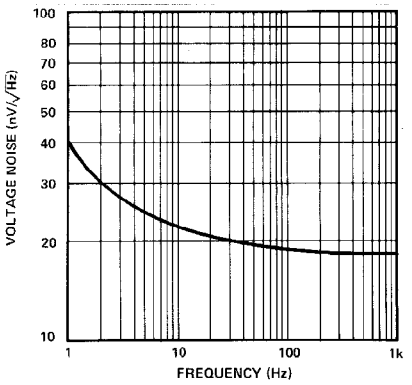

### MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



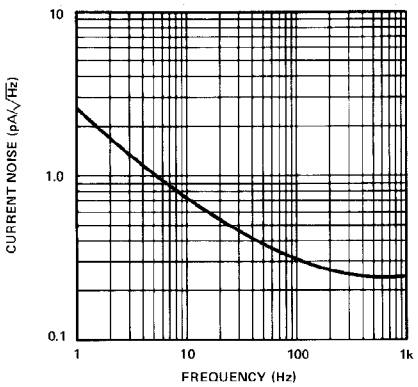

### MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



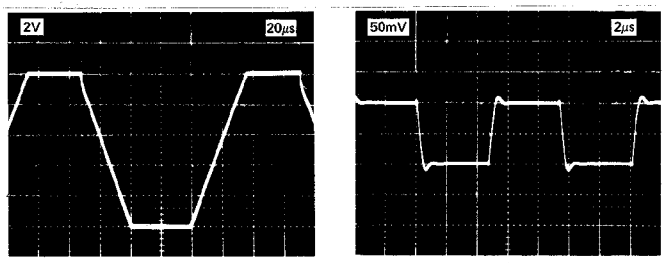

### VOLTAGE NOISE DENSITY ($e_n$) vs FREQUENCY

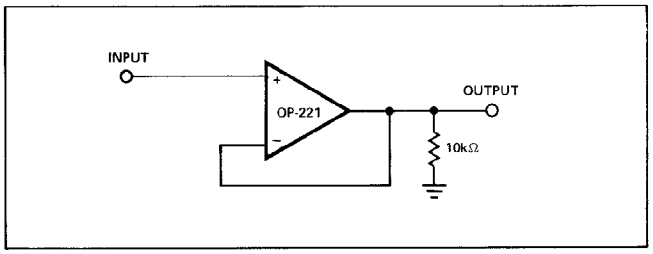



### CURRENT NOISE DENSITY ($I_n$) vs FREQUENCY

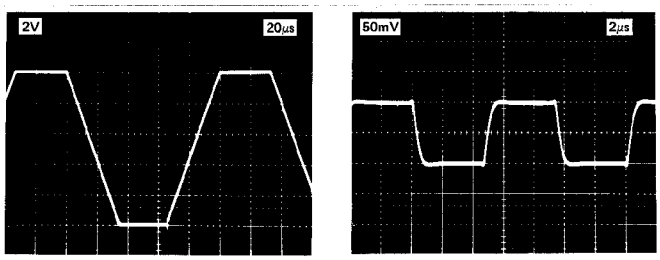


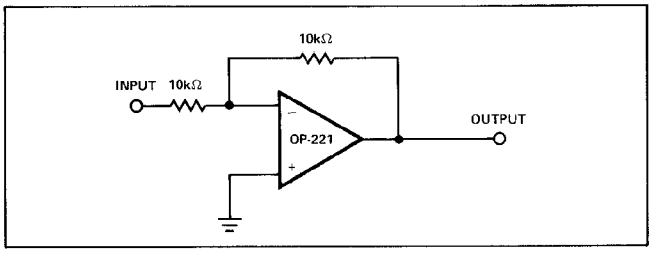

### NONINVERTING STEP RESPONSE




### INVERTING STEP RESPONSE



## SPECIAL NOTES ON THE APPLICATION OF DUAL MATCHED OPERATIONAL AMPLIFIERS

### ADVANTAGES OF DUAL MONOLITHIC OPERATIONAL AMPLIFIERS

Dual matched operational amplifiers provide the engineer with a powerful tool for designing instrumentation amplifiers and many other differential-input circuits. These designs are based on the principle that careful matching between two operational amplifiers can minimize the effect of DC errors in the individual amplifiers.

Reference to the circuit shown in Figure 1, a differential-in, differential-out amplifier, shows how the reductions in error can be accomplished. Assuming the resistors used are ideally matched, the gain of each side will be identical. If the offset voltages of each amplifier are perfectly matched, then the net differential voltage at the amplifier's output will be zero. Note that the output offset error of this amplifier is not a function of the offset voltage of the individual amplifiers, but only a function of the *difference* (degree of matching) between the amplifiers' offset voltages. This error-cancellation principle holds for a considerable number of input referred error parameters — offset voltage, offset voltage drift, inverting and noninverting bias currents, common-mode and power supply rejection ratios. Note also that the impedances of each input, both common-mode and differential-mode, are high and tightly matched, an important feature not practical with single operational amplifier circuits.

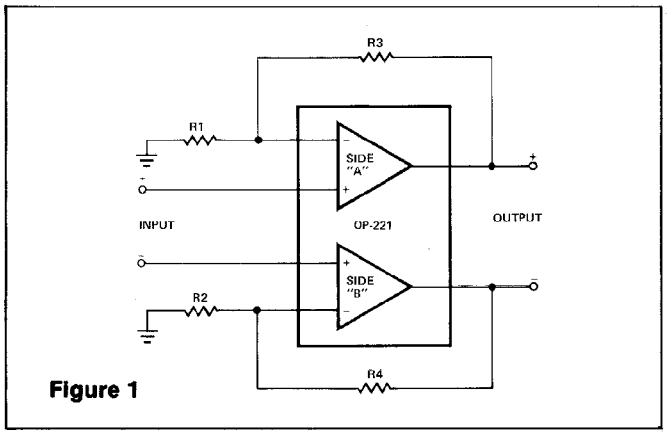



**Figure 1**

## INSTRUMENTATION AMPLIFIER APPLICATIONS

### Two-Op-Amp Configuration

The two-op-amp circuit (Figure 2), is recommended where the common-mode input voltage range is relatively limited; the common-mode and differential voltage both appear at V1.

The high open-loop gain of the OP-221 is very important in achieving good CMRR in this configuration. Finite open-loop gain of A1 ($A_{01}$) causes undesired feedthrough of the common-mode input. For $A_d/A_{01} << 1$, the common-mode error (CME) at the output due to this effect is approximately $(2\ A_d/A_{01}) \times V_{CM}$. This circuit features independent adjustment of CMRR and differential gain.

### Three-Op-Amp Configuration

The three-op-amp circuit (Figure 3), has increased common-mode voltage range because the common-mode voltage is not amplified as it is in Figure 2. The CMR of this amplifier is directly proportional to the match of the CMR of the input op amps. CMRR can be raised even further by trimming the output stage resistors.

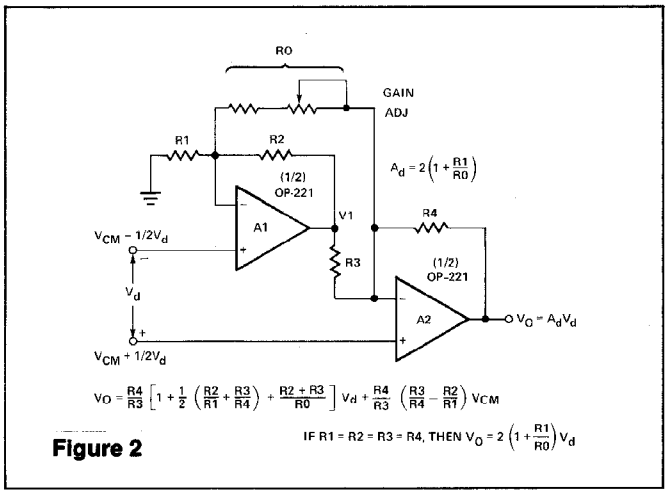



**Figure 2**

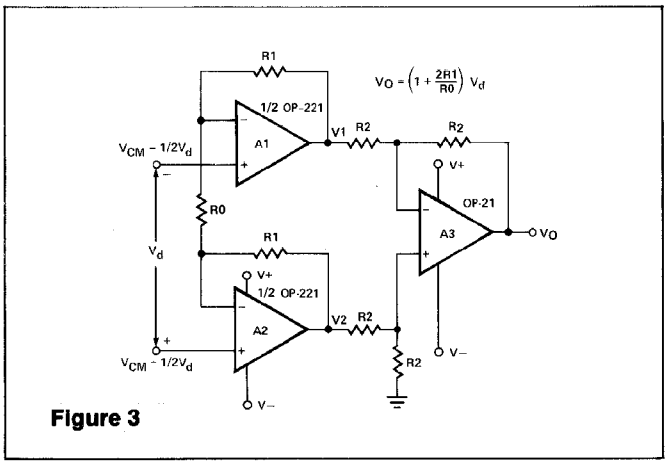



**Figure 3**