ZARLINK SEMICONDUCTOR™

ISSUE 3 March 1997

Features

- Microprocessor compatible control inputs
- On chip control memory and address decoding
- Row addressing
- Master reset
- 32 crosspoint switches in 8 x 4 array
- 5.0V to 15.0V operation
- Low crosstalk between switches
- Low on resistance: 90Ω (typ.) at 13V
- Matched switch characteristics
- Switches frequencies up to 40MHz

Applications

- PABX and key sytems
- Data acquisition systems
- Test equipment/instrumentation
- Analog/digital multiplexers

Ordering Information

MT8804AE	24 Pin Plastic DIP
MT8804AP	28 Pin PLCC

-40° to 85°C

Description

The MT8804A is a CMOS/LSI 8 x 4 Analog Switch Array incorporating control memory (32 bits), decoder and digital logic level converters. This circuit has digitally controlled analog switches having very low “ON“ resistance and very low “OFF” leakage current. Switches will operate with analog signals at frequencies to 40 MHz and up to 15.0Vp-p. A “HIGH“ on the Master Reset input switches all channels “OFF“ and clears the memory. This device is ideal for crosspoint switching applications.

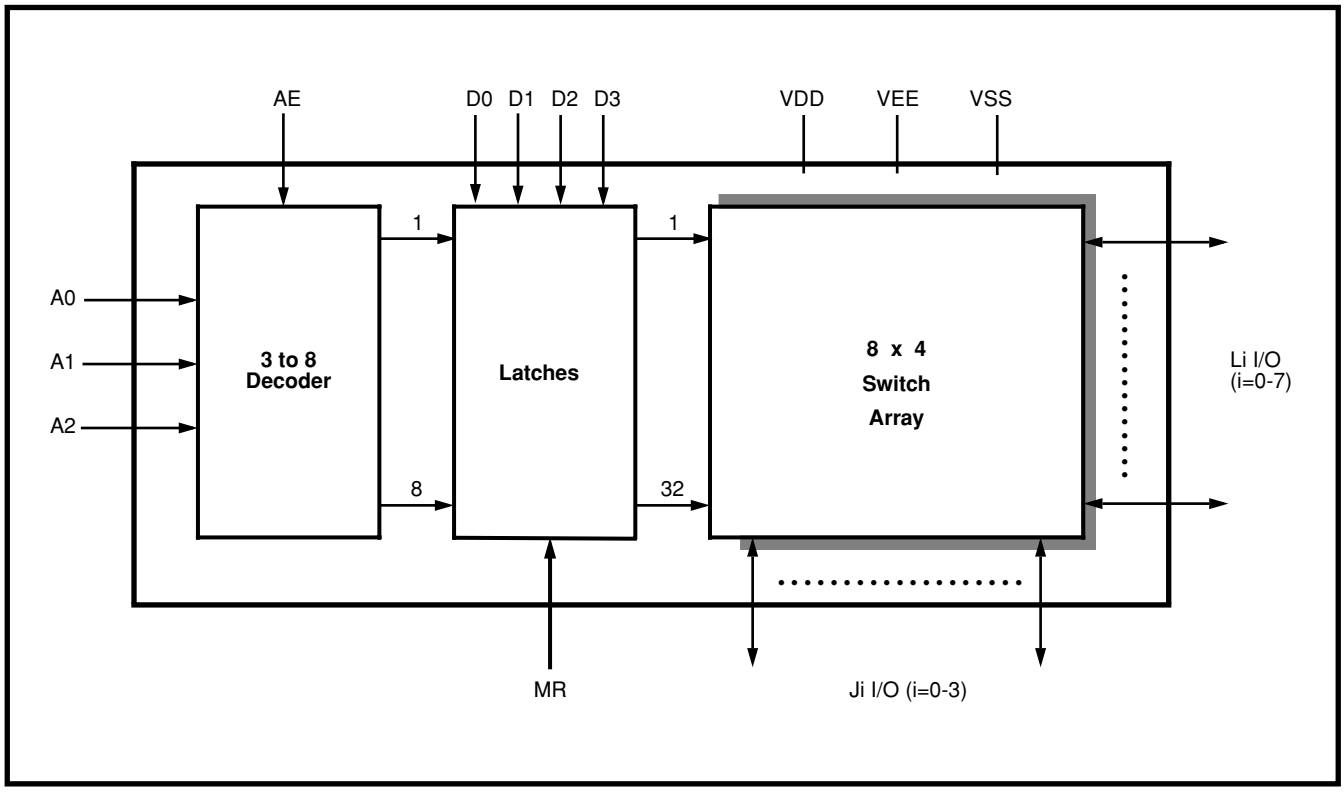


Figure 1 - Functional Block Diagram

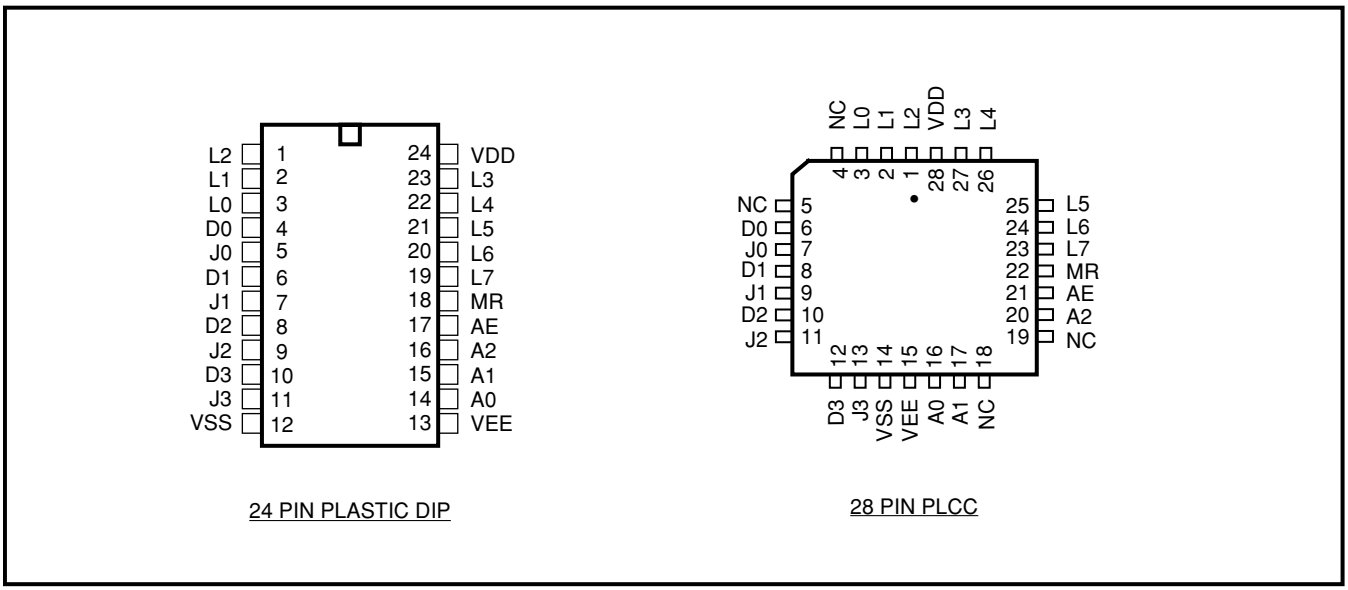


Figure 2 - Pin Connections

Pin Description

Pin #		Name	Description
PDIP	PLCC		
1-3	1-3	L2-L0	**L2-L0 Analog Lines (Inputs/Outputs):** These are connected to the L2-L0 columns of the switch array.
4	6	D0	**D0 Data (Input)**: Active High.
5	7	J0	**J0 Analog Junctor (Input/Output).** This is connected to the J0 row of the switch array.
6	8	DI	**DI Data (Input).** Active High.
7	9	J1	**J1 Analog Junctor (Input/Output).** This is connected to the J1 row of the switch array.
8	10	D2	**D2 Data (Input)**: Active High.
9	11	J2	**J2 Analog Junctor (Input/Output).** This is connected to the J2 row of the switch array.
10	12	D3	**D3 Data (Input)**: Active High.
11	13	J3	**J3 Analog Junctor (Input/Output).** This is connected to the J3 row of the switch array.
12	14	V_{SS}	**Digital Ground Reference.**
13	15	V_{EE}	**Negative Power Supply.**
14-16	16,17, 20	A0-A2	**A0-A2 Address Lines (Inputs)**.
17	21	AE	**Address Enable/Strobe (Input)**. Enables function selected by address and data. Address must be stable before AE goes high and D0-D3 must be stable on the falling edge of the AE. Active High.
18	22	MR	**Master RESET (Input).** This is used to turn off all switches. Active High.
19-23	23-27	L7-L3	**L7-L3 Analog Lines (Inputs/Outputs).** These are connected to the L7-L3 columns of the switch array.
24	28	V_{DD}	**Positive Power Supply.**
	4, 5,18, 19,	NC	**No Connect.**

Functional Description

The MT8804A is a CMOS/LSI 8 X 4 Analog Switch Array incorporating an 8 X 4 analog switch array, address decoder, control memory, and digital logic level converter.

The analog switch array is arranged in 8 rows and 4 columns. The row input/outputs are referred to as Lines (L0-L7) and the column input/outputs as Junctors (J0-J3). The crosspoint analog switches interconnect the lines and junctors when turned "ON" and provide a high degree of isolation when turned "OFF". Interchannel crosstalk is minimal despite the high density of the analog switch array. The control memory of the MT8804A can be treated as an 8 word by 4 bit random access memory. The 8 words are selected by the ADDRESS (A0-A2) inputs through the on chip address decoder. Data is presented to the memory via the four DATA inputs (D0-D3). This data is asynchronously written into the control memory whenever the ADDRESS ENABLE (AE) input is HIGH. A HIGH level written into a memory cell turns the corresponding crosspoint switch "ON" while a LOW level causes the crosspoint to turn "OFF".

Only the crosspoint switches corresponding to the addressed memory word are affected when data is written into the memory. The remaining switches retain their previous states. By establishing appropriate patterns in the control memory, any combination of lines and junctors may be interconnected. A HIGH level on the MASTER RESET (MR) input returns all memory locations to a LOW level and turns all crosspoint switches "OFF" effectively isolating the lines from the junctors. The digital logic level converters allow the digital input levels to differ from limits of the analog levels switched through the array. For example, with

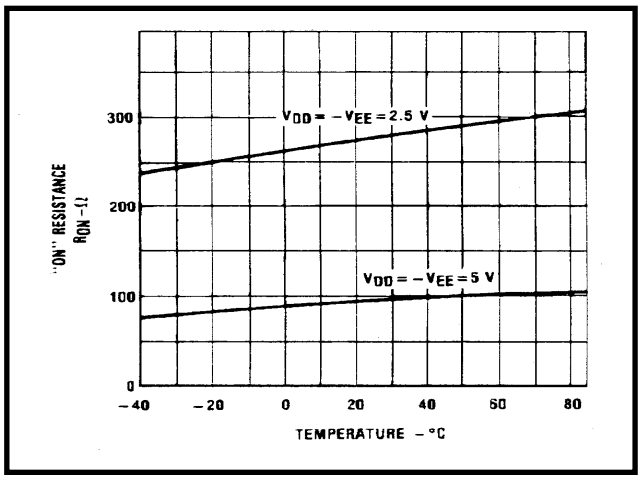


Figure 3 - On Resistance vs. Temperature (Input Signal Voltage=Supply Voltage/2)

V_{DD}=5V, V_{SS}=0V and V_{EE}=-6V, the control inputs can be driven by a 5V system while the analog voltages through the crosspoint switches can swing from +5V to -6V.

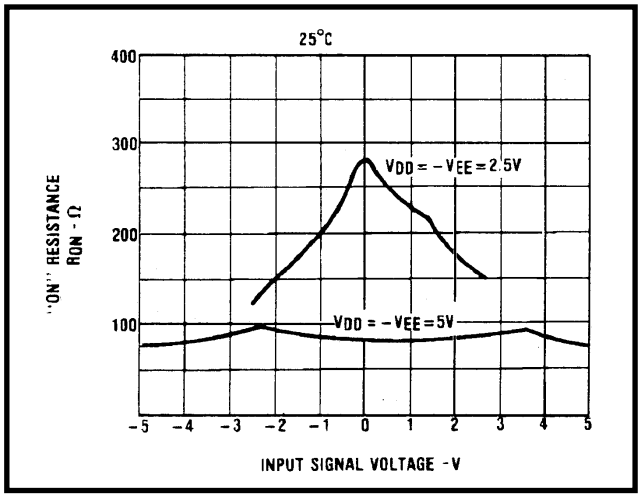


Figure 4 - On Resistance vs. Input Signal Voltage

8x8 Analog/Digital Switch

Two MT8804s configured as shown, implement an 8 x 8 analog/digital switch. The switch capacity can be expanded to an M x N array of inputs/outputs. Expansion in the M dimension is as shown with the MT8804A lines (L0-L7) commoned. Expansion in the N dimension is accomplished by replicating the circuit shown and connecting the MT8804A junctors (J0-J3) in common. The address and data control inputs of the MT8804A's can be connected in common for any size and switch provided that the address enable (AE) inputs are driven individually. A particular signal path is connected by setting up the appropriate signals or the address and data lines and taking the corresponding address enable input high. The master reset (MR), when taken high, disconnects all signal paths.

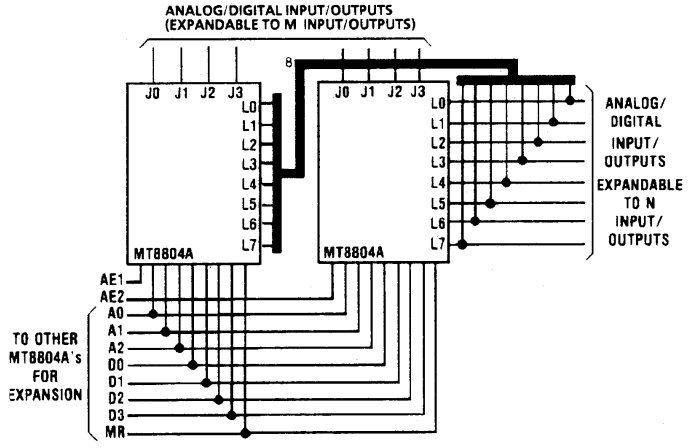


Figure 5 - 8 x 8 Analog/Digital Switch

Absolute Maximum Ratings* - Voltages are with respect to V_{EE} unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	V_{DD}-V_{SS} V_{DD}-V_{EE} V_{SS}-V_{EE}	-0.3 -0.3 -0.3	16 16 16	V V V
2	Analog Input Voltage	V_{INA}	V_{EE}-0.3	V_{DD}+0.3	V
3	Digital Input Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
4	Current on any Logic Pin	I		10	mA
5	Storage Temperature	T_S	-65	+150	°C
6	Package Power Dissipation PLASTIC DIP	P_D		0.6	W

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to V_{EE} unless otherwise stated.

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Operating Temperature	T_O	-40	25	85	°C	
2	Supply Voltage	V_{DD}-V_{SS} V_{DD}-V_{EE} V_{SS}-V_{EE}	5 5 0	5 10 5	15 15 10	V V V	
3	Analog Input Voltage	V_{INA}	V_{EE}		V_{DD}	V	
4	Digital Input Voltage	V_{IN}	V_{SS}		V_{DD}	V	

DC Electrical Characteristics† - Voltages are with respect to V_{EE}=V_{SS}=0V.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Quiescent Supply Current	I_{DD}		1	100	µA	V_{DD}=15V. All digital inputs at V_{IN}=V_{SS} or V_{DD}
2	Off-state Leakage Current (Any line to any junctor)	I_{OFF}		±0.1	±500	nA	V_{DD}=13V, Switch is 'Off' IV_{Ji} - $V_{Lj}I$ = V_{DD} - V_{EE}
3	Input Logic "0" level	V_{IL}			3.0 1.5	V V	V_{DD} =10V V_{DD}=5V V_{INA}=V_{DD} through 1kΩ
4	Input Logic "1" level	V_{IH}	7.0 3.5			V V	V_{DD} =10V V_{DD}=5V V_{INA}=V_{DD} through 1kΩ
5	Maximum current through Crosspoint Switch	I_{MAX}			±8.0	mA	V_{DD}=13V

† DC Electrical Characteristics are at ambient temperature (25°C).
‡ Typical figures are for design aid only; not guaranteed and not subject to production testing.

DC Electrical Characteristics- Switch Resistance - V_{DC} is the external DC offset applied at the analog I/O pins.

	Characteristics	Sym	25°C			70°C	85°C	Units	Test Conditions
			Min	Typ	Max	Typ	Typ		
1	On-state Resistance V_{DD}=13V V_{DD}=10V V_{DD}= 5V	R_{ON}	60	90 105 290	108 160 650	105 120 320	110 125 325	Ω Ω Ω	V_{SS}=V_{EE}=0V,V_{DC}=V_{DD}/2, IV_{Ji} - $V_{Lj}I$ = 0.6V
2	Difference in on-state resistance between two switches V_{DD}=13V V_{DD}=10V	ΔR_{ON}		 20 30		 20 30	 20 30	 Ω Ω	V_{SS}=V_{EE}=0V,V_{DC}=V_{DD}/2, IV_{Ji} - $V_{Lj}I$ = 0.6V

AC Electrical Characteristics† - Crosspoint Performance

-V_{DC} is the external DC offset applied at the analog I/O pins. Voltages are with respect to V_{DD}=10V, V_{SS}=V_{EE}=0V unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Switch Line Capacitance	C_{IS}		5		pF	
2	Switch Junctor Capacitance	C_{OS}		20		pF	
3	Feedthrough Capacitance	C_I		0.2		pF	
4	Frequency Response Channel "ON" 20LOG(V_{OUT} / V_{INA}) = -3dB	F_{3dB}		40		MHz	Switch is "ON"; V_{DC}=5V, V_{INA}=5Vpp sinewave f= 1kHz; R_L = 1kΩ
5	Total Harmonic Distortion V_{DD}=15V/V_{DC}=7.5V V_{DD}=10V/V_{DC}=5V V_{DD}=5V/V_{DC}=2.5V	THD		 0.1 0.2 1.0		 % % %	Switch is "ON"; V_{EE}=V_{SS}=0V V_{INA}=5Vpp sinewave f= 1kHz; R_L = 10kΩ
6	Feedthrough Channel "OFF" Feed.=20LOG (V_{OUT} / V_{INA})	FDT		-50		dB	All Switches "OFF"; V_{INA}= 5Vpp sinewave f= 1MHz; R_L= 1kΩ. V_{DC}=5V
7	Crosstalk between any two channels for switches Li - Ji and Lj - Jj. Li - Ji is "ON" Lj - Jj is "OFF" Xtalk=20LOG (V_{Jj}/V_{Li}).	X_{talk}		-40 -90		dB dB	V_{INA}=2Vpp sinewave f= 1.0MHz; R_L = 600Ω. V_{INA}=2Vpp sinewave f= 3.4kHz; R_L = 600Ω. V_{DC} = 5V
8	Propagation delay through switch	t_{PS}		10		ns	C_L=50pF

† AC Electrical Characteristics are at ambient temperature (25°C).
‡ Typical figures are for design aid only; not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Control and I/O Timings

- Voltages are with respect to V_{SS}=V_{EE}=0V unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Digital Input Capacitance	C_{DI}		5		pF	V_{DD}=10V
2	Setup Time D0-D3 to AE	t_{DS}	150 200			ns ns	V_{DD}=10V V_{DD}=5V
3	Hold Time D0-D3 to AE	t_{DH}	120 300			ns ns	V_{DD}=10V V_{DD}=5V
4	Setup Time Address to AE	t_{AS}	0 50			ns ns	V_{DD}=10V V_{DD}=5V
5	Hold Time Address to AE	t_{AH}	120 300			ns ns	V_{DD}=10V V_{DD}=5V
6	AE Pulse Width	t_{AEW}	100 250			ns ns	V_{DD}=10V V_{DD}=5V
7	AE to Switch Status Delay	t_{PAE}		200 650	300 900	ns ns	V_{DD}=10V V_{DD}=5V See Note 1
8	DATA to Switch Status Delay	t_{PLH} t_{PHL}		250 650	400 1000	ns ns	V_{DD}=10V V_{DD}=5V See Note 1
9	MR to Switch Status Delay	t_{MR} t_{MRR}		250 500 200 500	400 600 350 750	ns ns ns ns	V_{DD}=10V V_{DD}=5V See Note 2 V_{DD}=10V V_{DD}=5V

† AC Electrical Characteristics are at ambient temperature (25°C).
‡ Typical figures are for design aid only; not guaranteed and not subject to production testing.
Note 1 R_L= 10kΩ, C_L=50pF
Note 2 R_L= 1kΩ, C_L=50pF
Digital Input rise time (tr) and fall time (tf) = 5ns.

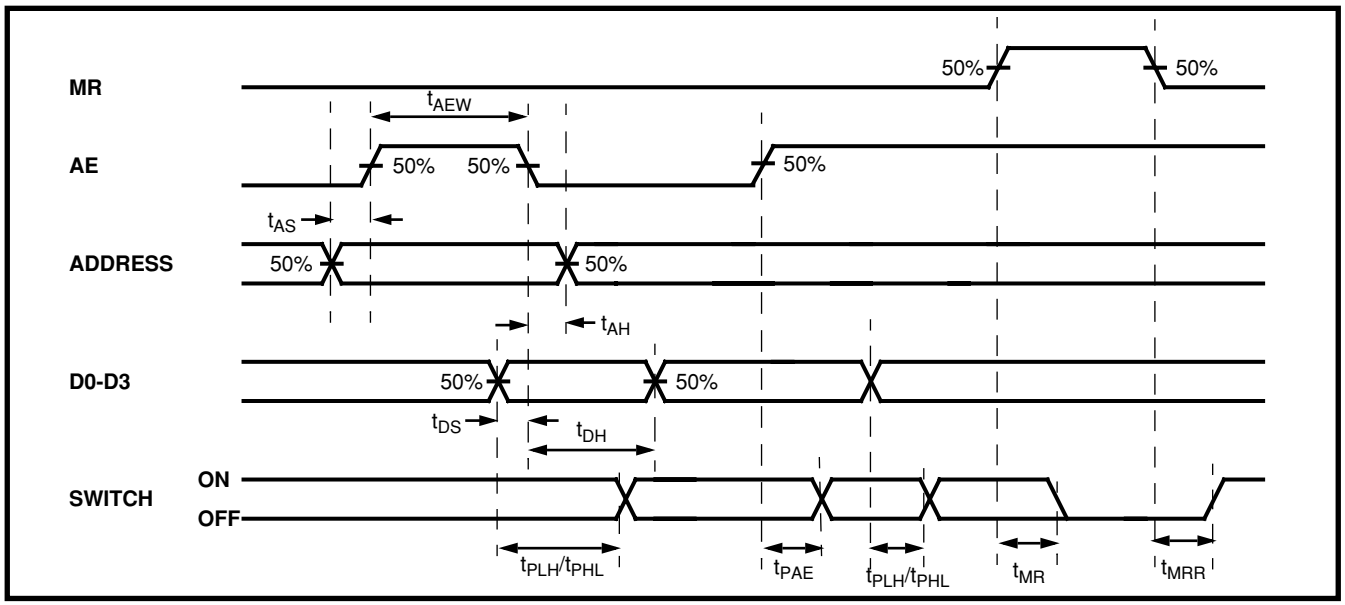
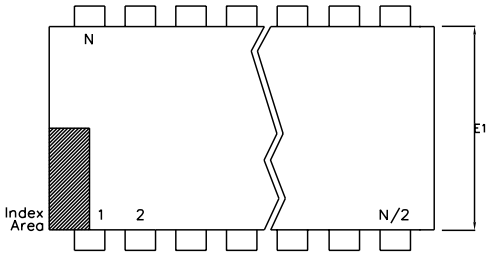


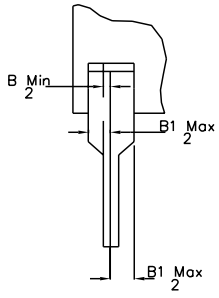
Figure 6 - Control Memory Timing Diagram

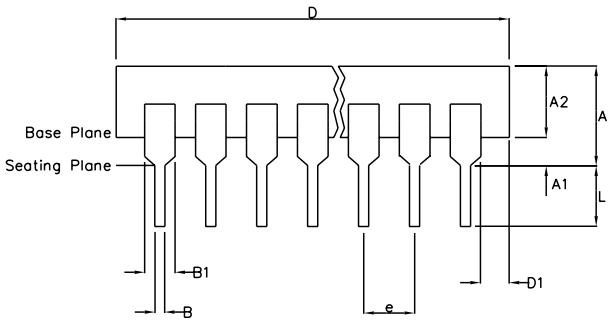
Memory Reset **MR**	Address Enable **AE**	Address			Addressed Line	Input Data To Control Memory				Junctors Connected To Addressed Line			
		A2	A1	A0		D3	D2	D1	D0	J3	J2	J1	J0
1	X	X	X	X	ALL	X	X	X	X	All Switches "OFF"			
0	0	X	X	X	NONE	X	X	X	X	No Change of State			
0	1	0	0	0	L0	0	0	0	0	•	•	•	•
0	1	0	0	0	L0	0	0	0	1	•	•	•	+
0	1	0	0	0	L0	0	0	1	0	•	•	+	•
0	1	0	0	0	L0	0	0	1	1	•	•	+	+
0	1	0	0	0	L0	0	1	0	0	•	+	•	•
0	1	0	0	0	L0	0	1	0	1	•	+	•	+
0	1	0	0	0	L0	0	1	1	0	•	+	+	•
0	1	0	0	0	L0	0	1	1	1	•	+	+	+
0	1	0	0	0	L0	1	0	0	0	+	•	•	•
0	1	0	0	0	L0	1	0	0	1	+	•	•	+
0	1	0	0	0	L0	1	0	1	0	+	•	+	•
0	1	0	0	0	L0	1	0	1	1	+	•	+	+
0	1	0	0	0	L0	1	1	0	0	+	+	•	•
0	1	0	0	0	L0	1	1	0	1	+	+	•	+
0	1	0	0	0	L0	1	1	1	0	+	+	+	•
0	1	0	0	0	L0	1	1	1	1	+	+	+	+
0	1	0	0	1	L1	0	0	0	0	•	•	•	•
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
0	1	0	0	1	L1	1	1	1	1	+	+	+	+
0	1	0	1	0	L2	0	0	0	0	•	•	•	•
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
0	1	0	1	0	L2	1	1	1	1	+	+	+	+
0	1	0	1	1	L3	0	0	0	0	•	•	•	•
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
0	1	0	1	1	L3	1	1	1	1	+	+	+	+
0	1	1	0	0	L4	0	0	0	0	•	•	•	•
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
0	1	1	0	0	L4	1	1	1	1	+	+	+	+
0	1	1	0	1	L5	0	0	0	0	•	•	•	•
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
0	1	1	0	1	L5	1	1	1	1	+	+	+	+
0	1	1	1	0	L6	0	0	0	0	•	•	•	•
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
0	1	1	1	0	L6	1	1	1	1	+	+	+	+
0	1	1	1	1	L7	0	0	0	0	•	•	•	•
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
0	1	1	1	1	L7	1	1	1	1	+	+	+	+

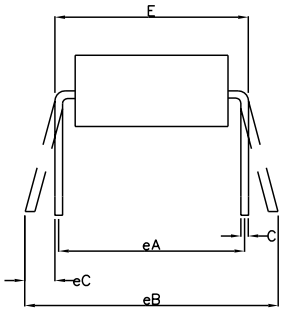
Table 1 - Address Decode Truth Table

NOTES: 0 - Low Logic Level
1 - High Logic Level
X - Don't Care Condition
+ - Indicates Connection Between Junctor and Addressed Line
• - Indicates No Connection Between Junctor and Addressed Line









	Min mm	Max mm	Min Inches	Max Inches
A		6.35		0.250
A1	0.38		0.015	
A2	3.18	4.95	0.125	0.195
B	0.36	0.56	0.014	0.022
B1	0.76	1.78	0.030	0.070
C	0.20	0.38	0.008	0.015
D	29.21	32.77	1.150	1.290
D1	0.13		0.005	
E	15.24	15.88	0.600	0.625
E1	12.32	14.73	0.485	0.580
e	2.54 BSC		0.100 BSC	
eA	15.24 BSC		0.600 BSC	
eB		17.78		0.700
L	2.92	5.08	0.115	0.200
N	24		24	
Conforms to Jedec MS-011AA ISS.B				

Notes:
1. Controlling Dimensions are in inches
2. Dimension A, A1 and L are measured with the package seated in the Seating Plane
3. Dimensions D & E1 do not include mould flash or protrusions. Mould flash or protrusion shall not exceed 0.010 inch.
4. Dimensions E & eA are measured with leads constrained to be perpendicular to plane T.
5. Dimensions eB & eC are measured at the lead tips with the leads unconstrained; eC must be zero or greater.

ISSUE	1	2	3	
ACN	7010	203400	213101	
DATE	20Apr95	4Nov97	15Jul02	
APPRD.				

ZARLINK SEMICONDUCTOR

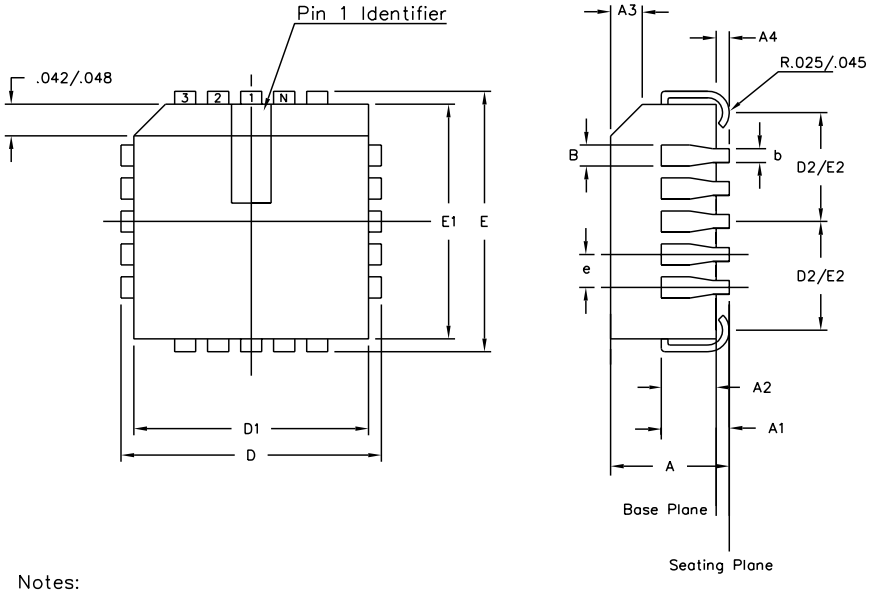
Previous package codes

DP / E

Package Code DA

Package Outline for 24 lead PDIP

GPD00071



Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.062	0.083	1.57	2.11
A3	0.042	0.056	1.07	1.42
A4	0.020	–	0.51	–
D	0.485	0.495	12.32	12.57
D1	0.450	0.456	11.43	11.58
D2	0.191	0.219	4.85	5.56
E	0.485	0.495	12.32	12.57
E1	0.450	0.456	11.43	11.58
E2	0.191	0.219	4.85	5.56
B	0.026	0.032	0.66	0.81
b	0.013	0.021	0.33	0.53
e	0.050 BSC		1.27 BSC	
	Pin features			
ND	7			
NE	7			
N	28			
Note	Square			
Conforms to JEDEC MS-018AB Iss. A				

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M–1982
2. Dimensions D1 and E1 do not include mould protrusions. Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
3. Controlling dimensions in Inches.
4. "N" is the number of terminals.
5. Not To Scale
6. Dimension R required for 120° minimum bend.

ISSUE	1	2	3	
ACN	5958	207469	212422	
DATE	15Aug94	10Sep99	22Mar02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes
HP / P

Package Code QA

Package Outline for 28 lead PLCC

GPD00002

For more information about all Zarlink products visit our Web Site at

www.zarlink.com