

DATA SHEET

NE5230/SA5230

Low voltage operational amplifier

Product data
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Low voltage operational amplifier

NE5230/SA5230

DESCRIPTION

The NE5230 is a very low voltage operational amplifier that can perform with a voltage supply as low as 1.8 V or as high as 15 V. In addition, split or single supplies can be used, and the output will swing to ground when applying the latter. There is a bias adjusting pin which controls the supply current required by the device and thereby controls its power consumption. If the part is operated at ± 0.9 V supply voltages, the current required is only 110 μ A when the current control pin is left open. Even with this low power consumption, the device obtains a typical unity gain bandwidth of 180 kHz. When the bias adjusting pin is connected to the negative supply, the unity gain bandwidth is typically 600 kHz while the supply current is increased to 600 μ A. In this mode, the part will supply full power output beyond the audio range.

The NE5230 also has a unique input stage that allows the common-mode input range to go above the positive and below the negative supply voltages by 250 mV. This provides for the largest possible input voltages for low voltage applications. The part is also internally-compensated to reduce external component count.

The NE5230 has a low input bias current of typically ± 40 nA, and a large open-loop gain of 125 dB. These two specifications are beneficial when using the device in transducer applications. The large open-loop gain gives very accurate signal processing because of the large "excess" loop gain in a closed-loop system.

The output stage is a class AB type that can swing to within 100 mV of the supply voltages for the largest dynamic range that is needed in many applications. The NE5230 is ideal for portable audio equipment and remote transducers because of its low power consumption, unity gain bandwidth, and 30 nV/ $\sqrt{\text{Hz}}$ noise specification.

FEATURES

- Works down to 1.8 V supply voltages
- Adjustable supply current
- Low noise
- Common-mode includes both rails
- V_{OUT} within 100 mV of both rails

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) Package	0 °C to +70 °C	NE5230D	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	0 °C to +70 °C	NE5230N	SOT97-1
8-Pin Plastic Small Outline (SO) Package	-40 °C to +85 °C	SA5230D	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	-40 °C to +85 °C	SA5230N	SOT97-1

PIN CONFIGURATION

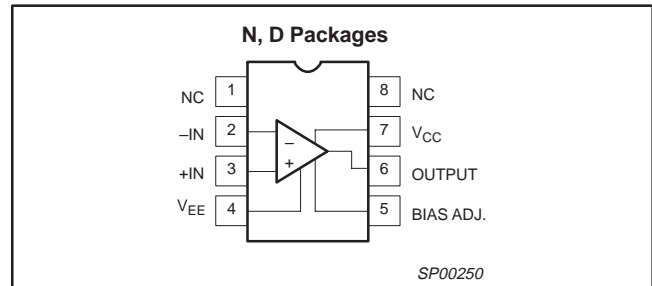


Figure 1. Pin Configuration

APPLICATIONS

- Portable precision instruments
- Remote transducer amplifier
- Portable audio equipment
- Rail-to-rail comparators
- Half-wave rectification without diodes
- Remote temperature transducer with 4 to 20 mA output transmission

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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Single supply voltage	18	V
V_S	Dual supply voltage	± 9	V
V_{IN}	Input voltage ¹	± 9 (18)	V
	Differential input voltage ¹	$\pm V_S$	V
V_{CM}	Common-mode voltage (positive)	$V_{CC}+0.5$	V
V_{CM}	Common-mode voltage (negative)	$V_{EE}-0.5$	V
P_D	Power dissipation ²	500	mW
T_j	Operating junction temperature ²	150	°C
	80Output short-circuit duration to either power supply pin ^{2, 3}	Indefinite	s
T_{stg}	Storage temperature	-65 to 150	°C
T_{sld}	Lead soldering temperature (10sec max)	230	°C

NOTES:

- Can exceed the supply voltages when $V_S \leq \pm 7.5$ V (15 V).
- The maximum operating junction temperature is 150 °C. At elevated temperatures, devices must be derated according to the package thermal resistance and device mounting conditions. Derate above 25 °C at the following rates:
N package at 9.5 mW/°C
D package at 6.25 mW/°C
- Momentary shorts to either supply are permitted in accordance to transient thermal impedance limitations determined by the package and device mounting conditions.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING	UNIT
Single supply voltage	1.8 to 15	V
Dual supply voltage	± 0.9 to ± 7.5	V
Common-mode voltage (positive)	$V_{CC}+0.25$	V
Common-mode voltage (negative)	$V_{EE}-0.25$	V
Temperature		
NE grade	0 to +70	°C
SA grade	-40 to +85	°C

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DC AND AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $\pm 0.9\text{V} \leq V_S \leq +7.5\text{V}$ or equivalent single supply, $R_L = 10\text{ k}\Omega$, full input common-mode range, over full operating temperature range.

SYMBOL	PARAMETER	TEST CONDITIONS	BIAS	NE5230/SA5230			UNIT		
				Min	Typ	Max			
V_{OS}	Offset voltage	$T_{amb} = 25\text{ }^\circ\text{C}$	Any		0.4	3	mV		
		$T_{amb} = 25\text{ }^\circ\text{C}$	Any		3	4			
V_{OS}	Drift		Any		2	5	$\mu\text{V}/^\circ\text{C}$		
I_{OS}	Offset current	$T_{amb} = 25\text{ }^\circ\text{C}$	High		3	50	nA		
		$T_{amb} = 25\text{ }^\circ\text{C}$	Low		3	30			
			High					100	
			Low					60	
I_{OS}	Drift		High		0.5	1.4	nA/ $^\circ\text{C}$		
			Low		0.3	1.4			
I_B	Bias current	$T_{amb} = 25\text{ }^\circ\text{C}$	High		40	150	nA		
		$T_{amb} = 25\text{ }^\circ\text{C}$	Low		20	60			
			High					200	
			Low					150	
I_B	Drift		High		2	4	nA/ $^\circ\text{C}$		
			Low		2	4			
I_S	Supply current	$V_S = \pm 0.9\text{ V}$	$T_{amb} = 25\text{ }^\circ\text{C}$	Low		110	160	μA	
			$T_{amb} = 25\text{ }^\circ\text{C}$	High		600	750		
				Low					250
				High					800
		$V_S = \pm 7.5\text{ V}$	$T_{amb} = 25\text{ }^\circ\text{C}$	Low		320	550	μA	
			$T_{amb} = 25\text{ }^\circ\text{C}$	High		1.1	1.6		
				Low					600
				High					1.7
V_{CM}	Common-mode input range	$V_{OS} \leq 6\text{ mV}$, $T_{amb} = 25\text{ }^\circ\text{C}$		Any	$V^- - 0.25$	$V^+ + 0.25$	V		
				Any	V^-	V^+			
CMRR	Common-mode rejection ratio	$V_S = \pm 7.5\text{ V}$	$R_S = 10\text{ k}\Omega$; $V_{CM} = \pm 7.5\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$	Any	85	95	dB		
			$R_S = 10\text{ k}\Omega$; $V_{CM} = \pm 7.5\text{ V}$	Any	80				
PSRR	Power supply rejection ratio	$T_{amb} = 25\text{ }^\circ\text{C}$		High	90	105	dB		
		$T_{amb} = 25\text{ }^\circ\text{C}$		Low	85	95			
				High	75				
				Low	80				
I_L	Load current	source	$V_S = \pm 7.5\text{ V}$	Any	4	10	mA		
		sink	$V_S = \pm 7.5\text{ V}$	Any	5	15			
		source	$V_S = \pm 7.5\text{ V}$	Any	1	5			
		sink	$V_S = \pm 7.5\text{ V}$	Any	2	6			
		source	$V_S = \pm 0.9\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$	High	4	6			
		sink	$V_S = \pm 0.9\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$	High	5	7			
		source	$V_S = \pm 7.5\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$	High		16			
		sink	$V_S = \pm 7.5\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$	High		32			
A_{VOL}	Large-signal open-loop gain	$V_S = \pm 7.5\text{ V}$	$R_L = 10\text{ k}\Omega$; $T_{amb} = 25\text{ }^\circ\text{C}$	High	120	2000	V/mV		
			$R_L = 10\text{ k}\Omega$; $T_{amb} = 25\text{ }^\circ\text{C}$	Low	60	750	V/mV		
				High	100				
				Low	50				

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DC AND AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	BIAS	NE5230/SA5230			UNIT
				Min	Typ	Max	
V _{OUT}	Output voltage swing	V _S = ±0.9 V	T _{amb} = 25 °C +SW	Any	750	800	mV
			T _{amb} = 25 °C -SW	Any	750	800	
			+SW	Any	700		
			-SW	Any	700		
		V _S = ±7.5 V	T _{amb} = 25 °C +SW	Any	7.30	7.35	V
			T _{amb} = 25 °C -SW	Any	-7.32	-7.35	
			+SW	Any	7.25	7.30	
			-SW	Any	-7.30	-7.35	
SR	Slew rate	T _{amb} = 25 °C	High		0.25	V/μs	
		T _{amb} = 25 °C	Low		0.09		
BW	Inverting unity gain bandwidth	C _L = 100 pF; T _{amb} = 25 °C	High		0.6	MHz	
		C _L = 100 pF; T _{amb} = 25 °C	Low		0.25		
θ _M	Phase margin	C _L = 100 pF; T _{amb} = 25 °C	Any		70	Deg.	
t _S	Settling time	C _L = 100 pF, 0.1%	High		2	μs	
		C _L = 100 pF, 0.1%	Low		5		
V _{INN}	Input noise	R _S = 0 Ω; f = 1 kHz	High		30	nV/√Hz	
		R _S = 0 Ω; f = 1 kHz	Low		60		
THD	Total Harmonic Distortion	V _S = ±7.5 V A _V = 1; V _{IN} = 500 mV; f = 1 kHz	High		0.003	%	
		V _S = ±0.9 V A _V = 1; V _{IN} = 500 mV; f = 1 kHz	High		0.002		

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THEORY OF OPERATION

Input Stage

Operational amplifiers which are able to function at minimum supply voltages should have input and output stage swings capable of reaching both supply voltages within a few millivolts in order to achieve ease of quiescent biasing and to have maximum input/output signal handling capability. The input stage of the NE5230 has a common-mode voltage range that not only includes the entire supply voltage range, but also allows either supply to be exceeded by 250 mV without increasing the input offset voltage by more than 6 mV. This is unequalled by any other operational amplifier today.

In order to accomplish the feat of rail-to-rail input common-mode range, two emitter-coupled differential pairs are placed in parallel so that the common-mode voltage of one can reach the positive supply rail and the other can reach the negative supply rail. The simplified schematic of Figure 2 shows how the complementary emitter-coupler transistors are configured to form the basic input stage cell. Common-mode input signal voltages in the range from 0.8V above V_{EE} to V_{CC} are handled completely by the NPN pair, Q3 and Q4, while common-mode input signal voltages in the range of V_{EE} to 0.8 V above V_{EE} are processed only by the PNP pair, Q1 and Q2. The intermediate range of input voltages requires that both the NPN and PNP pairs are operating. The collector currents of the input transistors are summed by the current combiner circuit composed of transistors Q8 through Q11 into one output current. Transistor Q8 is connected as a diode to ensure that the outputs of Q2 and Q4 are properly subtracted from those of Q1 and Q3.

The input stage was designed to overcome two important problems for rail-to-rail capability. As the common-mode voltage moves from the range where only the NPN pair was operating to where both of the input pairs were operating, the effective transconductance would change by a factor of two. Frequency compensation for the ranges where one input pair was operating would, of course, not be optimal for the range where both pairs were operating. Secondly, fast changes in the common-mode voltage would abruptly saturate and restore the emitter current sources, causing transient distortion. These problems were overcome by assuring that only the input transistor pair which is able to function properly is active. The NPN pair is normally activated by the current source I_{B1} through Q5 and the current mirror Q6 and Q7, assuming the PNP pair is non-conducting. When the common-mode input voltage passes below the reference voltage, $V_{B1} = 0.8$ V at the base of Q5, the emitter current is gradually steered toward the PNP pair, away from the NPN pair. The transfer of the emitter currents between the complementary input pairs occurs in a voltage range of about 120 mV around the reference voltage V_{B1} . In this way the sum of the emitter currents for each of the NPN and PNP transistor pairs is kept constant; this ensures that the transconductance of the parallel combination will be constant, since the transconductance of bipolar transistors is proportional to their emitter currents.

An essential requirement of this kind of input stage is to minimize the changes in input offset voltage between that of the NPN and PNP transistor pair which occurs when the input common-mode voltage crosses the internal reference voltage, V_{B1} . Careful circuit layout with a cross-coupled quad for each input pair has yielded a typical input offset voltage of less than 0.3 mV and a change in the input offset voltage of less than 0.1 mV.

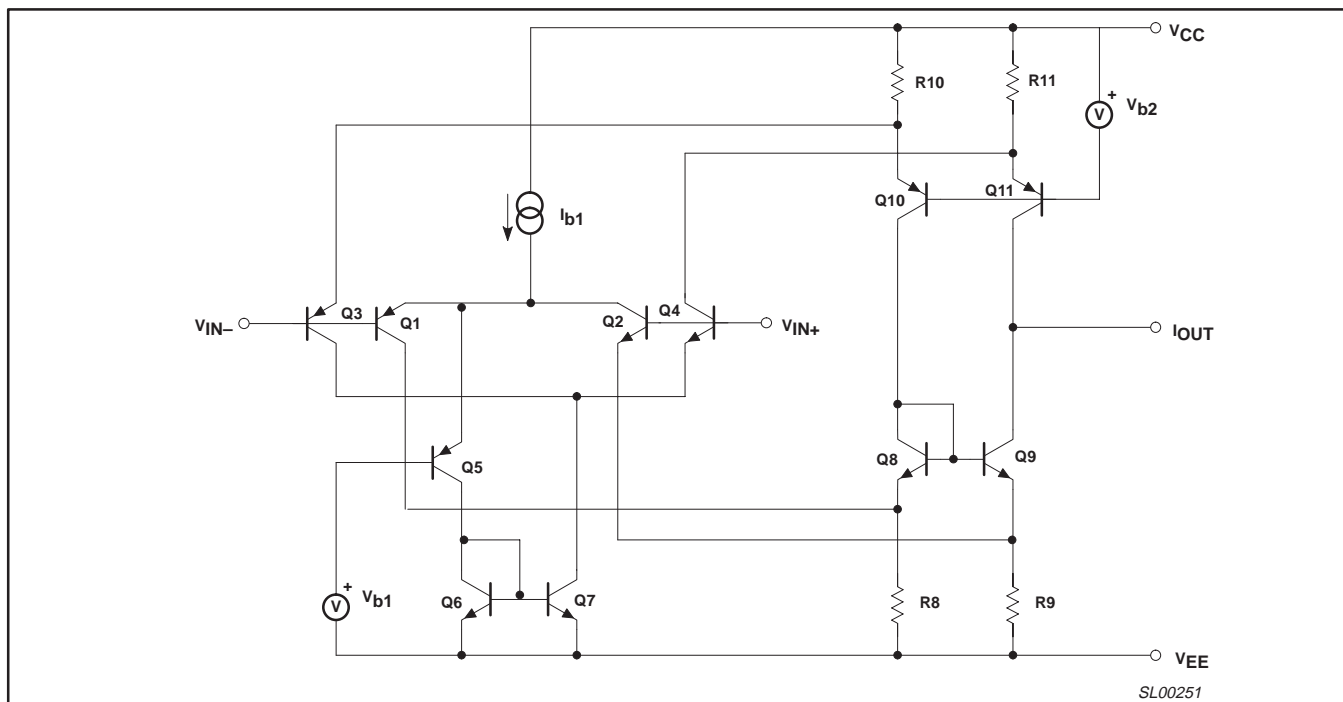


Figure 2. Input Stage

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Output Stage

Processing output voltage swings that nominally reach to less than 100 mV of either supply voltage can only be achieved by a pair of complementary common-emitter connected transistors. Normally, such a configuration causes complex feed-forward signal paths that develop by combining biasing and driving which can be found in previous low supply voltage designs. The unique output stage of the NE5230 separates the functions of driving and biasing, as shown in the simplified schematic of Figure 3, and has the advantage of a shorter signal path which leads to increasing the effective bandwidth.

This output stage consists of two parts: the Darlington output transistors and the class AB control regulator. The output transistor Q3 connected with the Darlington transistors Q4 and Q5 can source up to 10 mA to an output load. The output of NPN Darlington connected transistors Q1 and Q2 together are able to sink an output current of 10 mA. Accurate and efficient class AB control is necessary to insure that none of the output transistors are ever completely cut off. This is accomplished by the differential amplifier (formed by Q8 and Q9) which controls the biasing of the output transistors. The differential amplifier compares the summed voltages across two diodes, D1 and D2, at the base of Q8 with the summed voltages across the base-emitter diodes of the output transistors Q1 and Q3. The base-emitter voltage of Q3 is converted into a current by Q6 and R6 and reconverted into a voltage across the base-emitter diode of Q7 and R7. The summed voltage across the base-emitter diodes of the output transistors Q3 and Q1 is proportional to the logarithm of the product of the push and pull currents I_{OP} and I_{ON} , respectively. The combined voltages across

diodes D1 and D2 are proportional to the logarithm of the square of the reference current I_{B1} . When the diode characteristics and temperatures of the pairs Q1, D1 and Q3, Q2 are equal, the relation $I_{OP} \times I_{ON} = I_{B1} \times I_{B1}$ is satisfied.

Separating the functions of biasing and driving prevents the driving signals from becoming delayed by the biasing circuit. The output Darlington transistors are directly accessible for in-phase driving signals on the bases of Q5 and Q2. This is very important for simple high-frequency compensation. The output transistors can be high-frequency compensated by Miller capacitors CM1A and CM1B connected from the collectors to the bases of the output Darlington transistors.

A general-purpose op amp of this type must have enough open-loop gain for applications when the output is driving a low resistance load. The NE5230 accomplishes this by inserting an intermediate common-emitter stage between the input and output stages. The three stages provide a very large gain, but the op amp now has three natural dominant poles — one at the output of each common-emitter stage. Frequency compensation is implemented with a simple scheme of nested, pole-splitting Miller integrators. The Miller capacitors CM1A and CM1B are the first part of the nested structure, and provide compensation for the output and intermediate stages. A second pair of Miller integrators provide pole-splitting compensation for the pole from the input stage and the pole resulting from the compensated combination of poles from the intermediate and output stages. The result is a stable, internally-compensated op amp with a phase margin of 70 degrees.

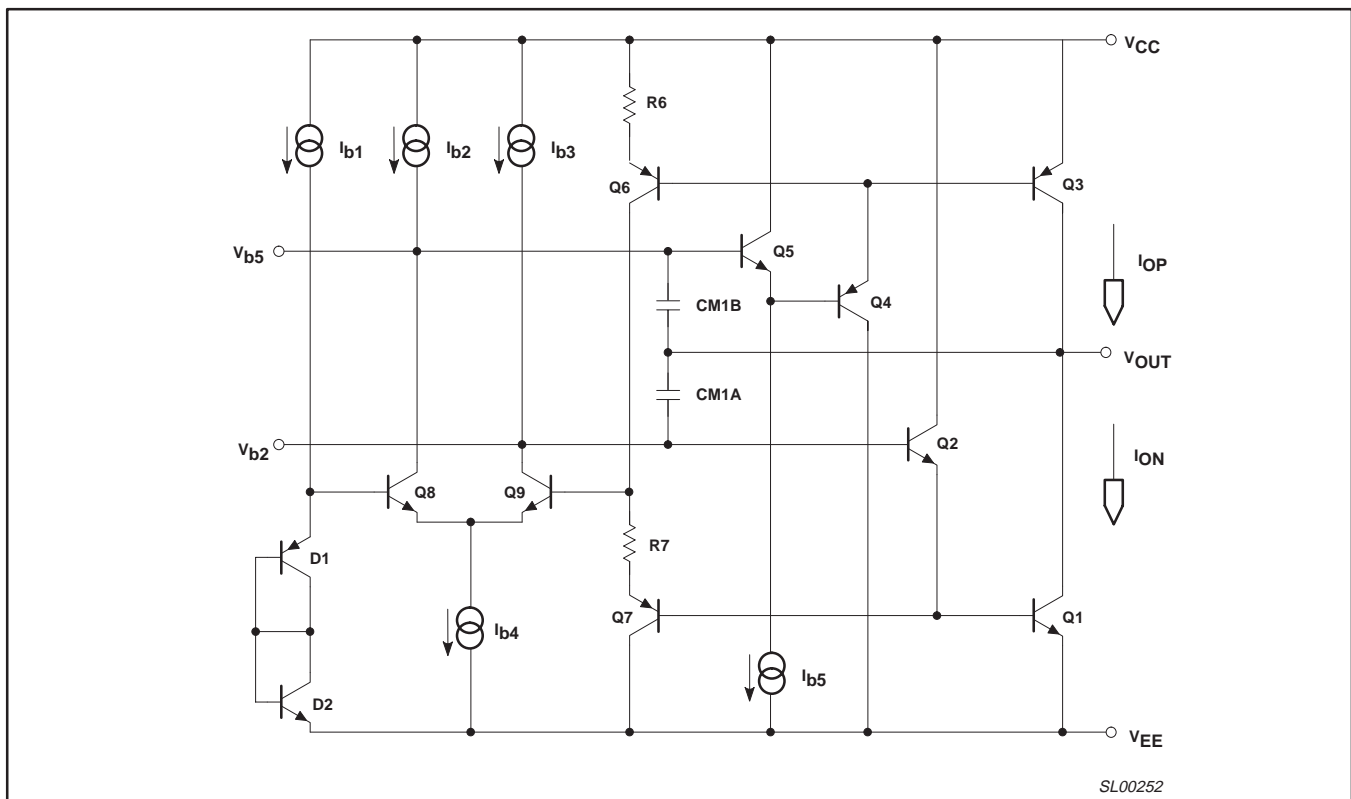


Figure 3. Output Stage

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THERMAL CONSIDERATIONS

When using the NE5230, the internal power dissipation capabilities of each package should be considered. Philips Semiconductors does not recommend operation at die temperatures above 110 °C in the SO package because of its inherently smaller package mass. Die temperatures of 150 °C can be tolerated in all the other packages. With this in mind, the following equation can be used to estimate the die temperature:

$$T_j = T_{amb} + (P_D \times \theta_{JA}) \quad (1)$$

Where

T_{amb} ≡ Ambient Temperature
 T_j = Die Temperature
 P_D ≡ Power Dissipation
 = $(I_{CC} \times V_{CC})$
 θ_{JA} ≡ Package thermal resistance
 = 270°C/W for SO8 in PC board mounting

See the packaging section for information regarding other methods of mounting.

$\theta_{JA} = 100$ °C/W for the plastic DIP.

The maximum supply voltage for the part is 15 V and the typical supply current is 1.1 mA (1.6 mA max). For operation at supply voltages other than the maximum, see the data sheet for I_{CC} versus V_{CC} curves. The supply current is somewhat proportional to temperature and varies no more than 100 µA between 25 °C and either temperature extreme.

Operation at higher junction temperatures than that recommended is possible but will result in lower MTBF (Mean Time Between Failures). This should be considered before operating beyond recommended die temperature because of the overall reliability degradation.

DESIGN TECHNIQUES AND APPLICATIONS

The NE5230 is a very user-friendly amplifier for an engineer to design into any type of system. The supply current adjust pin (Pin 5) can be left open or tied through a pot or fixed resistor to the most negative supply (i.e., ground for single supply or to the negative supply for split supplies). The minimum supply current is achieved by leaving this pin open. In this state it will also decrease the bandwidth and slew rate. When tied directly to the most negative supply, the device has full bandwidth, slew rate and I_{CC} . The programming of the current-control pin depends on the trade-offs which can be made in the designer's application. The graph in Figure 4 will help by showing bandwidth versus I_{CC} . As can be seen, the supply current can be varied anywhere over the range of 100 µA to 600 µA for a supply voltage of 1.8 V. An external resistor can be inserted between the current control pin and the most negative supply. The resistor can be selected between 1 Ω to 100 kΩ to provide any required supply current over the indicated range. In addition, a small varying voltage on the bias current control pin could be used for such exotic things as changing the gain-bandwidth for voltage controlled low pass filters or amplitude modulation. Furthermore, control over the slew rate and the rise time of the amplifier can be obtained in the same manner. This control over the slew rate also changes the settling time and overshoot in pulse response applications. The settling time to 0.1% changes from 5 µs at low bias to 2 µs at high bias. The supply current control can also be utilized for wave-shaping applications such as for pulse or triangular waveforms. The gain-bandwidth can be varied from

between 250 kHz at low bias to 600 kHz at high bias current. The slew rate range is 0.08 V/µs at low bias and 0.25 V/µs at high bias.

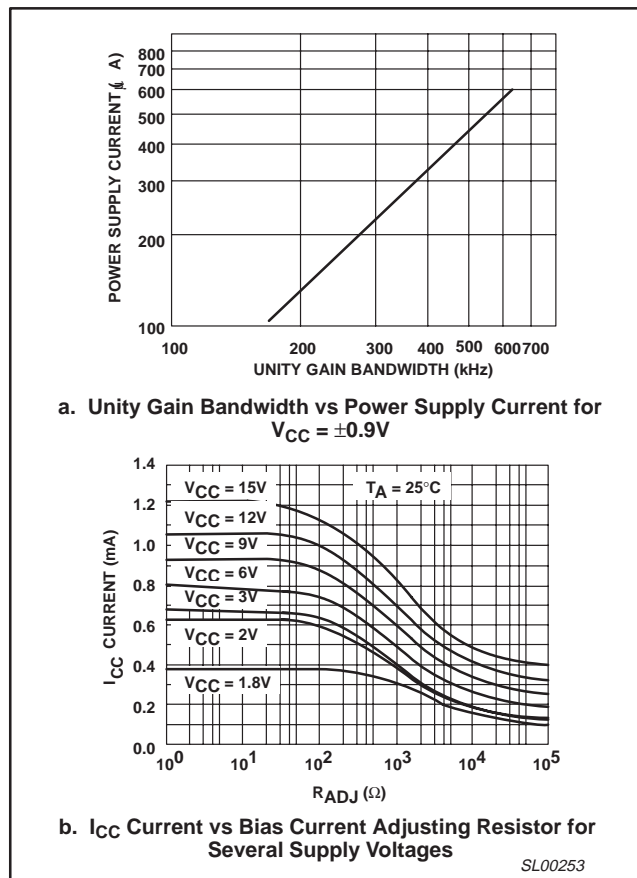


Figure 4.

The full output power bandwidth range for V_{CC} equals 2 V, is above 40 kHz for the maximum bias current setting and greater than 10 kHz at the minimum bias current setting.

If extremely low signal distortion (<0.05%) is required at low supply voltages, exclude the common-mode crossover point (V_{B1}) from the common-mode signal range. This can be accomplished by proper bias selection or by using an inverting amplifier configuration.

Most single supply designs necessitate that the inputs to the op amp be biased between V_{CC} and ground. This is to assure that the input signal swing is within the working common-mode range of the amplifier. This leads to another helpful and unique property of the NE5230 that other CMOS and bipolar low voltage parts cannot achieve. It is the simple fact that the input common-mode voltage can go beyond either the positive or negative supply voltages. This benefit is made very clear in a non-inverting voltage-follower configuration. This is shown in Figure 5 where the input sine wave allows an undistorted output sine wave which will swing less than 100mV of either supply voltage. Many competitive parts will show severe clipping caused by input common-mode limitations. The NE5230 in this configuration offers more freedom for quiescent biasing of the inputs close to the positive supply rail where similar op amps would not allow signal processing.

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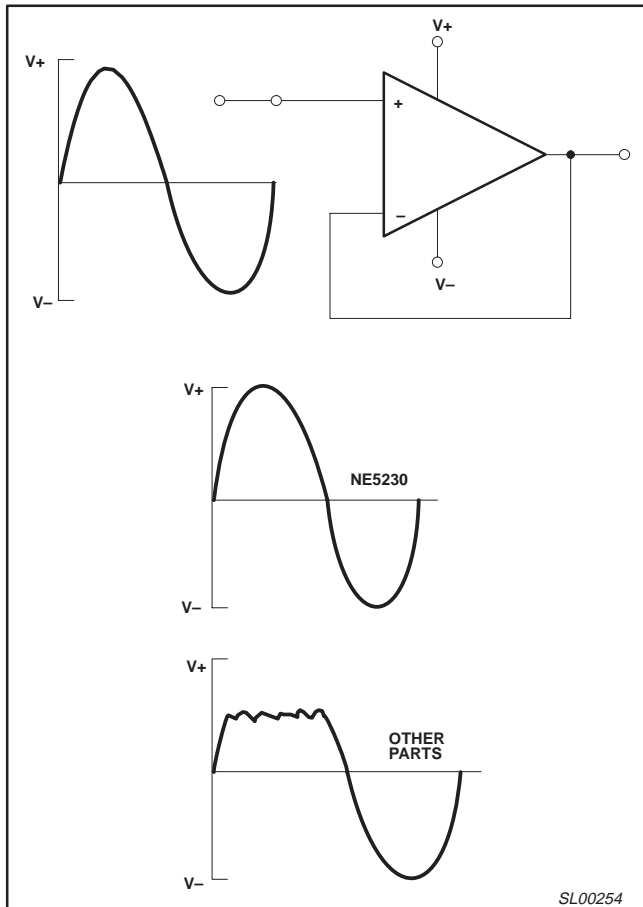


Figure 5. In a Non-Inverting Voltage-Follower Configuration, the NE5230 will Give Full Rail-to-Rail Swing. Other Low Voltage Amplifiers will not Because they are Limited by their Input Common-Mode Range and Output Swing Capability.

There are not as many considerations when designing with the NE5230 as with other devices. Since the NE5230 is internally-compensated and has a unity gain-bandwidth of 600 kHz, board layout is not so stringent as for very high frequency devices such as the NE5205. The output capability of the NE5230 allows it to drive relatively high capacitive loads and small resistive loads. The power supply pins should be decoupled with a low-pass RC network as close to the supply pins as possible to eliminate 60 Hz and other external power line noise, although the power supply rejection ratio (PSRR) for the part is very high. The pinout for the NE5230 is the same as the standard single op amp pinout with the exception of the bias current adjusting pin.

REMOTE TRANSDUCER WITH CURRENT TRANSMISSION

There are many ways to transmit information along two wires, but current transmission is the most beneficial when the sensing of remote signals is the aim. It is further enhanced in the form of 4 to 20 mA information which is used in many control-type systems. This method of transmission provides immunity from line voltage drops, large load resistance variations, and voltage noise pickup. The zero reference of 4mA not only can show if there is a break in

the line when no current is flowing, but also can power the transducer at the remote location. Usually the transducer itself is not equipped to provide for the current transmission. The unique features of the NE5230 can provide high output current capability coupled with low power consumption. It can be remotely connected to the transducer to create a current loop with minimal external components. The circuit for this is shown in Figure 6. Here, the part is configured as a voltage-to-current, or transconductance amplifier. This is a novel circuit that takes advantage of the NE5230's large open-loop gain. In AC applications, the load current will decrease as the open-loop gain rolls off in magnitude. The low offset voltage and current sinking capabilities of the NE5230 must also be considered in this application.

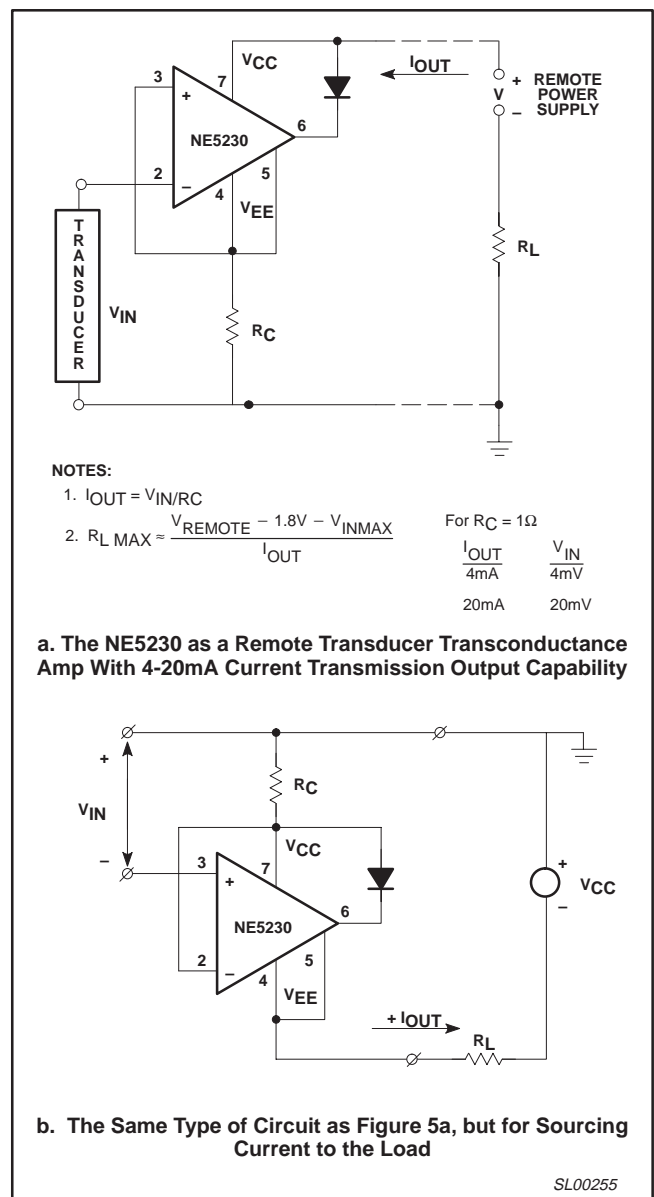


Figure 6.

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The NE5230 circuit shown in Figure 6 is a pseudo transistor configuration. The inverting input is equivalent to the “base,” the point where V_{EE} and the non-inverting input meet is the “emitter,” and the connection after the output diode meets the V_{CC} pin is the collector. The output diode is essential to keep the output from saturating in this configuration. From here it can be seen that the base and emitter form a voltage-follower and the voltage present at R_C must equal the input voltage present at the inverting input. Also, the emitter and collector form a current-follower and the current flowing through R_C is equivalent to the current through R_L and the amplifier. This sets up the current loop. Therefore, the following equation can be formulated for the working current transmission line. The load current is:

$$I_L = V_{IN}/R_C \tag{2}$$

and proportional to the input voltage for a set R_C . Also, the current is constant no matter what load resistance is used while within the operating bandwidth range of the op amp. When the NE5230's supply voltage falls past a certain point, the current cannot remain constant. This is the “voltage compliance” and is very good for this application because of the near rail output voltage. The equation that determines the voltage compliance as well as the largest possible load resistor for the NE5230 is as follows:

$$R_{L\ max} = [V_{remote\ supply} - V_{CC\ min} - V_{IN\ max}]/I_L \tag{3}$$

Where $V_{CC\ min}$ is the worst-case power supply voltage (approximately 1.8 V) that will still keep the part operational. As an example, when using a 15 V remote power supply, a current sensing resistor of 1 Ω , and an input voltage (V_{IN}) of 20 mV, the output current (I_L) is 20 mA. Furthermore, a load resistance of zero to approximately 650 Ω can be inserted in the loop without any change in current when the bias current-control pin is tied to the negative supply pin. The voltage drop across the load and line resistance will not affect the NE5230 because it will operate down to 1.8 V. With a 15 V remote supply, the voltage available at the amplifier is still enough to power it with the maximum 20 mA output into the 650 Ω load.

What this means is that several instruments, such as a chart recorder, a meter, or a controller, as well as a long cable, can be connected in series on the loop and still obtain accurate readings if the total resistance does not exceed 650 Ω . Furthermore, any variation of resistance in this range will not change the output current.

Any voltage output type transducer can be used, but one that does not need external DC voltage or current excitation to limit the maximum possible load resistance is preferable. Even this problem can be surmounted if the supply power needed by the transducer is compatible with the NE5230. The power goes up the line to the transducer and amplifier while the transducer signal is sent back via the current output of the NE5230 transconductance configuration.

The voltage range on the input can be changed for transducers that produce a large output by simply increasing the current sense resistor to get the corresponding 4 to 20 mA output current. If a very

long line is used which causes high line resistance, a current repeater could be inserted into the line. The same configuration of Figure 6 can be used with exception of a resistor across the input and line ground to convert the current back to voltage. Again, the current sensing resistor will set up the transconductance and the part will receive power from the line.

TEMPERATURE TRANSDUCER

A variation on the previous circuit makes use of the supply current control pin. The voltage present at this pin is proportional to absolute temperature (PTAT) because it is produced by the amplifier bias current through an internal resistor divider in a PTAT cell. If the control pin is connected to the input pin, the NE5230 itself can be used as a temperature transducer. If the center tap of a resistive pot is connected to the control pin with one side to ground and the other to the inverting input, the voltage can be changed to give different temperature versus output current conditions (see Figure 7). For additional control, the output current is still proportional to the input voltage differential divided by the current sense resistor.

When using the NE5230 as a temperature transducer, the thermal considerations in the previous section must be kept in mind.

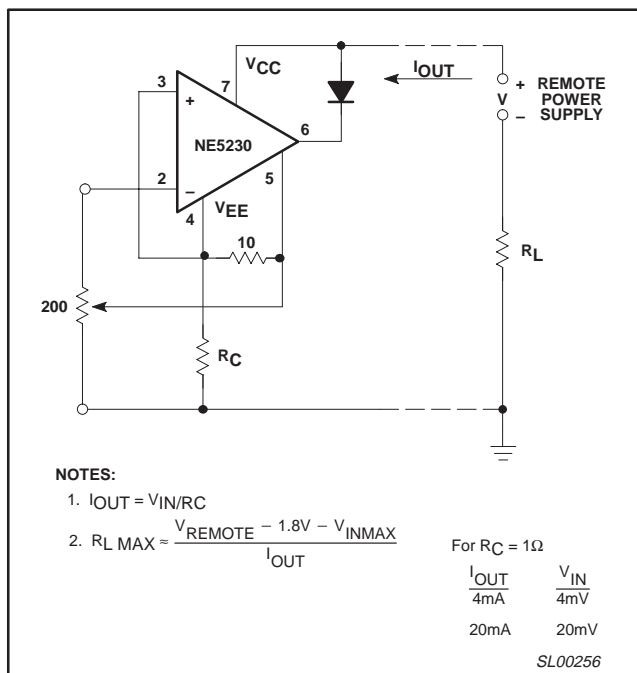


Figure 7. NE5230 Remote Temperature Transducer Utilizing 4–20 mA Current Transmission. This Application Shows the use of the Accessibility of the PTAT Cell in the Device to Make the Part, Itself, a Transducer

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HALF-WAVE RECTIFIER WITH RAIL-TO-GROUND OUTPUT SWING

Since the NE5230 input common-mode range includes both positive and negative supply rails and the output can also swing to either supply, achieving half-wave rectifier functions in either direction becomes a simple task. All that is needed are two external resistors; there is no need for diodes or matched resistors. Moreover, it can have either positive- or negative-going outputs, depending on the way the bias is arranged. This can be seen in Figure 8. Circuit (a) is biased to ground, while circuit (b) is biased to the positive supply. This rather unusual biasing does not cause any problems with the NE5230 because of the unique internal saturation detectors incorporated into the part to keep the PNP and NPN output transistors out of "hard" saturation. It is therefore relatively quick to recover from a saturated output condition. Furthermore, the device does not have parasitic current draw when the output is biased to either rail. This makes it possible to bias the NE5230 into "saturation" and obtain half-wave rectification with good recovery. The simplicity of biasing and the rail-to-ground half-sine wave swing are unique to this device. The circuit gain can be changed by the standard op amp gain equations for an inverting configuration.

It can be seen in these configurations that the op amp cannot respond to one-half of the incoming waveform. It cannot respond

because the waveform forces the amplifier to swing the output beyond either ground or the positive supply rail, depending on the biasing, and, also, the output cannot disengage during this half cycle. During the other half cycle, however, the amplifier achieves a half-wave that can have a peak equal to the total supply voltage. The photographs in Figure 9 show the effect of the different biasing schemes, as well as the wide bandwidth (it works over the full audio range), that the NE5230 can achieve in this configuration.

By adding another NE5230 in an inverting summer configuration at the output of the half-wave rectifier, a full-wave can be realized. The values for the input and feedback resistors must be chosen so that each peak will have equal amplitudes. A table for calculating values is included in Figure 10. The summing network combines the input signal at the half-wave and adds it to double the half-wave's output, resulting in the full-wave. The output waveform can be referenced to the supply or ground, depending on the half-wave configuration. Again, no diodes are needed to achieve the rectification.

This circuit could be used in conjunction with the remote transducer to convert a received AC output signal into a DC level at the full-wave output for meters or chart recorders that need DC levels.

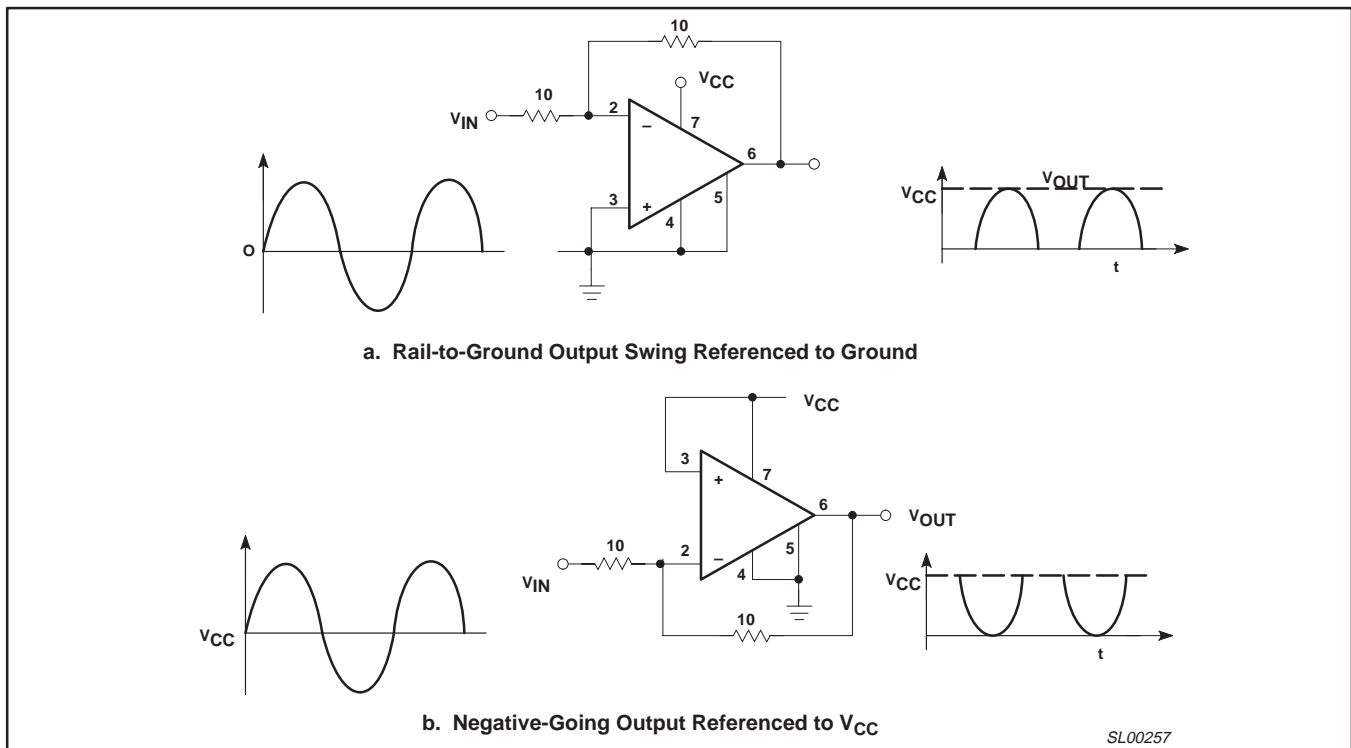


Figure 8. Half-Wave Rectifier With Positive-Going Output Swings

Low voltage operational amplifier

NE5230/SA5230

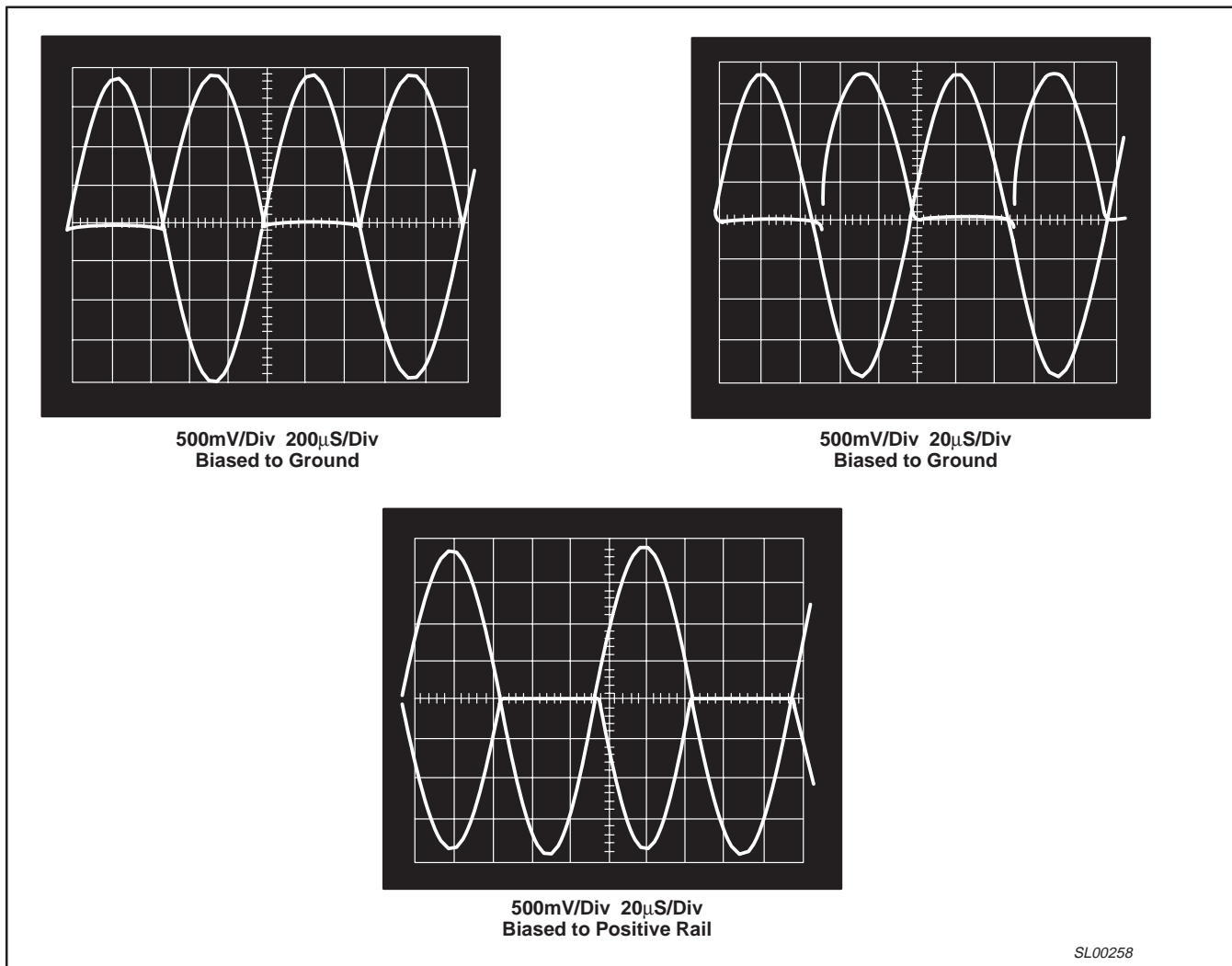


Figure 9. Performance Waveforms for the Circuits in Figure 8.
Good response is shown at 1 and 10 kHz for both circuits under full swing with a 2 V supply.

SL00258

Low voltage operational amplifier

NE5230/SA5230

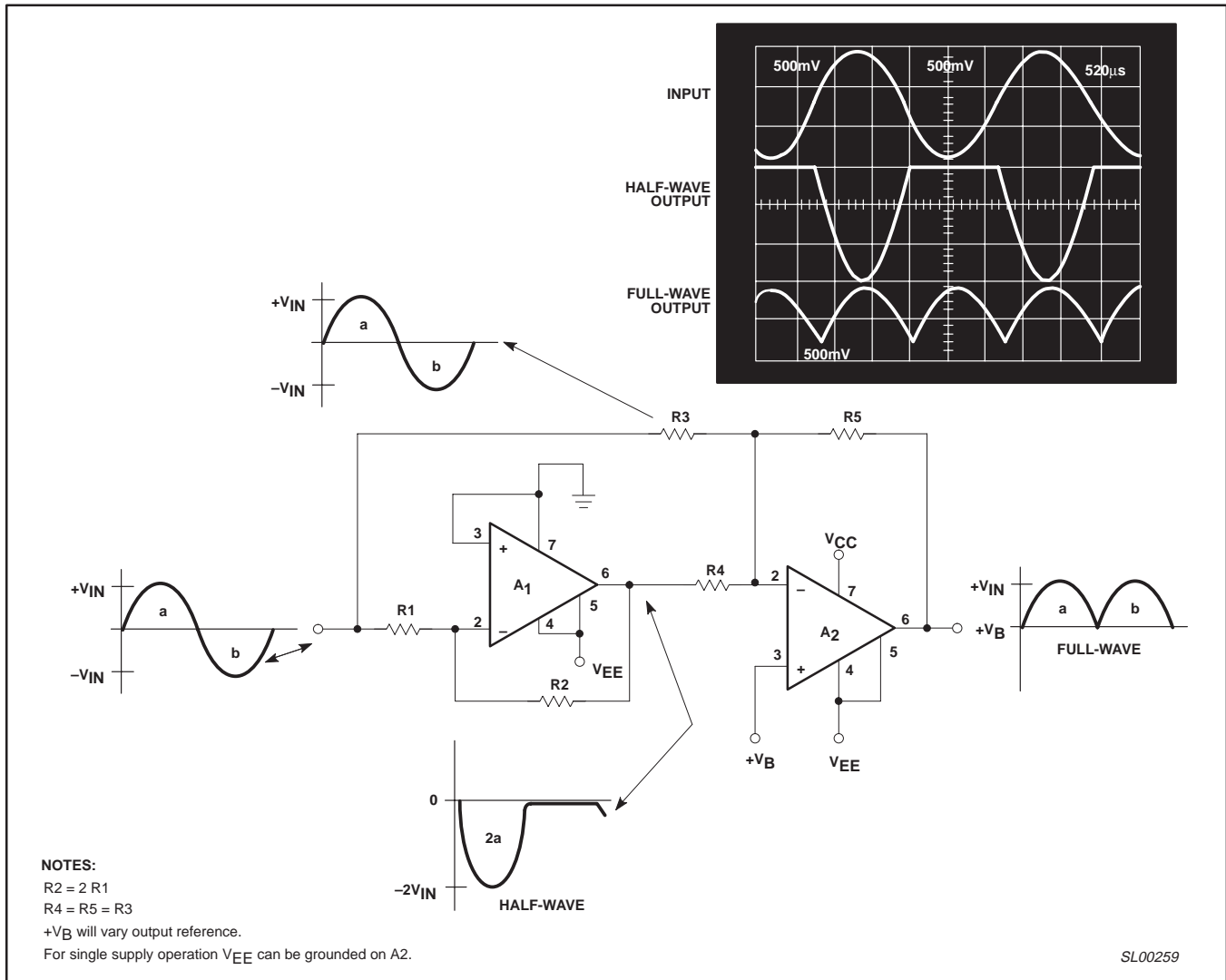


Figure 10. Adding an Inverting Summer to the Input and Output of the Half-Wave will Result in Full-Wave

CONCLUSION

The NE5230 is a versatile op amp in its own right. The part was designed to give low voltage and low power operation without the limitations of previously available amplifiers that had a multitude of problems. The previous application examples are unique to this amplifier and save the user money by excluding various passive components that would have been needed if not for the NE5230's special input and output stages.

The NE5230 has a combination of novel specifications which allows the designer to implement it easily into existing low-supply voltage designs and to enhance their performance. It also offers the engineer the freedom to achieve greater amplifier system design goals. The low input referenced noise voltage eases the restrictions on designs where S/N ratios are important. The wide full-power bandwidth and output load handling capability allow it to fit into portable audio applications. The truly ample open-loop gain and low power consumption easily lend themselves to the requirements of remote transducer applications. The low, untrimmed typical offset voltage and low offset currents help to reduce errors in signal processing designs. The amplifier is well isolated from changes on the supply lines by its typical power supply rejection ratio of 105 dB.

REFERENCES

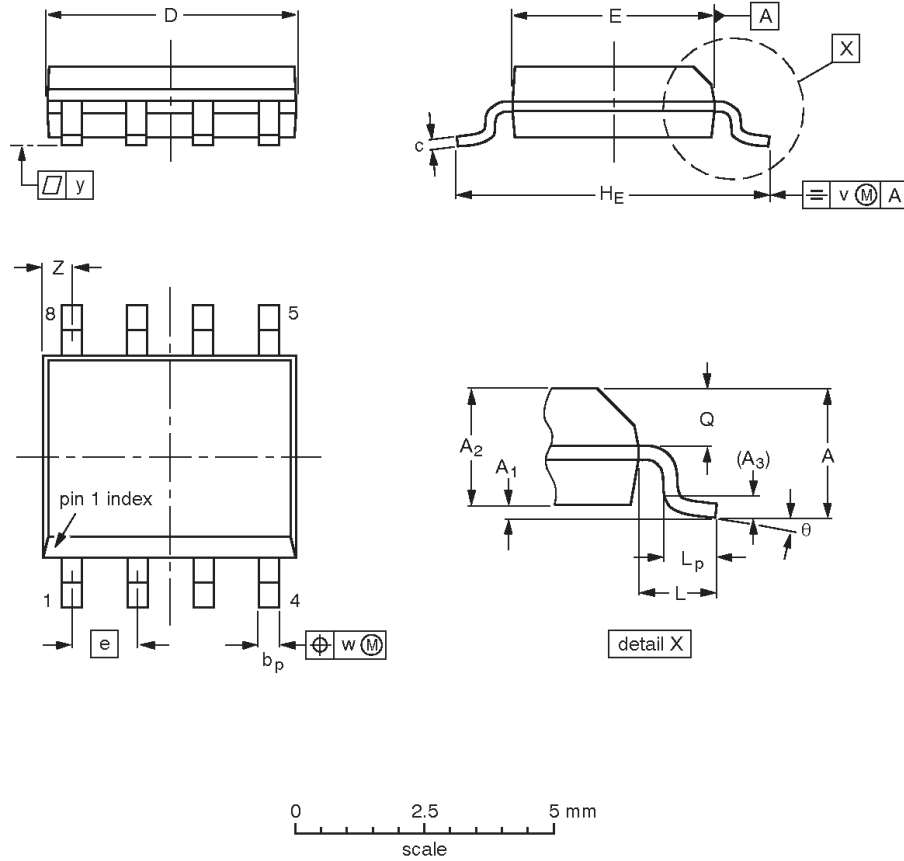
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Low voltage operational amplifier

NE5230/SA5230

S08: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

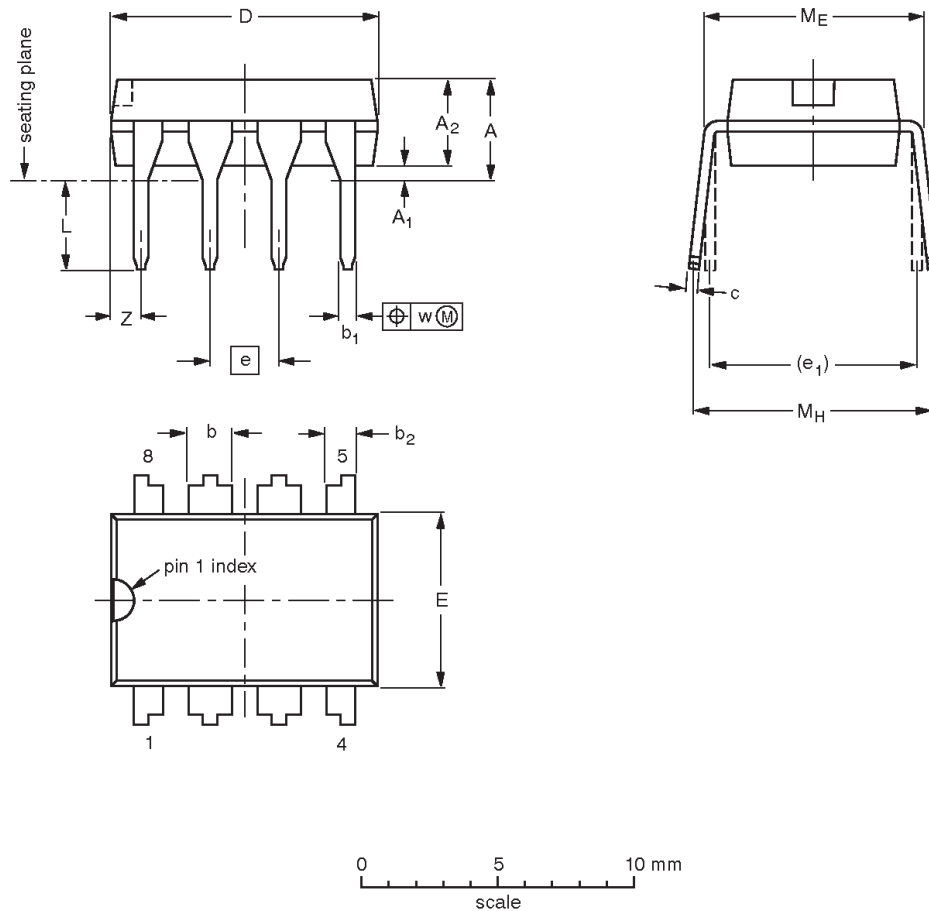
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				97-05-22 99-12-27

Low voltage operational amplifier

NE5230/SA5230

DIP8: plastic dual in-line package; 8 leads (300 mil)

SOT97-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001	SC-504-8			95-02-04 99-12-27

Low voltage operational amplifier

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Data sheet status ^[1]	Product status ^[2]	Definitions
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